RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A888A/E	Rev.	1.00
Title	SCIF Break Detection and Processing in Asynchronous Mode		Information Category	Technical Notification		
Applicable Product	SH7080 Series	Lot No.	Reference Document	SH7080 Group User's Manual: Hardware (R01UH0198EJ0500)		
		All lots				

A part of descriptions of FIFO internal serial communication interface (SCIF), for the applicable products above, in the section of break detection and processing in asynchronous mode contains unclear description and the description is corrected as shown below.

[Corrections in the User's Manual]

16.7.3 Break Detection and Processing

[Before Correction (p.859)]

Break signals can be detected by reading the RXD pin directly when a framing error (FER) is detected. In the break state the input from the RXD pin consists of all 0s, so the FER flag is set and the parity error flag (PER) may also be set.

Note that, although transfer of receive data to SCFRDR is halted in the break state, the SCIF receiver continues to operate.

[After Correction (p.859)]

When data containing a framing error is received and then space 0 (low level) is input for more than one frame length, a break (BRK) is detected. When a break is detected, not only the transfer of receive data (H'00) to SCFRDR but also the setting in SCRSR of serial data input on the RXD pin is stopped. If the RIE or REIE bit in SCSCR is set to 1, a break interrupt request (BRI) is issued. Reception resumes when the break ends and the receive signal is mark 1 (high level).

It is also possible to perform break detection by reading the value of the RXD pin directly when a framing error (FER) is detected. Use the port register to read the value of the RXD pin. In the break state the input from the RXD pin consists of all 0s, so the FER flag is set and the parity error flag (PER) may also be set.

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