Date: Jan. 20, 2023

# RENESAS TECHNICAL UPDATE

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| Product Category | MPU/MCU | | Document No. | TN-RL*-A0114A/E | Rev. | 1.00 |
|---|---|---|---|---|---|---|
| Title | Correction for Incorrect Description Notice RL78/G14 Descriptions in the User's Manual: Hardware Rev. 3.40 Changed | | Information Category | Technical Notification | | |
| Applicable Product | RL78/G14 Group | Lot No.<br>All lots | Reference Document | RL78/G14 User's Manual: Hardware Rev. 3.40<br>R01UH0186EJ0340 (Jun. 2022) | | |

This document describes misstatements found in the RL78/G14 User's Manual: Hardware Rev. 3.40 (R01UH0186EJ0340).

Corrections

| Applicable Item | Applicable Page | Contents |
|---|---|---|
| 10.3.4 Real-time clock control register 1 (RTCC1) | Page 561 | Incorrect descriptions revised |
| Figure 10 - 22. Procedure for Reading Real-time Clock | Page 573 | Incorrect descriptions revised |
| Figure 10 - 23. Procedure for Writing Real-time Clock | Page 574 | Incorrect descriptions revised |
| 34.3.2 Supply current characteristics | Page 1171 to Page 1182 | Incorrect descriptions revised |
| 35.3.2 Supply current characteristics | Page 1244 to Page 1255 | Incorrect descriptions revised |

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

| No. | Corrections and Applicable Items | | | Pages in this document for corrections |
|---|---|---|---|---|
| | Document No. | English | R01UH0186EJ0340 | |
| 1 | 10.3.4 Real-time clock control register 1 (RTCC1) | | Page 561 | Page 3 |
| 2 | Figure 10 - 22. Procedure for Reading Real-time Clock | | Page 573 | Page 4 |
| 3 | Figure 10 - 23. Procedure for Writing Real-time Clock | | Page 574 | Page 4 |
| 4 | 34.3.2 Supply current characteristics | | Page 1171 to Page 1182 | Page 5 to Page 13 |
| 5 | 35.3.2 Supply current characteristics | | Page 1244 to Page 1255 | Page 14 to Page 22 |

**Incorrect: Bold with underline**; Correct: Gray hatched

## Revision History

RL78/G14 Correction for incorrect description notice

| Document Number | Issue Date | Description |
|---|---|---|
| TN-RL*-A0114A/E | Jan. 20, 2023 | First edition issued<br>Corrections No.1 to No.5 revised (this document) |

## 1. 10.3.4 Real-time clock control register 1 (RTCC1) (Page 561)

Incorrect:

**Figure 10 - 6. Format of Real-time Clock Control Register 1 (RTCC1) (2/2)**

| RIFG | Constant-period interrupt status flag |
|---|---|
| 0 | Fixed-cycle interrupt is not generated. |
| 1 | Fixed-cycle interrupt is generated. |
| This flag indicates the status of generation of the fixed-cycle interrupt. When the fixed-cycle interrupt is generated, it is set to “1”.<br>This flag is cleared when “0” is written to it. Writing “1” to it is invalid. | |

| RWST | Wait status flag of real-time clock |
|---|---|
| 0 | Counter is operating. |
| 1 | Mode to read or write counter value |
| This status flag indicates whether the setting of the RWAIT bit is valid.<br>Before reading or writing the counter value, confirm that the value of this flag is 1. | |

| RWAIT | Wait control of real-time clock |
|---|---|
| 0 | Sets counter operation. |
| 1 | Stops SEC to YEAR counters. Mode to read or write counter value |
| This bit controls the operation of the counter.<br>Be sure to write “1” to it to read or write the counter value.<br>As the internal counter (16-bit) is continuing to run, complete reading or writing within one second and turn back to 0.<br>When RWAIT = 1, it takes up to one cycle of $f_{RTC}$ until the counter value can be read or written (RWST = 1).<br>When the internal counter (16-bit) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up.<br>However, when it wrote a value to second count register, it will not keep the overflow event. | |

Correct:

**Figure 10 - 6. Format of Real-time Clock Control Register 1 (RTCC1) (2/2)**

| RIFG | Constant-period interrupt status flag |
|---|---|
| 0 | Fixed-cycle interrupt is not generated. |
| 1 | Fixed-cycle interrupt is generated. |
| This flag indicates the status of generation of the fixed-cycle interrupt. When the fixed-cycle interrupt is generated, it is set to “1”.<br>This flag is cleared when “0” is written to it. Writing “1” to it is invalid. | |

| RWST | Wait status flag of real-time clock |
|---|---|
| 0 | Counter is operating. |
| 1 | Mode to read or write counter value |
| This status flag indicates whether the setting of the RWAIT bit is valid.<br>Before reading or writing the counter value, confirm that the value of this flag is 1. | |

| RWAIT | Wait control of real-time clock |
|---|---|
| 0 | Sets counter operation. |
| 1 | Stops SEC to YEAR counters. Mode to read or write counter value |
| This bit controls the operation of the counter.<br>Be sure to write “1” to it to read or write the counter value.<br>As the internal counter (16-bit) is continuing to run, complete reading or writing within one second and turn back to 0. When reading or writing to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second).<br>Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.<br>When RWAIT = 1, it takes up to one cycle of $f_{RTC}$ until the counter value can be read or written (RWST = 1).<br>When the internal counter (16-bit) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up.<br>However, when it wrote a value to second count register, it will not keep the overflow event. | |

## 2. Figure 10 - 22 Procedure for Reading Real-time Clock (Page 573)

Incorrect:

**Note** Be sure to confirm that RWST = 0 before setting HALT/STOP mode.

**Caution Complete the series of process of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second.**

**Remark** The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be read in any sequence. All the registers do not have to read and only some registers may be read.

Correct:

**Note** Be sure to confirm that RWST = 0 before setting HALT/STOP mode.

**Caution Complete the series of process of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second. When reading to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.**

**Remark** The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be read in any sequence. All the registers do not have to read and only some registers may be read.

## 3. Figure 10 - 23 Procedure for Writing Real-time Clock (Page 574)

Incorrect:

**Note** Be sure to confirm that RWST = 0 before setting HALT/STOP mode.

**Cautions 1. Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second.**

**Cautions 2. When changing the values of the SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR register while the counter operates (RTCE = 1), rewrite the values of the MIN register after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, clear the WAFG, RIFG and RTCIF flags after rewriting the MIN register.**

**Remark** The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be written in any sequence.

All the registers do not have to be set and only some registers may be written.

Correct:

**Note** Be sure to confirm that RWST = 0 before setting HALT/STOP mode.

**Cautions 1. Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second. When writing to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.**

**Cautions 2. When changing the values of the SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR register while the counter operates (RTCE = 1), rewrite the values of the MIN register after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, clear the WAFG, RIFG and RTCIF flags after rewriting the MIN register.**

**Remark** The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be written in any sequence.

All the registers do not have to be set and only some registers may be written.

## 4. 34.3.2 Supply current characteristics (Page 1171 to Page 1182)

Incorrect:

**34.3.2 Supply current characteristics**

**(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products**

**($T_A$ = −40 to +85° C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | IDD1 | Operating mode | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.4 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.4 | | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.1 | | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.1 | | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +70°C | Normal operation | Square wave input | | 4.8 | 7.5 | |
| | | | | | | Resonator connection | | 4.8 | 7.5 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | 5.4 | 8.9 | |
| | | | | | | Resonator connection | | 5.4 | 8.9 | |

**Notes 1.** Total current flowing into $V_{DD}$ and $EV_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$ or $V_{SS}$, $EV_{SS0}$. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.**

**Notes 2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Notes 3.** When high-speed system clock and subsystem clock are stopped.

**Notes 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). **However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.**

**Notes 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remarks 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remarks 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remarks 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remarks 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

Correct:

**34.3.2 Supply current characteristics**

**(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products**

**($T_A$ = −40 to +85° C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | IDD1 | Operating mode | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.4 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.4 | | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.1 | | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.1 | | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +70°C | Normal operation | Square wave input | | 4.8 | 7.5 | |
| | | | | | | Resonator connection | | 4.8 | 7.5 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | 5.4 | 8.9 | |
| | | | | | | Resonator connection | | 5.4 | 8.9 | |

**Notes 1.** Total current flowing into $V_{DD}$ and $EV_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$ or $V_{SS}$, $EV_{SS0}$. The following points apply in the HS (high-speed main), LS (low-speed main), and LV (low-voltage main) modes.
- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

**Notes 2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Notes 3.** When high-speed system clock and subsystem clock are stopped.

**Notes 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).

**Notes 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remarks 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remarks 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remarks 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remarks 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

**(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products**

**($T_A$ = −40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 7 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.80 | 3.09 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.80 | 3.09 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.49 | 2.40 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.49 | 2.40 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.62 | 2.40 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.62 | 2.40 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.4 | 1.83 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.4 | 1.83 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.37 | 1.38 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.37 | 1.38 | |
| | | | LS (low-speed main) mode Note 7 | $f_{HOCO}$ = 8 MHz, $f_{IH}$ = 8 MHz Note 4 | $V_{DD}$ = 3.0 V | | 260 | 710 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 260 | 710 | |
| | | | LV (low-voltage main) mode Note 7 | $f_{HOCO}$ = 4 MHz, $f_{IH}$ = 4 MHz Note 4 | $V_{DD}$ = 3.0 V | | 420 | 700 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 420 | 700 | |
| | | | HS (high-speed main) mode Note 7 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.28 | 1.55 | mA |
| | | | | | Resonator connection | | 0.40 | 1.74 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.28 | 1.55 | |
| | | | | | Resonator connection | | 0.40 | 1.74 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.19 | 0.86 | |
| | | | | | Resonator connection | | 0.25 | 0.93 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.19 | 0.86 | |
| | | | | | Resonator connection | | 0.25 | 0.93 | |
| | | | LS (low-speed main) mode Note 7 | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 95 | 550 | μA |
| | | | | | Resonator connection | | 140 | 590 | |
| | | | | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 2.0 V | Square wave input | | 95 | 550 | |
| | | | | | Resonator connection | | 140 | 590 | |
| | $I_{DD3}$ Note 6 | STOP mode Note 8 | $T_A$ = -40°C | | | | 0.18 | 0.51 | μA |
| | | | $T_A$ = +25°C | | | | 0.24 | 0.51 | |
| | | | $T_A$ = +50°C | | | | 0.29 | 1.10 | |
| | | | $T_A$ = +70°C | | | | 0.41 | 1.90 | |
| | | | $T_A$ = +85°C | | | | 0.90 | 3.30 | |

**Notes 1.** Total current flowing into $V_{DD}$ and $EV_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$ or $V_{SS}$, $EV_{SS0}$. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.**

**(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products**

**($T_A$ = −40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 6 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.80 | 3.09 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.80 | 3.09 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.49 | 2.40 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.49 | 2.40 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.62 | 2.40 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.62 | 2.40 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.4 | 1.83 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.4 | 1.83 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.37 | 1.38 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.37 | 1.38 | |
| | | | LS (low-speed main) mode Note 6 | $f_{HOCO}$ = 8 MHz, $f_{IH}$ = 8 MHz Note 4 | $V_{DD}$ = 3.0 V | | 260 | 710 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 260 | 710 | |
| | | | LV (low-voltage main) mode Note 6 | $f_{HOCO}$ = 4 MHz, $f_{IH}$ = 4 MHz Note 4 | $V_{DD}$ = 3.0 V | | 420 | 700 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 420 | 700 | |
| | | | HS (high-speed main) mode Note 6 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.28 | 1.55 | mA |
| | | | | | Resonator connection | | 0.40 | 1.74 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.28 | 1.55 | |
| | | | | | Resonator connection | | 0.40 | 1.74 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.19 | 0.86 | |
| | | | | | Resonator connection | | 0.25 | 0.93 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.19 | 0.86 | |
| | | | | | Resonator connection | | 0.25 | 0.93 | |
| | | | LS (low-speed main) mode Note 6 | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 95 | 550 | μA |
| | | | | | Resonator connection | | 140 | 590 | |
| | | | | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 2.0 V | Square wave input | | 95 | 550 | |
| | | | | | Resonator connection | | 140 | 590 | |
| | $I_{DD3}$ | STOP mode Note 7 | $T_A$ = -40°C | | | | 0.18 | 0.51 | μA |
| | | | $T_A$ = +25°C | | | | 0.24 | 0.51 | |
| | | | $T_A$ = +50°C | | | | 0.29 | 1.10 | |
| | | | $T_A$ = +70°C | | | | 0.41 | 1.90 | |
| | | | $T_A$ = +85°C | | | | 0.90 | 3.30 | |

**Notes 1.** Total current flowing into $V_{DD}$ and $EV_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$ or $V_{SS}$, $EV_{SS0}$. The following points apply in the HS (high-speed main), LS (low-speed main), and LV (low-voltage main) modes.

- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

In the STOP mode, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules.

**Notes 2.** During HALT instruction execution by flash memory.
**Notes 3.** When high-speed on-chip oscillator and subsystem clock are stopped.
**Notes 4.** When high-speed system clock and subsystem clock are stopped.
**Notes 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). **The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.**
**Notes 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.**
**Notes 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

| | |
|---|---|
| HS (high-speed main) mode: | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz |
| | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz |
| LS (low-speed main) mode: | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz |
| LV (low-voltage main) mode: | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz |

**Notes 8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
**Remarks 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)
**Remarks 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)
**Remarks 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)
**Remarks 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

**Notes 2.** During HALT instruction execution by flash memory.
**Notes 3.** When high-speed on-chip oscillator and subsystem clock are stopped.
**Notes 4.** When high-speed system clock and subsystem clock are stopped.
**Notes 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1).
**Notes 6.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

| | |
|---|---|
| HS (high-speed main) mode: | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz |
| | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz |
| LS (low-speed main) mode: | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz |
| LV (low-voltage main) mode: | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz |

**Notes 7.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
**Remarks 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)
**Remarks 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)
**Remarks 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)
**Remarks 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

**(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products**

**($T_A$ = −40 to +85° C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operating mode | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | | 2.6 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | | 2.6 | | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | | 2.3 | | |
| | | | | | | $V_{DD}$ = 3.0 V | | | 2.3 | | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +70°C | Normal operation | Square wave input | | | 5.5 | 10.5 | |
| | | | | | | Resonator connection | | | 5.5 | 10.5 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | | 6.5 | 14.5 | |
| | | | | | | Resonator connection | | | 6.5 | 14.5 | |

**Notes 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.**

**Notes 2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Notes 3.** When high-speed system clock and subsystem clock are stopped.

**Notes 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). **However, not including the current flowing into the 12-bit interval timer and watchdog timer.**

**Notes 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remarks 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remarks 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remarks 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remarks 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

**(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products**

**($T_A$ = −40 to +85° C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operating mode | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | | 2.6 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | | 2.6 | | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | | 2.3 | | |
| | | | | | | $V_{DD}$ = 3.0 V | | | 2.3 | | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +70°C | Normal operation | Square wave input | | | 5.5 | 10.5 | |
| | | | | | | Resonator connection | | | 5.5 | 10.5 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | | 6.5 | 14.5 | |
| | | | | | | Resonator connection | | | 6.5 | 14.5 | |

**Notes 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The following points apply in the HS (high-speed main), LS (low-speed main), and LV (low-voltage main) modes.

- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

**Notes 2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Notes 3.** When high-speed system clock and subsystem clock are stopped.

**Notes 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).

**Notes 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remarks 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remarks 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remarks 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remarks 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

**(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products**

**($T_A$ = −40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode ~~Note 7~~ | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.79 | 3.32 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.79 | 3.32 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.49 | 2.63 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.49 | 2.63 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.62 | 2.57 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.62 | 2.57 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.4 | 2.00 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.4 | 2.00 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.38 | 1.49 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.38 | 1.49 | |
| | | | LS (low-speed main) mode ~~Note 7~~ | $f_{HOCO}$ = 8 MHz, $f_{IH}$ = 8 MHz Note 4 | $V_{DD}$ = 3.0 V | | 250 | 800 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 250 | 800 | |
| | | | LV (low-voltage main) mode ~~Note 7~~ | $f_{HOCO}$ = 4 MHz, $f_{IH}$ = 4 MHz Note 4 | $V_{DD}$ = 3.0 V | | 420 | 755 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 420 | 755 | |
| | | | HS (high-speed main) mode ~~Note 7~~ | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.30 | 1.63 | mA |
| | | | | | Resonator connection | | 0.40 | 1.85 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.30 | 1.63 | |
| | | | | | Resonator connection | | 0.40 | 1.85 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.20 | 0.89 | |
| | | | | | Resonator connection | | 0.25 | 0.97 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.20 | 0.89 | |
| | | | | | Resonator connection | | 0.25 | 0.97 | |
| | | | LS (low-speed main) mode ~~Note 7~~ | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 110 | 580 | μA |
| | | | | | Resonator connection | | 140 | 630 | |
| | | | | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 2.0 V | Square wave input | | 110 | 580 | |
| | | | | | Resonator connection | | 140 | 630 | |
| | $I_{DD3}$ ~~Note 6~~ | STOP mode ~~Note 8~~ | $T_A$ = -40°C | | | | 0.19 | 0.57 | μA |
| | | | $T_A$ = +25°C | | | | 0.25 | 0.57 | |
| | | | $T_A$ = +50°C | | | | 0.33 | 2.26 | |
| | | | $T_A$ = +70°C | | | | 0.52 | 3.99 | |
| | | | $T_A$ = +85°C | | | | 1.46 | 8.00 | |

**Notes 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. **~~The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.~~**

**Notes 2.** During HALT instruction execution by flash memory.

**(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products**

**($T_A$ = −40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 6 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.79 | 3.32 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.79 | 3.32 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.49 | 2.63 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.49 | 2.63 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.62 | 2.57 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.62 | 2.57 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.4 | 2.00 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.4 | 2.00 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.38 | 1.49 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.38 | 1.49 | |
| | | | LS (low-speed main) mode Note 6 | $f_{HOCO}$ = 8 MHz, $f_{IH}$ = 8 MHz Note 4 | $V_{DD}$ = 3.0 V | | 250 | 800 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 250 | 800 | |
| | | | LV (low-voltage main) mode Note 6 | $f_{HOCO}$ = 4 MHz, $f_{IH}$ = 4 MHz Note 4 | $V_{DD}$ = 3.0 V | | 420 | 755 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 420 | 755 | |
| | | | HS (high-speed main) mode Note 6 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.30 | 1.63 | mA |
| | | | | | Resonator connection | | 0.40 | 1.85 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.30 | 1.63 | |
| | | | | | Resonator connection | | 0.40 | 1.85 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.20 | 0.89 | |
| | | | | | Resonator connection | | 0.25 | 0.97 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.20 | 0.89 | |
| | | | | | Resonator connection | | 0.25 | 0.97 | |
| | | | LS (low-speed main) mode Note 6 | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 110 | 580 | μA |
| | | | | | Resonator connection | | 140 | 630 | |
| | | | | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 2.0 V | Square wave input | | 110 | 580 | |
| | | | | | Resonator connection | | 140 | 630 | |
| | $I_{DD3}$ | STOP mode Note 7 | $T_A$ = -40°C | | | | 0.19 | 0.57 | μA |
| | | | $T_A$ = +25°C | | | | 0.25 | 0.57 | |
| | | | $T_A$ = +50°C | | | | 0.33 | 2.26 | |
| | | | $T_A$ = +70°C | | | | 0.52 | 3.99 | |
| | | | $T_A$ = +85°C | | | | 1.46 | 8.00 | |

**Notes 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The following points apply in the HS (high-speed main), LS (low-speed main), and LV (low-voltage main) modes.
- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

In the STOP mode, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules.

**Notes 2.** During HALT instruction execution by flash memory.

**Notes 3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Notes 4.** When high-speed system clock and subsystem clock are stopped.

**Notes 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). **The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.**

**Notes 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.**

**Notes 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

| | |
|---|---|
| HS (high-speed main) mode: | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz |
| | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz |
| LS (low-speed main) mode: | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz |
| LV (low-voltage main) mode: | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz |

**Notes 8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remarks 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remarks 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remarks 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remarks 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

**Notes 3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Notes 4.** When high-speed system clock and subsystem clock are stopped.

**Notes 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1).

**Notes 6.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

| | |
|---|---|
| HS (high-speed main) mode: | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz |
| | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz |
| LS (low-speed main) mode: | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz |
| LV (low-voltage main) mode: | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz |

**Notes 7.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remarks 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remarks 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remarks 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remarks 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

**(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products**

**($T_A$ = −40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operating mode | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.9 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.9 | | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.5 | | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.5 | | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +70°C | Normal operation | Square wave input | | 5.9 | 13.2 | |
| | | | | | | Resonator connection | | 6.0 | 13.2 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | 6.8 | 17.5 | |
| | | | | | | Resonator connection | | 6.9 | 17.5 | |

**Notes 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.**

**Notes 2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Notes 3.** When high-speed system clock and subsystem clock are stopped.

**Notes 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). **However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.**

**Notes 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remarks 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remarks 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remarks 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remarks 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

**(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products**

**($T_A$ = −40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operating mode | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.9 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.9 | | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.5 | | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.5 | | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +70°C | Normal operation | Square wave input | | 5.9 | 13.2 | |
| | | | | | | Resonator connection | | 6.0 | 13.2 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | 6.8 | 17.5 | |
| | | | | | | Resonator connection | | 6.9 | 17.5 | |

**Notes 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The following points apply in the HS (high-speed main), LS (low-speed main), and LV (low-voltage main) modes.
• The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
• The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.
In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

**Notes 2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Notes 3.** When high-speed system clock and subsystem clock are stopped.

**Notes 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).

**Notes 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remarks 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remarks 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remarks 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remarks 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

**(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products**

**($T_A$ = −40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode ~~Note 7~~ | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.93 | 3.32 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.93 | 3.32 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.5 | 2.63 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.5 | 2.63 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.72 | 2.60 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.72 | 2.60 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.42 | 2.03 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.42 | 2.03 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.39 | 1.50 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.39 | 1.50 | |
| | | | LS (low-speed main) mode ~~Note 7~~ | $f_{HOCO}$ = 8 MHz, $f_{IH}$ = 8 MHz Note 4 | $V_{DD}$ = 3.0 V | | 270 | 800 | µA |
| | | | | | $V_{DD}$ = 2.0 V | | 270 | 800 | |
| | | | LV (low-voltage main) mode ~~Note 7~~ | $f_{HOCO}$ = 4 MHz, $f_{IH}$ = 4 MHz Note 4 | $V_{DD}$ = 3.0 V | | 450 | 755 | µA |
| | | | | | $V_{DD}$ = 2.0 V | | 450 | 755 | |
| | | | HS (high-speed main) mode ~~Note 7~~ | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.31 | 1.69 | mA |
| | | | | | Resonator connection | | 0.41 | 1.91 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.31 | 1.69 | |
| | | | | | Resonator connection | | 0.41 | 1.91 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.21 | 0.94 | |
| | | | | | Resonator connection | | 0.26 | 1.02 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.21 | 0.94 | |
| | | | | | Resonator connection | | 0.26 | 1.02 | |
| | | | LS (low-speed main) mode ~~Note 7~~ | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 110 | 610 | µA |
| | | | | | Resonator connection | | 150 | 660 | |
| | | | | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 2.0 V | Square wave input | | 110 | 610 | |
| | | | | | Resonator connection | | 150 | 660 | |
| | $I_{DD3}$ ~~Note 6~~ | STOP mode ~~Note 8~~ | $T_A$ = -40°C | | | | 0.19 | | µA |
| | | | $T_A$ = +25°C | | | | 0.30 | 0.59 | |
| | | | $T_A$ = +50°C | | | | 0.41 | 3.42 | |
| | | | $T_A$ = +70°C | | | | 0.80 | 6.03 | |
| | | | $T_A$ = +85°C | | | | 1.53 | 10.39 | |

**Notes 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.**

**(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products**

**($T_A$ = −40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 6 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.93 | 3.32 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.93 | 3.32 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.5 | 2.63 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.5 | 2.63 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.72 | 2.60 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.72 | 2.60 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.42 | 2.03 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.42 | 2.03 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.39 | 1.50 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.39 | 1.50 | |
| | | | LS (low-speed main) mode Note 6 | $f_{HOCO}$ = 8 MHz, $f_{IH}$ = 8 MHz Note 4 | $V_{DD}$ = 3.0 V | | 270 | 800 | µA |
| | | | | | $V_{DD}$ = 2.0 V | | 270 | 800 | |
| | | | LV (low-voltage main) mode Note 6 | $f_{HOCO}$ = 4 MHz, $f_{IH}$ = 4 MHz Note 4 | $V_{DD}$ = 3.0 V | | 450 | 755 | µA |
| | | | | | $V_{DD}$ = 2.0 V | | 450 | 755 | |
| | | | HS (high-speed main) mode Note 6 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.31 | 1.69 | mA |
| | | | | | Resonator connection | | 0.41 | 1.91 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.31 | 1.69 | |
| | | | | | Resonator connection | | 0.41 | 1.91 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.21 | 0.94 | |
| | | | | | Resonator connection | | 0.26 | 1.02 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.21 | 0.94 | |
| | | | | | Resonator connection | | 0.26 | 1.02 | |
| | | | LS (low-speed main) mode Note 6 | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 110 | 610 | µA |
| | | | | | Resonator connection | | 150 | 660 | |
| | | | | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 2.0 V | Square wave input | | 110 | 610 | |
| | | | | | Resonator connection | | 150 | 660 | |
| | $I_{DD3}$ | STOP mode Note 7 | $T_A$ = -40°C | | | | 0.19 | | µA |
| | | | $T_A$ = +25°C | | | | 0.30 | 0.59 | |
| | | | $T_A$ = +50°C | | | | 0.41 | 3.42 | |
| | | | $T_A$ = +70°C | | | | 0.80 | 6.03 | |
| | | | $T_A$ = +85°C | | | | 1.53 | 10.39 | |

**Notes 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The following points apply in the HS (high-speed main), LS (low-speed main), and LV (low-voltage main) modes.

- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

In the STOP mode, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules.

**Notes 2.** During HALT instruction execution by flash memory.
**Notes 3.** When high-speed on-chip oscillator and subsystem clock are stopped.
**Notes 4.** When high-speed system clock and subsystem clock are stopped.
**Notes 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). **The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.**
**Notes 6.** **Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.**
**Notes 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

| | |
|---|---|
| HS (high-speed main) mode: | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz |
| | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz |
| LS (low-speed main) mode: | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz |
| LV (low-voltage main) mode: | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz |

**Notes 8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
**Remarks 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)
**Remarks 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)
**Remarks 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)
**Remarks 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

**Notes 2.** During HALT instruction execution by flash memory.
**Notes 3.** When high-speed on-chip oscillator and subsystem clock are stopped.
**Notes 4.** When high-speed system clock and subsystem clock are stopped.
**Notes 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1).
**Notes 6.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

| | |
|---|---|
| HS (high-speed main) mode: | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz |
| | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz |
| LS (low-speed main) mode: | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz |
| LV (low-voltage main) mode: | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz |

**Notes 7.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
**Remarks 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)
**Remarks 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)
**Remarks 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)
**Remarks 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

## 5. 35.3.2 Supply current characteristics (Page 1244 to Page 1255)

Incorrect:

**35.3.2 Supply current characteristics**

**(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products**

**($T_A$ = −40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, VSS = $EV_{SS0}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | IDD1 | Operating mode | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.4 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.4 | | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.1 | | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.1 | | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | 5.4 | 8.9 | |
| | | | | | | Resonator connection | | 5.4 | 8.9 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +105°C | Normal operation | Square wave input | | 7.2 | 21.0 | |
| | | | | | | Resonator connection | | 7.3 | 21.1 | |

**Notes 1.** Total current flowing into $V_{DD}$ and $EV_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$ or $V_{SS}$, $EV_{SS0}$. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.**

**Notes 2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Notes 3.** When high-speed system clock and subsystem clock are stopped.

**Notes 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). **However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.**

**Notes 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remarks 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remarks 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remarks 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remarks 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

Correct:

**35.3.2 Supply current characteristics**

**(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products**

**(TA = −40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | IDD1 | Operating mode | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.4 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.4 | | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.1 | | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.1 | | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | 5.4 | 8.9 | |
| | | | | | | Resonator connection | | 5.4 | 8.9 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +105°C | Normal operation | Square wave input | | 7.2 | 21.0 | |
| | | | | | | Resonator connection | | 7.3 | 21.1 | |

**Notes 1.** Total current flowing into $V_{DD}$ and $EV_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$ or $V_{SS}$, $EV_{SS0}$. The following points apply in the HS (high-speed main) mode.
- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

**Notes 2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Notes 3.** When high-speed system clock and subsystem clock are stopped.

**Notes 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).

**Notes 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remarks 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remarks 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remarks 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remarks 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

**(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products**

**($T_A$ = −40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, VSS = $EV_{SS0}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode ~~Note 7~~ | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.80 | 4.36 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.80 | 4.36 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.49 | 3.67 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.49 | 3.67 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.62 | 3.42 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.62 | 3.42 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.4 | 2.85 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.4 | 2.85 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.37 | 2.08 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.37 | 2.08 | |
| | | | HS (high-speed main) mode ~~Note 7~~ | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.28 | 2.45 | mA |
| | | | | | Resonator connection | | 0.40 | 2.57 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.28 | 2.45 | |
| | | | | | Resonator connection | | 0.40 | 2.57 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.19 | 1.28 | |
| | | | | | Resonator connection | | 0.25 | 1.36 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.19 | 1.28 | |
| | | | | | Resonator connection | | 0.25 | 1.36 | |
| | $I_{DD3}$ ~~Note 6~~ | STOP mode ~~Note 8~~ | $T_A$ = -40°C | | | | 0.18 | 0.51 | μA |
| | | | $T_A$ = +25°C | | | | 0.24 | 0.51 | |
| | | | $T_A$ = +50°C | | | | 0.29 | 1.10 | |
| | | | $T_A$ = +70°C | | | | 0.41 | 1.90 | |
| | | | $T_A$ = +85°C | | | | 0.90 | 3.30 | |
| | | | $T_A$ = +105°C | | | | 3.10 | 17.00 | |

**Notes 1.** Total current flowing into $V_{DD}$ and $EV_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$ or $V_{SS}$, $EV_{SS0}$. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.**

**Notes 2.** During HALT instruction execution by flash memory.

**Notes 3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Notes 4.** When high-speed system clock and subsystem clock are stopped.

**Notes 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). **The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.**

**(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products**

**($T_A$ = −40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, VSS = $EV_{SS0}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 6 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.80 | 4.36 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.80 | 4.36 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.49 | 3.67 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.49 | 3.67 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.62 | 3.42 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.62 | 3.42 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.4 | 2.85 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.4 | 2.85 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.37 | 2.08 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.37 | 2.08 | |
| | | | HS (high-speed main) mode Note 6 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.28 | 2.45 | mA |
| | | | | | Resonator connection | | 0.40 | 2.57 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.28 | 2.45 | |
| | | | | | Resonator connection | | 0.40 | 2.57 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.19 | 1.28 | |
| | | | | | Resonator connection | | 0.25 | 1.36 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.19 | 1.28 | |
| | | | | | Resonator connection | | 0.25 | 1.36 | |
| | $I_{DD3}$ | STOP mode Note 7 | $T_A$ = -40°C | | | | 0.18 | 0.51 | μA |
| | | | $T_A$ = +25°C | | | | 0.24 | 0.51 | |
| | | | $T_A$ = +50°C | | | | 0.29 | 1.10 | |
| | | | $T_A$ = +70°C | | | | 0.41 | 1.90 | |
| | | | $T_A$ = +85°C | | | | 0.90 | 3.30 | |
| | | | $T_A$ = +105°C | | | | 3.10 | 17.00 | |

**Notes 1.** Total current flowing into $V_{DD}$ and $EV_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$ or $V_{SS}$, $EV_{SS0}$. The following points apply in the HS (high-speed main) mode.

- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

In the STOP mode, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules.

**Notes 2.** During HALT instruction execution by flash memory.

**Notes 3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Notes 4.** When high-speed system clock and subsystem clock are stopped.

**Notes 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1).

**Notes 6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**Notes 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Notes 8.** Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
**Remarks 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)
**Remarks 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)
**Remarks 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)
**Remarks 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

**Notes 6.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Notes 7.** Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
**Remarks 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)
**Remarks 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)
**Remarks 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)
**Remarks 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

**(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products**

**($T_A$ = −40 to +105° C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operating mode | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.6 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.6 | | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.3 | | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.3 | | |
| | | | | | | Resonator connection | | 6.5 | 14.5 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +105°C | Normal operation | Square wave input | | 13.0 | 58.0 | |
| | | | | | | Resonator connection | | 13.0 | 58.0 | |

**Notes 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.**

**Notes 2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Notes 3.** When high-speed system clock and subsystem clock are stopped.

**Notes 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). **However, not including the current flowing into the 12-bit interval timer and watchdog timer.**

**Notes 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remarks 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remarks 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remarks 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remarks 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

**(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products**

**($T_A$ = −40 to +105° C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operating mode | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.6 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.6 | | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.3 | | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.3 | | |
| | | | | | | Resonator connection | | 6.5 | 14.5 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +105°C | Normal operation | Square wave input | | 13.0 | 58.0 | |
| | | | | | | Resonator connection | | 13.0 | 58.0 | |

**Notes 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The following points apply in the HS (high-speed main) mode.
- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

**Notes 2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Notes 3.** When high-speed system clock and subsystem clock are stopped.

**Notes 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).

**Notes 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remarks 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remarks 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remarks 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remarks 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

**(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products**

**($T_A$ = −40 to +105° C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 7 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.79 | 4.86 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.79 | 4.86 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.49 | 4.17 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.49 | 4.17 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.62 | 3.82 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.62 | 3.82 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.4 | 3.25 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.4 | 3.25 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.38 | 2.28 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.38 | 2.28 | |
| | | | HS (high-speed main) mode Note 7 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.30 | 2.65 | mA |
| | | | | | Resonator connection | | 0.40 | 2.77 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.30 | 2.65 | |
| | | | | | Resonator connection | | 0.40 | 2.77 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.20 | 1.36 | |
| | | | | | Resonator connection | | 0.25 | 1.46 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.20 | 1.36 | |
| | | | | | Resonator connection | | 0.25 | 1.46 | |
| | $I_{DD3}$ Note 6 | STOP mode Note 8 | $T_A$ = -40°C | | | | 0.19 | 0.57 | μA |
| | | | $T_A$ = +25°C | | | | 0.25 | 0.57 | |
| | | | $T_A$ = +50°C | | | | 0.33 | 2.26 | |
| | | | $T_A$ = +70°C | | | | 0.52 | 3.99 | |
| | | | $T_A$ = +85°C | | | | 1.46 | 8.00 | |
| | | | $T_A$ = +105°C | | | | 5.50 | 50.00 | |

**Notes 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.**

**Notes 2.** During HALT instruction execution by flash memory.

**Notes 3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Notes 4.** When high-speed system clock and subsystem clock are stopped.

**Notes 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). **The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.**

**Notes 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.**

**(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products**

**($T_A$ = −40 to +105° C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 6 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.79 | 4.86 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.79 | 4.86 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.49 | 4.17 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.49 | 4.17 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.62 | 3.82 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.62 | 3.82 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.4 | 3.25 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.4 | 3.25 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.38 | 2.28 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.38 | 2.28 | |
| | | | HS (high-speed main) mode Note 6 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.30 | 2.65 | mA |
| | | | | | Resonator connection | | 0.40 | 2.77 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.30 | 2.65 | |
| | | | | | Resonator connection | | 0.40 | 2.77 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.20 | 1.36 | |
| | | | | | Resonator connection | | 0.25 | 1.46 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.20 | 1.36 | |
| | | | | | Resonator connection | | 0.25 | 1.46 | |
| | $I_{DD3}$ | STOP mode Note 7 | $T_A$ = -40°C | | | | 0.19 | 0.57 | μA |
| | | | $T_A$ = +25°C | | | | 0.25 | 0.57 | |
| | | | $T_A$ = +50°C | | | | 0.33 | 2.26 | |
| | | | $T_A$ = +70°C | | | | 0.52 | 3.99 | |
| | | | $T_A$ = +85°C | | | | 1.46 | 8.00 | |
| | | | $T_A$ = +105°C | | | | 5.50 | 50.00 | |

**Notes 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The following points apply in the HS (high-speed main) mode.
- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

In the STOP mode, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules.

**Notes 2.** During HALT instruction execution by flash memory.

**Notes 3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Notes 4.** When high-speed system clock and subsystem clock are stopped.

**Notes 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1).

**Notes 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Notes 8.** Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
**Remarks 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)
**Remarks 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)
**Remarks 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)
**Remarks 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

**Notes 6.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Notes 7.** Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
**Remarks 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)
**Remarks 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)
**Remarks 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)
**Remarks 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

**(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products**

**($T_A$ = −40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operating mode | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.9 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.9 | | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.5 | | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.5 | | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | 6.8 | 17.5 | |
| | | | | | | Resonator connection | | 6.9 | 17.5 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +105°C | Normal operation | Square wave input | | 15.5 | 77.8 | |
| | | | | | | Resonator connection | | 15.5 | 77.8 | |

**Notes 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.**

**Notes 2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Notes 3.** When high-speed system clock and subsystem clock are stopped.

**Notes 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). **However, not including the current flowing into the 12-bit interval timer and watchdog timer.**

**Notes 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remarks 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remarks 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remarks 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remarks 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

**(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products**

**($T_A$ = −40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operating mode | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.9 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.9 | | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.5 | | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.5 | | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | 6.8 | 17.5 | |
| | | | | | | Resonator connection | | 6.9 | 17.5 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +105°C | Normal operation | Square wave input | | 15.5 | 77.8 | |
| | | | | | | Resonator connection | | 15.5 | 77.8 | |

**Notes 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The following points apply in the HS (high-speed main) mode.

- The currents in the "TYP." column do not include the operating currents of the peripheral modules.
- The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

**Notes 2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Notes 3.** When high-speed system clock and subsystem clock are stopped.

**Notes 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).

**Notes 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remarks 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remarks 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remarks 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remarks 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

**(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products**

**($T_A$ = −40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode ~~Note 7~~ | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.93 | 5.16 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.93 | 5.16 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.5 | 4.47 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.5 | 4.47 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.72 | 4.08 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.72 | 4.08 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.42 | 3.51 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.42 | 3.51 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.39 | 2.38 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.39 | 2.38 | |
| | | | HS (high-speed main) mode ~~Note 7~~ | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.31 | 2.83 | mA |
| | | | | | Resonator connection | | 0.41 | 2.92 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.31 | 2.83 | |
| | | | | | Resonator connection | | 0.41 | 2.92 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.21 | 1.46 | |
| | | | | | Resonator connection | | 0.26 | 1.57 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.21 | 1.46 | |
| | | | | | Resonator connection | | 0.26 | 1.57 | |
| | $I_{DD3}$ ~~Note 5~~ | STOP mode ~~Note 8~~ | $T_A$ = -40°C | | | | 0.19 | 0.63 | μA |
| | | | $T_A$ = +25°C | | | | 0.30 | 0.63 | |
| | | | $T_A$ = +50°C | | | | 0.41 | 3.47 | |
| | | | $T_A$ = +70°C | | | | 0.80 | 6.08 | |
| | | | $T_A$ = +85°C | | | | 1.53 | 10.44 | |
| | | | $T_A$ = +105°C | | | | 6.50 | 67.14 | |

**Notes 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.**

**Notes 2.** During HALT instruction execution by flash memory.

**Notes 3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Notes 4.** When high-speed system clock and subsystem clock are stopped.

**Notes 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). **The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.**

**Notes 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.**

**(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products**

**($T_A$ = −40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 6 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.93 | 5.16 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.93 | 5.16 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.5 | 4.47 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.5 | 4.47 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.72 | 4.08 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.72 | 4.08 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.42 | 3.51 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.42 | 3.51 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.39 | 2.38 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.39 | 2.38 | |
| | | | HS (high-speed main) mode Note 6 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.31 | 2.83 | mA |
| | | | | | Resonator connection | | 0.41 | 2.92 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.31 | 2.83 | |
| | | | | | Resonator connection | | 0.41 | 2.92 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.21 | 1.46 | |
| | | | | | Resonator connection | | 0.26 | 1.57 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.21 | 1.46 | |
| | | | | | Resonator connection | | 0.26 | 1.57 | |
| | $I_{DD3}$ | STOP mode Note 7 | $T_A$ = -40°C | | | | 0.19 | 0.63 | μA |
| | | | $T_A$ = +25°C | | | | 0.30 | 0.63 | |
| | | | $T_A$ = +50°C | | | | 0.41 | 3.47 | |
| | | | $T_A$ = +70°C | | | | 0.80 | 6.08 | |
| | | | $T_A$ = +85°C | | | | 1.53 | 10.44 | |
| | | | $T_A$ = +105°C | | | | 6.50 | 67.14 | |

**Notes 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The following points apply in the HS (high-speed main) mode.
- The currents in the "TYP." column do not include the operating currents of the peripheral modules.
- The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.
In the STOP mode, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules.

**Notes 2.** During HALT instruction execution by flash memory.

**Notes 3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Notes 4.** When high-speed system clock and subsystem clock are stopped.

**Notes 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1).

**Notes 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Notes 8.** Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
**Remarks 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)
**Remarks 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)
**Remarks 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)
**Remarks 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

**Notes 6.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Notes 7.** Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
**Remarks 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)
**Remarks 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)
**Remarks 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)
**Remarks 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C