Date: Nov. 24, 2020

# RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

| Product Category | MPU/MCU | | Document No. | TN-RH8-B0245B/E | Rev. | 2.00 |
|---|---|---|---|---|---|---|
| Title | RH850/C1x User's Manual Hardware Rev.1.60 Errata | | Information Category | Technical Notification | | |
| Applicable Product | RH850/C1x | Lot No.<br>- | Reference Document | Refer to the below | | |

1. Explanation

This document is errata of RH850/C1x User's Manual Hardware Rev.1.60.

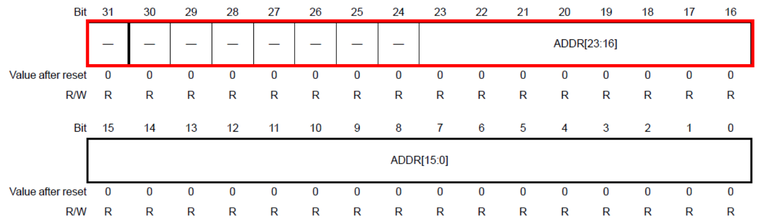
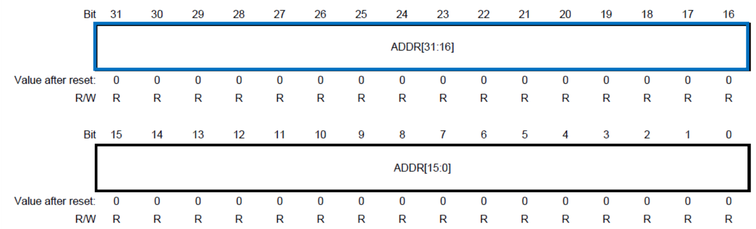
No.1 to No.9 have already been notified on the previous edition of TN-RH8-B0245A/E.

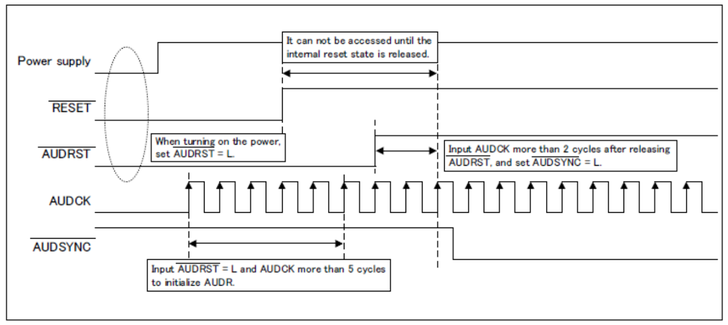
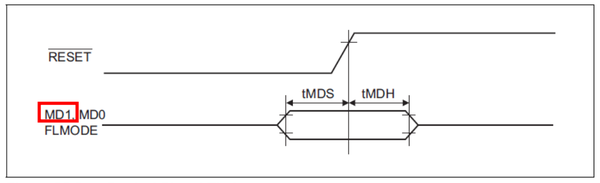
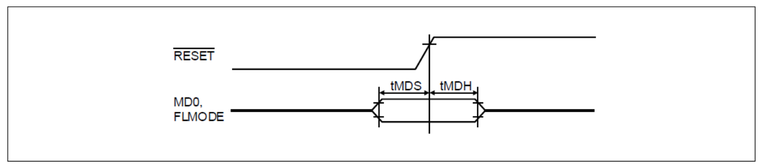
No.10 to No.39 are additional items.

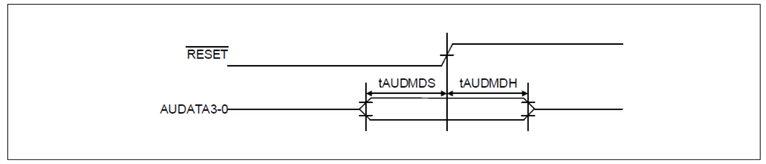
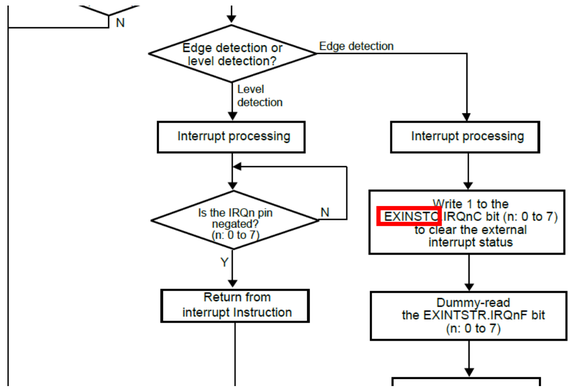
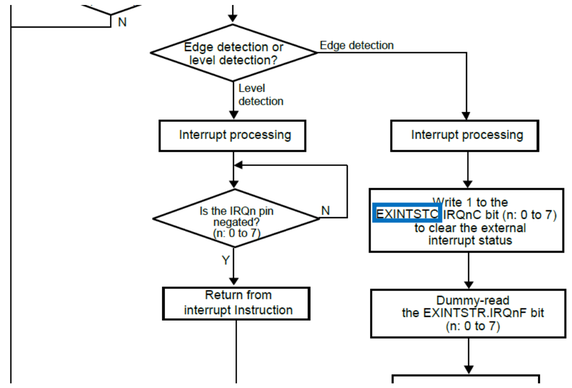
【Reference Documents】

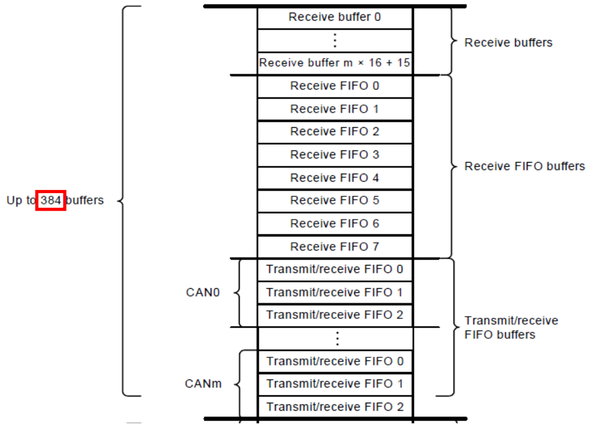
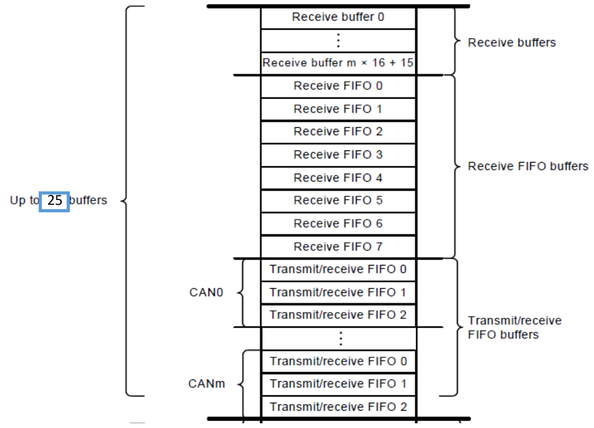
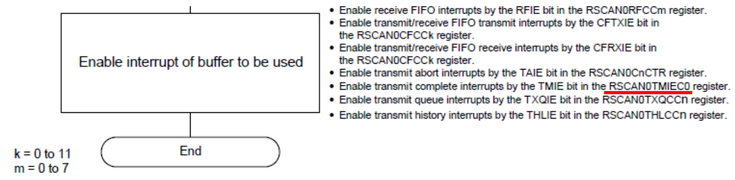
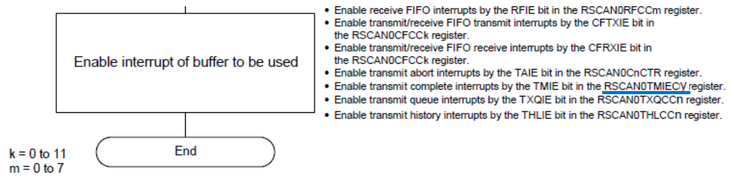
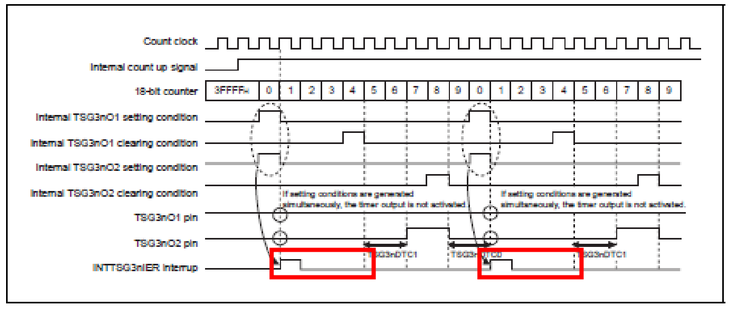
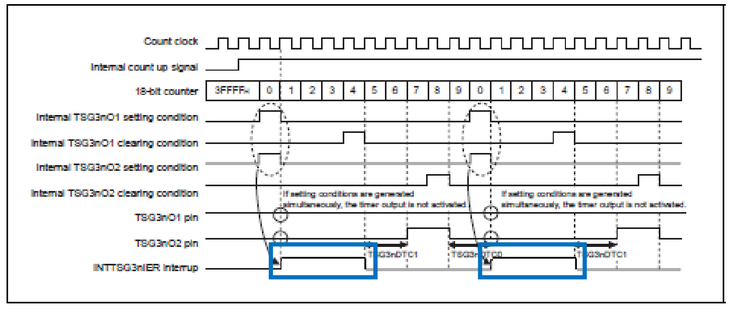
| Series | Series | Series | Rev. | Document No |
|---|---|---|---|---|
| RH850 | C1x | RH850/C1x User's Manual: Hardware | 1.60 | R01UH0414EJ0160 |

The changes are shown below. (Error: red, Correct: blue)

<table>
<tr><th>No.</th><th>PDF page<br>(Rev.1.60)</th><th>Section</th><th>Chapter title<br>(Chart title)</th><th>Error</th><th>Correct</th><th>Change reason</th><th>Notice situation</th><th>Note</th></tr>
<tr><td>1</td><td>2113</td><td>Functional Safety</td><td>(4) ERRSLVxxADDR — PBGxx Error Address Register</td><td>
(4) ERRSLVxxADDR — PBGxx Error Address Register<br>
ERRSLVxxADDR holds the address of the illegal access rejected with the PBGxx.<br>
 <br>
<br>
Table 27.97 ERRSLVxxADDR Register Contents<br>
<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr>
<tr><td>31 to 24</td><td>—</td><td>Reserved. These bits are always read as 0. The write value should also be 0.</td></tr>
<tr><td>23 to 0</td><td>ADDR[23:0]</td><td>When an illegal access occurs, the access address is calculated by addition of FF00 0000$_H$ to read value of these bits.</td></tr>
</table>
</td><td>
(4) ERRSLVxxADDR — PBGxx error address register<br>
ERRSLVxxADDR holds the address of the illegal access rejected with the PBGxx<br>
 <br>
<br>
Table 27.97 ERRSLVxxADDR Register Contents<br>
<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr>
<tr><td>31 to 0</td><td>ADDR[31:0]</td><td>Address at which an error has occurred.<br>CAUTION<br>ADDR[31:24] of PBG 2 to 5 are fixed to 0.<br>Access address is calculated by addition of FF00 0000$_H$ to read value of these bits.</td></tr>
</table>
</td><td>Description Change</td><td>TN-RH8-B0195A/E</td><td>–</td></tr>
<tr><td>2</td><td>2097</td><td>Functional Safety</td><td>27.3 Lockstep</td><td>none</td><td>27.3.3 Usage Notes<br>Reading a register with a value that is undefined after a reset without initializing the register may lead to a lock step compare error. Accordingly, such registers must be initialized with the desired settings.<br>Even if the branch instruction and the subsequent instruction is issued in parallel, the lock step compare error might be occurred by undefined register after the reset. It should be applied as specified below until the register which refer by subsequent instruction is initialized in case of branching in the preceding instruction.<br>● Insert the NOP instruction, the SYNCI instruction or the RIE instruction following the branch instruction.(It has to be added by assembler language. When C language is used, it could be optimized.)<br>Applicable branch instructions: Bcond, BR, JARL, JMP, JR</td><td>Description Change</td><td>TN-RH8-B0183C/E</td><td>–</td></tr>
<tr><td>3</td><td>218</td><td>Operating Mode</td><td>Table 5.1 Selection of Operating Mode</td><td>
Table 5.1 Selection of Operating Mode<br>
<table>
<tr><th colspan="3">Value Set in The Pin</th><th colspan="2">Value Set in Option Byte 0</th><th rowspan="2">Operating Mode</th><th rowspan="2">Startup Area</th><th rowspan="2">Types of I/F*1</th><th rowspan="2">Remarks</th></tr>
<tr><th>MD1</th><th>MD0</th><th>FLMODE</th><th>STM SEL1</th><th>STM SEL0</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>User boot mode</td><td>User area</td><td>It is possible to select I/F by OPBT2 in option byte. For details, see Section 31.10.2, OPBT2 — Option Byte 2 Register.</td><td>On-chip debug is available.</td></tr>
<tr><td></td><td></td><td></td><td>0</td><td>1</td><td>User boot mode</td><td>User boot area</td><td></td><td></td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>×</td><td>Serial programming mode</td><td>Boot area</td><td>Writer I/F (2-line UART)</td><td>Serial programming is available.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>×</td><td>×</td><td>Boundary scan mode</td><td>—</td><td>JTAG</td><td>Boundary scan is available.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>×</td><td>×</td><td>Serial programming mode</td><td>Boot area</td><td>Writer I/F (2-line UART)</td><td>Serial programming is available.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>×</td><td>×</td><td>Serial programming mode</td><td>Boot area</td><td>Writer I/F (3-line clock synchronization)</td><td>Serial programming is available.</td></tr>
</table>
Note: X = Don't care.<br>
Note 1. For the correspondence between the pin function and pin state in each interface, see Section 2.4.3, Pin State.
</td><td>
Table 5.1 Selection of Operating Mode<br>
<table>
<tr><th colspan="3">Value Set in The Pin</th><th colspan="2">Value Set in Option Byte 0</th><th rowspan="2">Operating Mode</th><th rowspan="2">Startup Area</th><th rowspan="2">Type of I/F*1</th><th rowspan="2">Remark</th></tr>
<tr><th>MD1*2</th><th>MD0</th><th>FLMODE</th><th>STMSEL1</th><th>STMSEL0</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>User boot mode</td><td>User area</td><td rowspan="2">The interface can be selected by OPBT2 in the option byte area. For details, see Section 31.10.2 OPBT2 — Option Byte 2 Register.</td><td rowspan="2">On-chip debug is available.</td></tr>
<tr><td></td><td></td><td></td><td>0</td><td>1</td><td>User boot mode</td><td>User boot area</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>x</td><td>Serial programming mode</td><td>Boot area</td><td>Writer I/F (2-line UART)</td><td>Serial programming is available.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>x</td><td>x</td><td>Boundary scan mode</td><td>—</td><td>JTAG</td><td>Boundary scan is available.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>x</td><td>x</td><td>Serial programming mode</td><td>Boot area</td><td>Writer I/F (2-line UART)</td><td>Serial programming is available.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>x</td><td>x</td><td>Serial programming mode</td><td>Boot area</td><td>Writer I/F (3-line clock synchronization)</td><td>Serial programming is available.</td></tr>
</table>
Note: X = Don't care<br>
Note 1. For the correspondence between the pin function and pin state in each interface, see Section 2.4.3, Pin State<br>
Note 2. Always input low level to MD1.
</td><td>Additional Description</td><td>–</td><td>–</td></tr>
<tr><td>4</td><td>2206</td><td>On-Chip Debugging Unit (OCD)</td><td>Table 34.2 I/O Pins of AUDR</td><td>
Table 30.2 I/O Pins of AUDR<br>
<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>AUDRST</td><td>Input</td><td>AUDR reset input pin<br>Inputting L to this pin resets the AUDR, ~~but it does not initialize the AUDISR, AUDMBR and AUDMBRC (described below).~~<br>When this pin is not connected, it is internally pulled-down.</td></tr>
</table>
</td><td>
Table 30.2 I/O Pins of AUDR<br>
<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>AUDRST</td><td>Input</td><td>AUDR reset input pin<br>Inputting L to this pin resets the AUDR.<br>When turning on the power, set this pin to Low regardless of the use of AUDR.<br>When this pin is not connected, it is internally pulled-down.<br>Make sure to initialize AUDR before inputting High to this pin.<br>CAUTION<br>AUDR is initialized when this pin is Low and AUDCK is input for a fixed number of cycles, but it does not initialize the AUDISR, AUDMBR and AUDMBRC (described below). Refer to Section 30.4.4.3, Usage Notes on the AUDR Function and Section 35, Electrical Characteristics for the number of cycles required for initialization.</td></tr>
</table>
</td><td>Description Change</td><td>TN-RH8-B0228A/E</td><td>–</td></tr>
</table>

<table>
<tr><th>No.</th><th>PDF page<br>(Rev.1.60)</th><th>Section</th><th>Chapter title<br>(Chart title)</th><th>Error</th><th>Correct</th><th>Change reason</th><th>Notice situation</th><th>Note</th></tr>
<tr><td>5</td><td>2219</td><td>On-Chip Debugging Unit (OCD)</td><td>30.4.4.3 Usage Notes on the AUDR Function</td><td>30.4.4.3 Usage Notes on the AUDR Function<br>• Do not negate the AUDSYNC pin until one cycle of AUDCK has elapsed after a command is input to the AUDATA pin and the Ready flag has been returned.<br>• When uninitialized memory is accessed through the AUDR, a bus error may occur due to ECC error detection.</td><td>30.4.4.3 Usage Notes on the AUDR Function<br>• Do not negate the AUDSYNC pin until one cycle of AUDCK has elapsed after a command is input to the AUDATA pin and the Ready flag has been returned.<br>• When uninitialized memory is accessed through the AUDR, a bus error may occur due to ECC error detection.<br>• Do not reset AUDR with AUDRST = L, while transferring data with AUDR ( AUDSYNC = L). The data transfer of AUDR is not completed in the System Interconnect, and it may interfere with the data transfer of other bus masters.<br>• AUDR can not transfer data when being in external or internal reset state.<br>• Do not assert AUDSYNC pin for a minimum of 2 AUDCK cycles after AUDR reset release with AUDRST = H.<br>• The timing from power on to data transfer is shown in Figure 30.xx.<br>  <br><br>Figure 30.xx Timings from power on to data transfer</td><td>Description Change</td><td>TN-RH8-B0228A/E</td><td>-</td></tr>
<tr><td>6</td><td>2219</td><td>On-Chip Debugging Unit (OCD)</td><td>30.5 Cautions on Using On-Chip Debugger</td><td>none</td><td>(5) Handling of /DCUTRSTpin at power on<br>Set the /DCUTRSTpin to the low level at power on, regardless of whether on-chip debugging is used.</td><td>Additional Description</td><td>-</td><td>-</td></tr>
<tr><td>7</td><td>2274</td><td>Electrical Characteristics</td><td>Figure 35.6 Control Signal Timing</td><td>  <br><br>Figure 35.6 Control Signal Timing</td><td>  <br><br>Figure 35.6 Control Signal Timing</td><td>Writing Error</td><td>-</td><td>-</td></tr>
<tr><td>8</td><td>2290</td><td>Electrical Characteristics</td><td>Table 35.31 AUD RAM Monitor Timing</td><td>Table 35.31 AUD RAM Monitor Timing<br>Condition: Tj = –40ºC to 150ºC, $C_L$ = 30 pF<br><table><tr><th>Item</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Unit</th></tr><tr><td>AUDCK cycle time (monitor mode)</td><td>tAUCKMcyc</td><td>50</td><td>—</td><td>ns</td></tr><tr><td>AUDCK high-level width (monitor mode)</td><td>tAUCKMH</td><td>0.4 × tAUCKMcyc</td><td>—</td><td>ns</td></tr><tr><td>AUDCK low-level width (monitor mode)</td><td>tAUCKML</td><td>0.4 × tAUCKMcyc</td><td>—</td><td>ns</td></tr><tr><td>AUDRST setup time (monitor mode, to AUDCK ↑)</td><td>tAURSTMS</td><td>30</td><td>—</td><td>ns</td></tr><tr><td>AUDRST input pulse width (monitor mode)</td><td>tAURSTMW</td><td>5 × tAUCKMcyc</td><td>—</td><td>ns</td></tr><tr><td>Monitor data output delay time (to AUDCK ↑)</td><td>tAUDTMD</td><td>—</td><td>35</td><td>ns</td></tr><tr><td>Monitor data input setup time (to AUDCK ↑)</td><td>tAUDTMS</td><td>15</td><td>—</td><td>ns</td></tr><tr><td>Monitor data input hold time (from AUDCK ↑)</td><td>tAUDTMH</td><td>5</td><td>—</td><td>ns</td></tr><tr><td>AUDSYNC input setup time (to AUDCK ↑)</td><td>tAUDSYS</td><td>15</td><td>—</td><td>ns</td></tr><tr><td>AUDSYNC input hold time (from AUDCK ↑)</td><td>tAUDSYH</td><td>5</td><td>—</td><td>ns</td></tr></table></td><td>Table 35.31 AUD RAM Monitor Timing<br>Conditions: Tj = – 40ºC to 150ºC, CL = 30 pF<br><table><tr><th>Item</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Unit</th></tr><tr><td>AUDCK cycle time (monitor mode)</td><td>tAUCKMcyc</td><td>50</td><td>—</td><td>ns</td></tr><tr><td>AUDCK high-level width (monitor mode)</td><td>tAUCKMH</td><td>0.4 × tAUCKMcyc</td><td>—</td><td>ns</td></tr><tr><td>AUDCK low-level width (monitor mode)</td><td>tAUCKML</td><td>0.4 × tAUCKMcyc</td><td>—</td><td>ns</td></tr><tr><td>AUDRST setup time (monitor mode, to AUDCK↑)</td><td>tAURSTMS</td><td>30</td><td>—</td><td>ns</td></tr><tr><td>AUDRST input pulse width (monitor mode)</td><td>tAURSTMW</td><td>5 × tAUCKMcyc</td><td>—</td><td>ns</td></tr><tr><td>Monitor data output delay time (to AUDCK ↑)</td><td>tAUDTMD</td><td>—</td><td>35</td><td>ns</td></tr><tr><td>Monitor data input setup time (to AUDCK ↑)</td><td>tAUDTMS</td><td>15</td><td>—</td><td>ns</td></tr><tr><td>Monitor data input hold time (from AUDCK ↑)</td><td>tAUDTMH</td><td>5</td><td>—</td><td>ns</td></tr><tr><td>AUDSYNC input setup time (to AUDCK ↑)</td><td>tAUDSYS</td><td>15</td><td>—</td><td>ns</td></tr><tr><td>AUDSYNC input hold time (from AUDCK ↑)</td><td>tAUDSYH</td><td>5</td><td>—</td><td>ns</td></tr><tr><td>AUDISR setup time</td><td>tAUDMDS</td><td>1</td><td>—</td><td>ms</td></tr><tr><td>AUDISR hold time</td><td>tAUDMDH</td><td>1</td><td>—</td><td>ms</td></tr></table></td><td>Additional Description</td><td>-</td><td>-</td></tr>
</table>

| No. | PDF page (Rev.1.60) | Section | Chapter title (Chart title) | Error | Correct | Change reason | Notice situation | Note |
|---|---|---|---|---|---|---|---|---|
| 9 | 2884 | Electrical Characteristics | 39.3.12 AUD RAM Monitor | none |  Figure 35.xx Timing to reflect settings on AUDISR | Additional Description | – | – |
| 10 | 70 | Pins | 2.1.2.3 Pin Data Input/Output | • PBDCn.PBDCn_m<br>In output mode, when this bit is set to 1, the pin enters the bidirectional mode. In bidirectional mode, the level of the signal on a Pn_m pin can be read from PPPn.PPRn_m. | • PBDCn.PBDCn_m<br>In output mode, when this bit is set to 1, the pin enters the bidirectional mode. In bidirectional mode, the level of the signal on a Pn_m pin can be read from PPRn.PPRn_m. | Writing Error | – | – |
| 11 | 250 | Interrupt | Figure 6.2 Example of External Interrupt Processing Flow |  |  | Writing Error | – | – |
| 12 | 631 | RS-CAN | 14.3.2 RSCAN0CmCFG | Set this register before requesting a transition to channel communication mode or channel wait mode. | Set this register before requesting a transition to channel communication mode or channel halt mode. | Writing Error | – | – |
| 13 | 688 | RS-CAN | 14.3.34 RSCAN0CFIDk | 28 to 0 CFID[28:0] Transmit/Receive FIFO Buffer ID Data<br>• When CFM[1:0] value is $01_B$ (transmit mode): Set standard ID or extended ID. For standard ID, write an ID to bits b10 to b0 and write 0 to bits b28 to b11.<br>• When CFM[1:0] value is $00_B$ (receive mode): Standard ID or extended ID in the received message can be read. For standard ID, read bits b10 to b0. Bits b28 to b11 are read as 0.<br>NOTE<br>To clear the CFTXIF, CFRXIF, and CFMLT flags to 0, the program must write 0 to these flags. Use a store instruction to write 0 to these flags and write 1 to the other flags. | 28 to 0 CFID[28:0] Transmit/Receive FIFO Buffer ID Data<br>• When CFM[1:0] value is $01_B$ (transmit mode): Set standard ID or extended ID. For standard ID, write an ID to bits b10 to b0 and write 0 to bits b28 to b11.<br>• When CFM[1:0] value is $00_B$ (receive mode): Standard ID or extended ID in the received message can be read. For standard ID, read bits b10 to b0. Bits b28 to b11 are read as 0. | Writing Error | – | – |
| 14 | 733 | RS-CAN | 14.3.61 RSCAN0THLPCTRm | At this time, the THLMC[4:0] (transmit history buffer unread data counter) value in the RSCAN0THLSTSm register is decremented. | At this time, the THLMC[4:0] (transmit history buffer unread data counter) value in the RSCAN0THLSTSm register is decremented by 1. | Writing Error | – | – |
| 15 | 746 | RS-CAN | Figure 14.5 Transitions of Global Modes | Figure 14.5 Transitions of Global Modes | Figure 14.5 Transitions of Channel Modes | Writing Error | – | – |
| 16 | 747 | RS-CAN | Table 14.88 Operation a Channel Transitions to Channel Reset Mode/Channel Halt Mode | Note 3. When the transition from channel reset mode to channel wait mode is to be made, set the RSCAN0CmCFG register in channel reset mode and then shift to channel wait mode. | Note 3. When the transition from channel reset mode to channel halt mode is to be made, set the RSCAN0CmCFG register in channel reset mode and then shift to channel halt mode. | Writing Error | – | – |
| 17 | 756 | RS-CAN | 14.4.4.1 Transmit Priority Determination | When messages are retransmitted due to an arbitration-lost or an error, transmit priority determination is made again regardless of the TPRI bit. | When messages are retransmitted due to an arbitration-lost or an error, transmit priority determination is made again according to the TPRI bit. | Writing Error | – | – |

| No. | PDF page (Rev.1.60) | Section | Chapter title (Chart title) | Error | Correct | Change reason | Notice situation | Note |
|---|---|---|---|---|---|---|---|---|
| 18 | 772 | RS-CAN | Figure 14.20 Buffer Configuration |  |  | Writing Error | – | – |
| 19 | 773 | RS-CAN | Figure 14.21 Buffer Setting Procedure |  |  | Writing Error | – | – |
| 20 | 776 | RS-CAN | 14.5.2.2 FIFO Buffer Reading Procedure | When received messages have been stored in one or more receive FIFO buffers or a transmit/receive FIFO buffer that is set to receive mode or gateway mode, the corresponding message count display counter (RFMC[7:0] bits in the RSCAN0RFSTSx register (x = 0 to 7) or CFMC[7:0] bits in the RSCAN0CFSTSk register (k = 0 to 11)) is incremented. | When received messages have been stored in one or more receive FIFO buffers or a transmit/receive FIFO buffer that is set to receive mode or gateway mode, the corresponding message count display counter (RFMC[7:0] bits in the RSCAN0RFSTSx register (x = 0 to 7) or CFMC[7:0] bits in the RSCAN0CFSTSk register (k = 0 to 11)) is incremented by 1. | Writing Error | – | – |
| 21 | 792 | RS-CAN | 14.6 Notes | • When linking transmit buffers to transmit/receive FIFO buffers or allocating transmit buffers to transmit queues, set the control register (RSCAN0TMCp) of the corresponding transmit buffer to 00H. The status register (RSCAN0TMSTSp) of the corresponding transmit buffer should not be used. Flags in other status registers (registers RSCAN0TMTRSTS0 to RSCAN0TMTRSTS2, RSCAN0TMTARSTS0 to RSCAN0TMTARSTS2, RSCAN0TMTCSTS0 to RSCAN0TMTCSTS2, and RSCAN0TMTASTS0 to RSCAN0TMTASTS2), which correspond to transmit buffers linked to transmit/receive FIFO buffers or allocated to transmit queues remain unchanged. Set the enable bit in the corresponding interrupt enable register (the RSCAN0TMIEC0, RSCAN0TMIEC1 and RSCAN0TMIEC2) to 0 (transmit buffer interrupt is disabled). | • When linking transmit buffers to transmit/receive FIFO buffers or allocating transmit buffers to transmit queues, set the control register (RSCAN0TMCp) of the corresponding transmit buffer to 00H. The status register (RSCAN0TMSTSp) of the corresponding transmit buffer should not be used. Flags in other status registers (registers RSCAN0TMTRSTS0, RSCAN0TMTRSTS1, RSCAN0TMTARSTS0, RSCAN0TMTARSTS1, RSCAN0TMTCSTS0, RSCAN0TMTCSTS1, RSCAN0TMTASTS0 and RSCAN0TMTASTS1), which correspond to transmit buffers linked to transmit/receive FIFO buffers or allocated to transmit queues remain unchanged. Set the enable bit in the corresponding interrupt enable register (the RSCAN0TMIEC0, RSCAN0TMIEC1 and RSCAN0TMIEC2) to 0 (transmit buffer interrupt is disabled). | Writing Error | – | – |
| 22 | 809 | OS Timer | 16.2.2 Block Diagram | The following block diagram shows the main components of the OSTM. | The following block diagram shows the main components of the OSTM. This product does not implement OSTMnTTOUT output. | Writing Error | – | – |
| 23 | 1341 | TSG3 | Figure 19.47 Example of Error Interrupt (INTTSG3nIER) Generation (PWM Mode) |  <br>Figure 19.47 Example of Error Interrupt (INTTSG3nIER) Generation (PWM Mode) |  <br>Figure 19.47 Example of Error Interrupt (INTTSG3nIER) Generation (PWM Mode) | Writing Error | – | – |
| 24 | 1353 | TSG3 | Figure 19.53 Example of Dead Time Control between TSG3nO1 and TSG3nO2 Outputs (2/2) | TSG3nCMP1E + TSG3nDTC1 ≥ TSG3nCMP0E + TSG3nCMP2E<br>(TSG3nO2 stays inactive)<br>TSG3nCMP2E + TSG3nDTC0 ≥ TSG3nCMP0E + TSG3nCMP1E<br>(TSG3nO1 stays inactive) | TSG3nCMP1E + TSG3nDTC1 ≥ TSG3nCMP0E + TSG3nCMP3E<br>(TSG3nO2 stays inactive)<br>TSG3nCMP3E + TSG3nDTC0 ≥ TSG3nCMP0E + TSG3nCMP1E<br>(TSG3nO1 stays inactive) | Writing Error | – | – |

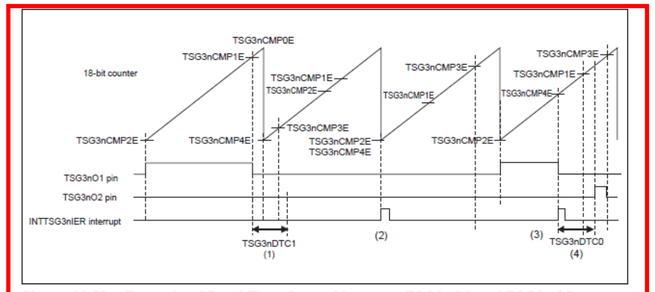
<table>
<tr><th>No.</th><th>PDF page<br>(Rev.1.60)</th><th>Section</th><th>Chapter title<br>(Chart title)</th><th>Error</th><th>Correct</th><th>Change reason</th><th>Notice situation</th><th>Note</th></tr>
<tr><td>25</td><td>1353</td><td>TSG3</td><td>Figure 19.53 Example of Dead Time Control between TSG3nO1 and TSG3nO2 Outputs (2/2)</td><td>At (4), the falling edge (inactive) of the TSG3nO1 output is caused by the simultaneous active state detected and the dead time counter starts counting. After the end of the dead time counter operation, the TSG3nO2 output becomes active.</td><td>At (4), the falling edge (inactive) of the TSG3nO1 output is caused by the simultaneous active state detected.<br>The dead time counter starts counting after compare match with the TSG3nCMP1 register.<br>After the end of the dead time counter operation, the TSG3nO2 output becomes active.</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>26</td><td>1353</td><td>TSG3</td><td>Figure 19.53 Example of Dead Time Control between TSG3nO1 and TSG3nO2 Outputs (2/2)</td><td> 

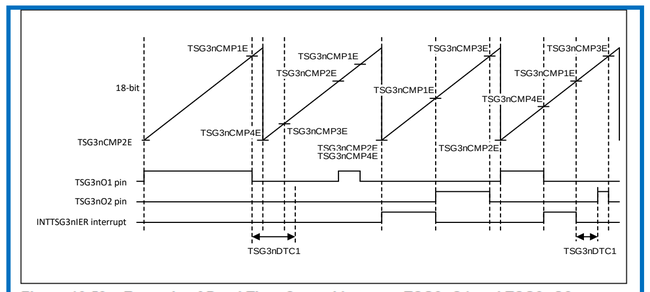
Figure 19.53 Example of Dead Time Control between TSG3nO1 and TSG3nO2 Outputs (2/2)</td><td> 

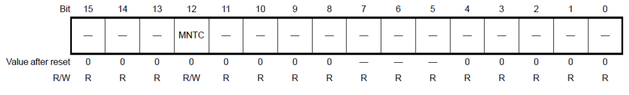
Figure 19.53 Example of Dead Time Control between TSG3nO1 and TSG3nO2 Outputs (2/2)</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>27</td><td>1760</td><td>EMU2</td><td>Table 24.73 EMU2nCTRINMD Register Contents</td><td>
<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr>
<tr><td>15 to 8</td><td>—</td><td>These bits are read as 0. The write value should be 0.</td></tr>
<tr><td>7, 6</td><td>INSTCTR[1:0]</td><td>Selects the activation timing of input IP*1.<br>0 0: On completion of all A/D conversion (scan of the A/D converter scan group 4 ended)<br>0 1: On completion of A/D conversion of CH0 (conversion of the A/D converter virtual channel 0 completed)<br>1 0: On completion of A/D conversion of CH1 (conversion of the A/D converter virtual channel 1 completed)<br>1 1: On completion of A/D conversion of CH2 (conversion of the A/D converter virtual channel 2 completed)</td></tr>
<tr><td>5 to 3</td><td>CMUVW[2:0]</td><td>Selects the object of current measurement when the CMES bit is set to 1.<br>0 0 0: Measures currents of 3 phases (U, V, and W)<br>0 0 1: Measures currents of 2 phases (V and W)<br>0 1 0: Measures currents of 2 phases (U and W)<br>0 1 1: Measures currents of 2 phases (U and V)<br>The other settings are prohibited.</td></tr>
<tr><td>2</td><td>CMES</td><td>Selects the object of current measurement.<br>0: 2 phases (V and W)<br>1: Object selected by the CMUVW[2:0] bits</td></tr>
<tr><td>1</td><td>—</td><td>This bit is read as 0. The write value should be 0.</td></tr>
<tr><td>0</td><td>FREGIN</td><td>Selects electrical angle to be used for input IP.<br>0: Uses User-set value<br>1: Uses electrical angle and resolver angle generated by angle generation IP</td></tr>
</table>
</td><td>
<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr>
<tr><td>15 to 8</td><td>—</td><td>These bits are read as 0. The write value should be 0.</td></tr>
<tr><td>7, 6</td><td>INSTCTR[1:0]</td><td>Selects the activation timing of input IP*1.<br>0 0: On completion of all A/D conversion (scan of the A/D converter scan group 4 ended)<br>0 1: On completion of A/D conversion of CH0 (conversion of the A/D converter virtual channel 0 completed)<br>1 0: On completion of A/D conversion of CH1 (conversion of the A/D converter virtual channel 1 completed)<br>1 1: On completion of A/D conversion of CH2 (conversion of the A/D converter virtual channel 2 completed)</td></tr>
<tr><td>5 to 3</td><td>CMUVW[2:0]</td><td>Selects the object of current measurement when the CMES bit is set to 1.<br>0 0 0: Measures currents of 3 phases (U, V, and W)<br>0 0 1: Measures currents of 2 phases (V and W)<br>0 1 0: Measures currents of 2 phases (U and W)<br>1 0 0: Measures currents of 2 phases (U and V)<br>The other settings are prohibited.</td></tr>
<tr><td>2</td><td>CMES</td><td>Selects the object of current measurement.<br>0: 2 phases (V and W)<br>1: Object selected by the CMUVW[2:0] bits</td></tr>
<tr><td>1</td><td>—</td><td>This bit is read as 0. The write value should be 0.</td></tr>
<tr><td>0</td><td>FREGIN</td><td>Selects electrical angle to be used for input IP.<br>0: Uses User-set value<br>1: Uses electrical angle and resolver angle generated by angle generation IP</td></tr>
</table>
</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>28</td><td>1762</td><td>EMU2</td><td>24.3.42 EMU2nADDOFSmk</td><td>Value after reset: $0000_H$</td><td>Value after reset: $0800_H$</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>29</td><td>1892</td><td>RDC2</td><td>25.3.7 RDC2nMNTC — RDC2n Monitor Pin Setting Register (n = 0, 1)</td><td>
25.3.7 RDC2nMNTC — RDC2n Monitor Pin Setting Register (n = 0, 1)<br>
Access: Readable/writable in 16-bit units.<br>
Address: <RDC2n_base> + $001A_H$<br>
Value After Reset: $00x0_H$<br>


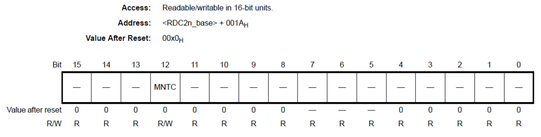
Table 25.23 RDC2nMNTC Register Contents
<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr>
<tr><td>15 to 13</td><td>Reserved</td><td>These bits are read as 0. The write value should be 0.</td></tr>
<tr><td>12</td><td>MNTC</td><td>Monitor Pin Control<br>0: Leaves RDC2nSINMNT and RDC2nCOSMNT pins open.<br>1: Outputs from RDC2nSINMNT and RDC2nCOSMNT pins.</td></tr>
<tr><td>11 to 0</td><td>Reserved</td><td>These bits are read as 0. The write value should be 0.</td></tr>
</table>
</td><td>
25.3.7 RDC2nMNTC — RDC2n Monitor Pin Setting Register (n = 0, 1)<br>
Access: Readable/writable in 16-bit units.<br>
Address: <RDC2n_base> + $001A_H$<br>
Value After Reset: $00x0_H$<br>


Table 25.23 RDC2nMNTC Register Contents
<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr>
<tr><td>15 to 13</td><td>Reserved</td><td>These bits are read as 0. The write value should be 0.</td></tr>
<tr><td>12</td><td>MNTC</td><td>Monitor Pin Control<br>0: Leaves RDC2nSINMNT and RDC2nCOSMNT pins open.<br>1: Outputs from RDC2nSINMNT and RDC2nCOSMNT pins.</td></tr>
<tr><td>11 to 8</td><td>Reserved</td><td>These bits are read as 0. The write value should be 0.</td></tr>
<tr><td>7 to 5</td><td>Reserved</td><td>The read value is undefined. The write value should be 0.</td></tr>
<tr><td>4 to 0</td><td>Reserved</td><td>These bits are read as 0. The write value should be 0.</td></tr>
</table>
</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>30</td><td>1892</td><td>RDC2</td><td>25.3.7 RDC2nMNTC</td><td>Value after reset: $00x0_H$</td><td>Value after reset: $00X0_H$</td><td>Writing Error</td><td>–</td><td>–</td></tr>
</table>

<table>
<tr><th>No.</th><th>PDF page<br>(Rev.1.60)</th><th>Section</th><th>Chapter title<br>(Chart title)</th><th>Error</th><th>Correct</th><th>Change reason</th><th>Notice situation</th><th>Note</th></tr>
<tr><td>31</td><td>1892</td><td>RDC2</td><td>Table 25.23 RDC2nMNTC Register Contents</td><td>Table 25.23 RDC2nMNTC Register Contents<br><table><tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr><tr><td>15 to 13</td><td>Reserved</td><td>These bits are read as 0. The write value should be 0.</td></tr><tr><td>12</td><td>MNTC</td><td>Monitor Pin Control<br>0: Leaves RDC2nSINMNT and RDC2nCOSMNT pins open.<br>1: Outputs from RDC2nSINMNT and RDC2nCOSMNT pins.</td></tr><tr><td>11 to 0</td><td>Reserved</td><td>These bits are read as 0. The write value should be 0.</td></tr></table></td><td>Table 25.23 RDC2nMNTC Register Contents<br><table><tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr><tr><td>15 to 13</td><td>Reserved</td><td>These bits are read as 0. The write value should be 0.</td></tr><tr><td>12</td><td>MNTC</td><td>Monitor Pin Control<br>0: Leaves RDC2nSINMNT and RDC2nCOSMNT pins open.<br>1: Outputs from RDC2nSINMNT and RDC2nCOSMNT pins.</td></tr><tr><td>11 to 8</td><td>Reserved</td><td>These bits are read as 0. The write value should be 0.</td></tr><tr><td>7 to 5</td><td>Reserved</td><td>The read value is undefined. The write value should be 0.</td></tr><tr><td>4 to 0</td><td>Reserved</td><td>These bits are read as 0. The write value should be 0.</td></tr></table></td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>32</td><td>1928</td><td>RDC2</td><td>Figure 25.12 RDC2 Initial Operation Flow</td><td>Note: n = 0, 1<br>Note 1. See Figure 25.13, Register Initial Setting Flow.<br>Note 2. For BIST test time, see Section 35.5.1, RDC Conversion Performance.<br>Note 3. For BIST recovery time, see Section 35.5.1, RDC Conversion Performance.<br>Note 4. For the settling time, see Section 35.5.1, RDC Conversion Performance.</td><td>Note: n = 0, 1<br>Note2: If the angle cannot be tracked when the R/D unit is started, apply a ki reset after the amplitude of RDC2nSINMNT or RDC2nCOSMNT rises to at least 1 V p-p and the amplitude of RDC2nRSO rises to at least 200 mV p-p.<br>Note 1. See Figure 25.13, Register Initial Setting Flow.<br>Note 2. For BIST test time, see Section 35.5.1, RDC Conversion Performance.<br>Note 3. For BIST recovery time, see Section 35.5.1, RDC Conversion Performance.<br>Note 4. For the settling time, see Section 35.5.1, RDC Conversion Performance.</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>33</td><td>1930</td><td>RDC2</td><td>25.6.1 Resolver Signal Input (Differential Input) Circuit</td><td>(1) RH ≈ {(RVDD − VCOM) / (22.0 × $10^{-6}$)} −RIN, where VCOM = RVDD/2[V]</td><td>(1) RH ≈ {(+VEXT − VCOM) / (22.0 × $10^{-6}$)} −RIN, where VCOM = RVDD/2[V]</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>34</td><td>2005</td><td>ADCC</td><td>Table 26.49 Notes on Setting Registers (2/2)</td><td><table><tr><td>ADCCnTHCR<br>ADCCnTHACR<br>ADCCnTHBCR<br>ADCCnTHER<br>ADCCnTHGSR<br>ADCCnSGCRx<br>ADCCnSGVCSPx<br>ADCCnSGVCEPx</td><td>When setting the registers shown in the left column, write these registers after they have been read.<br>If this procedure is not followed, the written register value may not be properly reflected, resuting in malfunction.</td></tr></table></td><td><table><tr><td>ADCCnTHCR<br>ADCCnTHACR<br>ADCCnTHBCR<br>ADCCnTHER<br>ADCCnTHGSR<br>ADCCnSGCRx<br>ADCCnSGVCSPx<br>ADCCnSGVCEPx</td><td>When setting the registers shown in the left column, write these registers after they have been read.<br>If writing to the register shown at the left occurs continuously without following this procedure, the written register value may not be correctly reflected in operations.</td></tr></table></td><td>Additional Description</td><td>–</td><td>–</td></tr>
<tr><td>35</td><td>2007</td><td>ADCC</td><td>Table 26.52 A/D Conversion Influential Formula</td><td>Table 26.52 A/D Conversion Influential Formula<br><table><tr><th>Item</th><th>Symbol</th><th>Reference</th><th>Unit</th></tr><tr><td>Signal source impedance</td><td>Re</td><td>Depends on user board</td><td>kΩ</td></tr><tr><td>Conversion cycle of T&H circuit</td><td>T2</td><td></td><td>ms</td></tr><tr><td>AnVREFH voltage (n = 0, 1)</td><td>Vavrefh</td><td></td><td>V</td></tr><tr><td>Parasitic capacitance of the last stage of channel multiplexer</td><td>C1</td><td>10</td><td>pF</td></tr><tr><td>| AnVCC voltage /2 – measured pin voltage | (n = 0, 1)</td><td>V3</td><td>Depends on user board</td><td>V</td></tr></table></td><td>Table 26.52 A/D Conversion Influential Formula of C1M (R7F701271EAFP #**0) and C1H (R7F701270EABG #**0)<br><table><tr><th>Item</th><th>Symbol</th><th>Reference</th><th>Unit</th></tr><tr><td>Signal source impedance</td><td>Re</td><td>Depends on user board</td><td>kΩ</td></tr><tr><td>Conversion cycle of T&H circuit</td><td>T2</td><td></td><td>ms</td></tr><tr><td>AnVREFH voltage (n = 0, 1)</td><td>Vavrefh</td><td></td><td>V</td></tr><tr><td>Parasitic capacitance of the last stage of channel multiplexer</td><td>C1</td><td>10</td><td>pF</td></tr><tr><td>| AnVCC voltage /2 – measured pin voltage | (n = 0, 1)</td><td>V3</td><td>Depends on user board</td><td>V</td></tr></table><br>Table 26.XX A/D Conversion Influential Formula of C1M (R7F701271EAFP #**4) and C1H (R7F701270EABG-C #**4)<br><table><tr><th>Item</th><th>Symbol</th><th>Reference</th><th>Unit</th></tr><tr><td>Signal source impedance</td><td>Re</td><td>Depends on user board</td><td>kΩ</td></tr><tr><td>Conversion cycle of T&H circuit</td><td>T2</td><td></td><td>ms</td></tr><tr><td>AnVREFH voltage (n = 0, 1)</td><td>Vavrefh</td><td></td><td>V</td></tr><tr><td>Parasitic capacitance of the last stage of channel multiplexer</td><td>C1</td><td>2</td><td>pF</td></tr><tr><td>| AnVCC voltage /2 – measured pin voltage | (n = 0, 1)</td><td>V3</td><td>Depends on user board</td><td>V</td></tr></table></td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>36</td><td>2157</td><td>ECM</td><td>Table 28.8 List of Error Sources and Safety Processing (1/2)</td><td><table><tr><td>6</td><td>RAM</td><td>Local RAM (CPU1, CPU2) 2-bit ECC error and local RAM (CPU1) address parity error*3</td></tr><tr><td>7</td><td></td><td>Local RAM (CPU1, CPU2) 1-bit ECC error and local RAM (CPU1) parity bit error*3</td></tr></table></td><td><table><tr><td>6</td><td>RAM</td><td>Local RAM (CPU1, CPU2) 2-bit ECC error and local RAM (CPU1, CPU2) address parity error*3</td></tr><tr><td>7</td><td></td><td>Local RAM (CPU1, CPU2) 1-bit ECC error and local RAM (CPU1, CPU2) parity bit error*3</td></tr></table></td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>37</td><td>2159</td><td>ECM</td><td>Table 28.9 Merging of Error Sources</td><td><table><tr><td>6</td><td>RAM</td><td>Local RAM (CPU1, CPU2): 2-bit ECC error<br>Local RAM (CPU1): Address parity error</td><td>2-bit ECC errors (local RAM for CPU1, CPU2) and address parity errors are merged.</td></tr><tr><td>7</td><td></td><td>Local RAM (CPU1, CPU2): 1-bit ECC error<br>Local RAM (CPU1): Parity bit error</td><td>1-bit ECC errors (local RAM for CPU1, CPU2) and parity bit errors are merged.</td></tr></table></td><td><table><tr><td>6</td><td>RAM</td><td>Local RAM (CPU1, CPU2): 2-bit ECC error<br>Local RAM (CPU1, CPU2): Address parity error</td><td>2-bit ECC errors and address parity errors of local RAM for CPU1, CPU2 are merged.</td></tr><tr><td>7</td><td></td><td>Local RAM (CPU1, CPU2): 1-bit ECC error<br>Local RAM (CPU1, CPU2): Parity bit error</td><td>1-bit ECC errors and address parity errors of local RAM for CPU1, CPU2 are merged.</td></tr></table></td><td>Writing Error</td><td>–</td><td>–</td></tr>
</table>

<table>
<tr><th>No.</th><th>PDF page<br>(Rev.1.60)</th><th>Section</th><th>Chapter title<br>(Chart title)</th><th>Error</th><th>Correct</th><th>Change reason</th><th>Notice situation</th><th>Note</th></tr>
<tr><td>38</td><td>2242</td><td>Flash Memory</td><td>31.11 Notes</td><td>(7) Items prohibited during programming and erasure<br>Do not perform the following operations during programming and erasure.</td><td>(7) Items prohibited during programming and erasure/blank checking<br>Do not perform the following operations during programming, erasure and blank checking.</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>39</td><td>2294</td><td>Electrical Characteristics</td><td>Table 35.35 RDC Conversion Performance</td><td>
<table>
<tr><td>BIST determination time*5</td><td>Angle conversion BIST (angle determination threshold is within ±8 LSB)</td><td>—</td><td>—</td><td>10</td><td>ms</td></tr>
<tr><td></td><td>Resolver signal error detection BIST</td><td>—</td><td>—</td><td>1.5</td><td>ms</td></tr>
<tr><td></td><td>Resolver signal cut off detection BIST</td><td>—</td><td>—</td><td>1</td><td>ms</td></tr>
<tr><td></td><td>Conversion error BIST</td><td>—</td><td>—</td><td>10</td><td>ms</td></tr>
</table>
</td><td>
<table>
<tr><td>BIST determination time*5</td><td>Angle conversion BIST (angle determination threshold is within ±16 LSB)</td><td>—</td><td>—</td><td>10</td><td>ms</td></tr>
<tr><td></td><td>Resolver signal error detection BIST</td><td>—</td><td>—</td><td>1.5</td><td>ms</td></tr>
<tr><td></td><td>Resolver signal cut off detection BIST</td><td>—</td><td>—</td><td>1</td><td>ms</td></tr>
<tr><td></td><td>Conversion error BIST</td><td>—</td><td>—</td><td>10</td><td>ms</td></tr>
</table>
</td><td>Writing Error</td><td>–</td><td>–</td></tr>
</table>

End of the list