RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RL*-A028B/E	Rev.	2.00
Title	Notification of correction for Incorrect Description RL78/G1A Descriptions in the Hardware User's Manual Rev. 2.00 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G1A R5F10Exx	Lot No. All lots	Reference Document	RL78/G1A User's Manual: Hardware Rev.2.00 R01UH0305EJ0200 (Jul. 2013)		

This document describes misstatements found in the RL78/G1A User's Manual: Hardware Rev.2.00 (R01UH0305EJ0200).

Corrections

Applicable Item	Applicable Page	Contents
2.4 Block Diagrams of Pins Figure 2-7. Pin Block Diagram for Pin Type 7-1-2	p.40	Caution added
2.4 Block Diagrams of Pins Figure 2-9. Pin Block Diagram for Pin Type 7-3-2	p.42	Caution added
2.4 Block Diagrams of Pins Figure 2-10. Pin Block Diagram for Pin Type 8-1-1	p.43	Caution added
2.4 Block Diagrams of Pins Figure 2-11. Pin Block Diagram for Pin Type 8-1-2	p.44	Caution added
2.4 Block Diagrams of Pins Figure 2-12. Pin Block Diagram for Pin Type 8-3-2	p.45	Caution added
2.4 Block Diagrams of Pins Figure 2-13. Pin Block Diagram for Pin Type 12-1-1	p.46	Caution added

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

No.	Corrections and Applicable Items		Pages in this document for corrections
	Document No. English	R01UH0305EJ0200	
1	4.3 Registers Controlling Port Function	p.103	Page 3 and Page 4
2	5.3.9 High-speed on-chip oscillator trimming register (HIOTRM)	p.157	Page 5
3	12.5.7 SNOOZE mode function	p.495 , p.497	Page 6 and 7
4	12.6.3 SNOOZE mode function	p.522	Page 8
5	12.6.3 SNOOZE mode function Timing Chart of SNOOZE Mode Operation	p.524 , p.525 , p.527	Pages 9 to 11
6	16.4.3 Multiple interrupt servicing Table 16-5. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing	p.710	Page 12
7	20.2 Configuration of Power-on-reset Circuit Figure 20-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (1/3)	p.751	Page 13
8	29.6.1 A/D converter characteristics	p.896	Page 14 and 15
9	29.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics	p.904	Page 16
10	30.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics	p.950	Page 17
11	7.3.4 Real-time clock control register 1 (RTCC1)	p.300	Page 18
12	2.4 Block Diagrams of Pins Figure 2-7. Pin Block Diagram for Pin Type 7-1-2	p.40	Page 19
13	2.4 Block Diagrams of Pins Figure 2-9. Pin Block Diagram for Pin Type 7-3-2	p.42	Page 20
14	2.4 Block Diagrams of Pins Figure 2-10. Pin Block Diagram for Pin Type 8-1-1	p.43	Page 21
15	2.4 Block Diagrams of Pins Figure 2-11. Pin Block Diagram for Pin Type 8-1-2	p.44	Page 22
16	2.4 Block Diagrams of Pins Figure 2-12. Pin Block Diagram for Pin Type 8-3-2	p.45	Page 23
17	2.4 Block Diagrams of Pins Figure 2-13. Pin Block Diagram for Pin Type 12-1-1	p.46	Page 24

Incorrect: Bold with underline; Correct: Gray hatched

Old: Bold with underline; New: Gray hatched

Revision History

RL78/G1A User's Manual: Hardware Rev.2.00 Notification of correction for Incorrect Description and Extended Specification

Document Number	Date	Description
TN-RL*-A028A/E	Apr.25.2014	First edition issued No.1 to 10 in corrections
TN-RL*-A046A/E	Jul. 6 , 2015	No.11 in corrections
TN-RL*-A028B/E	Feb. 22, 2016	Second edition issued No.12 to 17 in corrections (This notice)

1. 4.3 Registers Controlling Port Function

Incorrect:

Table 4-4. PMxx, Pxx, PUxx, PIMxx, POMxx, PMCxx registers and the bits mounted on each product (1/2)

Port		Bit Name						64-pin	48-pin	32-pin	25-pin
		PMxx Register	Pxx Register	PUxx Register	PIMxx Register	POMxx Register	PMCxx Register				
Port 0	0	PM00	P00	PU00	PIM00	–	–	√	–	–	–
	1	PM01	P01	PU01	PIM01	–	–	√	–	–	–
	2	PM02	P02	PU02	–	POM02	PMC02	√	√	√	√
	3	PM03	P03	PU03	PIM03	POM03	PMC03	√	√	√	√
	4	PM04	P04	PU04	PIM04	POM04	–	√	–	–	–
	5	PM05	P05	PU05	–	–	–	√	–	–	–
	6	PM06	P06	PU06	–	–	–	√	–	–	–
Port 1	0	PM10	P10	PU10	PIM10	POM10	**PMC00**	√	√	√	√
	1	PM11	P11	PU11	PIM11	POM11	**PMC01**	√	√	√	√
	2	PM12	P12	PU12	–	POM12	**PMC02**	√	√	√	√
	3	PM13	P13	PU13	–	POM13	**PMC03**	√	√	√	–
	4	PM14	P14	PU14	PIM14	POM14	**PMC04**	√	√	√	–
	5	PM15	P15	PU15	PIM15	POM15	**PMC05**	√	√	√	–
	6	PM16	P16	PU16	PIM16	–	–	√	√	–	–
Port 2	0	PM20	P20	–	–	–	–	√	√	√	√
	1	PM21	P21	–	–	–	–	√	√	√	√
	2	PM22	P22	–	–	–	–	√	√	√	√
	3	PM23	P23	–	–	–	–	√	√	√	√
	4	PM24	P24	–	–	–	–	√	√	√	–
	5	PM25	P25	–	–	–	–	√	√	–	–
	6	PM26	P26	–	–	–	–	√	√	–	–
	7	PM27	P27	–	–	–	–	√	√	–	–

Correct:

Table 4-4. PMxx, Pxx, PUxx, PIMxx, POMxx, PMCxx registers and the bits mounted on each product (1/2)

Port		Bit Name						64-pin	48-pin	32-pin	25-pin
		PMxx Register	Pxx Register	PUxx Register	PIMxx Register	POMxx Register	PMCxx Register				
Port 0	0	PM00	P00	PU00	PIM00	–	–	√	–	–	–
	1	PM01	P01	PU01	PIM01	–	–	√	–	–	–
	2	PM02	P02	PU02	–	POM02	PMC02	√	√	√	√
	3	PM03	P03	PU03	PIM03	POM03	PMC03	√	√	√	√
	4	PM04	P04	PU04	PIM04	POM04	–	√	–	–	–
	5	PM05	P05	PU05	–	–	–	√	–	–	–
	6	PM06	P06	PU06	–	–	–	√	–	–	–
Port 1	0	PM10	P10	PU10	PIM10	POM10	PMC10	√	√	√	√
	1	PM11	P11	PU11	PIM11	POM11	PMC11	√	√	√	√
	2	PM12	P12	PU12	–	POM12	PMC12	√	√	√	√
	3	PM13	P13	PU13	–	POM13	PMC13	√	√	√	–
	4	PM14	P14	PU14	PIM14	POM14	PMC14	√	√	√	–
	5	PM15	P15	PU15	PIM15	POM15	PMC15	√	√	√	–
	6	PM16	P16	PU16	PIM16	–	–	√	√	–	–
Port 2	0	PM20	P20	–	–	–	–	√	√	√	√
	1	PM21	P21	–	–	–	–	√	√	√	√
	2	PM22	P22	–	–	–	–	√	√	√	√
	3	PM23	P23	–	–	–	–	√	√	√	√
	4	PM24	P24	–	–	–	–	√	√	√	–
	5	PM25	P25	–	–	–	–	√	√	–	–
	6	PM26	P26	–	–	–	–	√	√	–	–
	7	PM27	P27	–	–	–	–	√	√	–	–

2. 5.3.9 High-speed on-chip oscillator trimming register (HIOTRM)

Incorrect:

5.3.9 High-speed on-chip oscillator trimming register (HIOTRM)

(omitted)

Figure 5-10. Format of High-Speed On-Chip Oscillator Trimming Register (HIOTRM)

Address: F00A0H After reset: undefined Note R/W

Symbol	7	6	5	4	3	2	1	0
HIOTRM	0	0	HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0

HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0	High-speed on-chip oscillator
0	0	0	0	0	0	Minimum speed
0	0	0	0	0	1	↑
0	0	0	0	1	0	
0	0	0	0	1	1	
0	0	0	1	0	0	
• • •						
1	1	1	1	1	0	↓
1	1	1	1	1	1	Maximum speed

Note The value after reset is the value adjusted at shipment.

Remarks 1. The HIOTRM register can be used to adjust the high-speed on-chip oscillator clock to an accuracy within about 0.05%.

2. For the usage example of the HIOTRM register, see the application note for RL78 MCU series High-speed On-chip Oscillator (HOCO) Clock Frequency Correction (R01AN0464).

Correct:

5.3.9 High-speed on-chip oscillator trimming register (HIOTRM)

(omitted)

Figure 5-10. Format of High-Speed On-Chip Oscillator Trimming Register (HIOTRM)

Address: F00A0H After reset: undefined Note R/W

Symbol	7	6	5	4	3	2	1	0
HIOTRM	0	0	HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0

HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0	High-speed on-chip oscillator
0	0	0	0	0	0	Minimum speed
0	0	0	0	0	1	↑
0	0	0	0	1	0	
0	0	0	0	1	1	
0	0	0	1	0	0	
• • •						
1	1	1	1	1	0	↓
1	1	1	1	1	1	Maximum speed

Note The value after reset is the value adjusted at shipment.

Remarks 1. The HIOTRM register holds a six-bit value used to adjust the high-speed on-chip oscillator with an increment of 1 corresponding to an increase of frequency by about 0.05%.

2. For the usage example of the HIOTRM register, see the application note for RL78 MCU series High-speed On-chip Oscillator (HOCO) Clock Frequency Correction (R01AN0464).

RENESAS

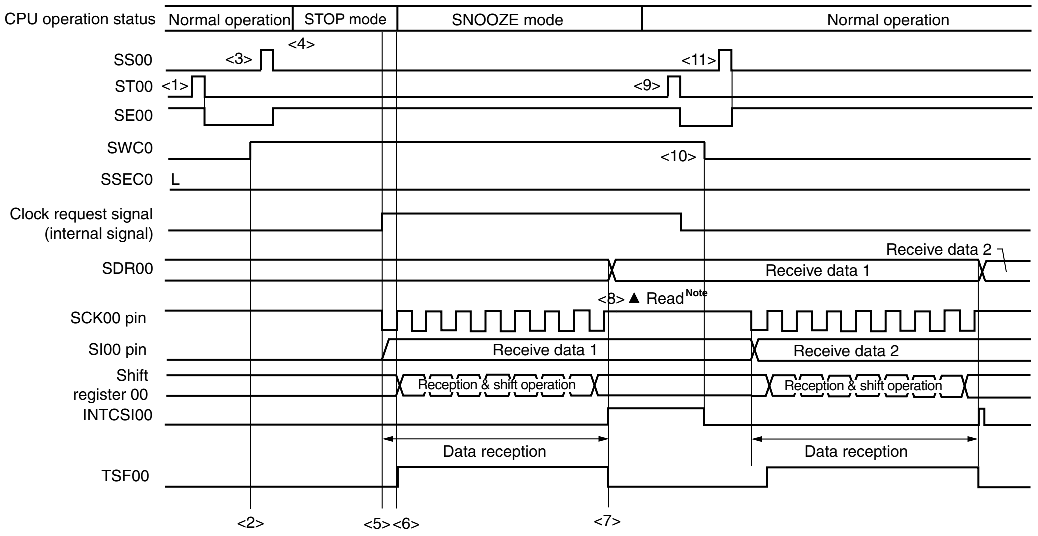
3. 12.5.7 SNOOZE mode function
Timing Chart of SNOOZE Mode Operation

It is correction of “Clock request signal (internal signal)” and TSF00 in this Figure.

Incorrect:

(1) SNOOZE mode operation (once startup)

Figure 12-70. Timing Chart of SNOOZE Mode Operation (Once Startup) (Type 1: DAPmn = 0, CKPmn = 0)

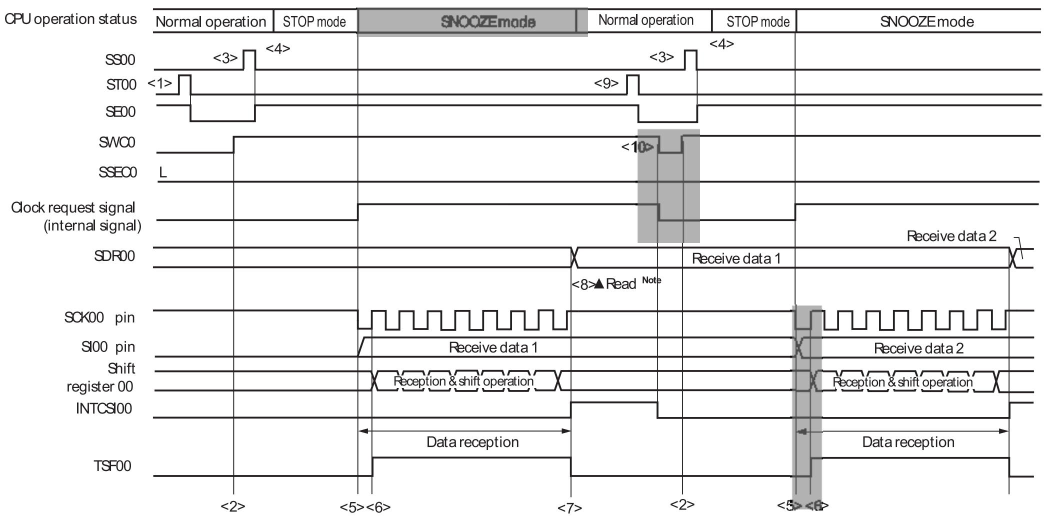


(omitted)

Correct:

(1) SNOOZE mode operation (once startup)

Figure 12-70. Timing Chart of SNOOZE Mode Operation (Once Startup) (Type 1: DAPmn = 0, CKPmn = 0)



(omitted)

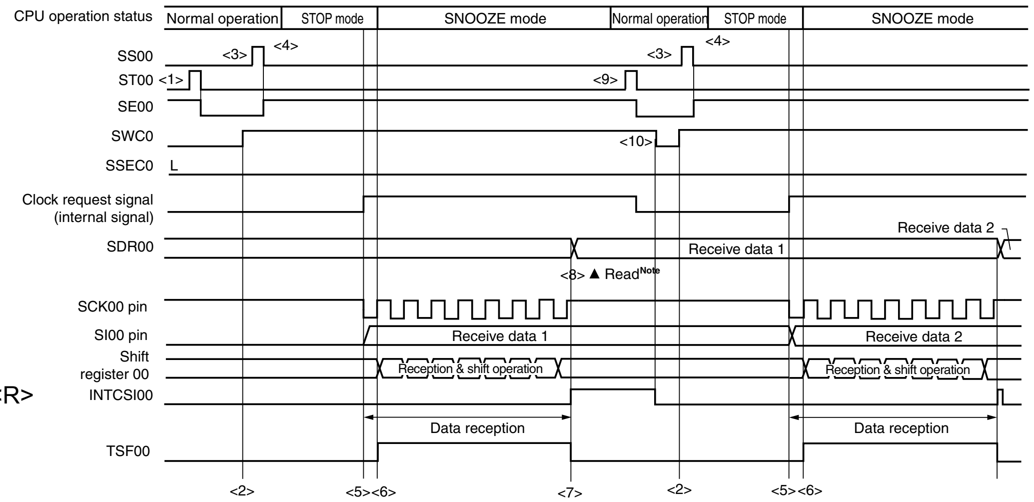
It is correction of "Clock request signal (internal signal)" in this Figure.

Incorrect:

(2) SNOOZE mode operation (continuous startup)

Figure 12-72. Timing Chart of SNOOZE Mode Operation (Continuous Startup) (Type 1: DAPmn = 0, CKPmn = 0)

<R>



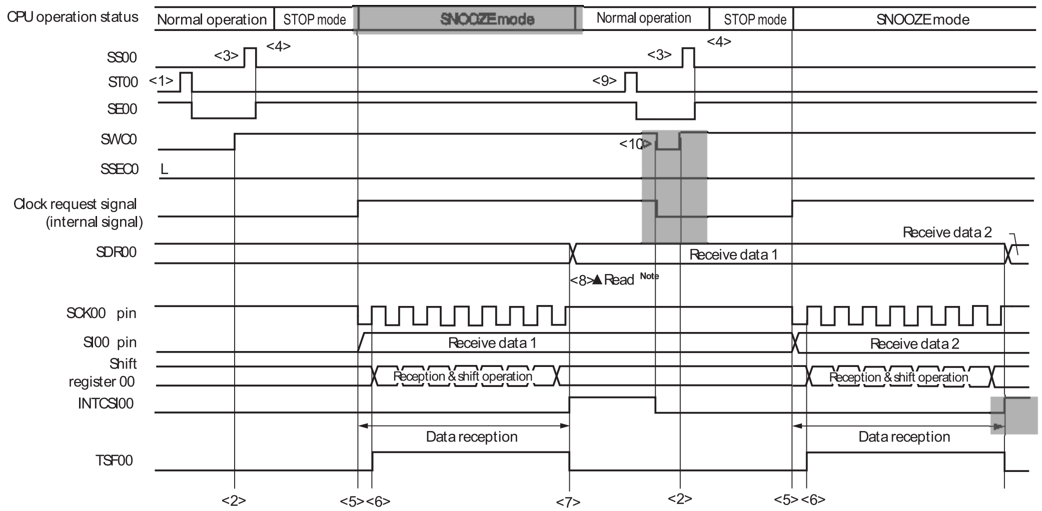
(omitted)

<R>

Correct:

(2) SNOOZE mode operation (continuous startup)

Figure 12-72. Timing Chart of SNOOZE Mode Operation (Continuous Startup) (Type 1: DAPmn = 0, CKPmn = 0)



(omitted)

4. 12.6.3 Attention added of SNOOZE mode function

12.6.3 SNOOZE mode function

Incorrect:

12.6.3 SNOOZE mode function

The SNOOZE mode makes the UART perform reception operations upon RxDq pin input detection while in the STOP mode. Normally the UART stops communication in the STOP mode. However, using the SNOOZE mode enables the UART to perform reception operations without CPU operation.

(omitted)

Cautions 1. The SNOOZE mode can only be used when the high-speed on-chip oscillator clock (f_{IH}) is selected for f_{CLK}.

(omitted)

4. If a parity error, framing error, or overrun error occurs while the SSECm bit is set to 1, the PEFmn, FEFmn, or OVFmn flag is not set and an error interrupt (INTSREq) is not generated. Therefore, when the setting of SSECm = 1 is made, clear the PEFmn, FEFmn, or OVFmn flag before setting the SWC0 bit to 1 and read the value in bits 7 to 0 (RxDq register) of the SDRm1 register.

Correct:

12.6.3 SNOOZE mode function

The SNOOZE mode makes the UART perform reception operations upon RxDq pin input detection while in the STOP mode. Normally the UART stops communication in the STOP mode. However, using the SNOOZE mode enables the UART to perform reception operations without CPU operation.

(omitted)

Cautions 1. The SNOOZE mode can only be used when the high-speed on-chip oscillator clock (f_{IH}) is selected for f_{CLK}.

(omitted)

4. If a parity error, framing error, or overrun error occurs while the SSECm bit is set to 1, the PEFmn, FEFmn, or OVFmn flag is not set and an error interrupt (INTSREq) is not generated. Therefore, when the setting of SSECm = 1 is made, clear the PEFmn, FEFmn, or OVFmn flag before setting the SWC0 bit to 1 and read the value in bits 7 to 0 (RxDq register) of the SDRm1 register.

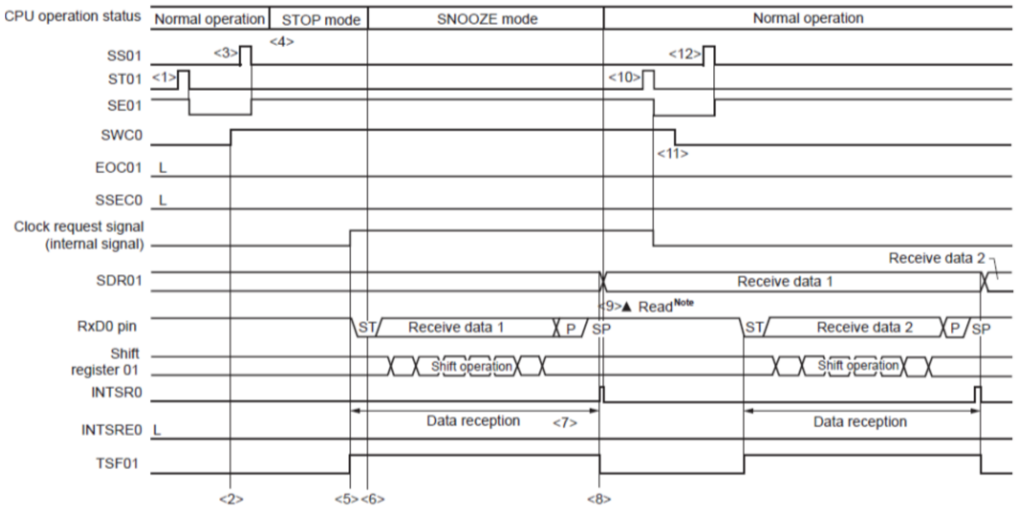
5.The CPU shifts from the STOP mode to the SNOOZE mode on detecting the valid edge of the RxDq signal. Note, however, that transfer through the UART channel may not start and the CPU may remain in the SNOOZE mode if an input pulse on the RxDq pin is too short to be detected as a start bit. In such cases, data may not be received correctly, and this may lead to a framing error or parity error in the next UART transfer.

5. 12.6.3 SNOOZE mode function Timing Chart of SNOOZE Mode Operation

It is correction of "Clock request signal (internal signal)" in this Figure.

Incorrect:

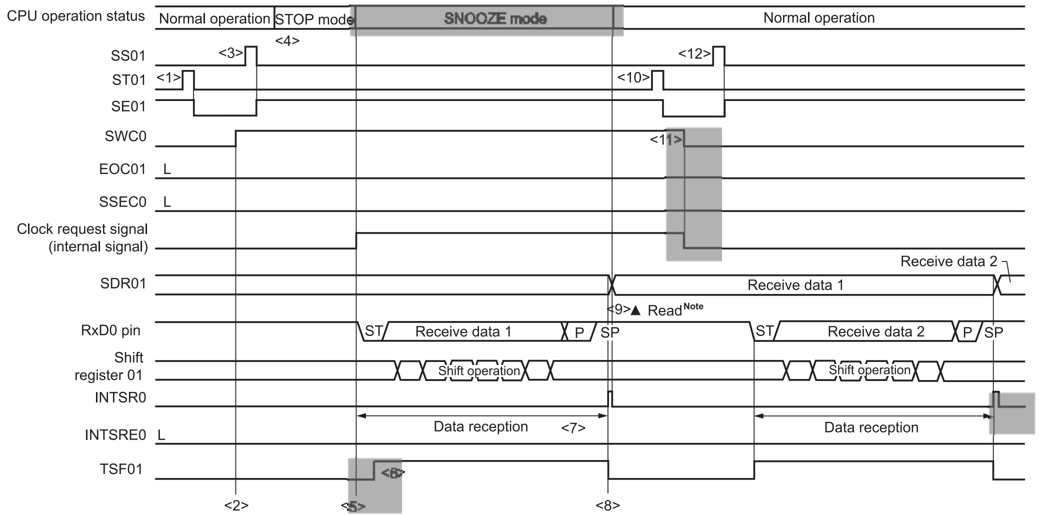
Figure 12-89. Timing Chart of SNOOZE Mode Operation (EOCm1 = 0, SSECm = 0/1)



(omitted)

Correct:

Figure 12-89. Timing Chart of SNOOZE Mode Operation (EOCm1 = 0, SSECm = 0/1)

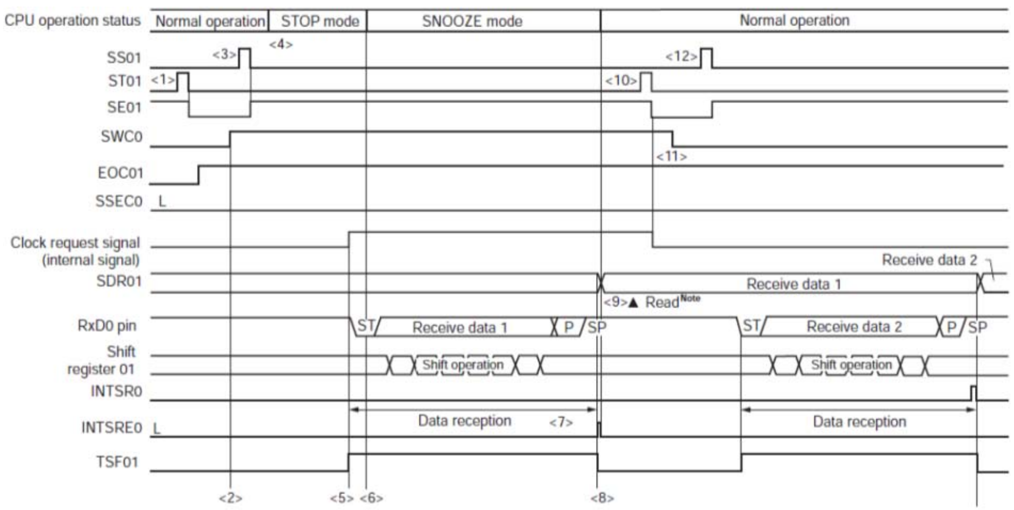


(omitted)

It is correction of "Clock request signal (internal signal)" in this Figure.

Incorrect:

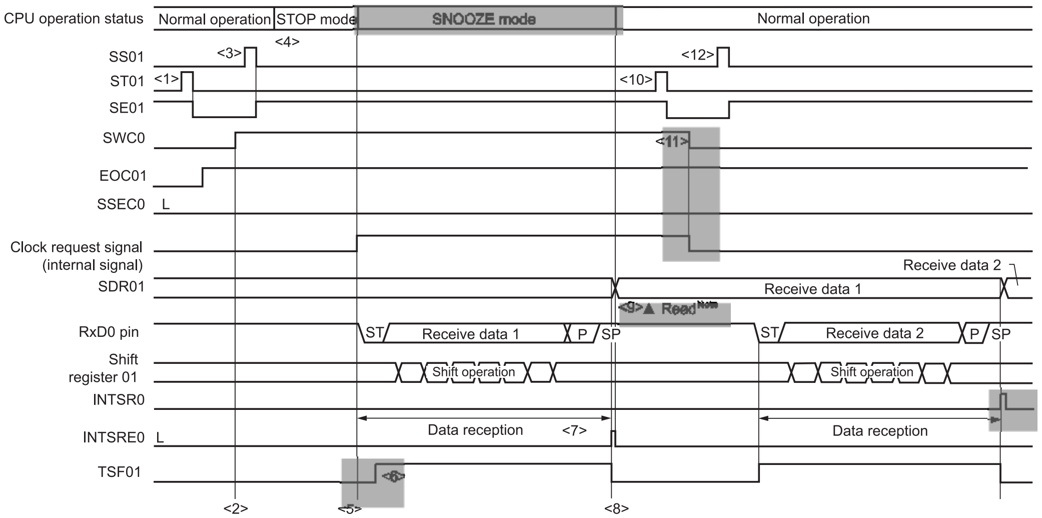
Figure 12-90. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 0)



(omitted)

Correct:

Figure 12-90. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 0)

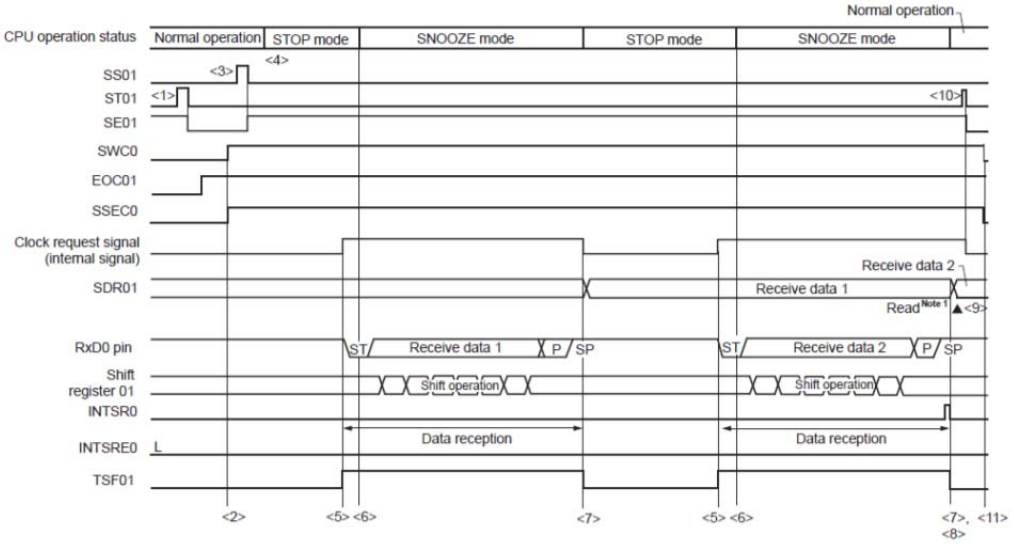


(omitted)

It is correction of "Clock request signal (internal signal)" in this Figure.

Incorrect:

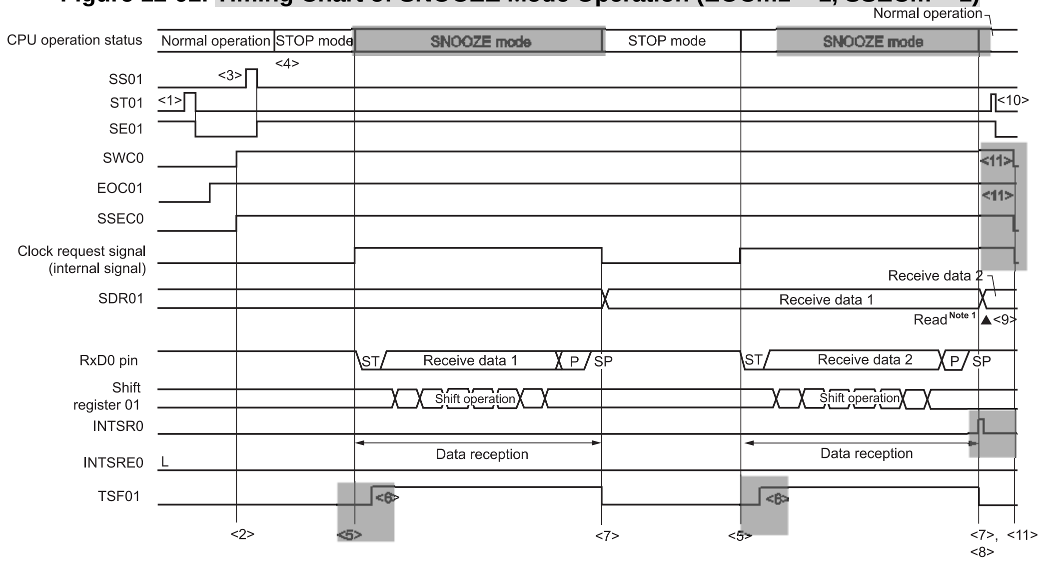
Figure 12-92. Timing Chart of SNOOZE Mode Operation (Abnormal Operation <2>)



(omitted)

Correct:

Figure 12-92. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 1)



(omitted)

6. 16.4.3 Multiple interrupt servicing
Table 16-5. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing

Incorrect:

Table 16-5. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing

Interrupt Being Serviced \ Multiple Interrupt Request		Maskable Interrupt Request								Software Interrupt Request
		Priority Level 0 (PR = 00)		Priority Level 1 (PR = 01)		Priority Level 2 (PR = 10)		Priority Level 3 (PR = 11)		
		IE = 1	IE = 0	IE = 1	IE = 0	IE = 1	IE = 0	IE = 1	IE = 0	
Maskable interrupt	ISP1 = 0 ISP0 = 0	○	×	×	×	×	×	×	×	○
	ISP1 = 0 ISP0 = 1	○	×	○	×	×	×	×	×	○
	ISP1 = 1 ISP0 = 0	○	×	○	×	○	×	×	×	○
	ISP1 = 1 ISP0 = 1	○	○	○	○	○	○	○	○	○
Software interrupt		○	×	○	×	○	×	○	×	○

(omitted)

Correct:

Table 16-5. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing

Interrupt Being Serviced \ Multiple Interrupt Request		Maskable Interrupt Request								Software Interrupt Request
		Priority Level 0 (PR = 00)		Priority Level 1 (PR = 01)		Priority Level 2 (PR = 10)		Priority Level 3 (PR = 11)		
		IE = 1	IE = 0	IE = 1	IE = 0	IE = 1	IE = 0	IE = 1	IE = 0	
Maskable interrupt	ISP1 = 0 ISP0 = 0	○	×	×	×	×	×	×	×	○
	ISP1 = 0 ISP0 = 1	○	×	○	×	×	×	×	×	○
	ISP1 = 1 ISP0 = 0	○	×	○	×	○	×	×	×	○
	ISP1 = 1 ISP0 = 1	○	×	○	×	○	×	○	×	○
Software interrupt		○	×	○	×	○	×	○	×	○

(omitted)

7. 20.2 Configuration of Power-on-reset Circuit

Figure 20-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (1/3)

Incorrect:

Figure 20-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (1/3)

(1) When the externally input reset signal on the $\overline{\text{RESET}}$ pin is used

(omitted)

Notes 3. **The time until normal operation starts includes the following reset processing time when the external reset is released (after the first release of POR) after the $\overline{\text{RESET}}$ signal is driven high (1) as well as the voltage stabilization wait time after VPOR (1.51 V, typ.) is reached.**
Reset processing time when the external reset is released is shown below.
After the first release of POR:
0.672 ms (typ.), 0.832 ms (max.) (when the LVD is in use)
0.399 ms (typ.), 0.519 ms (max.) (when the LVD is off)

4. **Reset processing time when the external reset is released after the second release of POR is shown below.**
After the second release of POR:
0.531 ms (typ.), 0.675 ms (max.) (when the LVD is in use)
0.259 ms (typ.), 0.362 ms (max.) (when the LVD is off)

(omitted)

Correct:

Figure 20-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (1/3)

(1) When the externally input reset signal on the $\overline{\text{RESET}}$ pin is used

(omitted)

Notes 3. The time until normal operation starts includes the following reset processing time when the external reset is released (release from the first external reset following release from the POR state) after the $\overline{\text{RESET}}$ signal is driven high (1) as well as the voltage stabilization wait time after VPOR (1.51 V, typ.) is reached.
Reset processing time when the external reset is released is shown below.
Release from the first external reset following release from the POR state:
0.672 ms (typ.), 0.832 ms (max.) (when the LVD is in use)
0.399 ms (typ.), 0.519 ms (max.) (when the LVD is off)

4. Reset times in cases of release from an external reset other than the above are listed below.
Release from the reset state for external resets other than the above case:
0.531 ms (typ.), 0.675 ms (max.) (when the LVD is in use)
0.259 ms (typ.), 0.362 ms (max.) (when the LVD is off)

(omitted)

8. 29.6.1 A/D converter characteristics

Voltage Range of A/D conversion was extended.

Old:

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target for conversion: ANI2 to ANI12

(T_A = –40 to +85°C, 2.7 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V, HALT mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}				12	bit
Overall error Notes 1, 2, 3	AINL	12-bit resolution		±1.7	±3.3	LSB
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	3.375			μs
Zero-scale error Notes 1, 2, 3	E_{ZS}	12-bit resolution		±1.3	±3.2	LSB
Full-scale error Notes 1, 2, 3	E_{FS}	12-bit resolution		±0.7	±2.9	LSB
Integral linearity error Notes 1, 2, 3	ILE	12-bit resolution		±1.0	±1.4	LSB
Differential linearity error Notes 1, 2, 3	DLE	12-bit resolution		±0.9	±1.2	LSB
Analog input voltage	V_{AIN}		0		AV_{REFP}	V

Notes 1. TYP. Value is the average value at AV_{DD} = AV_{REFP} = 3 V and T_A = 25°C. MAX. value is the average value ±3σ at normalized distribution.

2. These values are the results of characteristic evaluation and are not checked for shipment.

3. Excludes quantization error (±1/2 LSB).

Cautions 1. Route the wiring so that noise will not be superimposed on each power line and ground line, and insert a capacitor to suppress noise.

In addition, separate the reference voltage line of AV_{REFP} from the other power lines to keep it free from the influences of noise.

2. During A/D conversion, keep a pulse, such as a digital signal, that abruptly changes its level from being input to or output from the pins adjacent to the converter pins and P20 to P27 and P150 to P154.

New:

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target for conversion: ANI2 to ANI12

(T_A = –40 to +85°C, 2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V, HALT mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}				12	bit
Overall error[Notes 1, 2, 3]	AINL	12-bit resolution		±1.7	±3.3	LSB
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	3.375			μs
Zero-scale error[Notes 1, 2, 3]	E_{ZS}	12-bit resolution		±1.3	±3.2	LSB
Full-scale error[Notes 1, 2, 3]	E_{FS}	12-bit resolution		±0.7	±2.9	LSB
Integral linearity error[Notes 1, 2, 3]	ILE	12-bit resolution		±1.0	±1.4	LSB
Differential linearity error[Notes 1, 2, 3]	DLE	12-bit resolution		±0.9	±1.2	LSB
Analog input voltage	V_{AIN}		0		AV_{REFP}	V

Notes 1. TYP. Value is the average value at AV_{DD} = AV_{REFP} = 3 V and T_A = 25°C. MAX. value is the average value ±3σ at normalized distribution.

2. These values are the results of characteristic evaluation and are not checked for shipment.

3. Excludes quantization error (±1/2 LSB).

Cautions 1. Route the wiring so that noise will not be superimposed on each power line and ground line, and insert a capacitor to suppress noise.

In addition, separate the reference voltage line of AV_{REFP} from the other power lines to keep it free from the influences of noise.

2. During A/D conversion, keep a pulse, such as a digital signal, that abruptly changes its level from being input to or output from the pins adjacent to the converter pins and P20 to P27 and P150 to P154.

9. 29.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

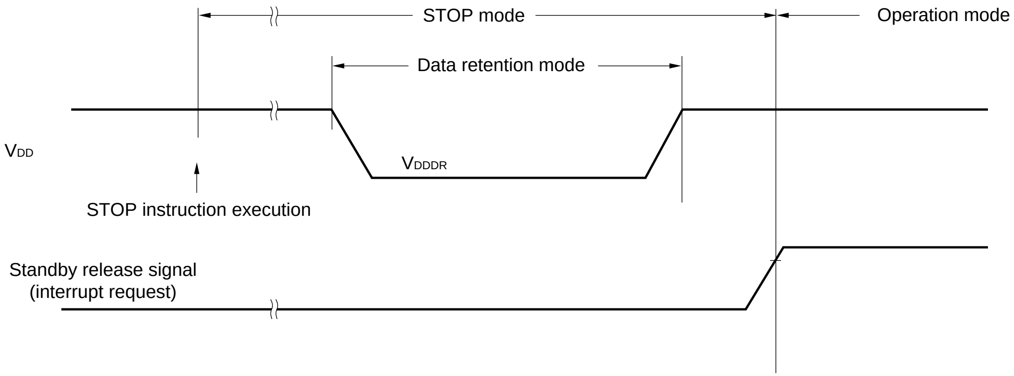
Old:

29.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46[Note]		3.6	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



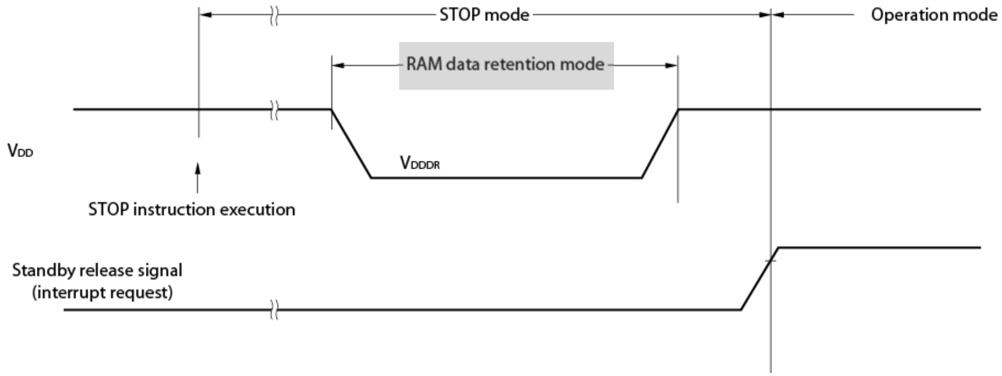
New:

29.7 RAM Data Retention Characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46[Note]		3.6	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



10. 30.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

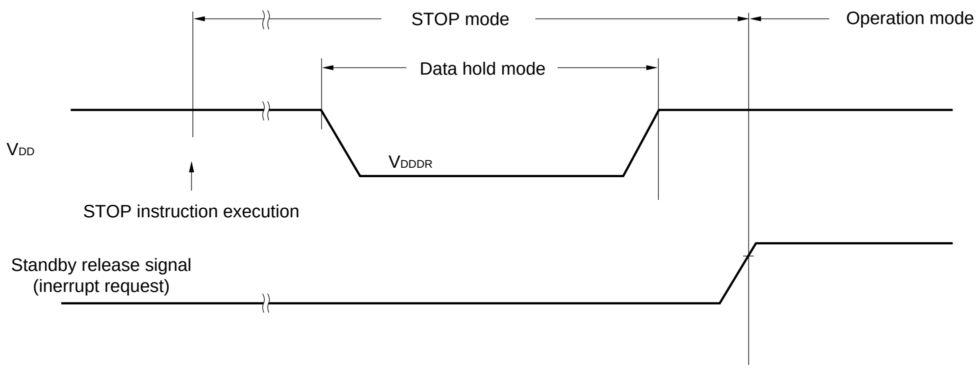
Old:

30.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = –40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44[Note]		3.6	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



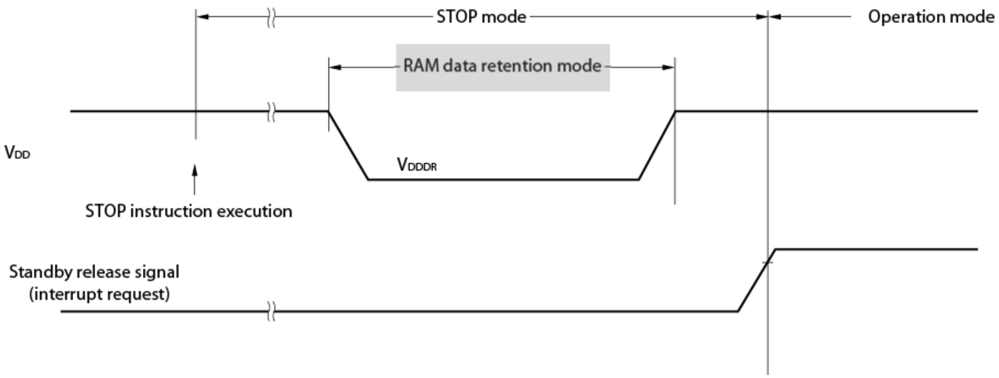
New:

30.7 RAM Data Retention Characteristics

(T_A = –40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44[Note]		3.6	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



11. 7.3.4 Real-time clock control register 1 (RTCC1)(p.300)

Old:

RWAIT	Wait control of real-time clock
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value

This bit controls the operation of the counter.
Be sure to write “1” to it to read or write the counter value.
As the internal counter (16 bits) is continuing to run, complete reading or writing within one second and turn back to 0.
When RWAIT = 1, it takes up to 1 operating clock (f_{RTC}) until the counter value can be read or written (RWST = 1).
When the internal counter (16 bits) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up.
However, when it wrote a value to second count register, it will not keep the overflow event.

New:

RWAIT	Wait control of real-time clock
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value

This bit controls the operation of the counter.
Be sure to write “1” to it to read or write the counter value.
As the internal counter (16 bits) is continuing to run, complete reading or writing within one second and turn back to 0.
When RWAIT = 1, it takes up to 1 operating clock (f_{RTC}) until the counter value can be read or written (RWST = 1). [Notes 1,2]
When the internal counter (16 bits) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up.
However, when it wrote a value to second count register, it will not keep the overflow event.

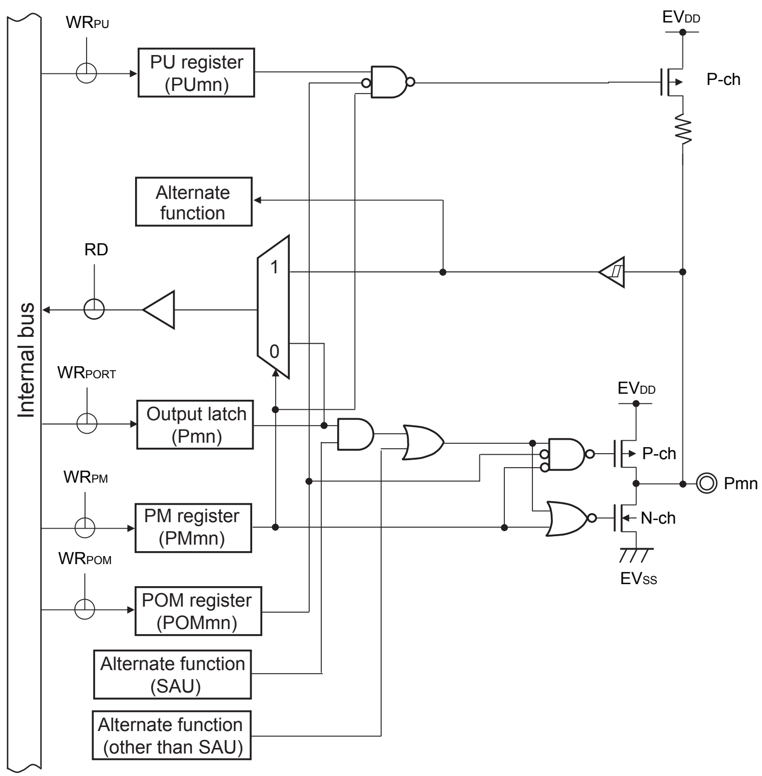
Note 1. When setting RWAIT=1 during 1 operating clock (f_{RTC}), after setting RTCE=1, it may take two clock time of the operation clock (f_{RTC}), until RWST bit is set to "1".

Note 2. When setting RWAIT=1 during 1 operating clock (f_{RTC}), after returning from a stand-by (HALT mode, STOP mode and SNOOZE mode), it may take two clock time of the operation clock (f_{RTC}), until RWST bit is set to "1".

12. 2.4 Block Diagrams of Pins Figure 2-7. Pin Block Diagram for Pin Type 7-1-2)(p.40)

Old:

Figure 2-7. Pin Block Diagram for Pin Type 7-1-2

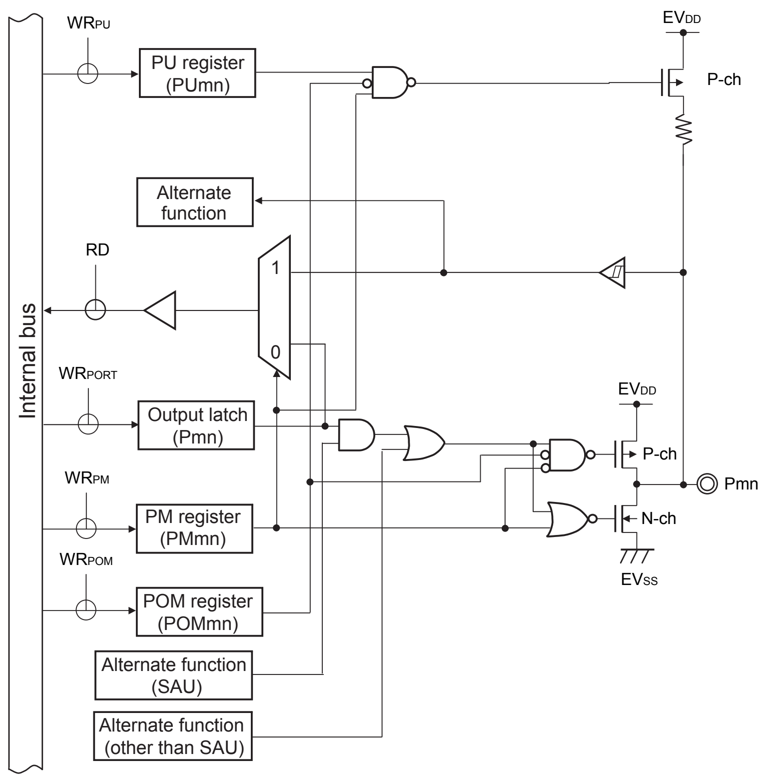


Remarks 1. For alternate functions, see **2.1 Port Function**.

2. SAU: Serial array unit

New:

Figure 2-7. Pin Block Diagram for Pin Type 7-1-2



Caution A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

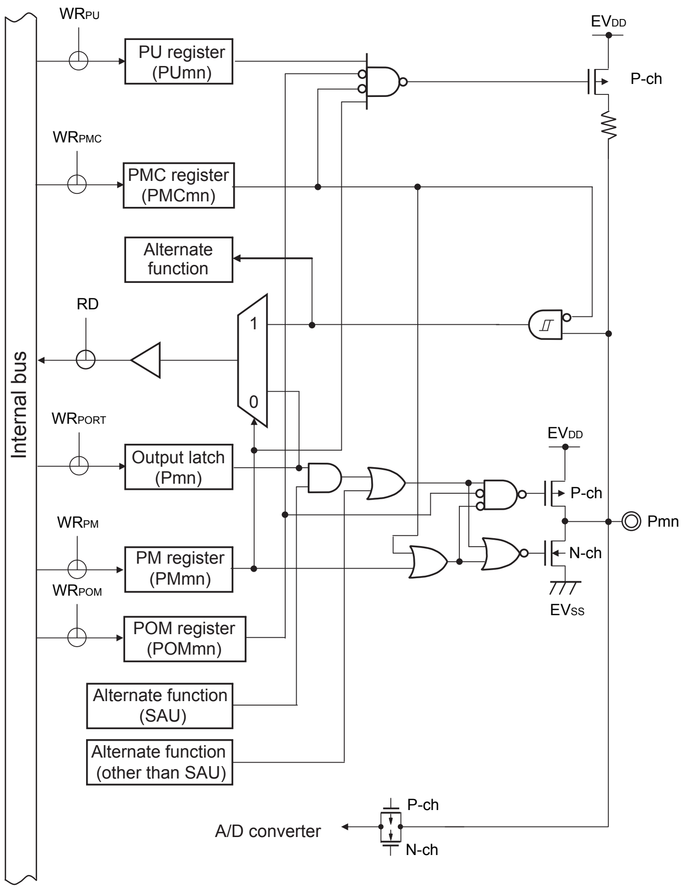
Remarks 1. For alternate functions, see **2.1 Port Function**.

2. SAU: Serial array unit

13. 2.4 Block Diagrams of Pins Figure 2-9. Pin Block Diagram for Pin Type 7-3-2)(p.42)

Old:

Figure 2-9. Pin Block Diagram for Pin Type 7-3-2

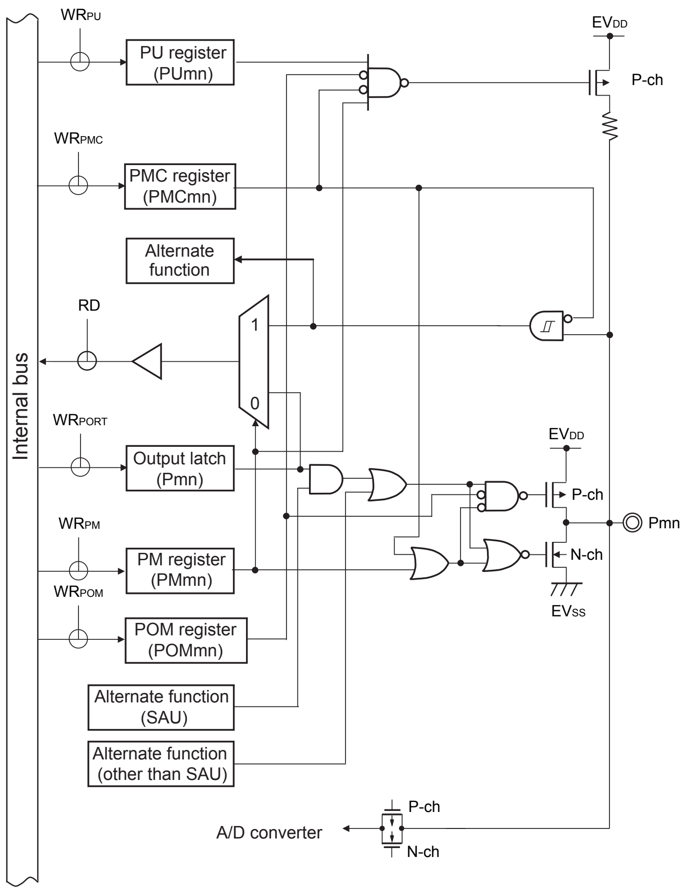


Remarks 1. For alternate functions, see **2.1 Port Function**.

2. SAU: Serial array unit

New:

Figure 2-9. Pin Block Diagram for Pin Type 7-3-2



Caution A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

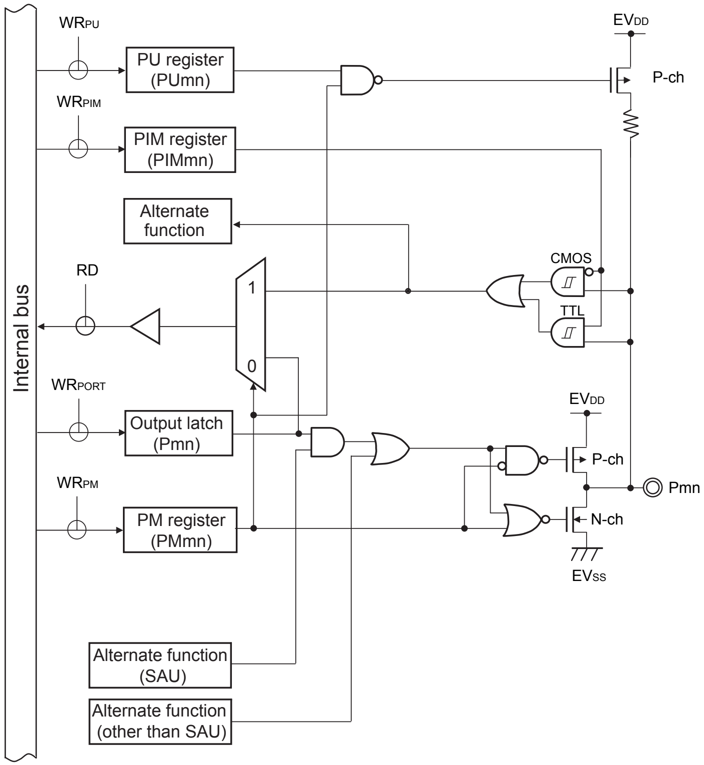
Remarks 1. For alternate functions, see **2.1 Port Function**.

2. SAU: Serial array unit

14. 2.4 Block Diagrams of Pins Figure 2-10. Pin Block Diagram for Pin Type 8-1-1)(p.43)

Old:

Figure 2-10. Pin Block Diagram for Pin Type 8-1-1

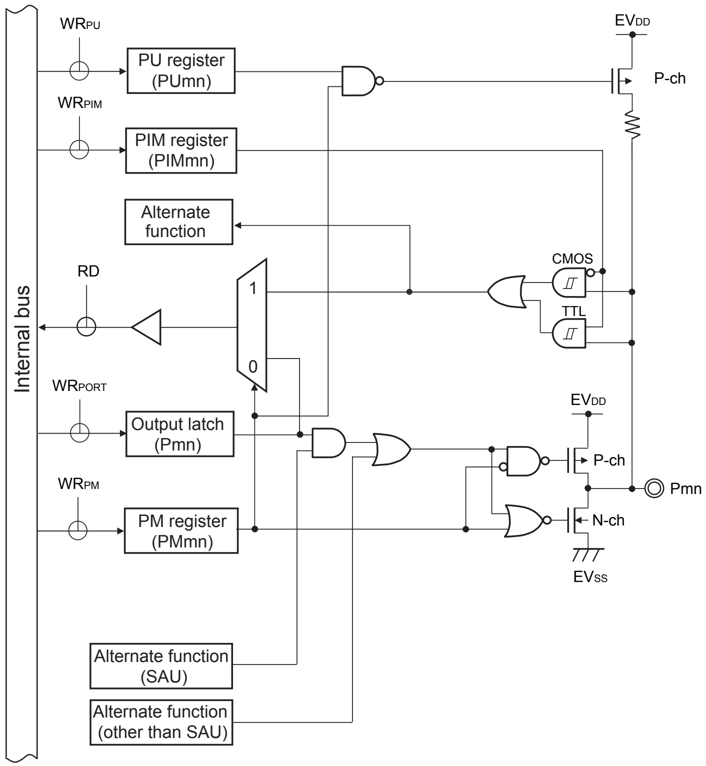


Remarks 1. For alternate functions, see **2.1 Port Function**.

2. SAU: Serial array unit

New:

Figure 2-10. Pin Block Diagram for Pin Type 8-1-1



Caution Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, a through current may flow through in the case of high level input. It is recommended to input a low level to prevent a through current.

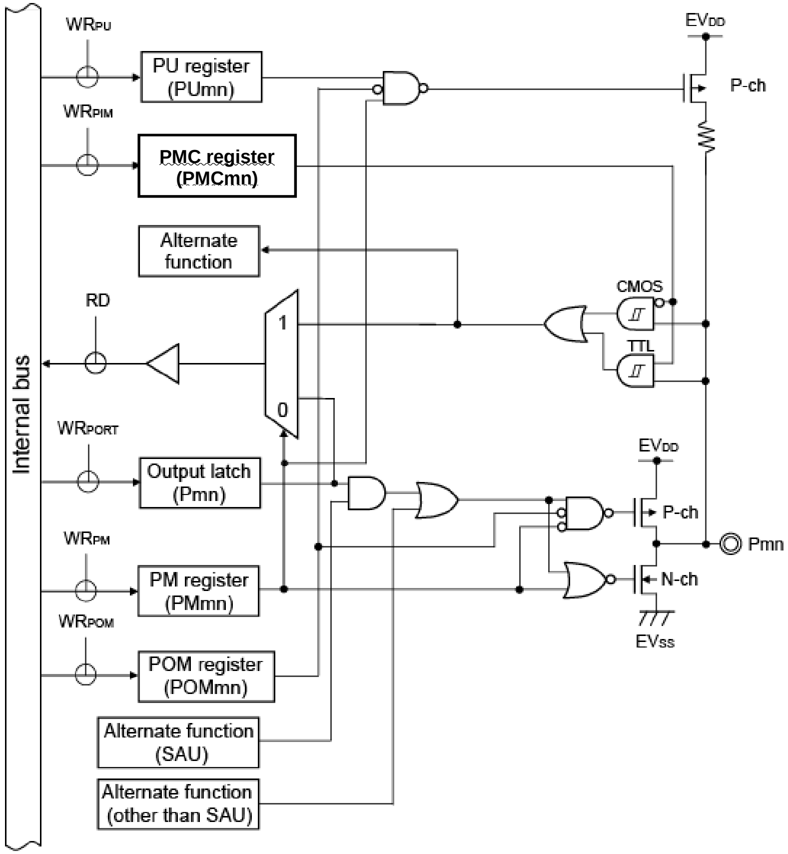
Remarks 1. For alternate functions, see **2.1 Port Function**.

2. SAU: Serial array unit

15. 2.4 Block Diagrams of Pins Figure 2-11. Pin Block Diagram for Pin Type 8-1-2)(p.44)

Old:

Figure 2-11. Pin Block Diagram for Pin Type 8-1-2

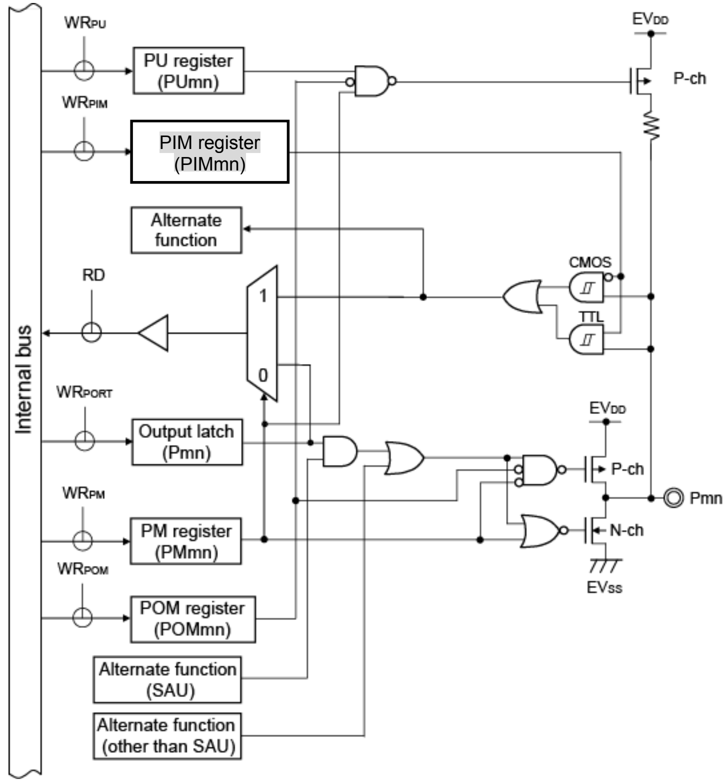


Remarks 1. For alternate functions, see **2.1 Port Function**.

2. SAU: Serial array unit

New:

Figure 2-11. Pin Block Diagram for Pin Type 8-1-2



Caution 1. A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

Caution 2. Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, a through current may flow through in the case of high level input. It is recommended to input a low level to prevent a through current.

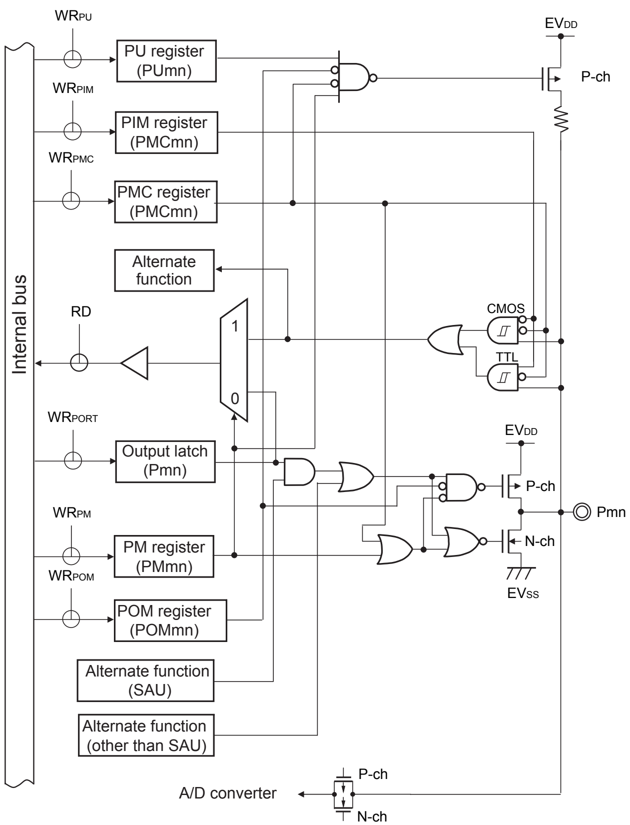
Remarks 1. For alternate functions, see **2.1 Port Function**.

2. SAU: Serial array unit

16. 2.4 Block Diagrams of Pins Figure 2-12. Pin Block Diagram for Pin Type 8-3-2)(p.45)

Old:

Figure 2-12. Pin Block Diagram for Pin Type 8-3-2

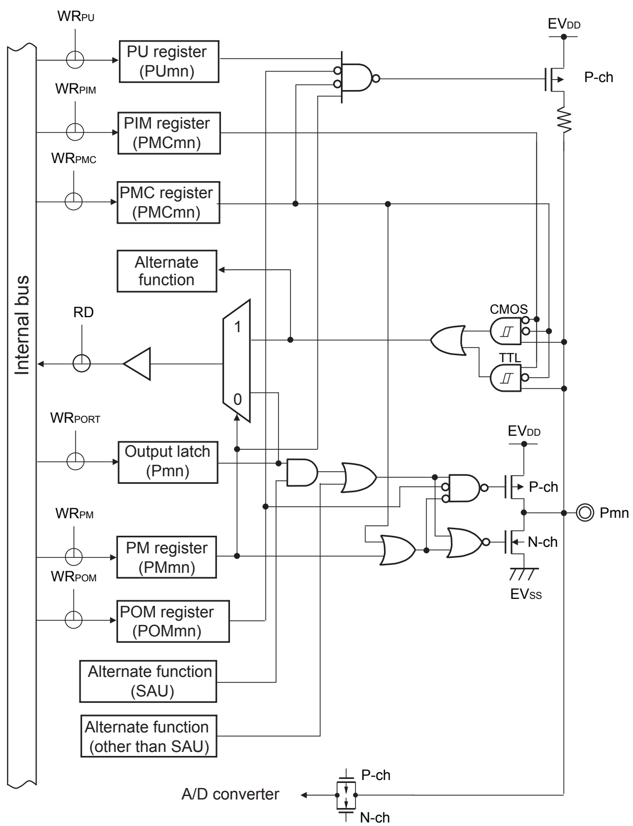


Remarks 1. For alternate functions, see **2.1 Port Function**.

2. SAU: Serial array unit

New:

Figure 2-12. Pin Block Diagram for Pin Type 8-3-2



Caution 1. A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

Caution 2. Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, a through current may flow through in the case of high level input. It is recommended to input a low level to prevent a through current.

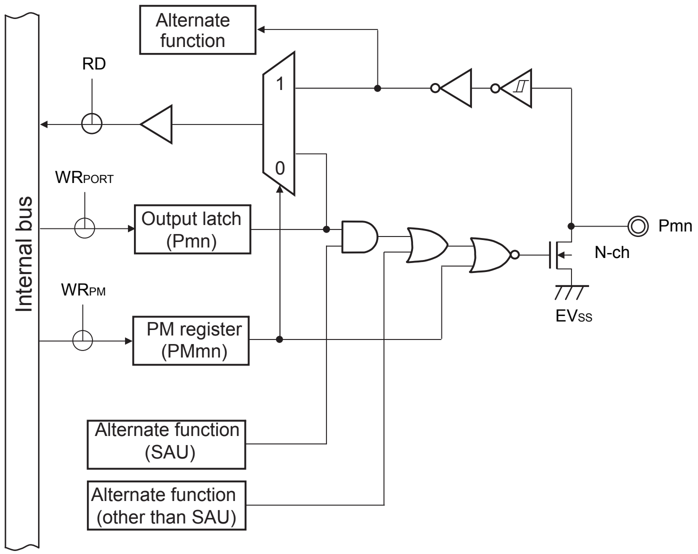
Remarks 1. For alternate functions, see **2.1 Port Function**.

2. SAU: Serial array unit

17. 2.4 Block Diagrams of Pins Figure 2-13. Pin Block Diagram for Pin Type 12-1-1)(p.46)

Old:

Figure 2-13. Pin Block Diagram for Pin Type 12-1-1

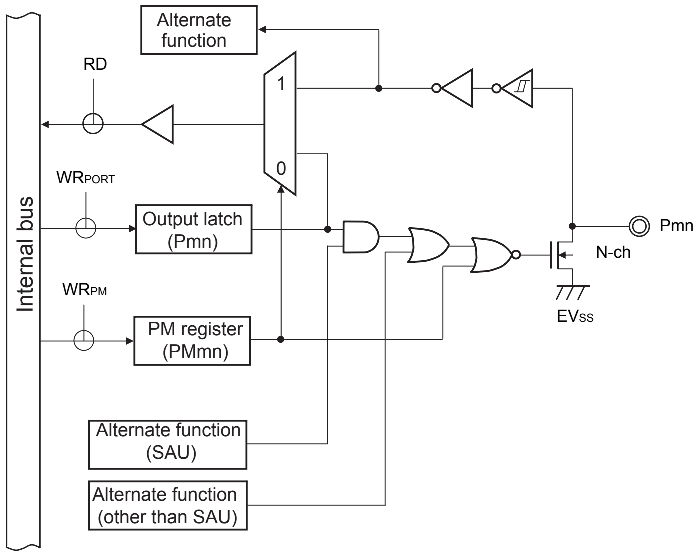


Remarks 1. For alternate functions, see **2.1 Port Function**.

2. SAU: Serial array unit

New:

Figure 2-13. Pin Block Diagram for Pin Type 12-1-1



Caution A through current may flow through if the pin is in the intermediate potential, because the input buffer is turned on when the pin is in output mode.

Remarks 1. For alternate functions, see **2.1 Port Function**.

2. SAU: Serial array unit