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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A183B/E	Rev.	2.00
Title	Notes on and Corrections to Descriptions for the P/E Suspension of Flash Memory in RX65N Group and RX651 Group		Information Category	Technical Notification		
Applicable Product	RX65N Group, RX651 Group	Lot No.	Reference Document	RX65N Group, RX651 Group Flash Memory User’s Manual: Hardware Interface Rev.2.00 (R01UH0602EJ0200)		
		All				

This document describes notes on P/E suspension and corrections to the flow chart of the P/E suspend command in RX65N Group, RX651 Group Flash Memory User’s Manual: Hardware Interface Rev.2.00.

1. Note on Issuing Programming Command During Erasure Suspension

• Note

When a programming command is issued for the blocks not to be erased while an erasure operation is suspended, an illegal-command error that should not occur may occur.

When a programming command is issued for the blocks to be erased while an erasure operation is suspended, an illegal-command error that should occur may not occur.

• Measure

When having changed the value of the FACI command start address register (FSADDR) while an erasure operation is suspended, restore the value saved before the P/E suspend command was issued to the FSADDR register before issuing the P/E resume command.

Programming to the blocks to be erased is prohibited while an erasure operation is suspended. Do not issue a programming command for the blocks to be erased while an erasure operation is suspended.

2. Corrections to the Flow Chart of the P/E Suspend Command

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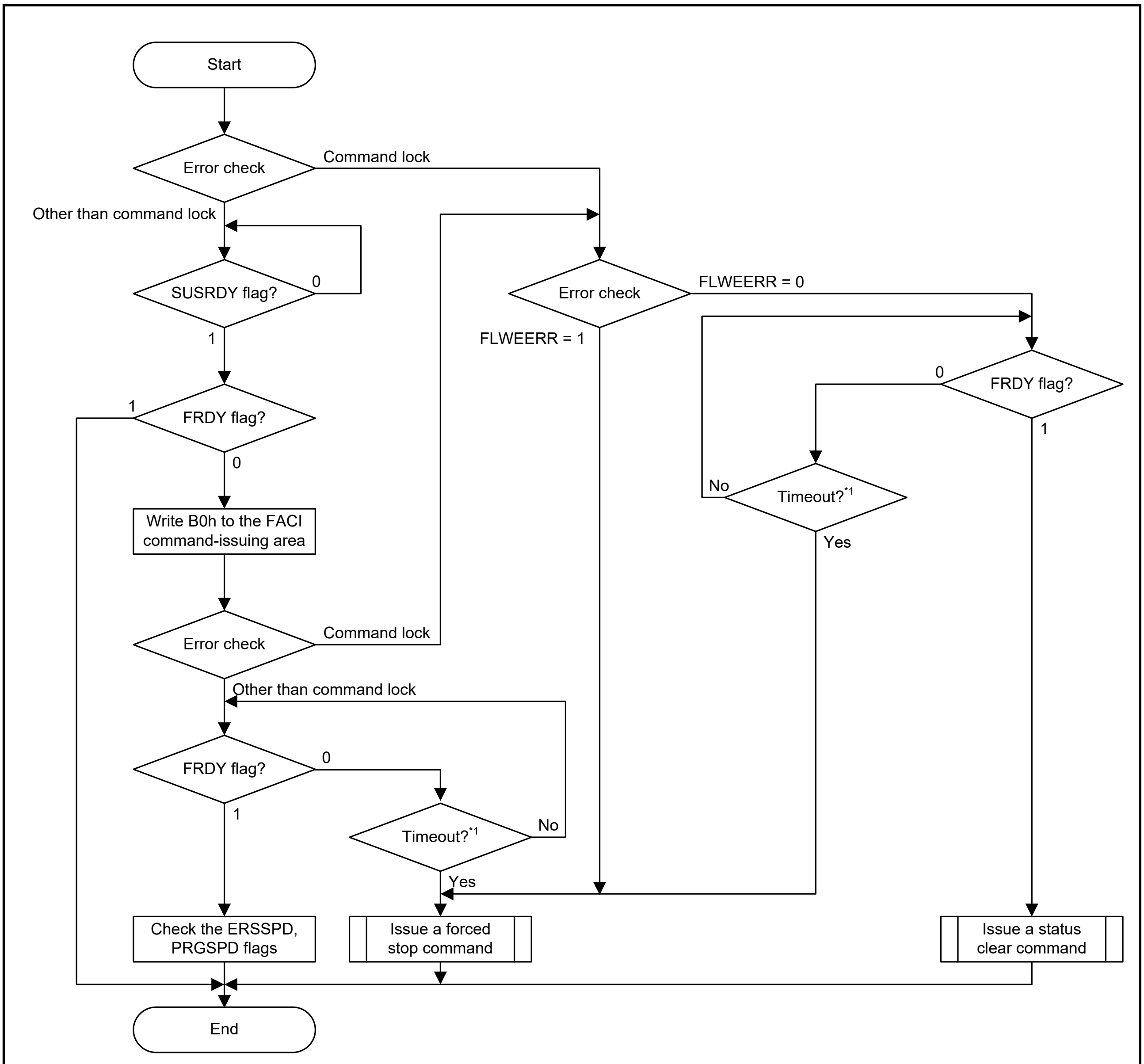
In Figure 6.9, Usage of the P/E Suspend Command, a processing flow never escapes from the loop for a checking procedure if the programming/erasure processing completed before checking the SUSRDY flag.

Therefore, a timeout processing and a breaking processing when the FRDY flag is 1 are to be added.

Also, the saving processing for the FSADDR register described in 1. Note on Issuing Programming Command During Erasure Suspension.

The changes made from TN-RX*-A183A/E to TN-RX*-A183B/E are indicated in blue as shown below.

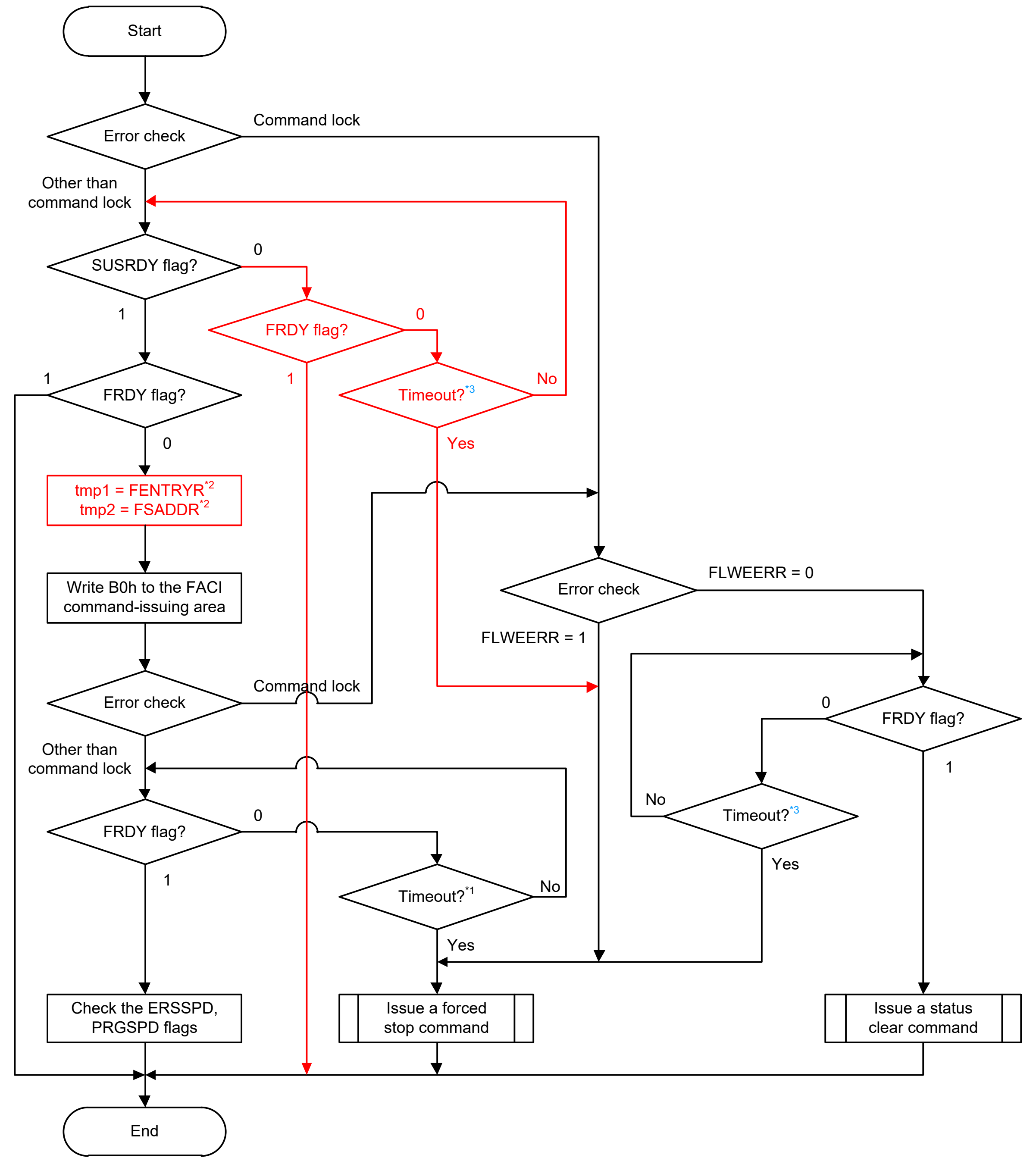
Before correction



Note 1. Judgment of the timeout is based on 1.1 times the suspend delay time during erasure (max) for both code flash memory and data flash memory.
For the suspend delay time during erasure, refer to the Electrical Characteristics chapter in the User's Manual: Hardware.

Figure 6.9 Usage of the P/E Suspend Command

After correction



Note 1. Judgment of the timeout is based on 1.1 times the suspend delay time during erasure (max) for both code flash memory and data flash memory.

Note 2. If the FENTRYR and FSADDR registers are not rewritten during suspension, these registers need not be saved.

Note 3. Judgment of the timeout is based on 1.1 times the erasure time (max) for both code flash memory and data flash memory.

For the suspend delay time during erasure and erasure time, refer to the Electrical Characteristics chapter in the User's Manual: Hardware.

Figure 6.9 Usage of the P/E Suspend Command

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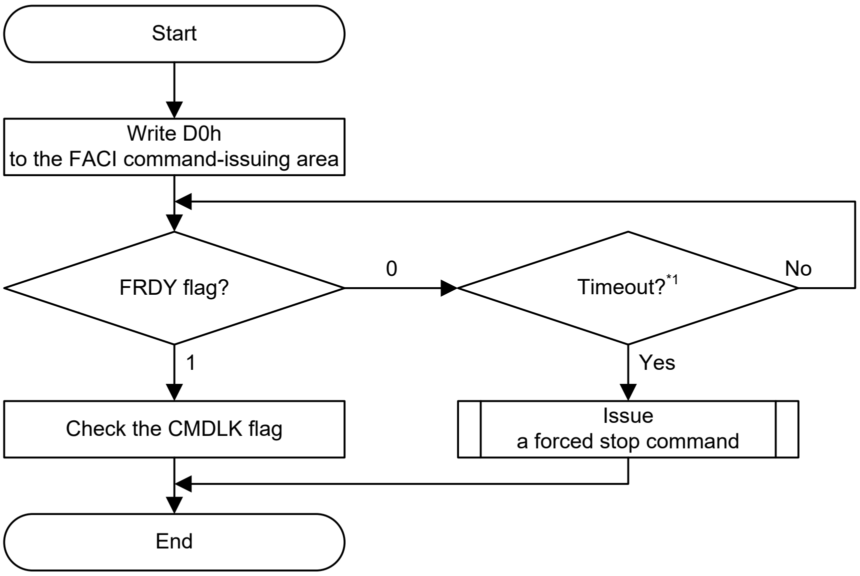
The restoring process for the FSADDR register described in 1. Note on Issuing Programming Command During Erasure Suspension is added to Figure 6.13, Usage of the P/E Resume Command.

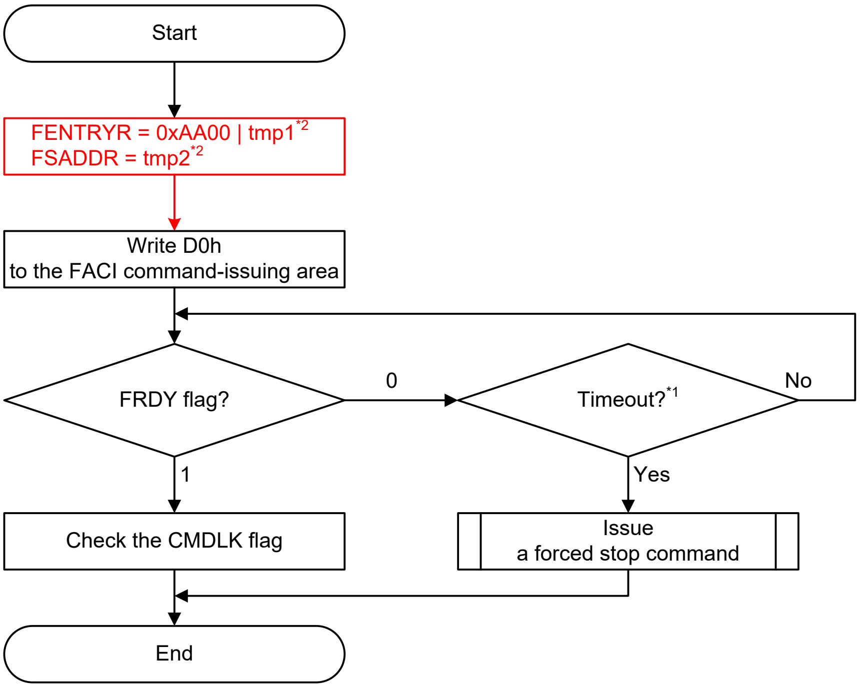
Before correction



Note 1. Judgment of the timeout is based on 1.1 times the maximum time for halted processing of the FACI command (refer to the Electrical Characteristics chapter in the User's Manual: Hardware).

Figure 6.13 Usage of the P/E Resume Command

After correction



Note 1. Judgment of the timeout is based on 1.1 times the maximum time for halted processing of the FACI command (refer to the Electrical Characteristics chapter in the User's Manual: Hardware).

Note 2. Restore the FENTRYR and FSADDR registers to the value saved before the P/E suspend command is issued. If these registers are not rewritten during suspension, restore is not needed.

Figure 6.13 Usage of the P/E Resume Command

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