

# RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU	Document No.	TN-SY*-A0036A/E	Rev.	1.00
Title	Functional Limitation of the JPEG Interface Decompression Control		Information Category	Technical Notification	
Applicable Product	Renesas Synergy™ S7G2 MCU Group	Lot No.	Reference Document	S7G2 Microcontroller Group User's Manual Rev.1.40 S5D9 Microcontroller Group User's Manual Rev.1.10	
	Renesas Synergy™ S5D9 MCU Group	All lots			

Renesas is adding a recommendation to deal with a limitation existing in the JPEG module of S7G2 and S5D9 devices to the JPEG module of S7G2 and S5D9 to prevent the incomplete JPEG decompression, which may result in locking JPEG module.

## 1. Revised information in User's Manual 57. JPEG Codec.

[Before] Chapter ends by 57.5 Bus Reset Processing

[After] Adding section 57.6 Usage Note as below

### 57.6 Usage Note

#### 57.6.1 Note on the decompression process

Renesas recommends that timeout detection mechanics would be implemented by software or operating system to prevent locking of the module in case invalid JPEG code data is detected. Especially when setting the JIFDCNT.JINC bit to 1b, timeout detection mechanics must be implemented by software or operation system because the decompression process might not be complete depending on the timing of input JPEG code data. If a timeout error occurs while decoding the image, reset the JPEG Codec by setting the BRST bit in the JCCMD register first and then follow the guidelines for decompression initial settings depicted in figure 57.7.

## 2. The reference information for decompression processing time in a specific case.

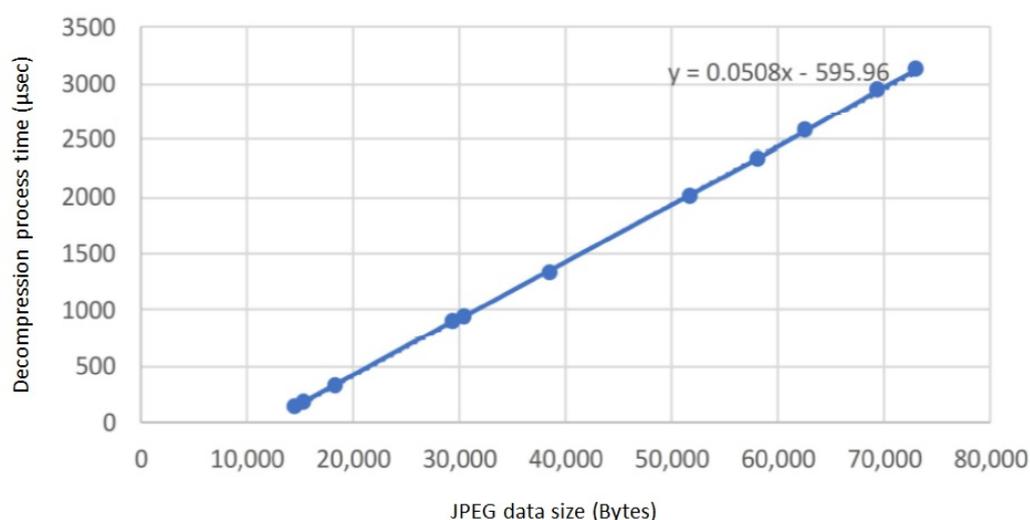


Figure 1. An example of the decompression process time (Reference data for S7G2 MCU)

The part of conditions The clock source is MOSC. ICLK=240MHz, PCLKA=120MHz,

Used memory is Code Flash (location of JPEG data), SRAM0 (location of Image data).

Figure 1 shows an example of the decompression process time in S7G2.

Note: The processing time depends on the compression ratio of JPEG code data, clock setting, used memory, bus state, and the other conditions, which has a dependency on entire software. This data is provided as a reference and guidelines for a software designer to implement and debug the SW timeout detection.