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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SY*-A023A/E	Rev.	1.00
Title	Additional description related to the store buffer of SRAM		Information Category	Technical Notification		
Applicable Product	Renesas Synergy™ Microcontrollers S7, S5, S3, and S1 Series	Lot No. All lots	Reference Document	S7G2 User's Manual (Rev.1.20), S5D9 User's Manual (Rev.1.00), S3A7 User's Manual (Rev.1.20), S3A3 User's Manual (Rev.1.00), S124 User's Manual (Rev.1.20), S128 User's Manual (Rev.1.00)		

Description for the store buffer of SRAM will be updated in the next revision of the affected documents.

1. SRAM section, Usage Notes

   The following text will be added in the next revision of the SRAM section.

   Store Buffer of SRAM

   For fast access between SRAM and CPU, a store buffer is used. When a load instruction is executed from the same address after a store instruction to SRAM, the load instruction might read out data from the buffer instead of data on the SRAM. To read data on the SRAM correctly, use either of the following procedures:

   - After writing to the SRAM (address = A), use the NOP instruction, then read the SRAM (address = A).
   - After writing to the SRAM (address = A), read data from area other than SRAM (address = A), then read the SRAM (address = A).