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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A181A/E	Rev.	1.00
Title	Addition of G Version (Topr = –40 to 105°C) Products for RX65N Group and RX651 Group		Information Category	Technical Notification		
Applicable Product	RX65N Group, RX651 Group	Lot No. All	Reference Document	RX65N Group, RX651 Group User's Manual: Hardware Rev.1.00 (R01UH0590EJ0100)		

The G-version products (Topr = –40 to 105°C) are added to the RX65N group and RX651 group MCU lineup.

This document contains a list and electrical characteristics of products to be added, and changes in the user's manual accompanying the addition of G-version products as shown below.

1. List of G-version Products

The following 48 products are added to the RX65N group and RX651 group MCU lineup.

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Operating Frequency (Max.)	Encryption Module	SDHI / SDSI	Operating Temperature (°C)
RX65N	R5F565N4AGFB	PLQP0144KA-B	512 K	256 K	120 MHz	Not available	Not available	–40 to +105
	R5F565N4BGFB	PLQP0144KA-B	512 K	256 K	120 MHz	Not available	Available	–40 to +105
	R5F565N4EGFB	PLQP0144KA-B	512 K	256 K	120 MHz	Available	Not available	–40 to +105
	R5F565N4FGFB	PLQP0144KA-B	512 K	256 K	120 MHz	Available	Available	–40 to +105
	R5F565N4AGFP	PLQP0100KB-B	512 K	256 K	120 MHz	Not available	Not available	–40 to +105
	R5F565N4BGFP	PLQP0100KB-B	512 K	256 K	120 MHz	Not available	Available	–40 to +105
	R5F565N4EGFP	PLQP0100KB-B	512 K	256 K	120 MHz	Available	Not available	–40 to +105
	R5F565N4FGFP	PLQP0100KB-B	512 K	256 K	120 MHz	Available	Available	–40 to +105
	R5F565N7AGFB	PLQP0144KA-B	768 K	256 K	120 MHz	Not available	Not available	–40 to +105
	R5F565N7BGFB	PLQP0144KA-B	768 K	256 K	120 MHz	Not available	Available	–40 to +105
	R5F565N7EGFB	PLQP0144KA-B	768 K	256 K	120 MHz	Available	Not available	–40 to +105
	R5F565N7FGFB	PLQP0144KA-B	768 K	256 K	120 MHz	Available	Available	–40 to +105
	R5F565N7AGFP	PLQP0100KB-B	768 K	256 K	120 MHz	Not available	Not available	–40 to +105
	R5F565N7BGFP	PLQP0100KB-B	768 K	256 K	120 MHz	Not available	Available	–40 to +105
	R5F565N7EGFP	PLQP0100KB-B	768 K	256 K	120 MHz	Available	Not available	–40 to +105
	R5F565N7FGFP	PLQP0100KB-B	768 K	256 K	120 MHz	Available	Available	–40 to +105
	R5F565N9AGFB	PLQP0144KA-B	1 M	256 K	120 MHz	Not available	Not available	–40 to +105
	R5F565N9BGFB	PLQP0144KA-B	1 M	256 K	120 MHz	Not available	Available	–40 to +105
	R5F565N9EGFB	PLQP0144KA-B	1 M	256 K	120 MHz	Available	Not available	–40 to +105

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Operating Frequency (Max.)	Encryption Module	SDHI / SDSI	Operating Temperature (°C)
RX65N	R5F565N9FGFB	PLQP0144KA-B	1 M	256 K	120 MHz	Available	Available	–40 to +105
	R5F565N9AGFP	PLQP0100KB-B	1 M	256 K	120 MHz	Not available	Not available	–40 to +105
	R5F565N9BGFP	PLQP0100KB-B	1 M	256 K	120 MHz	Not available	Available	–40 to +105
	R5F565N9EGFP	PLQP0100KB-B	1 M	256 K	120 MHz	Available	Not available	–40 to +105
	R5F565N9FGFP	PLQP0100KB-B	1 M	256 K	120 MHz	Available	Available	–40 to +105
RX651	R5F56514AGFB	PLQP0144KA-B	512 K	256 K	120 MHz	Not available	Not available	–40 to +105
	R5F56514BGFB	PLQP0144KA-B	512 K	256 K	120 MHz	Not available	Available	–40 to +105
	R5F56514EGFB	PLQP0144KA-B	512 K	256 K	120 MHz	Available	Not available	–40 to +105
	R5F56514FGFB	PLQP0144KA-B	512 K	256 K	120 MHz	Available	Available	–40 to +105
	R5F56514AGFP	PLQP0100KB-B	512 K	256 K	120 MHz	Not available	Not available	–40 to +105
	R5F56514BGFP	PLQP0100KB-B	512 K	256 K	120 MHz	Not available	Available	–40 to +105
	R5F56514EGFP	PLQP0100KB-B	512 K	256 K	120 MHz	Available	Not available	–40 to +105
	R5F56514FGFP	PLQP0100KB-B	512 K	256 K	120 MHz	Available	Available	–40 to +105
	R5F56517AGFB	PLQP0144KA-B	768 K	256 K	120 MHz	Not available	Not available	–40 to +105
	R5F56517BGFB	PLQP0144KA-B	768 K	256 K	120 MHz	Not available	Available	–40 to +105
	R5F56517EGFB	PLQP0144KA-B	768 K	256 K	120 MHz	Available	Not available	–40 to +105
	R5F56517FGFB	PLQP0144KA-B	768 K	256 K	120 MHz	Available	Available	–40 to +105
	R5F56517AGFP	PLQP0100KB-B	768 K	256 K	120 MHz	Not available	Not available	–40 to +105
	R5F56517BGFP	PLQP0100KB-B	768 K	256 K	120 MHz	Not available	Available	–40 to +105
	R5F56517EGFP	PLQP0100KB-B	768 K	256 K	120 MHz	Available	Not available	–40 to +105
	R5F56517FGFP	PLQP0100KB-B	768 K	256 K	120 MHz	Available	Available	–40 to +105
	R5F56519AGFB	PLQP0144KA-B	1 M	256 K	120 MHz	Not available	Not available	–40 to +105
	R5F56519BGFB	PLQP0144KA-B	1 M	256 K	120 MHz	Not available	Available	–40 to +105
	R5F56519EGFB	PLQP0144KA-B	1 M	256 K	120 MHz	Available	Not available	–40 to +105
	R5F56519FGFB	PLQP0144KA-B	1 M	256 K	120 MHz	Available	Available	–40 to +105
	R5F56519AGFP	PLQP0100KB-B	1 M	256 K	120 MHz	Not available	Not available	–40 to +105
	R5F56519BGFP	PLQP0100KB-B	1 M	256 K	120 MHz	Not available	Available	–40 to +105
	R5F56519EGFP	PLQP0100KB-B	1 M	256 K	120 MHz	Available	Not available	–40 to +105
	R5F56519FGFP	PLQP0100KB-B	1 M	256 K	120 MHz	Available	Available	–40 to +105

2. Electrical Characteristics

The electrical characteristics for the G-version products are listed below. Specifications not listed here are the same as D-version products.

Table 1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V

Item		Symbol	Value	Unit
Junction temperature	G version	T_j	–40 to +125	°C

Table 2 Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Operating temperature (G version)	T_{opr}	–40	—	105	°C

Table 3 DC Characteristics (1)

Conditions: VCC = AVCC0 = AVCC1 = VREFH0 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V, $T_a = T_{opr}$

Item				Symbol	G version Typ.	G version Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Full operation*2		I_{CC}*3	—	45	mA	ICLK = 120 MHz, PCLKA = 120 MHz, PCLKB = 60 MHz, PCLKC = 60 MHz, PCLKD = 60 MHz, FCLK = 60 MHz, BCLK = 120 MHz, BCLK pin = 60 MHz
		Normal operation	Peripheral module clocks are supplied*4		22	—		
			Peripheral module clocks are stopped*4, *5		12	—		
		CoreMark	Peripheral module clocks are stopped*4, *5		15	—		
		Sleep mode: Peripheral module clocks are supplied*4			16	28		
		All module clock stop mode (reference value)			8	19		
	Low-speed operating mode 1: Peripheral module clocks are stopped*4				1.1	—		All clocks 1 MHz
	Low-speed operating mode 2: Peripheral module clocks are stopped*4				1.1	—		All clocks 32.768 kHz
	Software standby mode				1.6	9.8		
	Deep software standby mode	Power is supplied to the standby RAM and USB resume detecting unit (USB0 only)			15.5	85	μA	
		Power is not supplied to the standby RAM and USB resume detecting unit (USB0 only)	Low power consumption function of the power-on reset circuit is disabled*6		11.5	48		
			Low power consumption function of the power-on reset circuit is enabled*7		4.9	39		
		Increase current by operating RTC	When a low C_L crystal is in use		1	—		
			When a standard C_L crystal is in use		2	—		
	When the RTC is operating while VCC is not supplied (Only the RTC and sub-clock oscillator operate with the battery backup function)		When a low C_L crystal is in use		0.9	—		V_{BATT} = 2.0 V, VCC = 0 V
					1.6	—		V_{BATT} = 3.3 V, VCC = 0 V
			When a low C_L crystal is in use		1.7	—		V_{BATT} = 2.0 V, VCC = 0 V
					3.3	—		V_{BATT} = 3.3 V, VCC = 0 V
	Inrush current on release from deep software standby mode		Inrush current*8	I_{RUSH}	—	70	mA	
			Total inrush current*8	E_{RUSH}	—	1.0	μC	

Note 1. Supply current values are measured when all output pins are unloaded and all input pull-up resistors are disabled.
Note 2. Peripheral module clocks are supplied.
Note 3. I_{CC} depends on the f (ICLK) as follows. (when ICLK/PCLKA : PCLKB/PCLKC/PCLKD : BCLK : BCLK pin = 2 : 1 : 2 : 1 and EXTAL = 12 MHz)
● G version
I_{CC} max = 0.33 × f + 9 (full operation in high-speed operating mode)
I_{CC} typ = 0.16 × f + 2.8 (normal operation in high-speed operating mode)
I_{CC} typ = 0.4 × f + 1.1 (ICLK 1 MHz max) (low-speed operating mode 1)
I_{CC} max = 0.21 × f + 9 (sleep mode)
Note 4. Whether the peripheral module clocks are supplied or stopped is controlled only by the bit settings in the module stop control registers A to D.
Note 5. When the peripheral module clock is stopped, the settings of the clock frequency are as follows:
ICLK = 120 MHz and PCLKA = PCLKB = PCLKC = PCLKD = FCLK = BCLK = BCLK pin = 3.75 MHz (divided by 64).
Note 6. When the low power consumption function is disabled, the DEEPCUT[1:0] bits are set to 01b.
Note 7. When the low power consumption function is enabled, the DEEPCUT[1:0] bits are set to 11b.
Note 8. Reference value

Table 4 DC Characteristics (2)

Conditions: VCC = AVCC0 = AVCC1 = VREFH0 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V, $T_a = T_{opr}$

Item			Symbol	G version			Unit	Test Conditions
				Min.	Typ.	Max.		
Analog power supply current*1	During 12-bit A/D conversion (unit 0)		AI_{CC}	—	0.8	1	mA	IAVCC0_AD
	During 12-bit A/D conversion (unit 0) with channel dedicated sample-and-hold circuits (3 channels)			—	1.7	2.5	mA	IAVCC0_AD+SH
	During 12-bit A/D conversion (unit 1)			—	0.6	1	mA	IAVCC1_AD
	During 12-bit A/D conversion (unit 1) + temperature sensor			—	0.7	1.1	mA	IAVCC1_AD+TEMP
	During D/A conversion (per channel)	Unbuffered output		—	0.25	0.4	mA	IAVCC1_DA
		Buffered output		—	0.57	0.8	mA	
	Waiting for A/D, D/A, and temperature sensor conversion (all units)			—	0.9	1.4	mA	IAVCC0 + IAVCC1
	A/D, D/A, and temperature sensor are in standby mode (all units)			—	1.4	9.0	μA	IAVCC0 + IAVCC1
Reference power supply current	During 12-bit A/D conversion (unit 0)		AI_{REFH}	—	38	60	μA	IVREFH0
	Waiting for 12-bit A/D conversion (unit 0)			—	0.07	0.6	μA	IVREFH0
	12-bit A/D conversion is in standby mode (unit 0)			—	0.07	0.5	μA	IVREFH0
USB operating current	Low speed	USB0	$I_{CCUSBLS}$	—	3.7	6.5	mA	VCC_USB
	Full speed	USB0	$I_{CCUSBFS}$	—	4.2	10	mA	VCC_USB
RAM retension voltage			V_{RAM}	2.7	—	—	V	
VCC rising gradient			SrVCC	8.4	—	20000	μs/V	
VCC falling gradient*2			SfVCC	8.4	—	—	μs/V	

Note 1. The reference power supply current is included in the power supply current value for 12-bit A/D converter (unit 1) and D/A converter.
Note 2. This applies when V_{BATT} is used.

3. Correction to the User's Manual

Accompanying the addition of G-version products, changes the user's manual as follows.

- Note 4 is added to Table 1.1.

Table 1.1 Outline of Specifications (8/8)

Classification	Module/Function	Description
		Omitted
Operating temperature		D-version: -40 to +85°C G-version: -40 to +105°C*4
		Omitted

Note 1. Magic Packet™ is a registered trademark of Advanced Micro Devices, Inc.
Note 2. The product part number differs according to whether or not it supports encryption.
Note 3. The product part number differs according to whether or not it includes an SDHI (SD host interface) / SDSI (SD slave interface).
Note 4. Please contact us if you are using a G-version.

- Note 3 is added to Table 57.35.

Table 57.35 QSPI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load condition: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving capacity control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions*2
QSPI	QSPCLK clock cycle time	t_{QScyc}	2	4080	t_{PBcyc}	Figure 57.51
	Data input setup time*3	t_{Su}	6.5	—	ns	Figure 57.52, Figure 57.53
	Omitted					

Note 1. t_{PBcyc}: Cycle time of the PCLKB
Note 2. When a letter “-A”, “-B”, etc. to indicate group membership is appended to the pin name, each pin is recommended to use in combination with the pins in the same group. All QSPI AC timings are measured in combination with the pins in the same group.
Note 3. When testing G version products at the condition of +85 < Ta ≤ +105°C, the drive capacity control register 2 for the QSPCLK pin is set to “high-speed interface high-drive output”.

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