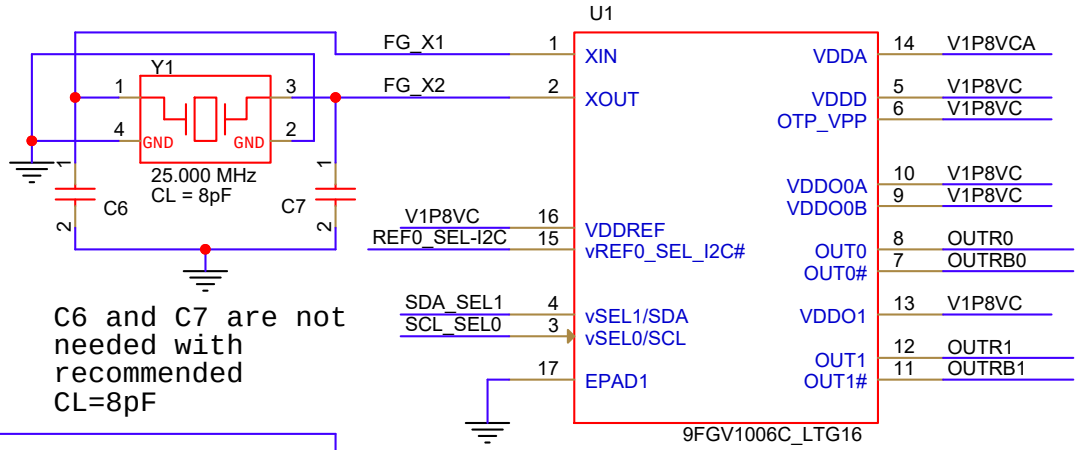
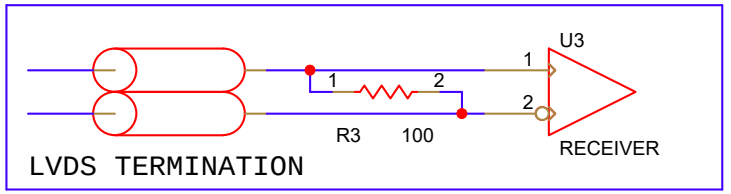
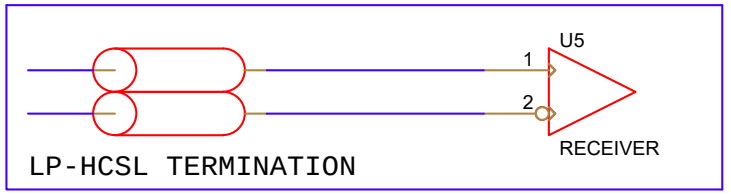
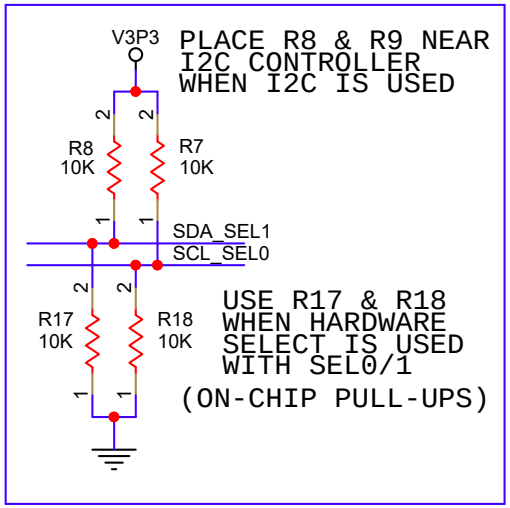
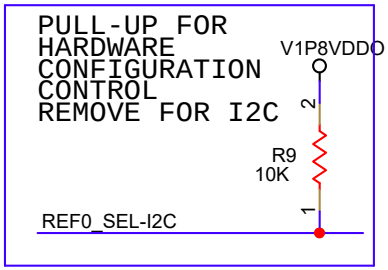


C6 and C7 are not needed with recommended CL=8pF



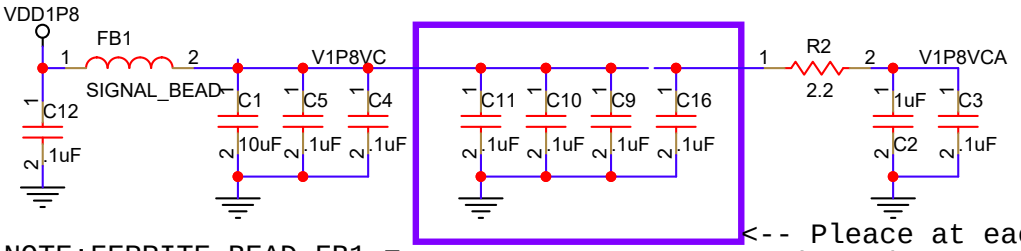






Layout notes.

1. Separate Xout and Xin traces by 3 x the trace width.
2. Do not share crystal load capacitor ground via with other components.
3. Route power from bead through bulk capacitor pad then through 0.1uF capacitor pad then to clock chip Vdd pad.
4. Place all 0.1uF caps as close as possible to the power pins, and on the same side of the PCB.
5. Do not share ground vias. One ground pin one ground via.



<-- Pleace at each VddO pin
Pin 6 does not need a capacitor

NOTE:FERRITE BEAD FB1 =

Manufacture	Part Number	Z@100MHz	PkgSz	DC res.	Current(Ma)
Fair-Rite	2504021217Y0	120	0402	0.5	200
muRata	BLM15AG221SN1	220	0402	0.35	300
muRata	BLM15BB121SN1	120	0402	0.35	300
TDK	MMZ1005S241A	240	0402	0.18	200
TECSTAR	TB4532153121	120	0402	0.3	300

Revision history
0.1 3/30/2017 first publication
0.3 2/12/2021 Updated symbol for rev C

Integrated Device Technology
San Jose, CA

Size	Document Number	Rev
A	9FGV1006C_SCH	0.4

Date: 07/02/2021 Sheet 1 of 1