

# Smart Configurator for RL78 V1.2.0

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## Release Note

### Introduction

Thank you for using the Smart Configurator for RL78.

This document describes the restrictions and points for caution. Read this document before using the product.

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## 1. Introduction

Smart Configurator is a utility for combining software to meet your needs. It supports the following three functions related to the embedding of Renesas drivers in your systems: importing middleware, generating driver code, and setting pins.

### 1.1 System requirements

Smart Configurator for RL78 V1.2.0 operating environment is as follows.

#### 1.1.1 PC

- IBM PC/AT compatibles (Windows® 10 64 bit, Windows® 8.1 64 bit)
- Processor: 1 GHz or higher (must support hyper-threading, multi-core CPUs)
- Memory capacity: 4 GB or more recommended.
- Hard disk capacity: 300 MB or more spare capacity
- Display: 1024 x 768 or higher resolution, 65,536 or more colors

#### 1.1.2 Development Environments

- Renesas Electronics Compiler for RL78 [CC-RL] V1.11 or later
- LLVM for Renesas RL78 10.0.0.202110 or later
- IAR Embedded Workbench for Renesas RL78 V4.21.1 or later
- SMS Assembler <sup>Note</sup> V1.00.00 or later

Note:

If you want to add SMS Assembler to e<sup>2</sup> studio, install it from the integrated installer of e<sup>2</sup> studio 21-04 or later. ([e<sup>2</sup> studio](#))

As with other compilers, select and install from the [Additional Software] - [Renesas Toolchains & Utilities] tab of the e<sup>2</sup> studio setup wizard.

## 2. Support List

### 2.1 Support Devices List

Below is a list of devices supported by the Smart Configurator for RL78 V1.2.0.

**Table 2-1 Support Devices**

Group (HW Manual number)	PIN	Device name
RL78/G23 Group (R01UH0896EJ0100)	30pin	R7F100GAFxSP, R7F100GAGxSP, R7F100GAHxSP, R7F100GAJxSP
	32pin	R7F100GBFxNP, R7F100GBGxNP, R7F100GBHxNP, R7F100GBJxNP, R7F100GBFxFP, R7F100GBGxFP, R7F100GBHxFP, R7F100GBJxFP
	36pin	R7F100GCFxLA, R7F100GCGxLA, R7F100GCHxLA, R7F100GCJxLA
	40pin	R7F100GEFxNP, R7F100GEGxNP, R7F100GEHxNP, R7F100GEJxNP
	44pin	R7F100GFFxFP, R7F100GFGxFP, R7F100GFHxFP, R7F100GFJxFP, R7F100GFKxFP, R7F100GFLxFP, R7F100GFNxFP
	48pin	R7F100GGFxFB, R7F100GGGxFB, R7F100GGHxFB, R7F100GGJxFB, R7F100GGKxFB, R7F100GGLxFB, R7F100GGNxFB, R7F100GGFNP, R7F100GGGxNP, R7F100GGHxNP, R7F100GGJxNP, R7F100GGKxNP, R7F100GGLxNP, R7F100GGNxNP
	52pin	R7F100GJFxFA, R7F100GJGxFA, R7F100GJHxFA, R7F100GJJxFA, R7F100GJKxFA, R7F100GJLxFA, R7F100GJNxFA
	64pin	R7F100GLFxFA, R7F100GLGxFA, R7F100GLHxFA, R7F100GLJxFA, R7F100GLKxFA, R7F100GLLxFA, R7F100GLNxFA, R7F100GLFxFB, R7F100GLGxFB, R7F100GLHxFB, R7F100GLJxFB, R7F100GLKxFB, R7F100GLLxFB, R7F100GLNxFB, R7F100GLFxLA, R7F100GLGxLA, R7F100GLHxLA, R7F100GLJxLA, R7F100GLKxLA, R7F100GLLxLA, R7F100GLNxLA
	80pin	R7F100GMGxFA, R7F100GMHxFA, R7F100GMJxFA, R7F100GMKxFA, R7F100GMLxFA, R7F100GMNxFA, R7F100GMGxFB, R7F100GMHxFB, R7F100GMJxFB, R7F100GMKxFB, R7F100GMLxFB, R7F100GMNxFB
	100pin	R7F100GPGxFB, R7F100GPHxFB, R7F100GPJxFB, R7F100GPKxFB, R7F100GPLxFB, R7F100GPNxFB, R7F100GPGxFA, R7F100GPHxFA, R7F100GPJxFA, R7F100GPKxFA, R7F100GPLxFA, R7F100GPNxFA
	128pin	R7F100GSJxFB, R7F100GSKxFB, R7F100GSLxFB, R7F100GSNxFB

## 2.2 Support Components List

Below is a list of Components supported by the Smart Configurator for RL78 V1.2.0.

**Table 2-2 Support Components (1/2)**

✓ : Support, -: Non-support

No	Components	Mode	RL78/G23	Remarks
1	A/D Converter	-	✓	
2	Clock Output/Buzzer Output Controller	-	✓	
3	Comparator	-	✓	
4	CSI Communication	Transmission	✓	
		Reception	✓	
		Transmission/reception	✓	
5	D/A Converter	-	✓	
6	Data Transfer Controller	-	✓	
7	Delay Counter	-	✓	
8	Divider Function	-	✓	
9	External Event Counter	-	✓	
10	IIC Communication (Master mode)	-	✓	
11	IIC Communication (Slave mode)	-	✓	
12	Input Pulse Interval Measurement	-	✓	
13	Input Signal High-/Low-Level Width Measurement	-	✓	
14	Interrupt Controller	-	✓	
15	Interval Timer	8 bit count mode	✓	
		16 bit count mode	✓	
		16 bit capture mode	✓	
		32 bit count mode	✓	
16	Key Interrupt	-	✓	
17	One-Shot Pulse Output	-	✓	
18	Ports	-	✓	
19	PWM Output	-	✓	
20	Real-Time Clock	-	✓	
21	Remote Control Signal Receiver	-	✓	
22	SNOOZE Mode Sequencer	-	✓	
23	Square Wave Output	-	✓	

Table 2-3 Support Components (2/2)

✓ : Support, -: Non-support

No	Components	Mode	RL78/G23	Remarks
24	UART Communication	Transmission	✓	
		Reception	✓	
		Transmission/reception	✓	
25	Voltage Detector	-	✓	
26	Watchdog Timer	-	✓	
27	Logic & Event Link Controller	-	✓	Need download in Smart Configurator RL78

## 2.3 New support

### 2.3.1 Import / Export component configuration feature is supported

The Import/Export configuration feature is supported. The component configurations can be exported to a xml file and can be imported from the xml file into another Smart Configurator project.

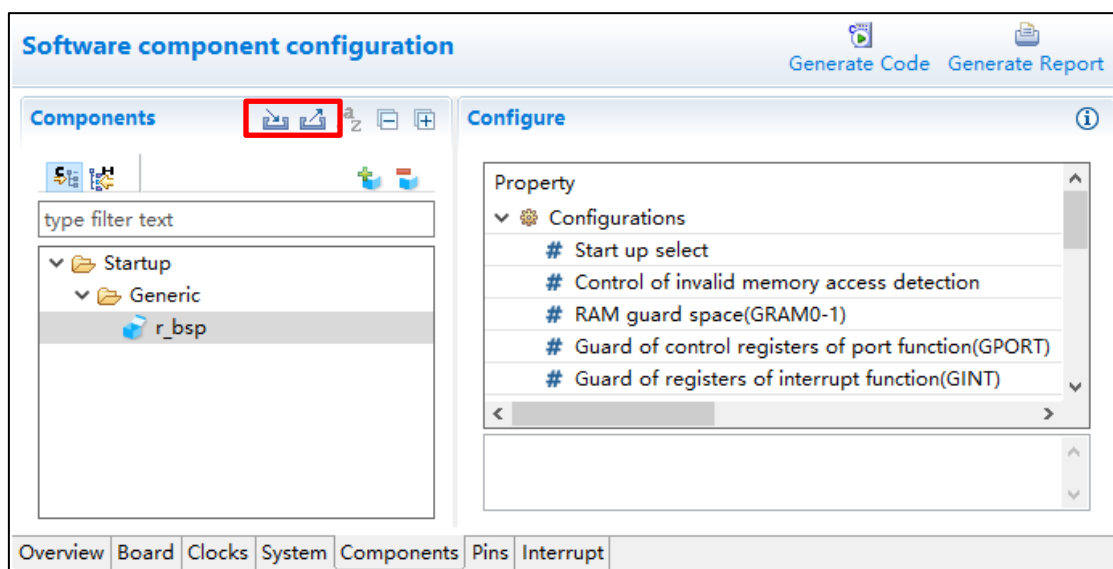


Figure 2-1 Import / Export configuration feature on the “Component” page

### 2.3.2 The default value for preference setting "Creation date" has been updated.

The default value for preference setting "Creation date" has been updated from "Output" to "No output".

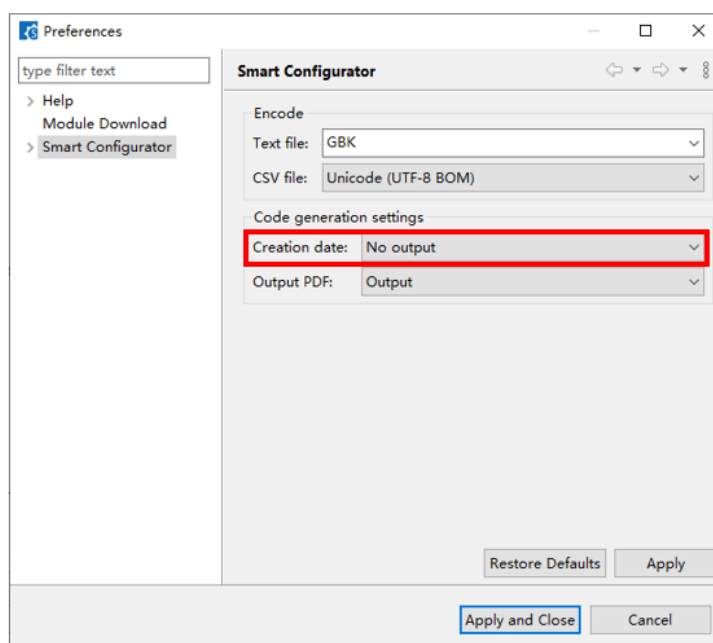


Figure 2-2 The default value for the “Create date” preference setting

### 2.3.3 Added the option to disable the generation of PDF files

Added the option to disable the generation of PDF files into the user project when the RL78 Software System Integration components are added.

To use this option, please navigate to the Smart Configurator preferences page in [Window] - [Preferences] - [Smart Configurator] and set the "Output PDF" item to 'No output'.

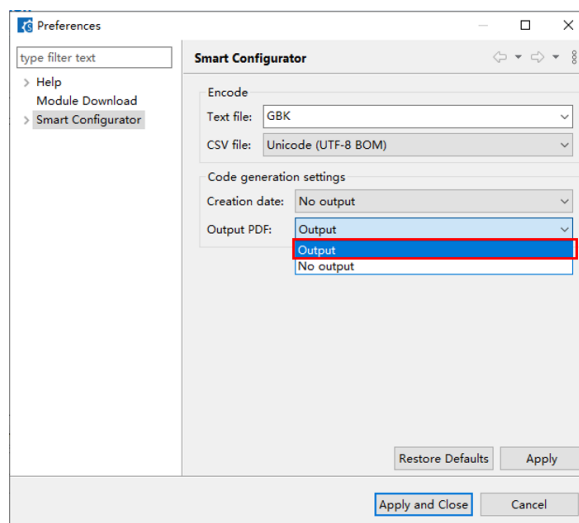


Figure 2-3 The option of output PDF files setting

### 2.3.4 Code generation operation will be triggered when build project

Under e<sup>2</sup> studio 2022-01, auto-generate code feature was introduced as when a project is built, code generation operation will be triggered firstly to prevent mismatch between the settings in the GUI and the built codes.

If user don't want to use this function, please use the below way to turn off it:

- Open project properties and unselect "SC Code Generation Builder"

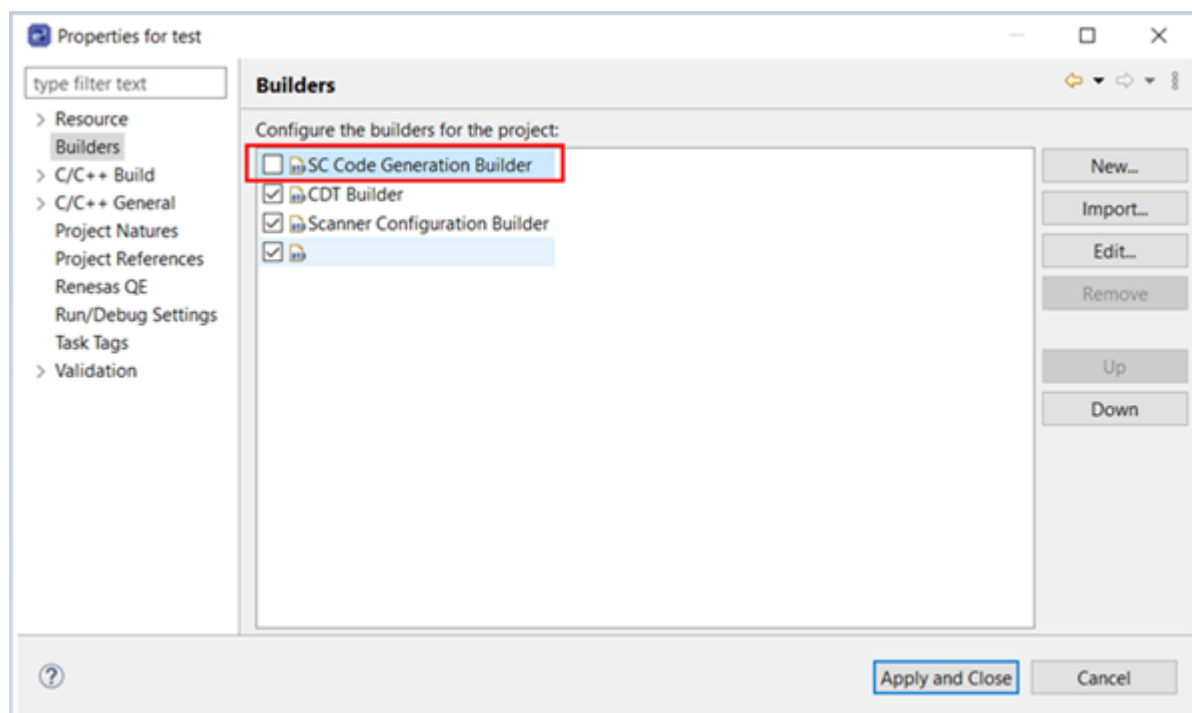


Figure 2-4 Project property setting to turn off code generation on build



### 2.3.5 BSP revision update and version check supported

- 1) Updated the default BSP added when creating a Smart Configurator project to rev.1.13.
- 2) Added a version check macro (BSP\_CFG\_CONFIGURATOR\_VERSION) to use Smart Configurator and BSP in the correct combination. The default value is 1020 (Smart Configurator version 1.2.0).
  - a) "BSP\_CFG\_CONFIGURATOR\_VERSION" was generated in r\_bsp\_config.h as following:

```

/* Version number of Smart Configurator.
This macro definitions is updated by Smart Configurator.
If you are using e2studio, set the following values.
2021-04 : 1001
2021-07 : 1010
2021-10 : 1010
If you are using Smart the standalone version of Smart Configurator,
set the following values.
v1.0.1 : 1001
v1.1.0 : 1010
*/
#define BSP_CFG_CONFIGURATOR_VERSION (1020) /* Generated value. Do not edit this
manually */

```

- b) When user use with older versions of Smart Configurator, there will occur with build errors as following.  
 error: "Make sure that the value of BSP\_CFG\_CONFIGURATOR\_VERSION defined in r\_config/r\_bsp\_config.h matches the version of Smart Configurator you are using. If they do not match, change the settings. If they match, you need to upgrade your Smart Configurator. Please upgrade Smart Configurator."

### 2.3.6 Improvement for Overview page

The "Overview" page has been updated to provide additional links to "Videos" and "What's New" information etc.

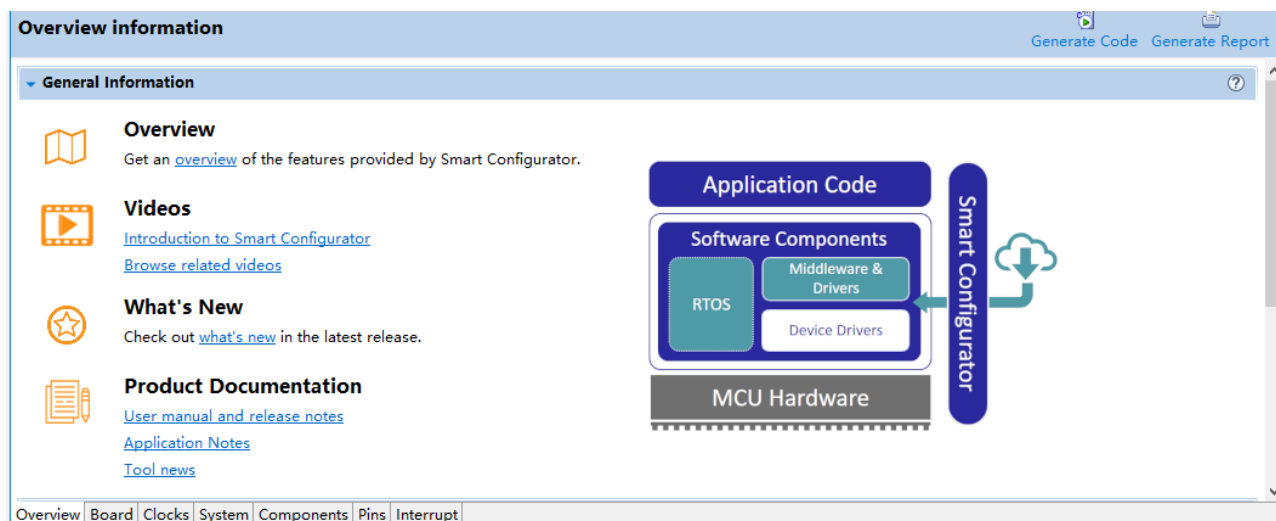


Figure 2-5 Overview page

### 3. Changes

This chapter describes changes to the Smart Configurator for RL78 V1.2.0.

#### 3.1 Correction of issues/limitations

**Table 3-1 List of Correction of issues/limitations**

✓ : Applicable, -: Not Applicable

No	Description	RL78/G23	Remarks
1	Fixed the UARTA callback function calling for 1-byte transmission	✓	

##### 3.1.1 Fixed the UARTA callback function calling for 1-byte transmission

When using UARTA transmission function to transmit data in [Continuous transmission by polling] mode, no matter 1-byte or several data, the generation code specification is unified as the following:

- [Transmission end] callback function cannot be selected on GUI.
- In {Config\_UARTAn}\_user.c file,
  - r\_{Config\_UARTAn}\_PollingEnd\_UserCode () is added
  - r\_{Config\_UARTAn}\_send\_1byte () and R\_{Config\_UARTAn}\_Send\_Polling () are removed

Detailed usage can be referred to latest User's Manual of RL78 API Reference.

## 3.2 Specification changes

Table 3-2 List of Specification changes

✓ : Applicable, - : Not Applicable

No	Description	RL78/G23	Remarks
1	Improvement for deleting E20 emulator selection in on-chip debug setting	✓	
2	Adding output disable code to R_Config_UARTn_Stop() function	✓	
3	Improvement for no R_Systeminit() function declaration issue in macrodriver.h	✓	
4	Improvement for Smart Configurator can be opened when porting the e <sup>2</sup> studio project into CS+	✓	
5	Improvement for "Input buffer" function in PORT	✓	
6	New API added for ELCL	✓	
7	Improvement for IIC Communication code	✓	
8	Improvement for ELCL initialization function calling	✓	
9	Improvement for pin allocation to use "PIORn=0" as default selection	✓	
10	Improvement for the register banks can be the same if they have the same priority	✓	
11	Improvement for reserving RAM area when On-Chip debug trace function used	✓	
12	Improvement for supporting LLVM C++ project	✓	
13	Improvement for UARTA transfer rate range	✓	
14	Improvement for avoiding create an entry in DTC reserved RAM area of the on-chip debug trace	✓	

### 3.2.1 Improvement for deleting E20 emulator selection in on-chip debug setting

The E20 emulator doesn't support RL78/G23. From Smart Configurator for RL78 V1.2.0, E20 emulator selection is deleted from [System] page. When the old project with E20 selected loaded, the setting will be changed to "E2 Lite" automatically.

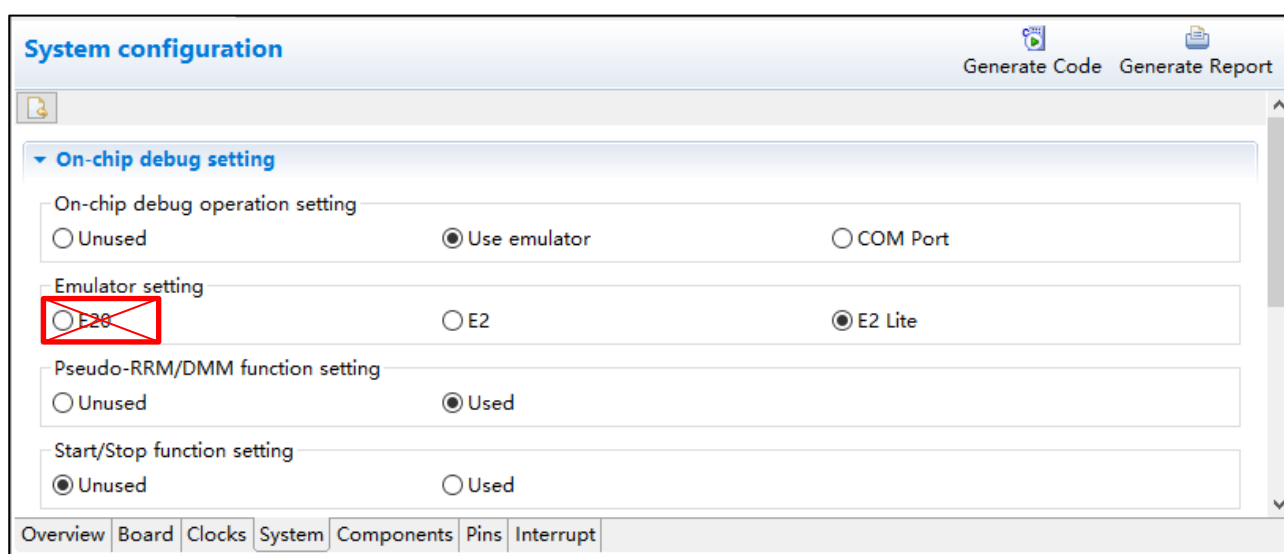


Figure 3-1 Deleted E20 emulator support

### 3.2.2 Adding output disable code to *R\_Config\_UARTn\_Stop()* function

When UARTn in SAUm operate as Transmission mode, UARTn output disable setting (SOEmn = 0) is generated in *R\_Config\_UARTn\_Stop()* function.

```

/*****
 * Function Name: R_Config_UART0_Stop
 * Description  : This function stops UART0 module operation.
 * Arguments    : None
 * Return Value : None
 *****/
void R_Config_UART0_Stop(void)
{
    STMK0 = 1U; /* disable INTST0 interrupt */
    ST0 |= 0001 SAU_CH0_STOP_TRG_ON; /* disable UART0 transmit */
    SOE0 &= (uint16_t)~ 0001 SAU_CH0_OUTPUT_ENABLE; /* disable UART0 output */
    STIF0 = 0U; /* clear INTST0 interrupt flag */
}

```

Figure 3-2 Added UART0 output disable operation in Stop function

### 3.2.3 Improvement for no *R\_Systeminit()* function declaration issue in *r\_cg\_macrodriver.h*

When set the API output function as [Output only initialization API function] in Preferences setting, the *R\_Systeminit()* function declaration can be generated in *r\_cg\_macrodriver.h*.

### 3.2.4 Improvement for Smart Configurator can be opened when porting the e<sup>2</sup> studio project into CS+

From Smart Configurator for RL78 V1.2.0, when open an existing e<sup>2</sup> studio Smart configuration project (exported by e<sup>2</sup> studio "Renesas common project file" feature) in CS+, the configuration settings can be opened after launching Smart Configurator.

### 3.2.5 Improvement for "Input buffer" function in PORT

The "Input buffer" is changed to "Input buffer OFF". And "Input buffer OFF" selection is only available when port is used as output function.



Figure 3-3 "Input buffer OFF" function in PORT

In *R\_<Config\_PORT>\_Create()* code generation:

- When "Input buffer OFF" is inactive or uncheck, *\_00\_PDIDISnx\_INPUT\_BUFFER\_ON* is set into PDIDIS register.
- When "Input buffer OFF" is active and checked, *\_xx\_PDIDISnx\_INPUT\_BUFFER\_OFF* is set into PDIDIS register.

```

void R_Config_PORT_Create(void)
{
    /* Set PORT0 registers */
    .....
    PDIDIS0 = _00_PDIDISn4_INPUT_BUFFER_ON | _00_PDIDISn3_INPUT_BUFFER_ON |
              _00_PDIDISn2_INPUT_BUFFER_ON | _01_PDIDISn0_INPUT_BUFFER_OFF;
    .....
    R_Config_PORT_Create_UserInit();
}

```

### 3.2.6 New API added for ELCL

New API functions are generated for ELCL component when output ELCL signal is selected as INTELCL:

- R\_Config\_ELCL\_xxxFunction\_Start
- R\_Config\_ELCL\_xxxFunction\_Stop
- interrupt handler function r\_Config\_ELCL\_xxxFunction\_interrupt

### 3.2.7 Improvement for IIC Communication code

When using IIC Communication (Master mode) component and selected resource as IIC0n, the generation code is improved to easily understand.

- 1) Added detailed comment for the SDA&SCL pin's waiting operation in R\_Config\_IICmn\_StartCondition() and R\_Config\_IICmn\_StopCondition() functions.

```

/* *****
 * Function Name: R_Config_IIC00_StartCondition
 * Description : This function starts the IIC00 condition.
 * Arguments   : None
 * Return Value : None
 * *****
 */
void R_Config_IIC00_StartCondition(void)
{
    volatile uint8_t w_count;

    S00 &= (uint16_t)~_0001_SAU_CH0_DATA_OUTPUT_1; /* clear IIC00 SDA */

    /* Set delay to secure a hold time after SDA output low. The delay time depend on slave device.
     Here set 5us as default base on current clock */
    for (w_count = 0U; w_count <= IIC00_WAITTIME; w_count++)
    {
        NOP();
    }

    S00 &= (uint16_t)~_0100_SAU_CH0_CLOCK_OUTPUT_1; /* clear IIC00 SCL */
    S0E0 |= _0001_SAU_CH0_OUTPUT_ENABLE; /* enable IIC00 output */
    SS0 |= _0001_SAU_CH0_START_TRG_ON; /* enable IIC00 */

    /* Set delay to secure a hold time after SCL output low. The delay time depend on slave device.
     Here set 5us as default base on current clock */
    for (w_count = 0U; w_count <= IIC00_WAITTIME; w_count++)
    {
        NOP();
    }
}

```

Figure 3-4 Added detail comment for SDA/SCL pin's waiting operation

- 2) Added the code to clear error detection flag and calling R\_Config\_IICmn\_StopCondition() function in IICm interrupt handler function, so that the next send/receive operation can work correctly.

```

static void __near r_Config_IIC00_interrupt(void)
{
    volatile uint16_t w_count;

    /* Set delay to secure a hold time after SDA, SDL output. The delay time depend on slave device.
     Here set 20us as default base on current clock */
    for (w_count = 0U; w_count <= IIC00_WAITTIME_2; w_count++)
    {
        NOP();
    }

    if ((0x0002U == (SSR00 & _0002_SAU_PARITY_ERROR)) && (0U != g_iic00_tx_count))
    {
        SIR00 |= _0002_SAU_SIRMN_PECTMN; /* clear ACK error detection flag */
        R_Config_IIC00_StopCondition();
        r_Config_IIC00_callback_master_error(MD_NACK);
    }
    else if ((0x0001U == (SSR00 & _0001_SAU_OVERRUN_ERROR)) && (0U != g_iic00_tx_count))
    {
        SIR00 |= _0001_SAU_SIRMN_OVCTMN; /* clear overrun error detection flag */
        R_Config_IIC00_StopCondition();
        r_Config_IIC00_callback_master_error(MD_OVERRUN);
    }
    else
    {
        // ...
    }
}

```

Figure 3-5 Clear error detection flag and calling R\_Config\_IICmn\_StopCondition() function

### 3.2.8 Improvement for ELCL initialization function calling

From Smart Configurator for RL78 V1.2.0, ELCL initialize function: `R_Config_ELCL_xxxFunction_Create()` is called in `R_Systeminit()` in generated code.

### 3.2.9 Improvement for pin allocation to use "PIORn=0" as default selection

From Smart Configurator for RL78 V1.2.0, improve pin allocation to use "PIORn=0" as default selection,

The screenshot shows the 'Pin configuration' window. On the left, there's a 'Hardware Resource' tree. The main area is 'Pin Function' with a search bar and a table. The table has columns: Enabled, Function, PIOR, Assignment, Pin Number, Direction, and Remarks. A red box highlights the 'PIOR' column, showing values like PIOR5, PIOR4, etc. To the right, there's a table with columns: Bit, Alternative function, and Setting value. A red box highlights the 'PIOR' column in this table as well.

Bit	Alternative function	Setting value
PIOR5	INTP1	P46
	INTP3	P30
	INTP4	P31
	INTP5	P143
	INTP7	P141
	INTP8	P74
	INTP9	P75
	TxD1	P02
	RxD1	P03
	SCL10	P04
	SDA10	P03
	SI10	P03
	SO10	P02
	SC10	P04
PIOR4	PCLBUZ1	P141
	INTP5	P15

Figure 3-6 PIOR default setting

### 3.2.10 Improvement for the register banks can be the same if they have the same priority

User can config the same register bank value when the priority of interrupts is same.

The screenshot shows the 'Interrupt configuration' window. The main area is 'Interrupt vectors' with a search bar and a table. The table has columns: Vector, Vector Ta..., Interrupt, Interrupt r..., Perip..., Priority, Status, Bank specify, and Remarks. A red box highlights the 'Priority' column, showing values like Level 3 (low), Level 0 (high), and Level 1. Another red box highlights the 'Bank specify' column, showing values like 1, 2, and None. A red box also highlights the 'Remarks' column, showing a warning message: 'One register bank cannot be specified for multiple interrupt functions with different priorities.'

Vector	Vector Ta...	Interrupt	Interrupt r...	Perip...	Priority	Status	Bank specify	Remarks
0	00004H	INTWD1	Watchdog ...	WDT	Level 3 (low)	1		
1	00006H	INTLVI	Voltage de...	LVD	Level 3 (low)	1		
2	00008H	INTP0	Pin input e...	INTC	Level 0 (high)	2		One register bank cannot be specified for multiple interrupt functions with different priorities.
3	0000AH	INTP1	Pin input e...	INTC	Level 1	Used	2	One register bank cannot be specified for multiple interrupt functions with different priorities.
4	0000CH	INTP2	Pin input e...	INTC	Level 3 (low)	Used	None	
5	0000EH	INTP3	Pin input e...	INTC	Level 3 (low)	Used	None	
6	00010H	INTP4	Pin input e...	INTC	Level 3 (low)	Used	None	
7	00012H	INTP5	Pin input e...	INTC	Level 3 (low)	Used	None	
> 8	00014H	INTST2/INT...			Level 3 (low)	None		
> 9	00016H	INTSR2/INT...			Level 3 (low)	None		
> 10	00018H	INTSRE2/IN...			Level 3 (low)	None		
11	0001AH	INTELCL	Event link i...	ELCL	Level 3 (low)	None		
12	0001CH	INTSMSE	Event outp...	SMS	Level 3 (low)	None		
> 13	0001EH	INTST0/INT			Level 3 (low)	None		

Figure 3-7 Interrupt register bank

### 3.2.11 Improvement for reserving RAM area when On-Chip debug trace function used

Smart Configurator can set the trace RAM area setting in CS+ and e<sup>2</sup> studio automatically.

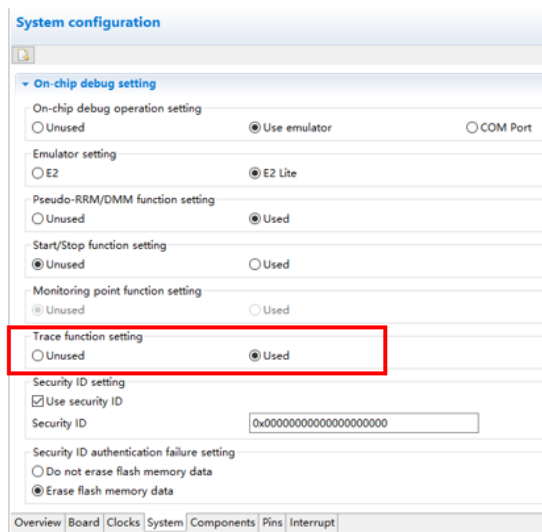


Figure 3-8 Smart Configurator trace function setting

In CS+:

The “Control allocation to trace RAM area” option is affected by Smart Configurator trace function setting:

- 1) When the Smart Configurator trace function setting is Used

The Control allocation to trace RAM area value is “Yes(Error message)(-OCDTR)”.

- 2) When the Smart Configurator trace function setting is Unused

The Control allocation to trace RAM area value is “No”.

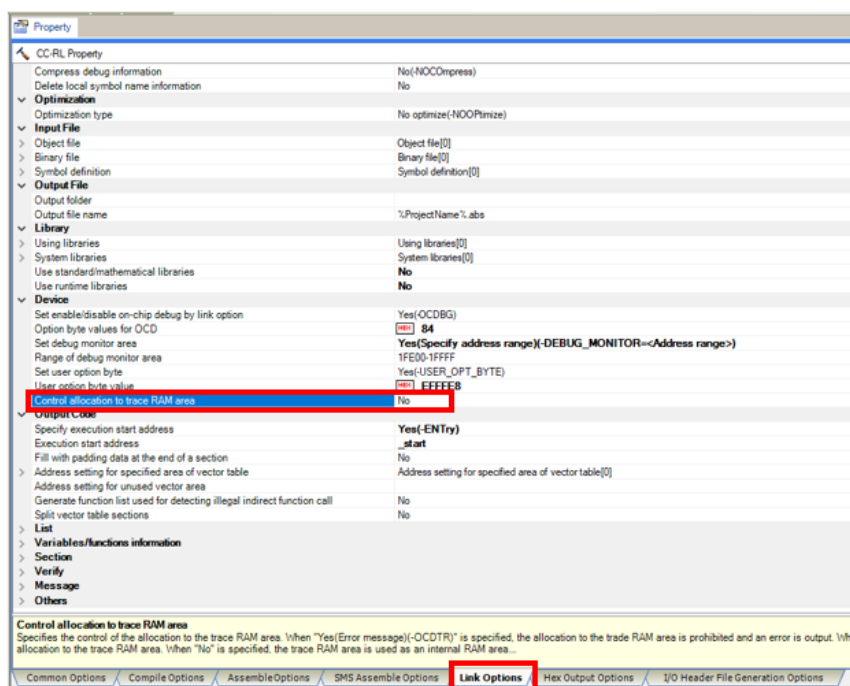


Figure 3-9 Control allocation to trace RAM area setting in CS+



In e<sup>2</sup> studio with LLVM for Renesas RL78 C/C++ Executable Project:

- 1) When the Smart Configurator trace function setting is Used  
linker\_script.ld file:

```
.....
.o cd_traceram 0xfc300Note1 (NOLOAD) : AT(0xfc300)
{
    KEEP(*(.cd_traceram))
} >RAM
.....
```

**Note1:** Start RAM address depending on the products.

r\_cg\_vector\_table.c:

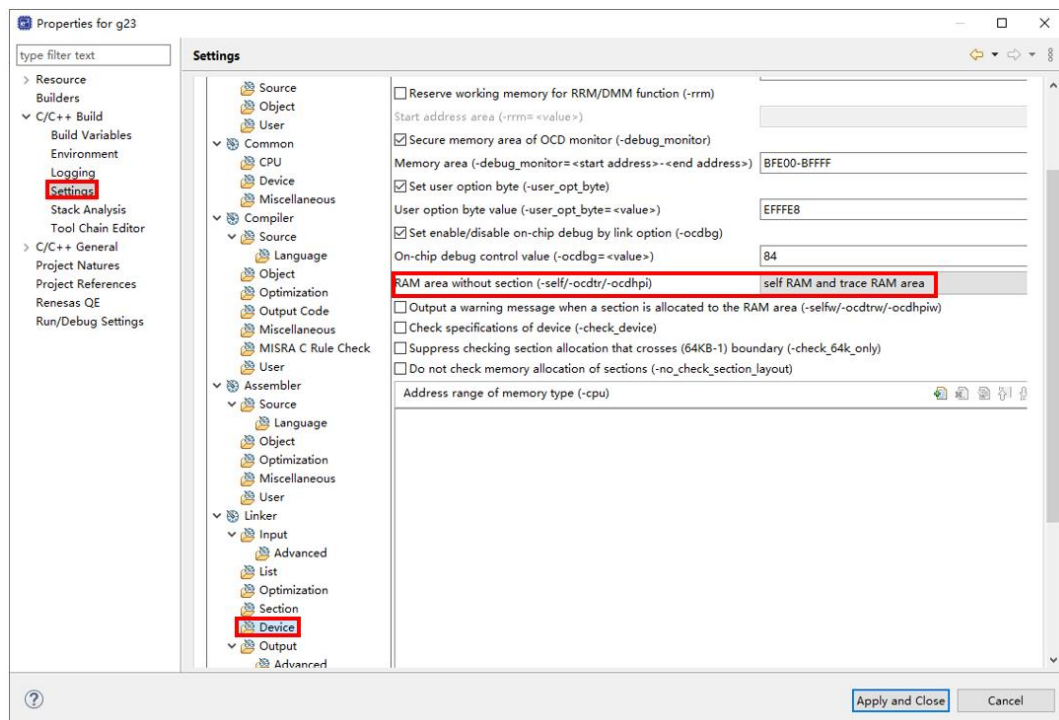
```
.....
/* Secure trace RAM area */
#define OCDTRACERAM_SECT __attribute__((section (".cd_traceram")))
uint8_t Ocd_TraceRam[1024Note1] OCDTRACERAM_SECT;
.....
```

**Note1:** RAM size depending on the products.

In e2 studio with Renesas CC-RL C/C++ Executable Project

The "The RAM area without section" option is affect by Smart Configurator trace function setting:

- 1) When the Smart Configurator trace function setting is Used  
The RAM area without section value is "Self RAM and trace RAM area".
- 2) When the Smart Configurator trace function setting is Unused  
The RAM area without section value is "None".



**Figure 3-10 RAM area without section in e2 studio**



### 3.2.12 Improvement for supporting LLVM C++ project

Extern "C" code can be generated by Smart Configurator, so that Smart Configurator generation code can be built successfully with a RL78 LLVM C++ project in e<sup>2</sup> studio.

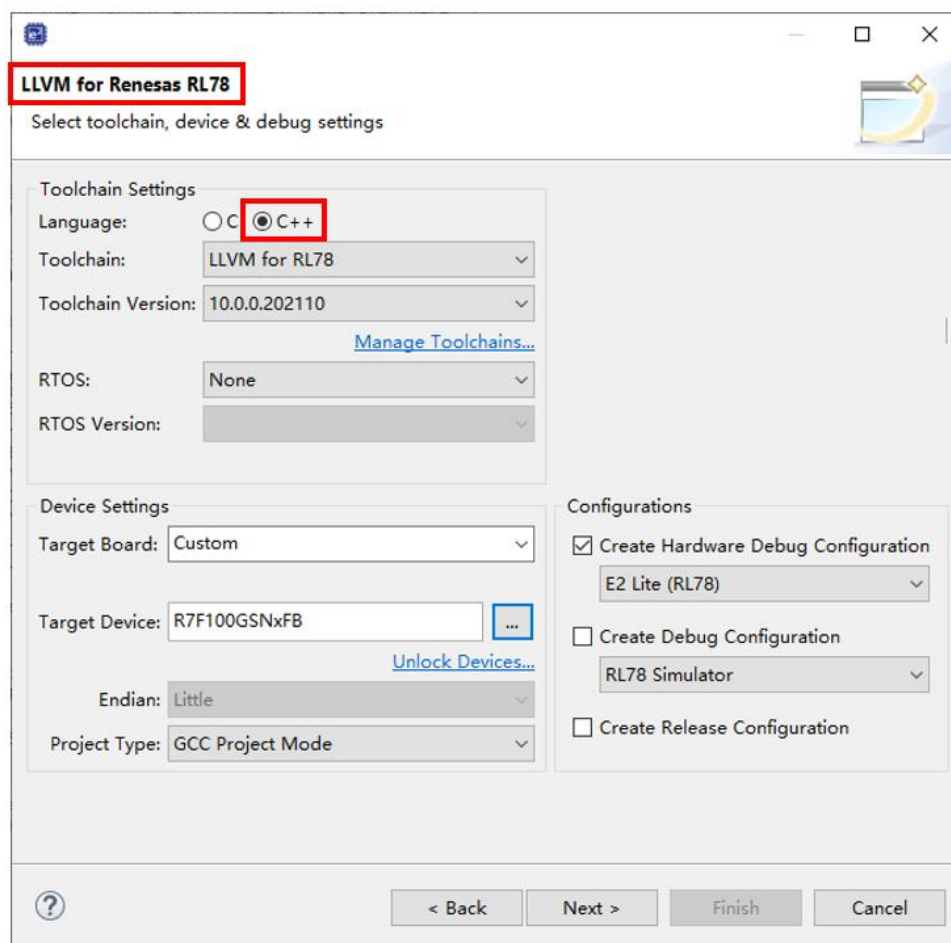


Figure 3-11 C++ project in LLVM compiler

### 3.2.13 Improvement for UARTA transfer rate range

UARTA maximum transfer rate is change from 19200 bps to 153600 bps.

### 3.2.14 Improvement for avoiding create an entry in DTC reserved RAM area of the on-chip debug trace

"NOLOAD" handling is added in linker script file to avoid creating an entry when use the reserved RAM area of the on-chip debug trace.

linker\_script.ld file:

```
.....
.dtc_vectortable 0xffd00 (NOLOAD) : AT(0xffd00)
{
    KEEP(*(.dtc_vectortable))
} >RAM
.dtc_controldata_0 0xffd40 (NOLOAD) : AT(0xffd40)
{
    KEEP(*(.dtc_controldata_0))
} >RAM
.....
```

#### 4. List of RENESAS TOOL NEWS AND TECHNICAL UPDATE

Below is a list of notifications delivered by RENESAS TOOL NEWS and TECHNICAL UPDATE.

Issue date	Document No.	Description	Applicable MCUs	Fixed version
Oct. 01, 2021	R20TS0757	1. Notes on creating LLVM for Renesas RL78 C/C++ Executable Project 2. Notes on using Port Input buffer function <a href="https://www.renesas.com/jp/zh/document/tnn/notes-e-studio-smart-configurator-plug-smart-configurator-rl78">https://www.renesas.com/jp/zh/document/tnn/notes-e-studio-smart-configurator-plug-smart-configurator-rl78</a>	RL78/G23	V1.2.0

## 5. Points for Limitation

This section describes points for limitation regarding the Smart Configurator for RL78 V1.2.0.

### 5.1 List of Limitation

Table 5-1 List of Limitation

✓ : Applicable, -: Not Applicable

No	Description	RL78/G23	Remarks
1	Note on extra help document issue	✓	
2	Note on the clock setting in UART transmission/reception function	✓	
3	Note on using communication components simultaneously	✓	
4	Note on opening smart configurator in CS+	✓	
5	Note on Smart Configurator Component menu in e <sup>2</sup> studio "Preferences" dialogue	✓	
6	Note on "Download ELCL modules" function	✓	

### 5.2 Details of Limitation

#### 5.2.1 Note on extra help document issue

For Smart Configurator, there is an extra help "Smart Browser" under "[Help] > [Help Contents]".

Please ignore it.

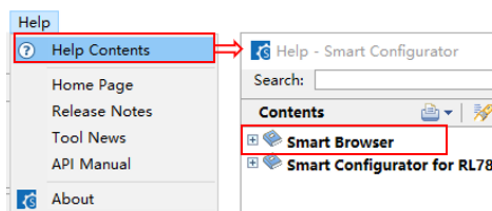


Figure 5-1 Extra help issue

#### 5.2.2 Note on the clock setting in UART transmission/reception function

When use UART transmission/reception functions, the clock setting on "Transmission" and "Reception" should be set as the same value. Otherwise, the reception side cannot receive data correctly.

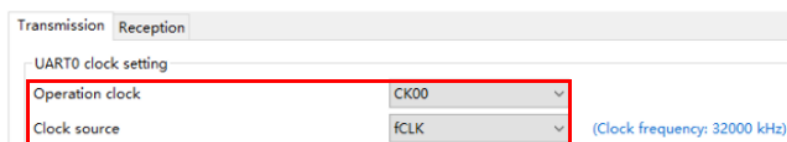


Figure 5-2 The clock setting in Transmission and Reception side of UART

### 5.2.3 Note on using communication components simultaneously

When use UARTn reception function, please note to avoid using CSIn1 and IICn1 functions of odd channels at the same time.

<80-, 100-, and 128-pin products>

Unit	Channel	Used as SPI (CSI)	Used as UART	Used as Simplified I2C
0	0	CSI00	UART0	IIC00
	1	CSI01		IIC01
	2	CSI10	UART1	IIC10
	3	CSI11		IIC11
1	0	CSI20	UART2 (supporting LIN-bus)	IIC20
	1	CSI21		IIC21
	2	CSI30	UART3	IIC30
	3	CSI31		IIC31

Figure 5-3 Multiple communication components

### 5.2.4 Note on opening smart configurator in CS+

To open smart configurator in CS+ successfully, the \*.scfg file (which is under CS+ project folder) name should be same as the project name. Otherwise, smart configurator will be opened with an empty window.

Due to this restriction, please take care in the following two operations:

- When exporting e<sup>2</sup> studio project (by e<sup>2</sup> studio "Renesas common project file" feature) to CS+, please check the \*.scfg file name should be same as the project name
- When creating a new CS+ project, please be sure there is no extra .scfg file under the target project folder. If there are more than one .scfg file under this folder, you will see the [File selection] dialogue when open smart configurator. Please ignore it by click [OK] with any selection.

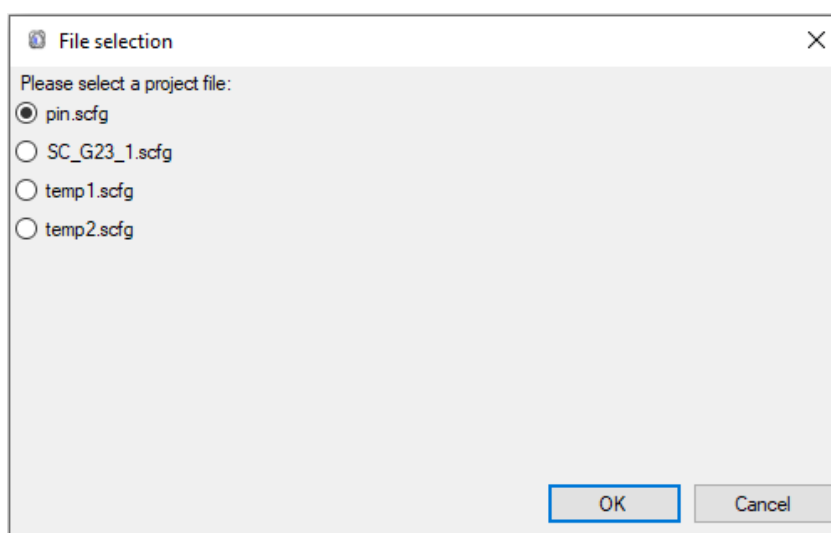


Figure 5-4 [File selection] dialogue

### 5.2.5 Note on Smart Configurator Component setting in e<sup>2</sup> studio “Preferences” dialogue

When user not selected RX family for e<sup>2</sup> studio 2022-01 installation, the Smart Configurator's Component setting menu in e<sup>2</sup> studio Preference dialog will not be shown.

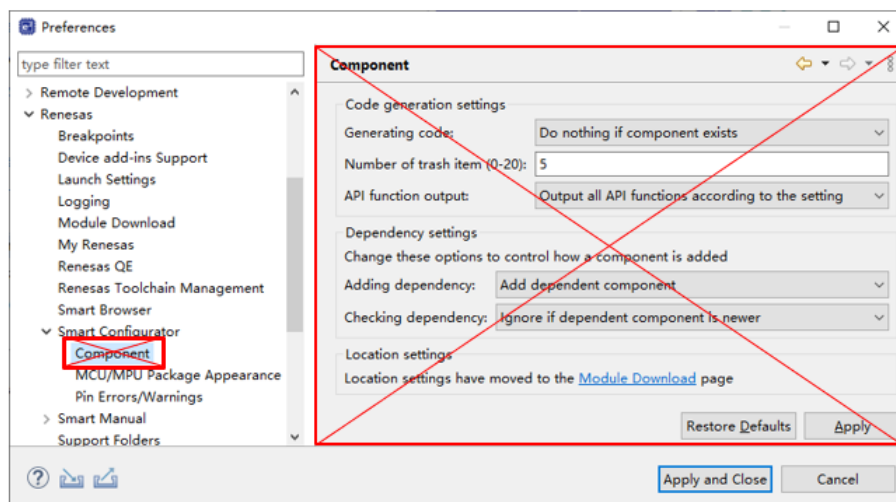


Figure 5-5 Smart Configurator Component menu in e<sup>2</sup> studio Preference dialog will not be shown

If user want to set Smart Configurator Component preference setting rather than using default preference setting, please select RX family in Setup wizard during installation, then Smart Configurator Component menu will be shown in Preferences dialogue.

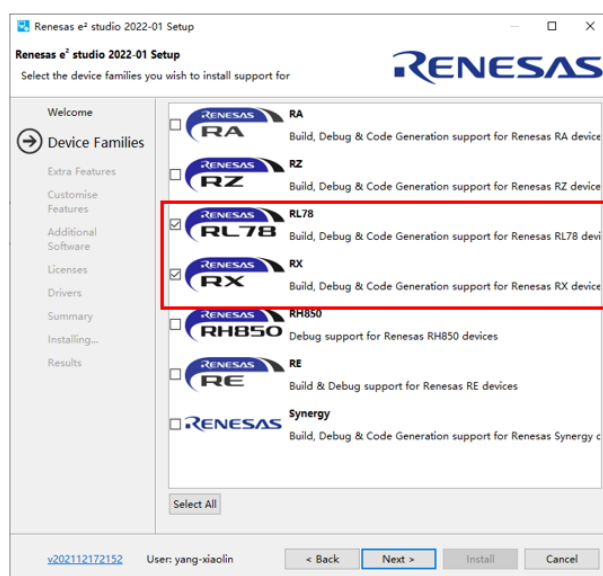


Figure 5-6 Select RX family during e<sup>2</sup> studio Setup wizard

### 5.2.6 Note on "Download ELCL modules" function

For Smart Configurator for RL78 V1.2.0, the ELCL download function is not available. When user click [Download ELCL modules](#) link in New Component dialog, the user selected ELCL modules will not be downloaded from web. Therefore, the ELCL module published on the Web is included in Smart Configurator for RL78 V1.2.0, so you can use it without having to download it.

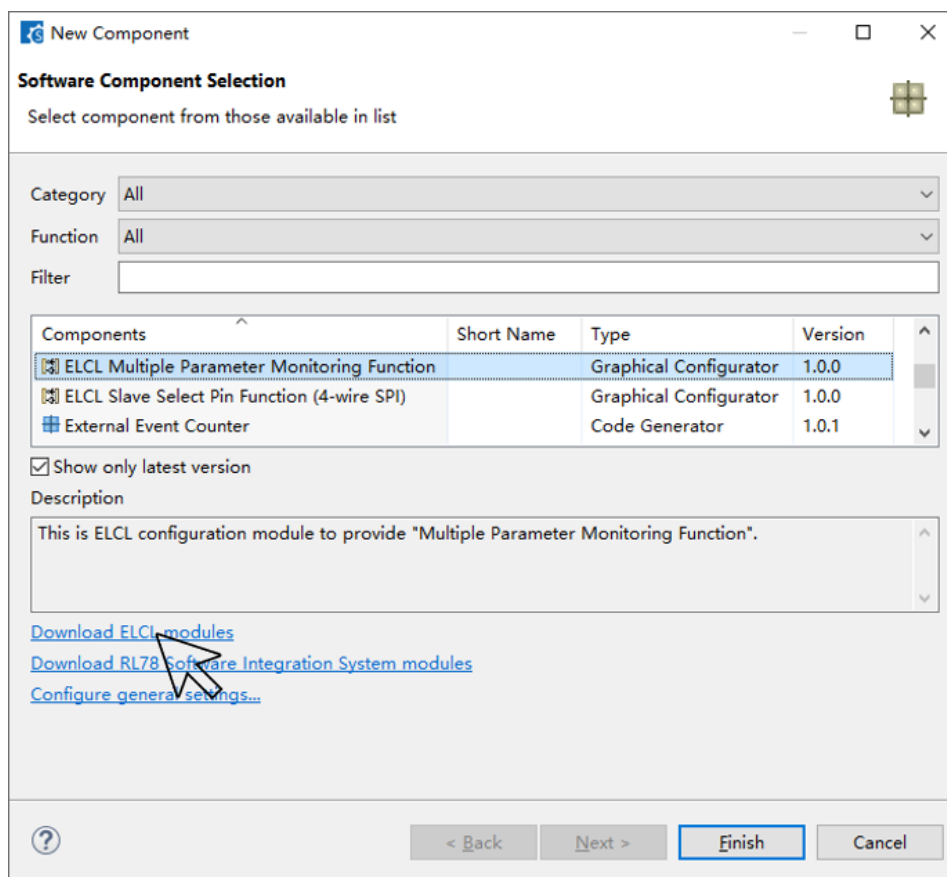


Figure 5-7 ELCL modules download link in New Component dialog

If the ELCL sample code uses an ELCL module that is not displayed in the component list, copy the ELCL module included in the sample code to the "RL78\_Modules\ELCL\_Modules" folder in the folder where Smart Configurator is installed. After copying the ELCL module, restart the Smart Configurator.

- \${Smart Configurator installation folder}\RL78\_Modules\ELCL\_Modules

## 6. Points for Caution

This section describes points for caution regarding the Smart Configurator for RL78 V1.2.0.

### 6.1 List of Caution

Table 6-1 List of Caution

✓: Applicable, -: Not Applicable

No	Description	RL78/G23	Remarks
1	About the build error message such as “section .bss virtual address range overlaps with .dtc_vectortable”.	✓	
2	About the installation of the Smart Configurator.	✓	

#### 6.1.1 About the build error message such as “section .bss virtual address range overlaps with .dtc\_vectortable”.

When user use many components and DTC component together, the generated code build might fail due to some section address overlaps.

```

CDT Build Console [LLVM_R7F100GCJxLA_case1]
ld.lld: error: section .bss virtual address range overlaps with .dtc_vectortable
>>> .bss range is [0xF9F00, 0xF9F31]
>>> .dtc_vectortable range is [0xF9F00, 0xF9F27]

ld.lld: error: section .bssf virtual address range overlaps with .dtc_controldata_0
>>> .bssf range is [0xF9F32, 0xF9F7F]
>>> .dtc_controldata_0 range is [0xF9F40, 0xF9F47]

ld.lld: error: section .bss load address range overlaps with .dtc_vectortable
>>> .bss range is [0xF9F00, 0xF9F31]
>>> .dtc_vectortable range is [0xF9F00, 0xF9F27]

ld.lld: error: section .bssf load address range overlaps with .dtc_controldata_0
>>> .bssf range is [0xF9F32, 0xF9F7F]
>>> .dtc_controldata_0 range is [0xF9F40, 0xF9F47]
clang: error: ld.lld command failed with exit code 1 (use -v to see invocation)
makefile:110: recipe for target 'LLVM_R7F100GCJxLA_case1.elf' failed
make: *** [LLVM_R7F100GCJxLA_case1.elf] Error 1
"make -j8 all" terminated with exit code 2. Build might be incomplete.

18:09:07 Build Failed. 2 errors, 0 warnings. (took 1s.846ms)

```

Figure 6-1 Build error message

Workaround:

The smart configurator cannot set “.bss” and “.bssf” section address. So user should consider to modify “.bss” and “.bssf” section address manually or change the DTC base address to avoid such section overlap error.

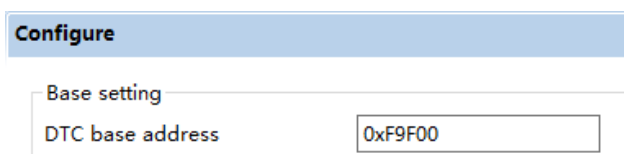


Figure 6-2 DTC base address setting

**6.1.2 About the installation of the Smart Configurator.**

Do not set more than 64 characters for the installation directory.

You might see an error message "The specified path is too long" and will not be able to install Smart Configurator.



**Revision History**

Rev.	Date	Description	
		Page	Summary
1.01	Apr 13, 2021	-	First edition issued
1.02	Jul 20, 2021	3	Update 1.1.2 Development Environments
		4	Update HW manual number in table "Table 2 1 Support Devices"
		7 - 10	Update "2.3 New support"
		9 - 13	Update "3. Changes"
		14-15	Update "4. Points for Limitation"
1.03	Jan 20, 2022	7 - 9	Update "2.3 New support"
		10 - 17	Update "3. Changes"
		18	Add 4. List of RENESAS TOOL NEWS AND TECHNICAL UPDATE
		19-23	Update "5. Points for Limitation"
		24	Add 6. Points for Caution

## General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

### 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

### 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

### 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

### 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

### 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

### 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

### 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

### 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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