

This document is an overview Renesas Low-Latency-DRAM [LLDRAM-III] Control IP

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1. Control IP Solution

1.1 Introduction

The motivation behind Renesas' LLDRAM-III control IP development is to provide high random access memory solution for network applications.

This user-friendly control IP makes it possible to develop a variety of memory subsystems like the one shown in figure 1. From statistical memory, which stores packet statistics to buffer memory for packets storage. Although LLDRAM-III is optimized for network accesses, it can also be used in non-network applications.

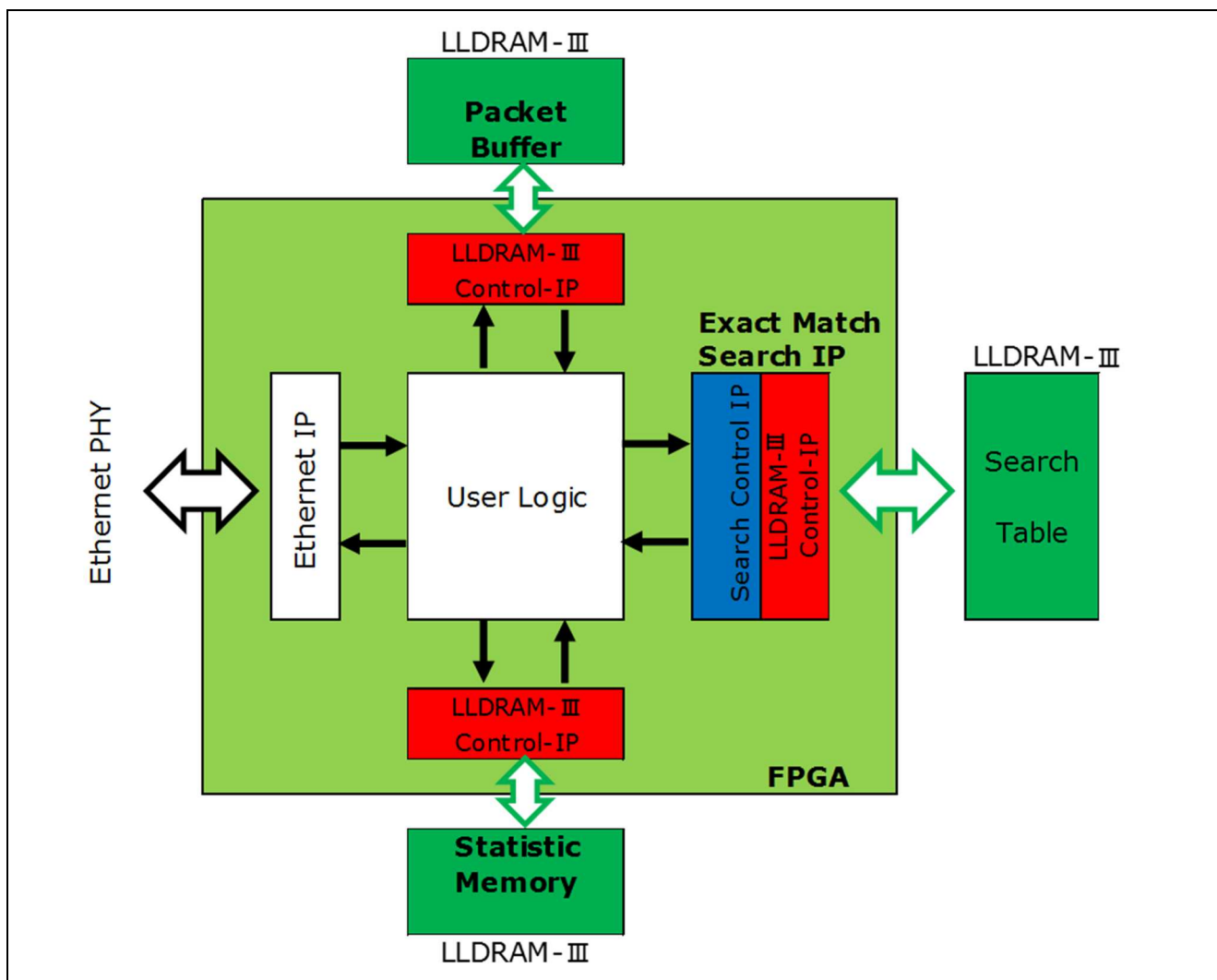


Figure 1 Example of Network Application Memory Sub-System using LLDRAM-III

1.2 What's LLDRAM-III ?

Renesas' Low-latency memory LLDRAM-III is a specialized DRAM that is capable of performing 400M accesses per second. This is four times higher access when compared to standard DDR3 SDRAM. Moreover, power consumption is kept to an extremely low 2 watts.

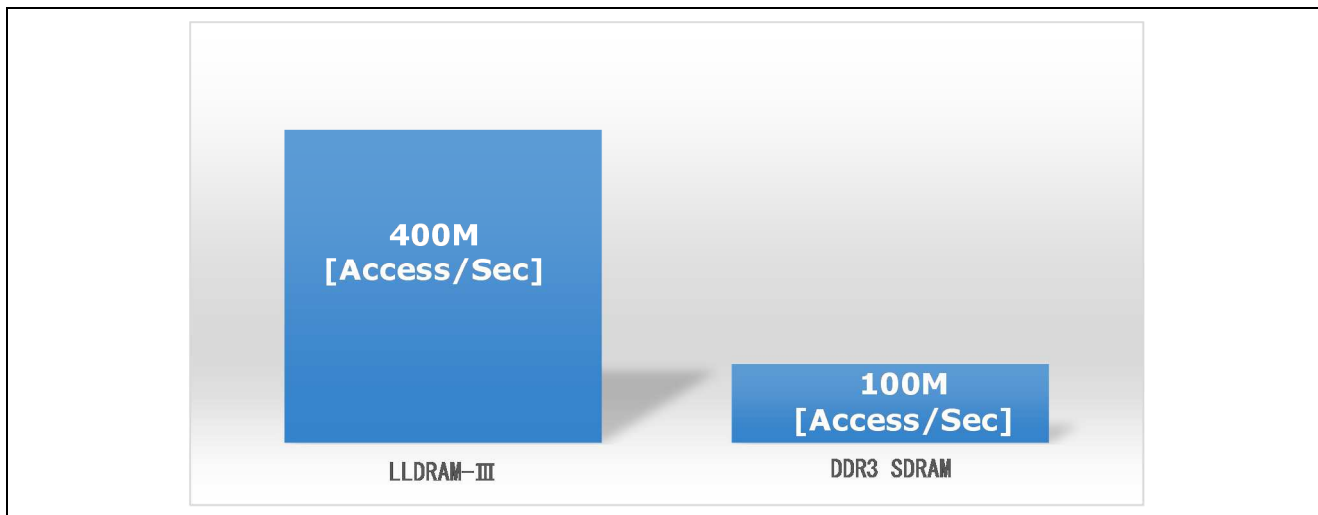


Figure 2 Access rate comparison between LLDRAM-III and DDR3 SDRAM

There are 2 types of product lineups of LLDRAM-III

- 『RMHE41A364AGBG』 Data width 36bits (x36)
- 『RMHE41A184AGBG』 Data width 18bits (x18)

Key features

- ✓ Density: 1.1Gbit
- ✓ Organization
 - 8M words x 18bits x 8 bank (x18)
 - 4M words x 36bits x 8 bank (x36)
- ✓ Operating frequency 800 MHz (MAX.) @ $t_{RC}=13.75$ ns
- ✓ Burst length: 4
- ✓ Address bus 2 cycle DDR address
- ✓ Package 180-pin FCBGA(18.5 mm x 14 mm)
- ✓ Power supply
 - V_{EXT} 2.5 V
 - V_{DD} 1.5 V
 - V_{DDQ} 1.0 V or 1.2 V

For more information, please refer to the datasheet.

1.3 Control IP Structure and Features

LLDRAM-III control IP is composed of 3 blocks – User I/F, Controller block and PHY block (See figure.3)

Key features of each block

- User I/F block
 - 200Mhz parallel I/F
- Controller block
 - Scheduler to achieve Higher Access Rate
 - Automatic Refresh by refresh counter integrated in controller block
- PHY block
 - Power on auto calibration
 - Debug I/F for calibration

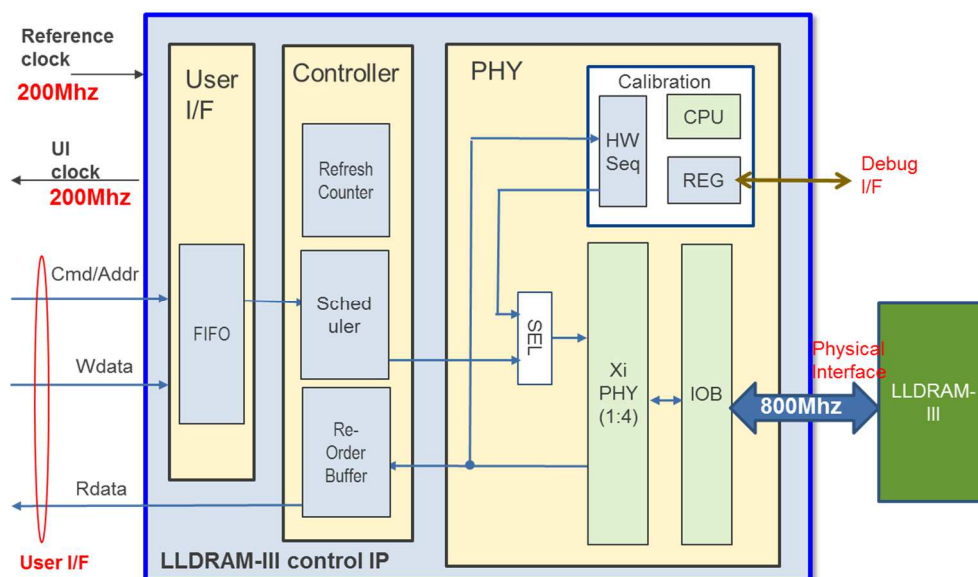


Figure 3 Structure of LLD RAM-III control IP

1.4 Performance

LLDRAM-III control IP has an intelligent scheduler which is optimized to bring out the maximum performance during random access. In order to achieve this level of performance, the scheduling function changes orders of memory access commands such as WRITE/READ issued by user and refresh commands issued by internal refresh counter to avoid access limitation such as bank conflict.

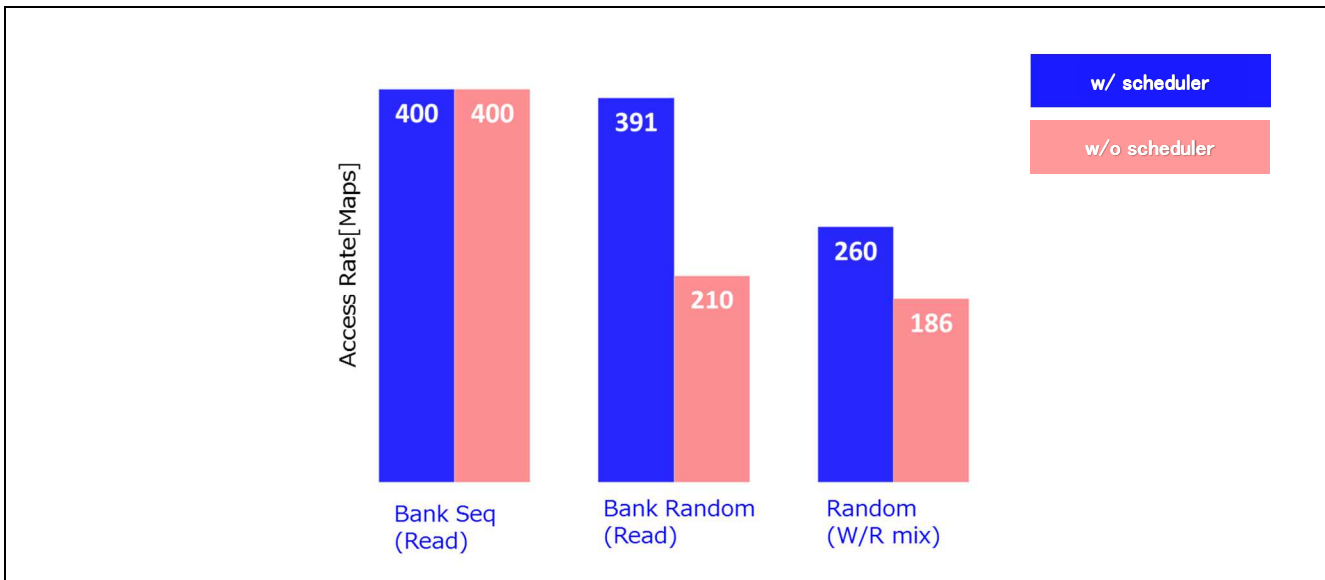


Figure 4 Comparison of LLD RAM-III access rate between w/ scheduler and w/o scheduler

Figure.4 shows the actual LLD RAM-III access rate comparison between w/ scheduler and w/o scheduler control IP implementations on FPGA.

- BANK sequential access [Bank seq(Read) at left]

This graph shows access rate with BANK sequential pattern which is the ideal access for LLD RAM-III. It is found that both w/ scheduler and w/o scheduler implementations achieve 400M access per second, which is peak performance of the memory.

- READ Only Random access [Bank Random(Read) at middle]

This graph shows access rate with READ only random access pattern which is assumed that some applications need to access to the memory with except BANK sequential pattern. In the case of w/o scheduler, the access rate fell 50% of peak access rate of the memory. In the case of w/ scheduler, Renesas' control IP can maintain peak access rate by scheduling function.

- WRITE/READ mixed Random access [Random(W/R mix) at right]

This graph shows access rate with mixed WRITE and READ random access patterns which assume that some applications need more complex accesses to the memory. As the memory needs more than 1 cycle to change the direction of data transfer (WRITE to READ or READ to WRITE), the access rates are less than the access rate during same types of commands. Though in case of w/ scheduler, it is found that LLD RAM-III performs over 200 M access per second.

Renesas' control IP contributes to reducing system development time because users do not need to build a scheduler or consider various access patterns.

1.5 Configurations

Multiple configurations of LLDRAM-III control IP is available to accommodate different user requirements.

Type	Refresh Control Needed
w/ scheduler x18/x36	No
w/o scheduler x18/x36	Yes
	No

Figure.5 Configurations of control IP

- For x36 and x18

This control IP requires 2 banks of FPGA IO BANKs in X36 mode. In X18 mode, Control IP is composed of a single FPGA IO BANK.

- Selection of scheduler

There are three types of scheduler

- ✓ w/ schedule and Refresh Control Needed:No
 - WRITE/READ commands issued by user and refresh commands from internal refresh counter of control IP are sent to LLDRAM-III with changing the order. It enables to bring out maximum access rate of LLDRAM-III.
- ✓ w/o schedule and Refresh Control Needed:Yes
 - WRITE/READ commands and REFRESH commands issued by user are sent to LLDRAM-III in order. Users need to consider how to avoid access limitation, like bank conflict, in order to bring out maximum access rate of LLDRAM-III.
- ✓ w/o schedule and Refresh Control Needed:No
 - WRITE/READ commands issued by user are sent to the memory in order. Internal refresh counter issues refresh commands on a regular basis. A slight drop in access rate will occur due to the commands issued by user will have to wait during intensive refresh.

1.6 Reliable Interoperability by Calibration

LLDRAM-III is high speed memory using 1.6Gbps high speed DDR parallel interface which requires strict timing calibration to execute stable communication between devices. LLDRAM-III enables stable high speed communications by automatically executing timing calibration sequence which includes skew adjustment between pins. By providing reliable interoperability by calibration, LLDRAM-III control IP reduces the complexity of system board design.

Key features of calibration

- Per pin skew adjustment from data pins, address pins to clock pins
- Programmable calibration sequence control using CPU on FPGA + C program
- Calibration debug tool which can execute calibration sequence step by step. See figure.6.

Sequence No	Action
SEQ0	Reset LLDRAM-III
SEQ1	Read DQ Calibration Test with Loop Back mode
SEQ2	Address and Command pins Calibration Test with Loop Back mode
SEQ3	Turn on the PLL of LLDRAM-III
SEQ4	QVLD Calibration test with Read operation
SEQ5	Set read data for Read Calibration (SEQ6 and 7) with auto DM mode
SEQ6	Read DQ Calibration Test with Read operation
SEQ7	Read DINV Calibration Test with Read operation
SEQ8	Write DQ Calibration Test with Write operation
SEQ9	Write DM Calibration Test with Write operation
SEQ10	Write DINV Calibration Test with Write operation
SEQ11	Set Mode register

Figure.6 Calibration Sequence

2. Development Support Environment

2.1 Reference Design with Verified Interoperability

Renesas development support tools consist of 1) reference board (RDK board) with voltage, current and power sensors 2) sample design including verified control IP, 3) a complete verification environment, and 4) a complete evaluation environment. With already verified interoperability between the FPGA and LLDRAM-III, these tools enable any user to get started with internal FPGA design and verification in parallel with network equipment system development. This will reduce the total development time and time-to-market.

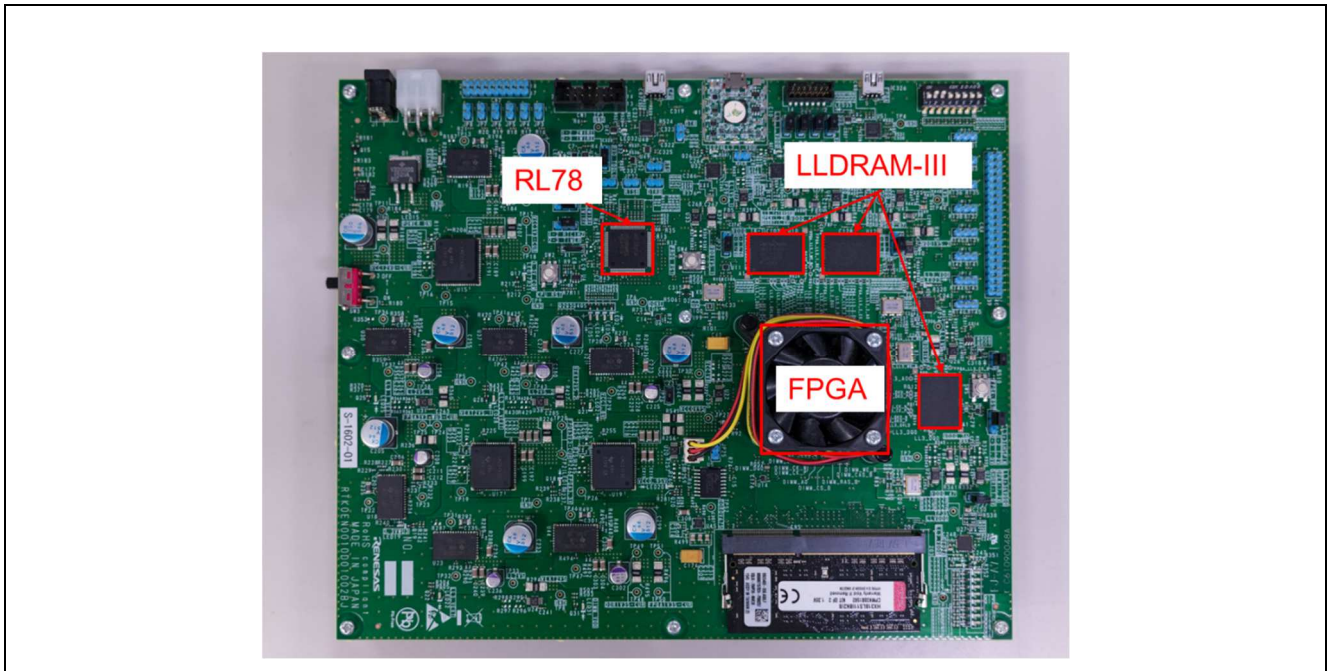


Figure.7 Reference Design Board (RDK board)

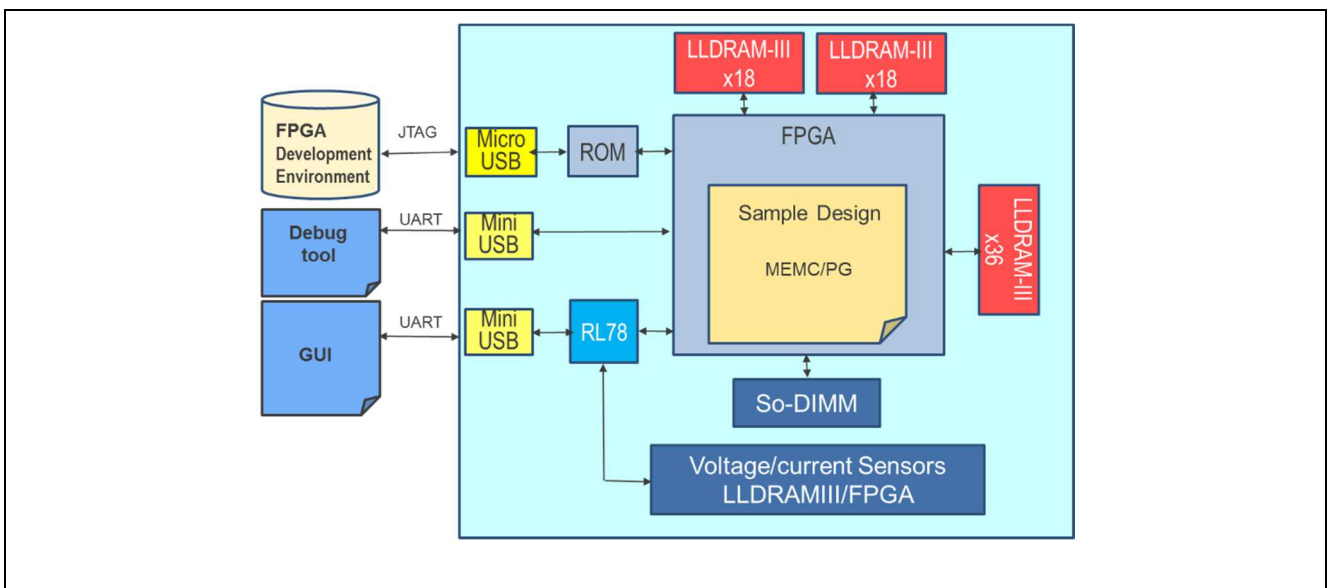


Figure.8 Structure of Reference Design Board

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Revision History

Rev.	Date	Description	
		Page	Summary
Rev. 1.00	2016.07.20		Rev. 1.00 Issued

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