Register Descriptions

The register descriptions section describes the behavior and function of the customer-programmable non-volatile-memory registers in the VersaClock 6 family of clock generators. Table 1 showcases the array of products under the VersaClock 6 family.

Table 1: VersaClock 6 Family Products

Product	Description	Package
5P49V6901	5-Output VersaClock 6	24 pins
5P49V6913	3-Output VersaClock 6	24 pins
5P49V6914	4-Output VersaClock 6	24 pins

For details of product operation, refer to the product datasheet.

VersaClock 6 Family Register Set

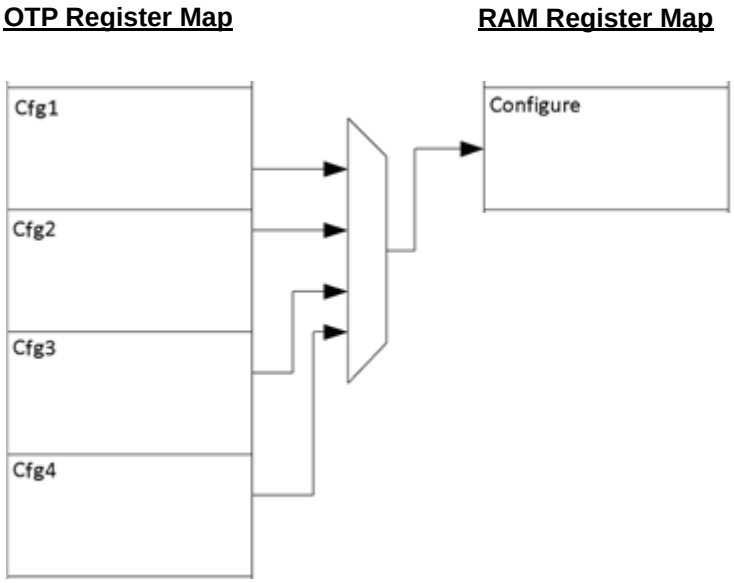
The device contains volatile (RAM) 8-bit registers and non-volatile 8-bit registers (Figure 1). The non-volatile registers are One-Time Programmable (OTP), and bit values can only be changed from 1 (unburned state) to 0.

The OTP registers include factory trim data and four user configuration tables (Figure 1, Table 3). This document does not describe the format or methods for programming factory trim data, which is programmed by the factory before shipment.

Each configuration table contains all the information to set up the device's output frequencies. When these configuration tables are programmed, the device will automatically load the RAM registers with the desired configuration on power-up. The device initializes in either I^2C mode or selection-pin mode, depending on the state of the OUT0/SELB_I2C pin on power-up, and remains in the selected mode until power is toggled (Table 2). When powered up in I²C mode, the first configuration table, CFG0, is loaded. When powered up in selection-pin mode, the SEL0 and SEL1 inputs are decoded to select one of the four configuration tables CFG0-CFG3.

The RAM registers (Table 4) include Status registers for read-back of the device's operating conditions in I^2C mode.

Figure 1. Register Maps



User Configuration Table Selection

At power up, the voltage at OUT0_SEL_I2CB pin 24 is latched by the part and used to select the state of SEL0/SCL pin 9 and SEL1/SDA pin 8 (Table 2).

If a weak pull up (10Kohms) is placed on OUT0_SEL_I2CB, the SEL0/SCL and SEL1/SDA pins will be configured as hardware select inputs, SEL0 and SEL1. Connecting SEL0 and SEL1 to VDDD and/or GND selects one of 4 configuration register sets, CFG0 through CFG3, which is then loaded into the volatile configuration registers to configure the clock synthesizer.

If a weak pull down is placed on OUT0_SEL_I2CB (or if it is left floating to use internal pulldown), the pins SEL0 and SEL1 will be configured as a I^2C interface's SDA and SCL slave bus. Configuration register set CFG0 is always loaded into the volatile configuration registers to configure the clock synthesizer. The host system can use the I^2C bus to update the volatile configuration registers to change the configuration, and to read status registers.

Table 2: Power-Up Setting of Hardware Select Pin vs I^2C Mode, and Default OTP Configuration Register

OUT0_SEL_I2CB Strap at Power Up	SEL1/SDA pin	SEL0/SCL pin	Function
10kΩ pullup	0	0	OTP bank CFG0 used to initialize RAM configuration registers
	0	1	OTP bank CFG1 used to initialize RAM configuration registers
	1	0	OTP bank CFG2 used to initialize RAM configuration registers
	1	1	OTP bank CFG3 used to initialize RAM configuration registers
10kΩ pulldown or floating	SDA	SCL	I^2C bus enabled to access registers OTP bank CFG0 used to initialize RAM configuration registers

I²C Interface and Register Access

When powered up in I²C mode (Table 2), the device allows access to internal RAM registers (Table 4). The OTP registers (Table 3) are programmed by loading the desired values into the RAM registers that shadow the target OTP registers (Table 4), and initiating the internal programming sequence for the desired register range.

Users should not write to the Trim RAM in address range 0x01 - 0x0F, or the Test RAM in address range 0x6A - 0x6F, and should only write to the OTP Control in address range 0x70 - 0x7F when programming the OTP.

The RAM in address range 0x80 - 0x8F is not used by the device and may be used for any purpose.

Table 3: OTP Register Map Summary

Register Range	OTP Register Block Name	Register Block Description
0x000	OTP Control	OTP burned status & I²C address setting
0x001 - 0x00F	Factory Use	Factory settings - do not over-program
0x010 - 0x069	CFG0	User configuration settings bank 0
0x06A - 0x0C3	CFG1	User configuration settings bank 1
0x0C4 - 0x11D	CFG2	User configuration settings bank 2
0x11E - 0x177	CFG3	User configuration settings bank 3
0x178 - 0x1AF	Factory Use	Factory settings - do not over-program

Table 4: RAM Register Map Summary

Register Range	RAM Register Block	Corresponding OTP Register Block Name	Corresponding OTP Register Block Address Range
0x00	OTP Control	OTP Control	0x000
0x01 - 0x0F	Trim	Trim	0x000 - 0x00F
0x10 - 0x1F	Configuration - Main	CFG0 CFG1 CFG2 CFG3	0x010 - 0x069 0x06A - 0x0C3 0x0C4 - 0x11D 0x11E - 0x177
0x20 - 0x2F	Configuration - CLK1		
0x30 - 0x3F	Configuration - CLK2		
0x40 - 0x4F	Configuration - CLK3		
0x50 - 0x5F	Configuration - CLK4		
0x60 - 0x69	Configuration - Outputs		
0x6A - 0x6F	Factory Use	—	—
0x70 - 0x7F	OTP Control	—	—
0x80 - 0x8F	Unused RAM	—	—
0x90 - 0x9F	Factory Use	—	—

VersaClock 6 Family Power-Up Behavior

On power-up, the following RAM register loading sequence occurs:

1. The RAM registers always initialize to a hard-wired set of default values, which are also the 'Default register values' for OTP shown in subsequent tables.
2. **If OTP_ burned bit D7=0** in the OTP Control register (Table 7), this indicates that the both the Trim OTP tables and at least one of the four OTP user configuration tables have been programmed.
   - Standard product is typically shipped in this condition, with factory trim performed, and with either standard or customer-specific configuration tables.
   - Trim RAM data will be updated from the Trim OTP registers into the appropriate trim RAM registers, overwriting the initial default values.
   - Configuration data will be read from the one of the four OTP user configuration tables into the appropriate configuration RAM registers, overwriting the initial default values. When powered up in I^2C mode, the first configuration table, CFG0, is loaded. When powered up in selection-pin mode, the SEL0 and SEL1 input pins are decoded to select one of the four configuration tables (Table 23).
   - Initialization is now complete, and the part will operate per the configuration settings.
3. **If OTP_ burned bit D7=1 & OTP_TRIM bit D6=0** in the OTP Control register (Table 7), this indicates that the Trim OTP tables are programmed and the four OTP user configuration tables are unconfigured.
   - Standard product can also be shipped in this condition, with factory trim performed, and ready for configuration table(s) to be customer-programmed.
   - Trim RAM data will be updated from the Trim OTP registers into the appropriate trim RAM registers, overwriting the initial default values.
   - Configuration RAM data remains at the hard-wired set of default values.
   - Initialization is now complete, and the part will operate per the default configuration settings.
   - When powered up in I^2C mode, the Configuration RAM registers can be written with the user's desired settings by the host system, and the clock generator operated without ever programming any of the four OTP user configuration tables. Alternatively, the host system (or a programming system) can program one of more of the four OTP user configuration tables, and also clear the OTP_ burned bit D7 in the OTP Control register (Table 7) to 0. The VersaClock 6 device will follow the behavior according to section 0 above for subsequent power ups.

OTP Programming

The steps for OTP programming are given in Table 5. The procedure is to write the desired default data to the appropriate RAM registers, and then to instruct the part to burn a desired register address range into OTP.

The RAM registers have an 8-bit register address (0x00 to 0x9F), while the user OTP registers have a 9-bit address (0x000 to 0x177). This is because there are 4 banks of configuration data in OTP. The OTP addressing therefore extends across two RAM registers (Table 5). The 9-bit user start address is set by register 0x73[7:0] + 0x74[7]. The 9-bit user end address is set by register 0x75[7:0] + 0x76[7].

Table 5: OTP Programming Procedure

Step	Procedure	Notes
0	Connect all VDD pins to a single 3.3V, with OUT0_SEL_I2CB pin left floating	Power on the part in I²C mode
1	Wait 100ms	Part power-up initialization
2	Write device RAM configuration registers 0x10 to 0x69 to the desired state	These RAM values will be programmed into OTP as new default register values
3	Write registers 0x73 to 0x78 following the procedure in Table 5	Set burn register source address range and destination register bank CFG0, 1, 2, or 3
4	Write register 0x72 = 0xF0	Reset burn bit.
5	Write register 0x72 = 0xF8	Burn the OTP range defined above
6	Wait 500ms	Wait for burn to complete. Device stops acknowledging while burning.
7	Write register 0x72 = 0xF0	Reset burn bit
8	Write register 0x72 = 0xF8	Repeat the burn
9	Wait 500ms	Wait for burn to complete. Device stops acknowledging while burning.
10	Write register 0x72 = 0xF0	Reset burn bit.
11	Done Programming	Programming complete
12	Write register 0x72 = 0xF2	Perform margin read
13	Write register 0x72 = 0xF0	Reset margin read bit
14	Read register 0x9F: If bit D1 = 0, programming was successful If bit D1 = 1, programming failed	Test if OTP programming was successful.
15	Write register 0x9F = 0x00	Reset margin read status bit
16	One configuration register bank (CFG0, 1, 2, or 3) is now burned. To burn another bank, repeat the procedure from Step 2	Burn further configuration register banks if desired
17	When all desired configuration register bank have been burned, write device OTP Control register 0x00 with OTP_burned bit D7 clear	Burn OTP Control register clearing OTP_burned bit D7. This sets the part to load configuration data from OTP on power-up
18	Exit	Done

Table 6: OTP Addressing For Programming

Register	User Start Address[8:0] Part-Select Bit 0x73	Enable Sub-block's Test Mode 0x74	User End Address[8:0] Part-Select Bit 0x75	User End Address[8:0] Part-Select Bits 0x76	Burned Register Start Address 0x77	Read Register Start Address 0x78	Registers Burned To OTP
OTP Control register	0x00	0x4E	0x00	0x61	0x00	0x00	0x00
Configuration CFG0	0x08	0x4E	0x34	0xE1	0x10	0x10	0x10 to 0x69
Configuration CFG1	0x35	0x4E	0x61	0xE1	0x10	0x10	0x10 to 0x69
Configuration CFG2	0x62	0x4E	0x8E	0xE1	0x10	0x10	0x10 to 0x69
Configuration CFG3	0x8F	0x4E	0xBB	0xE1	0x10	0x10	0x10 to 0x69

Use the steps in the following example as guidelines to program trim and configuration 0 OTP registers:

1. Write the value from register address 0x00 to 0x69 (first bank) to RAM registers

Reg Address (hex): 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10 11 12 13 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F 20 21 22 23 24 25 26 27 28 29 2A 2B 2C 2D 2E 2F 30 31 32 33 34 35 36 37 38 39 3A 3B 3C 3D 3E 3F 40 41 42 43 44 45 46 47 48 49 4A 4B 4C 4D 4E 4F 50 51 52 53 54 55 56 57 58 59 5A 5B 5C 5D 5E 5F 60 61 62 63 64 65 66 67 68 69

Configuration 0: 61 ff 00 00 00 00 00 00 ff 01 00 00 b6 b4 92 80 0c 01 00 00 03 8c 06 40 00 00 00 9f 4d 92 32 00 81 00 00 00 00 00 00 00 00 00 00 01 00 a0 00 00 0c 00 00 00 00 00 00 00 00 00 00 00 00 a0 00 00 81 00 00 00 00 00 00 00 00 00 00 00 00 00 50 00 00 81 00 55 55 54 00 00 00 00 00 00 00 03 40 00 7b 01 3b 01 7b 01 3b 01 ff fc

In above example, 61 is the value in register 0x00 that correspond to I2C address of D4.

2. Write the following values to program the OTP with config0 and trim bits (Table 6):

   Reg Address (hex): 73 74 75 76 77 78

   Configuration 0: 08 4E 34 E1 10 10

3. Start Burn with Reg 0x72 set to F8

4. Wait 500ms

5. Reset Burn Start Bit 0x72 set to F0

Please note that this example programs the register range 0x10 ~ 0x69, skipping the 0x01 ~ 0x0F Trim Range and the 0x00 OTP Control register. When programming OTP of the 5P49V6901A000 "blank" device, the 0x01 ~ 0x0F Trim Range is preprogrammed at the factory and should not be over written. However, register 0x00 still needs to be programmed, commonly with 61# for I2C device address D4. You can write OTP in two burn sessions, one for the range 0x10 ~ 0x69 and one for register 0x00 only (see Table 6, row 1). You can also write OTP in one session for the whole range 0x00 ~ 0x69 but make sure to write the same values in the trim range as what is already programmed, to avoid changing the trim range. The values that should be in the 0x01 ~ 0x0F trim range of the 5P49V6901A000 are "ff 00 00 00 00 00 00 ff 01 00 00 b6 b4 92". Set registers 0x73 ~ 0x78 to "00 4E 34 E1 00 00" for writing registers 0x00 ~ 0x69 to OTP when starting "burn".

In-System VersaClock 5 / VersaClock 6 OTP Non-Volatile Programming via I2C

1. Conditions: Ambient temperature 25°C, 3.3V. For any other conditions, contact IDT.
2. Procedure:
   a. Power-up the device
   b. Write all relevant bits to the device to program PLL, FOD and output types
   c. Provide a reference clock to the IC corresponding to the configuration.
   d. Specific bits need to be set:
      • Set VCO Monitoring in address x1D, bit[1] to “0”
      • Set “AFC Enable” bit in address x16, bit[3] to “0”
      • Set Test mode bit in register 0x11 (bit[5]) to “0”
   e. Perform VCO Calibration:
      • Toggle bit[7] in 0x1C by writing the bit to 0 then 1 and then back to 0. Final state of the bit should be 0.
      • Wait 100 ms
      • Read band in I2C register 0x99 bit[7:3]

      (read only register located in the factory programmable section of the RAM)
      • The value read from register 0x99 has to be different from 0 or 23. If this is not the case then repeat the Calibration step.
      • Write the content of the I2C register 0x99 bit[7:3] to register 0x11 bit[4:0]. Also write Test Mode bit[5] in 0x11 to "1" at this time. Remaining bits 7 and 6 in 0x11 need to be "0".
   f. Programming the OTP

When Test Mode bit[5] in 0x11 is "1", it instructs the chip to use the VCO band number programmed into 0x11 bits[4:0].

Now program the OTP by following the steps on page 5.

Default Register Values

The following tables have a column "Default Value". These are values as they show in a 5P49V6901A000, so called "blank" device that is meant for field programming. When the device is still un-programmed, it runs a default mode with OUT0 enabled and OUT1=100MHz, assuming a 25MHz crystal is connected. The default values are the register settings for this default mode.

OTP Control Register

The I^2C slave address can be changed from the default 0xD4 to 0xD0 by programming the I2C_ADDR bit D0. Note that the I^2C address change occurs on the I^2C ACK of the write transaction. An I^2C write sequence to register 0x00 that changes the value of I2C_ADDR bit D0 should be followed by an I2C STOP condition. Further I^2C transactions to the part use the new address.

In the OTP Control Register (Table 7) bits can be set for the OTP Burn and OTP Trim status, VC6 or MEMS use and I^2C address setting. Four bits are left unused.

Table 7: RAM0 0x00 – OTP Control Register

Bits	Default Value	Name	Function
D7	1	OTP_burned	It's an active low state that indicates all the OTP burn process is done. D7=1 tells the chip that OTP is not burned and it will run the default mode. D7=0 tells the chip that OTP is burned and it will transfer OTP content to the registers for operating settings.
D6	1	OTP_TRIM	It's an active low state that indicates OTP trim part is burned.
D5	1	unused	unused
D4	1	unused	unused
D3	1	unused	unused
D2	1	unused	unused
D1	1	unused	unused
D0	1	Device I2C_ADDR	If I2C_ADDR = 0 then D0 and if I2C_ADDR=1 then D4

Factory Reserved Registers for Internal Use Only

Registers from Address 0x01 to 0x0F are for Factory Use. Do not over program them.

Table 8: RAM0 – 0x01: Factory Reserved Bits - Device ID for Chip Identification

Bits	Default Value	Name	Function
D7	1	CFG0_LOCK	Lock bits will lock the config0 of the OTP after programming. 0 indicates OTP is locked and 1 indicates OTP is not locked
D6	1	CFG1_LOCK	Lock bits will lock the config1 of the OTP after programming. 0 indicates OTP is locked and 1 indicates OTP is not locked
D5	1	CFG2_LOCK	Lock bits will lock the config2 of the OTP after programming. 0 indicates OTP is locked and 1 indicates OTP is not locked
D4	1	CFG3_LOCK	Lock bits will lock the config3 of the OTP after programming. 0 indicates OTP is locked and 1 indicates OTP is not locked
D3	1	DEVICE_ID[3]	Device ID bit 3
D2	1	DEVICE_ID[2]	Device ID bit 2
D1	1	DEVICE_ID[1]	Device ID bit 1
D0	1	DEVICE_ID[0]	Device ID bit 0

Table 9: RAM0 – 0x02: Factory Reserved Bits - ADC Gain Setting

Bits	Default Value	Name	Function
D7	0	ADC gain[7:0]	ADC gain setting - Factory reserved bits
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 10: RAM0 – 0x03: Factory Reserved Bits - ADC Gain Setting

Bits	Default Value	Name	Function
D7	0	ADC gain[15:8]	ADC gain setting - Factory reserved bits
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 11: RAM0 – 0x04: Factory Reserved Bits - ADC OFFSET

Bits	Default Value	Name	Function
D7	0	ADC offset[7:0]	ADC offset - Factory reserved bits
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 12: RAM0 – 0x05: Factory reserved bits - ADC OFFSET

Bits	Default Value	Name	Function
D7	0	ADC offset[15:8]	ADC offset - Factory reserved bits
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 13: RAM0 – 0x06: Factory Reserved Bits

Bits	Default Value	Name	Function
D7	0	TEMPY[7:0]	Factory reserved bits
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 14: RAM0 – 0x07: Factory Reserved Bits

Bits	Default Value	Name	Function
D7	0	OFFSET_TBIN<7:0>	Unused Factory reserved bits
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 15: RAM0 – 0x08: Factory Reserved Bits

Bits	Default Value	Name	Function
D7	0	GAIN<7:0>	Unused Factory reserved bits
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 16: RAM0 – 0x09: Factory Reserved Bits

Bits	Default Value	Name	Function
D7	1	test[3:0]	Factory reserved bits
D6	1		
D5	1		
D4	1		
D3	1	NP[3:0]	Factory reserved bits
D2	1		
D1	1		
D0	1		

Table 17: RAM0 – 0x0A: Factory Reserved Bits

Bits	Default Value	Name	Function
D7	0	unused	Factory reserved bits
D6	0	unused	
D5	0	unused	
D4	0	unused	
D3	0	unused	
D2	0	unused	
D1	0	unused	
D0	1	unused	

Table 18: RAM0 – 0x0B: Factory Reserved Bits

Bits	Default Value	Name	Function
D7	0	bandgap_trim_up [5:0]	bandgap voltage trim, one step is 1.2mV higher than current–Factory reserved bits Please note that the Timing Commander software for VersaClock 6 suggests a C0 hex value for this register. The 5P49V6901A000 "blank" device is pre-programmed with a 00 hex value and this cannot be changed. When trying to over-write a C0 value, this OTP register will remain at 00 and the burn status bit will report "fail".
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0	unused bit	
D0	0	unused bit	

Table 19: RAM0 – 0x0C: Factory Reserved Bits

Bits	Default Value	Name	Function
D7	0	bandgap_trim_dn [5:0]	bandgap voltage trim, one step is 1.2mV higher than current
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0	unused bit	
D0	0	unused bit	

Table 20: RAM0 – 0x0D: Factory Reserved Bits

Bits	Default Value	Name	Function
D7	1	clk1_R_trim[2:0]	clk_R_trim: trim for "R" variation, 1LSB is 10%, default is in the middle level
D6	0		
D5	1		
D4	1	clk2_R_trim[2:0]	clk_R_trim: trim for "R" variation, 1LSB is 10%, default is in the middle level
D3	0		
D2	1		
D1	1	CLK4_amp[2]	clk_amp: tune the amplitude of PAD, 1LSB is 10%, default is in the middle level
D0	0	CLK4_amp[1]	clk_amp: tune the amplitude of PAD, 1LSB is 10%, default is in the middle level

Table 21: RAM0 – 0x0E: Factory Reserved Bits

Bits	Default Value	Name	Function
D7	1	clk3_R_trim[2:0]	clk_R_trim: trim for "R" variation, 1LSB is 10%, default is in the middle level
D6	0		
D5	1		
D4	1	clk4_R_trim[2:0]	clk_R_trim: trim for "R" variation, 1LSB is 10%, default is in the middle level
D3	0		
D2	1		
D1	0	CLK4_amp[2]	clk_amp: tune the amplitude of PAD, 1LSB is 10%, default is in the middle level
D0	0	CLK3_amp[1]	clk_amp: tune the amplitude of PAD, 1LSB is 10%, default is in the middle level

Table 22: RAM0 – 0x0F: Factory Reserved Bits

Bits	Default Value	Name	Function
D7	1	CLK1_amp[2]	clk_amp: tune the amplitude of PAD, 1LSB is 10%, default is in the middle level–Factory reserved bits
D6	0	CLK1_amp[1]	
D5	0	CLK1_amp[0]	
D4	1	CLK2_amp[2]	
D3	0	CLK2_amp[1]	
D2	0	CLK2_amp[0]	
D1	1	CLK3_amp[2]	
D0	0	CLK3_amp[1]	

Configuration Registers

The internal RAM configuration registers occupy 0x10 to 0x69 (Table 4).

The 4 OTP configuration banks CFG0, CFG1, CFG2, and CFG3 use the same register structure and setting behavior.

The tables with register details refer to the RAM register address for simplicity. Table 23 shows the 3-digit OTP register addresses 0x010 to 0x177 for the four banks of identical configuration registers, and the corresponding RAM register address.

Table 23: RAM Configuration Registers and OTP Configuration Registers CFG0, CFG1, CFG2, CFG3 Summary

Register Address					Function
RAM	CFG0	CFG1	CFG2	CFG3	
0x10	0x010	0x06A	0x0C4	0x11E	Primary Source and Shutdown Register
0x11	0x011	0x06B	0x0C5	0x11F	VCO Band and Factory Reserved Bits
0x12	0x012	0x06C	0x0C6	0x120	Crystal X1 Load Capacitor Register
0x13	0x013	0x06D	0x0C7	0x121	Crystal X2 Load Capacitor Register
0x14	0x014	0x06E	0x0C8	0x122	Factory Reserved Register
0x15	0x015	0x06F	0x0C9	0x123	Reference Divider Register
0x16	0x016	0x070	0x0CA	0x124	VCO Control Register and Pre-Divider
0x17	0x017	0x071	0x0CB	0x125	Feedback Integer Divider Register
0x18	0x018	0x072	0x0CC	0x126	Feedback Integer Divider Bits
0x19	0x019	0x073	0x0CD	0x127	Feedback Fractional Divider Register
0x1A	0x01A	0x074	0x0CE	0x128	Feedback Fractional Divider Register
0x1B	0x01B	0x075	0x0CF	0x129	Feedback Fractional Divider Register
0x1C	0x01C	0x076	0x0D0	0x12A	Factory Reserved Register
0x1D	0x01D	0x077	0x0D1	0x12B	Factory Reserved Register
0x1E	0x01E	0x078	0x0D2	0x12C	RC Control Register
0x1F	0x01F	0x079	0x0D3	0x12D	RC Control Register
0x20	0x020	0x07A	0x0D4	0x12E	Unused Factory Reserved Register
0x21	0x021	0x07B	0x0D5	0x12F	Output Divider 1 Control Register Settings
0x22	0x022	0x07C	0x0D6	0x130	Output Divider 1 Fractional Settings
0x23	0x023	0x07D	0x0D7	0x131	Output Divider 1 Fractional Settings
0x24	0x024	0x07E	0x0D8	0x132	Output Divider 1 Fractional Settings
0x25	0x025	0x07F	0x0D9	0x133	Output Divider1 Fractional Settings
0x26	0x026	0x080	0x0DA	0x134	Output Divider 1 Step Spread Configuration Register
0x27	0x027	0x081	0x0DB	0x135	Output Divider 1 Step Spread Configuration Register
0x28	0x028	0x082	0x0DC	0x136	Output Divider 1 Step Spread Configuration Register
0x29	0x029	0x083	0x0DD	0x137	Output Divider 1 Spread Modulation Rate Configuration Register
0x2A	0x02A	0x084	0x0DE	0x138	Output Divider 1 Spread Modulation Rate Configuration Register
0x2B	0x02B	0x085	0x0DF	0x139	Output Divider 1 Skew Integer Part
0x2C	0x02C	0x086	0x0E0	0x13A	Output Divider 1 Skew Integer Part
0x2D	0x02D	0x087	0x0E1	0x13B	Output Divider 1 Integer Part
0x2E	0x02E	0x088	0x0E2	0x13C	Output Divider 1 Integer Part
0x2F	0x02F	0x089	0x0E3	0x13D	Output Divider 1 Skew Fractional part
0x30	0x030	0x08A	0x0E4	0x13E	Unused Factory Reserved Register
0x31	0x031	0x08B	0x0E5	0x13F	Output Divider 2 Control Register Settings
0x32	0x032	0x08C	0x0E6	0x140	Output Divider 2 Fractional Settings
0x33	0x033	0x08D	0x0E7	0x141	Output Divider 2 Fractional Settings
0x34	0x034	0x08E	0x0E8	0x142	Output Divider 2 Fractional Settings

Register Address					Function
RAM	CFG0	CFG1	CFG2	CFG3	
0x35	0x035	0x08F	0x0E9	0x143	Output Divider2 Fractional Settings
0x36	0x036	0x090	0x0EA	0x144	Output Divider 2 Step Spread Configuration Register
0x37	0x037	0x091	0x0EB	0x145	Output Divider 2 Step Spread Configuration Register
0x38	0x038	0x092	0x0EC	0x146	Output Divider 2 Step Spread Configuration Register
0x39	0x039	0x093	0x0ED	0x147	Output Divider 2 Spread Modulation Rate Configuration Register
0x3A	0x03A	0x094	0x0EE	0x148	Output Divider 2 Spread Modulation Rate Configuration Register
0x3B	0x03B	0x095	0x0EF	0x149	Output Divider 2 Skew Integer Part
0x3C	0x03C	0x096	0x0F0	0x14A	Output Divider 2 Skew Integer Part
0x3D	0x03D	0x097	0x0F1	0x14B	Output Divider 2 Integer Part
0x3E	0x03E	0x098	0x0F2	0x14C	Output Divider 2 Integer Part
0x3F	0x03F	0x099	0x0F3	0x14D	Output Divider 2 Skew Fractional part
0x40	0x040	0x09A	0x0F4	0x14E	Unused Factory Reserved Register
0x41	0x041	0x09B	0x0F5	0x14F	Output Divider 3 Control Register Settings
0x42	0x042	0x09C	0x0F6	0x150	Output Divider 3 Fractional Settings
0x43	0x043	0x09D	0x0F7	0x151	Output Divider 3 Fractional Settings
0x44	0x044	0x09E	0x0F8	0x152	Output Divider 3 Fractional Settings
0x45	0x045	0x09F	0x0F9	0x153	Output Divider 3 Fractional Settings
0x46	0x046	0x0A0	0x0FA	0x154	Output Divider 3 Step Spread Configuration Register
0x47	0x047	0x0A1	0x0FB	0x155	Output Divider 3 Step Spread Configuration Register
0x48	0x048	0x0A2	0x0FC	0x156	Output Divider 3 Step Spread Configuration Register
0x49	0x049	0x0A3	0x0FD	0x157	Output Divider 3 Spread Modulation Rate Configuration Register
0x4A	0x04A	0x0A4	0x0FE	0x158	Output Divider 3 Spread Modulation Rate Configuration Register
0x4B	0x04B	0x0A5	0x0FF	0x159	Output Divider 3 Skew Integer Part
0x4C	0x04C	0x0A6	0x100	0x15A	Output Divider 3 Skew Integer Part
0x4D	0x04D	0x0A7	0x101	0x15B	Output Divider 3 Integer Part
0x4E	0x04E	0x0A8	0x102	0x15C	Output Divider 3 Integer Part
0x4F	0x04F	0x0A9	0x103	0x15D	Output Divider 3 Skew Fractional part
0x50	0x050	0x0AA	0x104	0x15E	Unused Factory Reserved Register
0x51	0x051	0x0AB	0x105	0x15F	Output Divider 4 Control Register Settings
0x52	0x052	0x0AC	0x106	0x160	Output Divider 4 Fractional Settings
0x53	0x053	0x0AD	0x107	0x161	Output Divider 4 Fractional Settings
0x54	0x054	0x0AE	0x108	0x162	Output Divider 4 Fractional Settings
0x55	0x055	0x0AF	0x109	0x163	Output Divider 4 Fractional Settings
0x56	0x056	0x0B0	0x10A	0x164	Output Divider 4 Step Spread Configuration Register
0x57	0x057	0x0B1	0x10B	0x165	Output Divider 4 Step Spread Configuration Register
0x58	0x058	0x0B2	0x10C	0x166	Output Divider 4 Step Spread Configuration Register
0x59	0x059	0x0B3	0x10D	0x167	Output Divider 4 Spread Modulation Rate Configuration Register
0x5A	0x05A	0x0B4	0x10E	0x168	Output Divider 4 Spread Modulation Rate Configuration Register
0x5B	0x05B	0x0B5	0x10F	0x169	Output Divider 4 Skew Integer Part
0x5C	0x05C	0x0B6	0x110	0x16A	Output Divider 4 Skew Integer Part
0x5D	0x05D	0x0B7	0x111	0x16B	Output Divider 4 Integer Part
0x5E	0x05E	0x0B8	0x112	0x16C	Output Divider 4 Integer Part
0x5F	0x05F	0x0B9	0x113	0x16D	Output Divider 4 Skew Fractional Part
0x60	0x060	0x0BA	0x114	0x16E	Clock 1 Output Configuration
0x61	0x061	0x0BB	0x115	0x16F	Clock 2 Output Configuration

Register Address					Function
RAM	CFG0	CFG1	CFG2	CFG3	
0x62	0x062	0x0BC	0x116	0x170	Clock 1 Output Configuration
0x63	0x063	0x0BD	0x117	0x171	Clock 2 Output Configuration
0x64	0x064	0x0BE	0x118	0x172	Clock 1 Output Configuration
0x65	0x065	0x0BF	0x119	0x173	Clock 2 Output Configuration
0x66	0x066	0x0C0	0x11A	0x174	Clock 1 Output Configuration
0x67	0x067	0x0C1	0x11B	0x175	Clock 2 Output Configuration
0x68	0x068	0x0C2	0x11C	0x176	CLK_OE/Shutdown Function
0x69	0x069	0x0C3	0x11D	0x177	CLK_OS/Shutdown Function

Configuration Register Detail and Functionality Description

Shutdown Function

The shutdown logic offers flexible configuration of shutdown signaling and clock output enable control. The shutdown logic is summarized in Table 24.

When SP bit D1=0 in the Shutdown register 0x00 (Table 25), the SD/OE input is active low. When SP bit D1=1, SD/OE is active high.

SH bit D0 in the Shutdown register 0x00 (Table 25) configures the SD/OE input's action as either output enable (OE) for the clock outputs (leaving the PLL running), or full part shutdown. SH bit D1=0 for OE function, or 1 for shutdown function.

In shutdown, the part is shut down, differential outputs are driven High/low, and the single-ended LVCMOS outputs are driven low. In output-disable, individual outputs can be selected to be either Hi-Z or driven high/low, depending on the configuration of the CLKx_OS and CLKx_OE bits shown in Table 24.

Table 24: Shutdown Truth Table

SH bit	SP bit	OSn bit	OEn bit	SD/OE	OUTn
0	x	1	0	x	Output Active
x	0	1	1	0	Output Active
0	1	1	1	1	Output Active
1	x	1	0	0	Output Active
0	0	1	1	1	Output Driven High Low
x	1	1	1	0	Output Driven High Low
1	x	x	x	1	Global Shutdown
x	x	0	x	x	That Output Only depending on input bit

Note: If the SH and SD/OE bits are both high (1) and the OSn bit and OEn bits can be don't care for the output to be Global Shutdown. If the SH and SD/OE bits are don't care and OSn bit being 0, the output would also be 0 for CLK_OS and output of CLK_OE depends on whatever the OEn bit is.

The shutdown logic diagram is shown in Figure 2, where:

SD/OE is an input pin on the package.

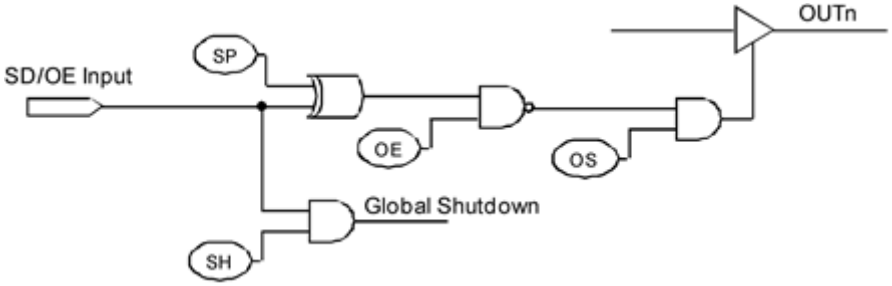
SP is bit D1 in the Shutdown register 0x10 and sets SD/OE input to be either active high or active low.

SH is bit D0 in the Shutdown register 0x10 and can force software shutdown.

OE is the appropriate output enable CLK0_OE, CLK1_OE, CLK2_OE, CLK3_OE, or CLK4_OE.

OS is the appropriate output select CLK0_OS, CLK1_OS, CLK2_OS, CLK3_OS, or CLK4_OS.

Figure 2. Shutdown Logic



To Enter Shutdown Mode through I^2C

1. Tristate the outputs by writing b'001ss000' to registers 0x60, 0x62, 0x64, and 0x66 where ss = 00, 10, or 11 for output clock supply voltages 1.8V, 2.5V, or 3.3V.
2. Program all outputs to single-ended CMOS by writing 0x00 to registers 0x68.
3. Enable shutdown functionality by either writing 0x83 or 0x43 to register 0x10, for crystal clock source or external clock respectively.
4. Disable all output dividers by writing 0x80 to registers 0x21, 0x31, 0x41, and 0x51.
5. Take the SD/OE input pin 7 high.

Table 25: RAM1 – 0x10: Primary Source and Shutdown Register

Bits	Default Value	Name	Function
D7	1	en_xtal	XTAL(Crystal Frequency) is disabled in 0 and enabled if 1 - Enable Crystal Input
D6	0	en_clkin	clkin which is clock input is disabled if 0 and enabled if 1
D5	1	cnf_vreg_sync<1:0>	cnf_vreg_sync<1:0>: 00=1.2V, 10=1.3V, 11=1.3V
D4	0		
D3	0	en_double XTAL freq_0	Enables frequency doubler when set to 1
D2	0	en_refmode	0 indicates FOD1 is operating normally and 1 indicates reference input to FOD1 - Factory reserved bit
D1	0	SP	SD/OE input pin is active low if this bit is 0 and active high if this bit is 1. (If D0 = 0 then D1 reverses SD/OE pin polarity, affecting OE bits in output polarity. If D0=1, SD/OE pin = 1 causes global shutdown)
D0	0	en_global shutdown	D1 reverses SD/OE pin polarity, affecting OE bits in output buffers and SD/OE input pin is ShutDown(SD) if this bit is 1

Table 26: RAM6 – 0x68: CLK_OE/Shutdown Function

Bits	Default Value	Name	Function
D7	1	CLK0_OE	CLK_OE checks the shut down truth table - See Shutdown Function and Shutdown Truth Table - Output Enable (Active High)
D6	1	CLK1_OE	CLK_OE checks the shut down truth table - See Shutdown Function and Shutdown Truth Table - Output Enable (Active High)
D5	1	CLK2_OE	CLK_OE checks the shut down truth table - See Shutdown Function and Shutdown Truth Table - Output Enable (Active High)
D4	1	CLK3_OE	CLK_OE checks the shut down truth table - See Shutdown Function and Shutdown Truth Table - Output Enable (Active High)
D3	1	CLK4_OE	CLK_OE checks the shut down truth table - See Shutdown Function and Shutdown Truth Table - Output Enable (Active High)
D2	1	clk0_slewrate[1]	Depends on Slew Rate (Depends on Shutdown function/truth table) - Set Slew Rate
D1	1	clk0_pwr_sel[1:0]	Clock Output Drive Voltage is indicated by these bits. D1 D0 = 0x indicates 1.8v D1 D0 = 10 indicates 2.5v D1 D0 = 11 indicates 3.3v - Set Output Amplitude
D0	1		

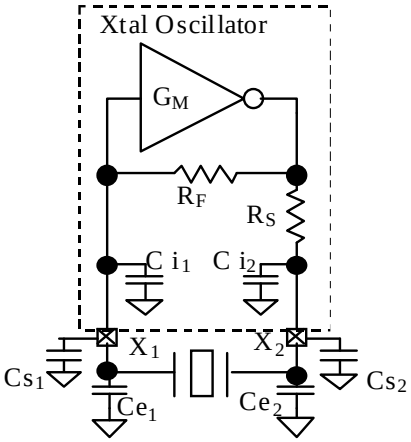
Table 27: RAM6 – 0x69: CLK_OS/Shutdown Function

Bits	Default Value	Name	Function
D7	1	CLK0_OS	CLK_OS checks the shut down truth table - See Shutdown Function and Shutdown Truth Table - Output Suspend (Active Low)
D6	1	CLK1_OS	CLK_OS checks the shut down truth table - See Shutdown Function and Shutdown Truth Table - Output Suspend (Active Low)
D5	1	CLK2_OS	CLK_OS checks the shut down truth table - See Shutdown Function and Shutdown Truth Table - Output Suspend (Active Low)
D4	1	CLK3_OS	CLK_OS checks the shut down truth table - See Shutdown Function and Shutdown Truth Table - Output Suspend (Active Low)
D3	1	CLK4_OS	CLK_OS checks the shut down truth table - See Shutdown Function and Shutdown Truth Table - Output Suspend (Active Low)
D2	1	clk0_slewrate[0]	Depends on Slew Rate (Depends on Shutdown function/truth table) - Set Slew Rate for clk0
D1	0	otp_pwr_sel[1:0]	Set Output Amplitude for OTP voltage: D1 D0=00 indicates 3.3v, D1 D0=01 indicates 1.8v, D1 D0=10 indicate 2.5v D1 D0=11 indicate no value
D0	0		

Crystal Load Capacitor Registers

Registers 0x12 and 0x13 are Crystal X1 and X2 Load capacitor registers respectively that are used to add load capacitance to X1 and X2 respectively. In X1 Switch mode is provided with different mode selection options and in X2 polarity selection of clock can be made whose values are given in the table.

Figure 3. Crystal Oscillator



Short Example of Programming Crystal

Ci1 and Ci2 are on-chip capacitors that are programmable.

Cs is stray capacitance in the PCB and Ce is external capacitors for frequency fine tuning or for achieving load capacitance values beyond the range of the on-chip programmability.

All these capacitors combined make the load capacitance for the crystal.

Capacitance on pin X1: Cx1 = Ci1+Cs1+Ce1
Capacitance on pin X2: Cx2 = Ci2+Cs2+Ce2
Total Crystal Load Capacitance CL = Cx1×Cx2 / (Cx1+Cx2)

Example: For a Xtal CL of 8pF, the registers need to be programmed with X1=X2=6.92 pF to get a total CL= (6.92pF+7.5pF+1.5pF)/2=7.9pF which is the closest value to 8pF.

Here, Cstray = 1.5pF; Package stray = 7.5pF

The binary settings corresponding to this value will be: X1=X2="10000"

Table 28: RAM1 – 0x12: Crystal X1 Load Capacitor Register

Bits	Default Value	Name	Function
D7	0	xtal_load_cap_x1[5:0]	Add 6.92pF load capacitance to X1
D6	0		Add 3.46pF load capacitance to X1
D5	0		Add 1.73pF load capacitance to X1
D4	0		Add 0.86pF load capacitance to X1
D3	0		Add 0.43pF load capacitance to X1
D2	0		Add 0.43pF load capacitance to X1
D1	0	otp_pwr_sel[1:0]	It's a switch mode that indicates D1 D0 = 00: manual, D1 D0 = 10: auto and non-revertive, D1 D0 = 11: auto and revertive
D0	1		

Table 29: RAM1 – 0x13: Factory Reserved Bits

Bits	Default Value	Name	Function
D7	0	xtal_load_cap_x2[5:0]	Add 6.92pF load capacitance to X2
D6	0		Add 3.46pF load capacitance to X2
D5	0		Add 1.73pF load capacitance to X2
D4	0		Add 0.86pF load capacitance to X2
D3	0		Add 0.43pF load capacitance to X2
D2	0		Add 0.43pF load capacitance to X2
D1	0	PRIMSRC	The PRIMSRC(primary source) bit inverts CLKSEL pin 6's reference clock selection and is normally set to 0 i.e., If PRIMSRC and clkok1024 is 00 or 10 respectively, then reference clock selected is XIN/REF and If it's 01 or 11 respectively, then CLKIN/CLKINB. PRIMSRC: 0 for clksel to be active high and 1 to be active low. Clkok1024 is factory reserved bit.
D0	0	clkok1024	

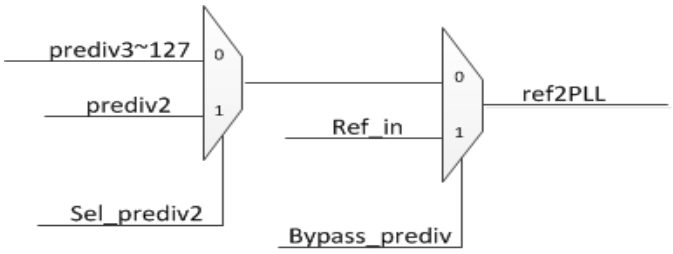
Table 30: NRAM1 – 0x14: Factory Reserved Bits

Bits	Default Value	Name	Function
D7	0	cnf_vreg_xtal<1:0>	cnf_vreg_xtal<1:0>: 00=1.2V, 10=1.25V
D6	0		
D5	0		
D4	0		
D3	0	xtal_I_sel[3:0]	Unused Factory reserved bit
D2	0		
D1	0		
D0	0		

PLL Pre-Divider Options

The reference presented to the fractional PLL can be either directly connected, divided by two or divided by the any value from the range of three to 127 as set in the register Ref_Div[6:0]. The phase detector of the PLL has a maximum frequency of 50 MHz, therefore the default is to bypass the pre-divider by setting Bypss_prediv = 1 (Table 32). For the functionality of Sel_prediv2 and bypss_prediv bits, see Figure 4. Table 31 and Table 32 explains the bit selections.

Figure 4. PLL Pre-Divider Options



If pre-divider is selected by selecting bypass_ prediv =0 (Table 32) then user can select divider by 2 or divider values from 3 to 127.

Table 31: RAM1 – 0x15: Reference Divider Register

Bits	Default Value	Name	Function
D7	0	Sel_prediv2	Select the divider by 2 function; Divide by 2 if set to 1. And if bypass is set to 0. If divide bit set 0 and bypass bit set to 0 then reference divider bits (D6 to D0) will take effect.
D6	0	Ref_div[6:0]	Reference Divider divides by 64
D5	0		Reference Divider divides by32
D4	0		Reference Divider divides by 16
D3	0		Reference Divider divides by 8
D2	0		Reference Divider divides by 4
D1	0		Reference Divider divides by 2
D0	0		Reference Divider divides by 1

Table 32: RAM1 – 0x16: VCO Control Register and Pre-Divider

Bits	Default Value	Name	Function
D7	1	Bypass_prediv	0 indicates reference clock from pre-divider is present and 1 indicates reference clock from pre-divider is not present
D6	0	dither_gain_cfg[2]	dither gain settings: D6 D5 D4 = 000 indicates no dither, D6 D5 D4 = 001 indicates 1LSB, D6 D5 D4 = 010 indicates 2LSB, D6 D5 D4 = 011 indicates 4LSB, D6 D5 D4 = 100 indicates 8LSB, D6 D5 D4 = 101 indicates 16LSB, D6 D5 D4 = 110 indicates 32LSB, D6 D5 D4 = 111 indicates 64LSB - factory reserved bits.
D5	0	dither_gain_cfg[1]	
D4	0	dither_gain_cfg[0]	
D3	1	afc_en	Open loop vco control is enabled if 1 and disabled if 0 - factory reserved bit.
D2	1	cnf_afc[2:0]	Open loop vco control voltage bits- factory reserved bits.
D1	0		
D0	0		

Table 33: RAM1 – 0x11: VCO Band and Factory Reserved Bits

Bits	Default Value	Name	Function
D7	1	cnf_vreg_xtal<1:0>	cnf_vreg_xtal<1:0>: 00=1.2V, 10=1.3V, 11=1.33V
D6	1		
D5	0	test_mode_vco_band	Select test_mode_vco_band from I2C. Enable the test mode
D4	0	vco_band[4:0]	Select vco_band from I2C. Force the VCO band value
D3	1		
D2	1		
D1	0		
D0	0		

PLL Fractional Feedback Divider and Loop Filter

The PLL feedback divider M is composed of a 12 bit integer portion, FB_intdiv[11:0] and a 24 bit fractional portion, FB_frcdiv[23:0].

$$M = INT(M) + FRAC(M) = \frac{F_{VCO}}{F_{REF2PLL}} \quad (1)$$

Convert FRAC(M) to hex with Eq.2 where ROUND2INT means to round to the nearest integer. The round-off error of M in ppm is the VCO frequency error in ppm.

$$FB\_frcdiv[23:0] = DEC2HEX(ROUND2INT[2^{24} * FRAC(M)]) \quad (2)$$

The recommended frequency range for the VCO is 2500MHz to 3000MHz. Please select the feedback and output counter values such that the VCO operates inside this range.

Example: If the Feedback divider value is given as 112.4:

Then INT(M) =112 and FRAC(M)=0.4 that gives:
2^{24} × FRAC(M) = 2^{24} × 0.4 = 6710886.4
ROUND2INT(6710886.4) = 6710886
FB_frcdiv[23:0] = DEC2HEX(6710886) = 666666

Table 34: RAM1 – 0x17: Feedback Integer Divider Register

Bits	Default Value	Name	Function
D7	0	FB_intdiv[11:4]	The Feedback Integer Divider Register has 12 bits spread on 2 registers 0x17 and 0x18.
D6	0		
D5	0		
D4	0		
D3	0		
D2	1		
D1	1		
D0	1		

Table 35: RAM1 – 0x18: Feedback Integer Divider Bits

Bits	Default Value	Name	Function
D7	0	FB_intdiv[3:0]	The Feedback Integer Divider Register has 12 bits spread on 2 registers 0x17 and 0x18.
D6	0		
D5	0		
D4	0		
D3	0	sdm_order_cfg[1]	Factory Reserved bits. These both bits are for Sigma Delta Modulator setting. D3 D2 = 00 : sdm bypass, D3 D2 = 01: selects 1st order, D3 D2 = 10: selects 2nd order, D3 D2 = 11: selects 3rd order.
D2	0	sdm_order_cfg[0]	
D1	0	i2c_ssce	Factory reserved bit.
D0	0	unused	Unused Factory Reserved Bit

Table 36: RAM1 – 0x19: Feedback Fractional Divider Registers

Bits	Default Value	Name	Function
D7	0	FB_frcdiv[23:16]	The Feedback fractional divider has 24 bits divided amongst 3 registers (0x19, 0x1A and 0x1B)
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 37: RAM1 – 0x1A: Feedback Fractional Divider Bits

Bits	Default Value	Name	Function
D7	0	FB_frcdiv[15:8]	The Feedback fractional divider has 24 bits divided amongst 3 registers (0x19, 0x1A and 0x1B)
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 38: RAM1 – 0x1B: Feedback Fractional Divider Registers

Bits	Default Value	Name	Function
D7	0	FB_frcdiv[7:0	The Feedback fractional divider has 24 bits divided amongst 3 registers (0x19, 0x1A and 0x1B)
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 39: RAM1 – 0x1C: Factory Reserved Bits

Bits	Default Value	Name	Function
D7	1	calibration_start	Forces VCO band calibration manually. Needs to be toggled from 0 to 1 to activate the VCO calibration
D6	0	cnf_vreg[1:0]	LDO output voltage adjustment (00, 01, 10, 11). D6 D5= 00 or 01 sets LDO to 1.1V, D6 D5= 10 sets LDO to 1.2V D6 D5=11 sets the LDO to 1.25V
D5	0		
D4	0	cnf_vreg_vco[1:0]	VCO regulator voltage adjustment (00, 01, 10, 11) D4 D3= 00 or 01 sets LDO to 1.1V, D4 D3= 10 sets LDO to 1.2V D4 D3=11 sets the LDO to 1.25V
D3	0		
D2	1	cnf_vco_bias[1:0]	VCO bias control (00, 01, 10, 11) D2 D1= 00 or 01 sets LDO to 1.1V, D2 D1= 10 sets LDO to 1.2V D2 D1=11 sets the LDO to 1.25V
D1	0		
D0	1	en_cp	Enable charge pump. Active high

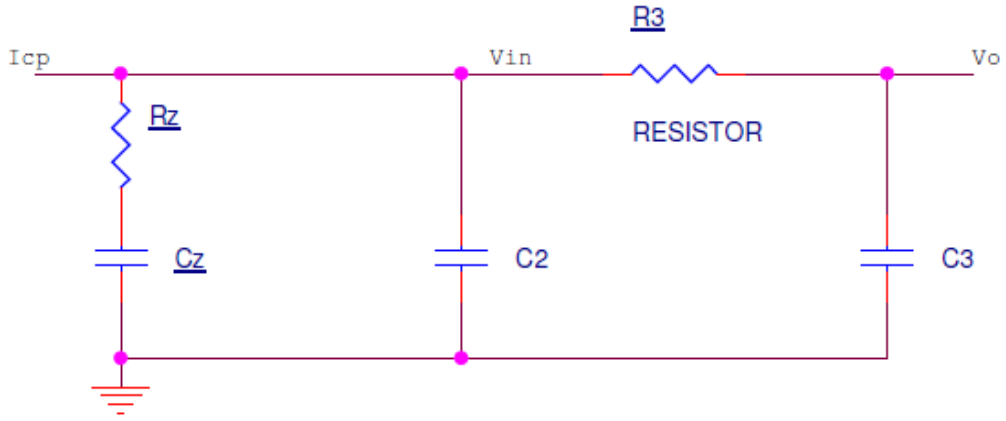
Table 40: RAM1 – 0x1D: Factory Reserved Bits

Bits	Default Value	Name	Function
D7	0	cfg_cp[3:0]	Charge-pump current control - Factory Reserved Bits 30µA step from 0 to 450µA
D6	1		
D5	1		
D4	0		
D3	1	en_vco	Enable or disable the VCO block.VCO needs to be enabled by default.
D2	1	i2c_bypb_dl	Bypass global reset. 0 means the reset is bypassed (default value). 1 means the part will reset. Used to re-synchronize the outputs when reprogramming of the device is performed
D1	1	vco_monitor_en	Enable VCO monitoring and select automatically the VCO band.
D0	1	en_pll_bias	Enable or disable biasing blocks in the PLL. Active high. Enable by default.

PLL Loop Filter Settings

Figure 5 below shows the Loop Filter components that are programmable via the RC control registers.

Figure 5. PLL Loop Filter Components



where

Rz is programmable with register 0x1E.
Cz is fixed and not programmable.
C2 is the 2nd Pole capacitor and programmable with Register 0x1E.
R3 and C3 are the 3rd pole RC values programmable with register x1F.
The Icp charge pump current is programmable in register x1D.

Table 41: RAM1 – 0x1E: RC Control Register

Bits	Default Value	Name	Function
D7	1	lpf_cnf_rz[4:0]	LPF resistor control, Rz = (15 - cnf_rz) *4 1.5K =0000 46.5K=1111
D6	0		
D5	1		
D4	1		
D3	1		
D2	0	lpf_cnf_cp[2:0]	LPF 2nd pole capacitance control 000=12pF to 111= 28pF step of 4pF
D1	1		
D0	0		

Table 42: RAM1 – 0x1F: RC Control Register

Bits	Default Value	Name	Function
D7	0	p3byp	Enable or disable bypass 3rd pole filter
D6	0	cnf_p3[5:0]	3rd pole RC configuration. Following values are programmable with bits D1 through D6 D3D2D1=001-> 2KOhm D6D5D4=001-> 1.8pF D3D2D1=010-> 8KOhm D6D5D4=011-> 3.6pF D3D2D1=011->1.6KOhm D6D5D4=111-> 5.4pF D3D2D1=100->1KOhm D3D2D1=101->7KOhm D3D2D1=110->5.3KOhm D3D2D1=111->1.45KOhm
D5	1		
D4	1		
D3	0		
D2	0		
D1	1		
D0	0	cnf_pfddly	Phase Frequency Detector delay configuration bit

Fractional Output Dividers and Spread Spectrum

Spread spectrum capability is contained within the Fractional-N output dividers associated with each output clock. When applied, triangle wave modulation of any spread spectrum amount, SS%AMT, from ±0.25% to ±2.5% center spread and - 0.5% to -5% down spread between 30 and 63kHz may be generated, independent of the output clock frequency. Five variables define Spread Spectrum in FODx (see Table 43).

Table 43: Spread Spectrum Variables in FODx

Name	Function	RAM Register (see Table 23)	Register Length	Note
ODx_ssce	Spread spectrum control enable	0x25,0x35,0x45,0x55	1	If ODx_ssce = 0, contents of ODx_period and ODx_step are Don't Care.
ODx_intdiv	Integer portion of the FODx divider, N	0x2D, 0x2E,0x3D,0x3E, 0x4D, 0x4E,0x5D,0x5E	12	
ODx_period	Spread spectrum modulation period	0x29,0x2A,0x39,0x3A, 0x49,0x4A,0x59,0x5A	13	Defined as half the reciprocal of the modulation frequency and measured in cycles of the FODx output frequency. See Eq.5 below.
ODx_step	Modulation step size	0x26,0x27,0x28,0x36, 0x37,0x38,0x46,0x47, 0x48,0x56,0x57,0x58	24	Sets the time rate of change or time slope of the output clock frequency
ODx_offset	Spread spectrum modulation offset, which defines down spread or center spread and is the fractional portion of the divider	0x22,0x23,0x24,0x25, 0x32,0x33,0x34,0x35, 0x42,0x43,0x44,0x45, 0x52,0x53,0x54,0x55	30	ODx_offset is the actual spread spectrum offset subtracted from the Fractional portion of the FODx divider N. It is the fractional portion of the FODx divider and accounts for the fact that there is no ODx_frcdiv in the Memory map.

To calculate the spread spectrum registers (fractional portion), first determine the value in decimal of the FOD output divider, N, for the nominal output frequency without spread spectrum. The VCO frequency is divided by two to account for a fixed divide by 2 between the VCO output and the input to the FOD. Convert the integer portion into hex to define ODx_intdiv.

$$N(dec) = INT(N) + FRAC(N) = \frac{\left(F_{VCO}/_2\right)}{F_{OUT}} \quad (3)$$

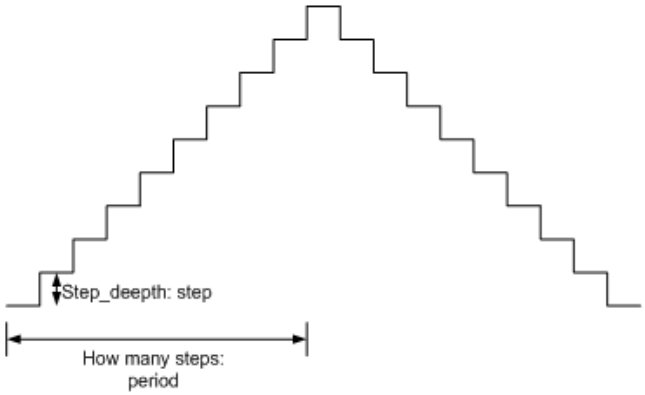
$$\text{ODx\_intdiv}[11:0] = \text{DEC2HEX}(\text{INT}(N)) \quad (4)$$

If no spread is to be applied to FODx (ODx_ssce =0) then ODx_period and ODx_step registers are don't Care and it is permissible to skip to Eq.9. Convert FRAC(N) to 30 bits as per Eq.10.

When the ODx_period and ODx_step registers are calculated below, ODx_period and ODx_step are explicitly set to 0 if ODx_ssce will always be 0. This is done for reasons of style, it reinforces the fact that there is no spread spectrum invoked when ODx_ssce =0. If down spread is to be turned on by just setting ODx_ssce =1, then ODx _period and ODx_step must be calculated and registered. See Eq.9 to see why changing only ODx_ssce works only for down spread.

Consider one cycle of down spread triangular modulation; the output divider, N, is ramped up linearly from the non-spread value of N followed by a linear ramp back down to the non-spread value of N. N is always greater than or equal to the non-spread value of N, therefore the output frequency is always less than or equal to the non-spread frequency.

Figure 6. Spread Step and Period



As normally defined, ODx_period (dec) would be 1/ F SS, but the modulation period is defined instead as ½*1/ FSS for the most direct calculation of ODx_step as will be seen below in the following Equations. An added benefit is that the up ramp and the down ramp are guaranteed to be symmetric. Note that ODx_period does not have units of time; it is the dimensionless number of FOUT periods that fit in a half period of FSS.

$$\text{ODx\_period(dec)} = \begin{Bmatrix} 0 & if\ \text{ssce} = 0 \\ \frac{1}{2} * \frac{F_{OUT}}{F_{SS}} & if\ \text{ssce} = 1 \end{Bmatrix} \quad (5)$$

$$\text{ODx\_period}[12:0] = \text{DEC2HEX(ROUND2INT(ODx\_period(dec)))} \quad (6)$$

Calculate the step size.

$$\text{ODx\_step(dec)} = \begin{Bmatrix} 0 & if\ \text{ssce} = 0 \\ \frac{SS_{\%AMT}/100 * N}{\text{ODx\_period}} & if\ \text{ssce} = 1 \end{Bmatrix} \quad (7)$$

$$\text{ODx\_step}[23:0] = \text{DEC2HEX(ROUND2INT}(2^{24} * \text{ODx\_step(dec)})) \quad (8)$$

Since the spread spectrum ramp as implemented only decreases the frequency of FOUT, then the actual offset for down spread is zero. But if the spread is to be centered, an offset equal to half the peak modulation, SS%AMT *N, is to be subtracted from the value of FRAC(N).

$$ODx\text{\_offset(dec)} = \begin{Bmatrix} FRAC(N) & if\ \text{ssce} = 0\ or\ Down\ spread \\ FRAC(N) - \frac{SS_{\%AMT}/100 * N}{2} & if\ \text{ssce} = 1\ and\ Center\ spread \end{Bmatrix} \quad (9)$$

$$ODx\text{\_offset}[29:0] = DEC2HEX(ROUND2INT[2^{24} * ODx\text{\_offset(dec)}]) \quad (10)$$

If FRAC(N) is a small positive value, it is possible that after the center spread offset is subtracted ODx_offset will be negative. In this case, retain only the lower 30 bits of the 32 bit hex value and assign them to ODx_offfset[29:0].

In this manner it can be seen that ODx_offset is the value of FRAC(N), appropriately adjusted should center spread be enabled.

Example of FOD calculation for SSCE =1:

Out1 of clock1= 99MHz, Spread enabled with total spread 0.5% and SS 31.5KHz
Feedback divider = 112.4, and VCO = 2810MHz. Let's calculate the FOD 1 value according to the equations above

FVCO/2 = 2810/2 = 1405. And FOUT = 99MHz (given)

(FVCO/2)/ FOUT = 1405/99 = 14.19191919…

OD1 Integer = 14 then ODx_intdiv[11:0]= E

As ssce = 1, ODx_period(dec) = (½) * (FOUT / FSS).

Fss = 31.5 KHz and Fout = 99 MHz then **ODx_period(dec)** = 1571.42857143

Now, from Eq.6, **ODx_period** [12:0] =623

From Eq.7, **ODx_Step(dec)** = [((0.5/100)*(14.19191919)] / 1571 = 0.00004516842.

From Eq.8 ⟶ (0.00004516842 * 2^{24}) = 757.800338719 then **Odx_Step** [23:0]= 2F5

From Eq.9, **ODx_offset(dec)**=0.19191919 - ((0.5 / 100) * 14.19191919)/ 2] = 0.15643939

From Eq.10,(2^{24} * 0.15643939) = 2624617.502. ⟶ Odx_offset [29:0] =280C69

Some calculated examples with SSCE=0 for frequency margining purposes:

Table 44: Table for PLL Configured Values

input clock(MHz)	25
ref_div(real)	0
ref_div(Hex)	0
bypass_pre_div	1
Ref for PLL (MHz)	25
VCO (GHz)	2.8
FB_div(real)	112
FB_intdiv(Hex)	70
FB_frcdiv(Hex)	0

Table 45: Output Values with SSCE=0

Frequency Margining	Output (MHz)	ssce	Divider (real)	out_intdiv (HEX)	Period (Hex)	Step (real)	Step (HEX)	Offset (real)	Offset (HEX)	skew_int (HEX)	skew_frac (HEX)
-3%	97.1455	0	14.41137	D	0	0	0	1.411373	1694FB7	1	0
-2%	98.147	0	14.26432	D	0	0	0	1.264318	143AA55	0	0
-1%	99.1485	0	14.12023	D	0	0	0	1.120234	11EC7A4	0	0
0%	100.15	0	13.97903	D	0	0	0	0.979031	FAA1CE	0	0
1%	101.1515	0	13.84063	D	0	0	0	0.840625	D73337	0	0
2%	102.153	0	13.70493	D	0	0	0	0.704933	B4767A	0	0
3%	103.1545	0	13.57188	D	0	0	0	0.571875	92666A	0	0

Table 46: FOD1 Register Table

	Register Offsets													
Output (MHz)	0x22	0x23	0x24	0x25	0x26	0x27	0x28	0x29	0x2A	0x2B	0x2C	0x2C	0x2E	0x2F
97.1455	5	A5	3E	DC	00	00	00	00	00	00	00	0	D0	00
98.147	5	0E	A9	54	00	00	00	00	00	00	00	0	D0	00
99.1485	4	7B	1E	90	00	00	00	00	00	00	00	0	D0	00
100.15	3	EA	87	38	00	00	00	00	00	00	00	0	D0	00
101.1515	3	5C	CC	DC	00	00	00	00	00	00	00	0	D0	00
102.153	2	D1	D9	E8	00	00	00	00	00	00	00	0	D0	00
103.1545	2	49	99	A8	00	00	00	00	00	00	00	0	D0	00

Output Divider Control Settings (Table 47, Table 48, Table 49, Table 50)

These bits are for Output divider's control register settings and are reserved in general. The reset bit for the FOD is active low. The combination of en_fod(fractional output divider enable bit), sel_ext(the output from previous channel FOD) and selb_norm (the output from current FOD), will set the divider mode. The integer mode only can be enabled with int_mode bit.

Table 47: RAM2 – 0x21: Output Divider 1 Control Register Settings

Bits	Default Value	Name	Function
D7	1	i2c_resetb1	Reset Fractional Output Divider 1 (FOD) circuit when set to 0 - Factory Reserved Bit
D6	0	en_pi_out_cap<2:0>	Factory Reserved /Unused bits
D5	0		
D4	0		
D3	0	selb_norm1	**For 5P49V6901, 5P49V6913, 5P49V6914**: (en_fod1, sel_ext1, selb_norm1) = (1, x, 0) use output's divider 1 settings. (en_fod1, sel_ext1, selb_norm1) = (0, 1, 1) use previous channel's clock output. (en_fod1, sel_ext1, selb_norm1) = (0, 0, 0) then sets output divider off. Int_mode1 enables integer mode for output divider 1.
D2	0	sel_ext1	
D1	0	int_mode1	
D0	1	en_fod1	

Table 48: RAM3 – 0x31: Output Divider 2 Control Register Settings

Bits	Default Value	Name	Function
D7	0	i2c_resetb2	Reset Fractional Output Divider 2 (FOD) circuit when set to 0 - Factory Reserved Bit
D6	0	en_pi_out_cap<2:0>	Factory Reserved /Unused bits
D5	0		
D4	0		
D3	0	selb_norm2	**For 5P49V6901, 5P49V6913, 5P49V6914**: (en_fod2, sel_ext2, selb_norm2) = (1, x, 0) use output's divider 2 settings. (en_fod2, sel_ext2, selb_norm2) = (0, 1, 1) use previous channel's clock output. (en_fod2, sel_ext2, selb_norm2) = (0, 0, 0) then sets output divider off. Int_mode2 enables integer mode for output divider 2
D2	0	sel_ext2	
D1	0	int_mode2	
D0	0	en_fod2	

Table 49: RAM4 – 0x41: Output Divider 3 Control Register Settings

Bits	Default Value	Name	Function
D7	0	i2c_resetb3	Reset Fractional Output Divider 3 (FOD) circuit when set to 0 - Factory Reserved Bit
D6	0	en_pi_out_cap<2:0>	Factory Reserved /Unused bits
D5	0		
D4	0		
D3	0	selb_norm3	**For 5P49V6901, 5P49V6913, 5P49V6914**: (en_fod3, sel_ext3, selb_norm3) = (1, x, 0) use output's divider 3 settings. (en_fod3, sel_ext3, selb_norm3) = (0, 1, 1) use previous channel's clock output. (en_fod3, sel_ext3, selb_norm3) = (0, 0, 0) then sets output divider off. Int_mode3 enables integer mode for output divider 3
D2	0	sel_ext3	
D1	0	int_mode3	
D0	0	en_fod3	

Table 50: RAM5 – 0x51: Output Divider 4 Control Register Settings

Bits	Default Value	Name	Function
D7	0	i2c_resetb4	Reset Fractional Output Divider 4 (FOD) circuit when set to 0 - Factory Reserved Bit
D6	0	en_pi_out_cap<2:0>	Factory Reserved /Unused bits
D5	0		
D4	0		
D3	0	selb_norm4	**For 5P49V6901, 5P49V6913, 5P49V6914:** (en_fod4, sel_ext4, selb_norm4) = (1, x, 0) use output's divider 4 settings. (en_fod4, sel_ext4, selb_norm4) = (0, 1, 1) use previous channel's clock output. (en_fod4, sel_ext4, selb_norm4) = (0, 0, 0) then sets output divider off. Int_mode4 enables integer mode for output divider 4
D2	0	sel_ext4	
D1	0	int_mode4	
D0	0	en_fod4	

Output Divider Integer Settings (Table 51 through Table 58)

Output divider's integer part consists of 12 bits spread on 2 consecutive registers. The 4 dividers are assigned to respectively to each output 1,2,3,4.

Table 51: RAM2 – 0x2D: Output Divider 1 Integer Part

Bits	Default Value	Name	Function
D7	0	OD1_intdiv[11:4	Output divider 1 integer part has 12 bit spread over 2 registers x2D and x2E
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 52: RAM2 – 0x2E: Output Divider 1 Integer Part

Bits	Default Value	Name	Function
D7	1	OD1_intdiv[3:0]	Output divider 1 integer part has 12 bit spread over 2 registers x2D and x2E
D6	1		
D5	1		
D4	0		
D3	0	unused bits	Unused Factory Reserved Bit
D2	0	unused bits	Unused Factory Reserved Bit
D1	0	unused bits	Unused Factory Reserved Bit
D0	0	unused bits	Unused Factory Reserved Bit

Table 53: RAM3 – 0x3D: Output Divider 2 Integer Part

Bits	Default Value	Name	Function
D7	0	OD2_intdiv[11:4]	Output divider 2 integer part has 12 bit spread over 2 registers x3D and x3E
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 54: RAM3 – 0x3E: Output Divider 2 Integer Part

Bits	Default Value	Name	Function
D7	0	OD2_intdiv[3:0]	Output divider 2 integer part has 12 bit spread over 2 registers x3D and x3E
D6	0		
D5	0		
D4	0		
D3	0	unused bits	Unused Factory Reserved Bit
D2	0	unused bits	Unused Factory Reserved Bit
D1	0	unused bits	Unused Factory Reserved Bit
D0	0	unused bits	Unused Factory Reserved Bit

Table 55: RAM4 – 0x4D: Output Divider 3 Integer Part

Bits	Default Value	Name	Function
D7	0	OD3_intdiv[11:4]	Output divider 3 integer part has 12 bit spread over 2 registers x4D and x4E
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 56: RAM4 – 0x4E: Output Divider 3 Integer Part

Bits	Default Value	Name	Function
D7	0	OD3_intdiv[3:0]	Output divider 3 integer part has 12 bit spread over 2 registers x4D and x4E
D6	0		
D5	0		
D4	0		
D3	0	unused bits	Unused Factory Reserved Bit
D2	0	unused bits	Unused Factory Reserved Bit
D1	0	unused bits	Unused Factory Reserved Bit
D0	0	unused bits	Unused Factory Reserved Bit

Table 57: RAM5 – 0x5D: Output Divider 4 Integer Part

Bits	Default Value	Name	Function
D7	0	OD4_intdiv[11:4]	Output divider 4 integer part has 12 bit spread over 2 registers x5D and x5E
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 58: RAM5 – 0x5E: Output Divider 4 Integer Part

Bits	Default Value	Name	Function
D7	0	OD4_intdiv[3:0]	Output divider 4 integer part has 12 bit spread over 2 registers X5D and x5E
D6	0		
D5	0		
D4	0		
D3	0	unused bits	Unused Factory Reserved Bit
D2	0	unused bits	Unused Factory Reserved Bit
D1	0	unused bits	Unused Factory Reserved Bit
D0	0	unused bits	Unused Factory Reserved Bit

Output Divider Fractional and Spread settings (Table 59 through Table 94)

ODx_offset is the actual spread spectrum offset subtracted from the Fractional portion of the FODx divider N. It is the fractional portion of the FODx divider. 30 bits spread over 4 registers. MSB is a sign bit. Set to 1 for negative numbers.

ODx_period bits are used to tune the spread rate from 30KHz to 63KHz according to the output frequency (period = Fout/Fss/2).13 bits spread on 2 registers.

ODx_step is the Modulation step size; it sets the time rate of change or time slope of the output clock frequency. 24 bits spread on 3 registers.

If ODx_ssce = 0, contents of ODx_period and ODx_step are don't care only the ODx_offset are taken into account.
If ODx_ssce =1, means the spread is enabled for center spread offset. (See example of spread calculation "Example of FOD calculation for SSCE =1:")

Table 59: RAM2 – 0x22: Output Divider 1 Fractional Settings

Bits	Default Value	Name	Function
D7	0	OD1_offset[29:22]	30 bits to configure the fraction value of FOD1 in register addr. x22, x23, x24 and x25.
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 60: RAM2 – 0x23: Output Divider 1 Fractional Settings

Bits	Default Value	Name	Function
D7	0	OD1_offset[21:14]	30 bits to configure the fraction value of FOD1 in register addr. x22, x23, x24 and x25
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 61: RAM2 – 0x24: Output Divider 1 Fractional Settings

Bits	Default Value	Name	Function
D7	0	OD1_offset[13:6]	30 bits to configure the fraction value of FOD1 in register addr. x22, x23, x24 and x25
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 62: RAM2 – 0x25: Output Divider 1 Fractional Settings

Bits	Default Value	Name	Function
D7	0	OD1_offset[5:0	30 bits to configure the fraction value of FOD1 in register addr. x22, x23, x24 and x25
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0	OD1_ssce	Enable Spread Spectrum with center spread offset. Active High
D0	0	Unused	Unused Factory Reserved Bit

Table 63: RAM2 – 0x26: Output Divider 1 Step Spread Configuration Register

Bits	Default Value	Name	Function
D7	0	OD1_step[7:0]	24 bits used for Modulation Step Size in register x26 x27 and x28
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 64: RAM2 – 0x27: Output Divider 1 Step Spread Configuration Register

Bits	Default Value	Name	Function
D7	0	OD1_step[15:8]	24 bits used for Modulation Step Size in register x26 x27 and x28
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 65: RAM2 – 0x28: Output Divider 1 Step Spread Configuration Register

Bits	Default Value	Name	Function
D7	0	OD1_step[23:16]	24 bits used for Modulation Step Size in register x26 x27 and x28
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 66: RAM2 – 0x29: Output Divider 1 Spread Modulation Rate Configuration Register

Bits	Default Value	Name	Function
D7	0	OD1_period[12:5	13 bits used to configure spread modulation period in register x29 and x2A
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 67: RAM2 – 0x2A: Output Divider 1 Spread Modulation Rate Configuration Register

Bits	Default Value	Name	Function
D7	0	OD1_period[4:0]	13 bits used to configure spread modulation period in register x29 and x2A
D6	0		
D5	0		
D4	0		
D3	0		
D2	1	cnf_vreg_fod1<1:0>	cnf_vreg_fod1<1:0>: 00=1.2V, 10=1.3V, 11=1.33V
D1	0	Unused Bits	Unused Factory Reserved Bit
D0	0	Unused Bits	Unused Factory Reserved Bit

Table 68: RAM3 – 0x32: Output Divider 2 Fractional Settings

Bits	Default Value	Name	Function
D7	0	OD2_offset[29:6	30 bits to configure the fraction value of FOD2 in register addr. x32, x33, x34 and x35
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 69: RAM3 – 0x33: Output Divider 2 Fractional Settings

Bits	Default Value	Name	Function
D7	0	OD2_offset[29:6	30 bits to configure the fraction value of FOD2 in register addr. x32, x33, x34 and x35
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 70: RAM3 – 0x34: Output Divider 2 Fractional Settings

Bits	Default Value	Name	Function
D7	0	OD2_offset[29:6]	30 bits to configure the fraction value of FOD2 in register addr. x32, x33, x34 and x35
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 71: RAM3 – 0x35: Output Divider 2 Fractional Settings

Bits	Default Value	Name	Function
D7	0	OD2_offset[5:0]	30 bits to configure the fraction value of FOD2 in register addr. x32, x33, x34 and x35
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0	OD2_ssce	Enable Spread Spectrum with center spread offset. Active High
D0	0	Unused Bit	Unused Factory Reserved Bit

Table 72: RAM3 – 0x36: Output Divider 2 Step Spread Configuration Register

Bits	Default Value	Name	Function
D7	0	OD2_step[7:0	24 bits used for Modulation Step Size in register x36 x37 and x38
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 73: RAM3 – 0x37: Output Divider 2 Step Spread Configuration Register

Bits	Default Value	Name	Function
D7	0	OD2_step[15:8]	24 bits used for Modulation Step Size in register x36 x37 and x38
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 74: RAM3 – 0x38: Output Divider 2 Step Spread Configuration Register

Bits	Default Value	Name	Function
D7	0	OD2_step[23:16]	24 bits used for Modulation Step Size in register x36 x37 and x38
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 75: RAM3 – 0x39: Output Divider 2 Spread Modulation Rate Configuring Register

Bits	Default Value	Name	Function
D7	0	OD2_period[12:5]	13 bits used to configure spread modulation period in register x39 and x3A
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 76: RAM3 – 0x3A: Output Divider 2 Spread Modulation Rate Configuring Register

Bits	Default Value	Name	Function
D7	0	OD2_period[4:0]	13 bits used to configure spread modulation period in register x39 and x3A
D6	0		
D5	0		
D4	0		
D3	0		
D2	0	cnf_vreg_fod2<1:0>	cnf_vreg_fod2<1:0>: 00=1.2V, 10=1.3V, 11=1.33V
D1	0	Unused Bit	Unused Factory Reserved Bit
D0	0	Unused Bit	Unused Factory Reserved Bit

Table 77: RAM4 – 0x42: Output Divider 3 Fractional Settings

Bits	Default Value	Name	Function
D7	0	OD3_offset[29:6]	30 bits to configure the fraction value of FOD3 in register addr. x42, x43, x44 and x45
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 78: RAM4 – 0x43: Output Divider 3 Fractional Settings

Bits	Default Value	Name	Function
D7	0	OD3_offset[29:6]	30 bits to configure the fraction value of FOD3 in register addr. x42, x43, x44 and x45
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 79: RAM4 – 0x44: Output Divider 3 Fractional Settings

Bits	Default Value	Name	Function
D7	0	OD3_offset[29:6]	30 bits to configure the fraction value of FOD3 in register addr. x42, x43, x44 and x45
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 80: RAM4 – 0x45: Output Divider 3 Fractional Settings

Bits	Default Value	Name	Function
D7	0	OD3_offset[5:0	30 bits to configure the fraction value of FOD3 in register addr. x42, x43, x44 and x45
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0	OD3_ssce	Enable Spread Spectrum with center spread offset. Active High
D0	0	Unused	Unused Factory Reserved Bit

Table 81: RAM4 – 0x46: Output Divider 3 Step Spread Configuration Register

Bits	Default Value	Name	Function
D7	0	OD3_step[7:0]	24 bits used for Modulation Step Size in register x46 x47 and x48
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 82: RAM4 – 0x47: Output Divider 3 Step Spread Configuration Register

Bits	Default Value	Name	Function
D7	0	OD3_step[15:8]	24 bits used for Modulation Step Size in register x46 x47 and x48
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 83: RAM4 – 0x48: Output Divider 3 Step Spread Configuration Register

Bits	Default Value	Name	Function
D7	0	OD3_step[23:16]	24 bits used for Modulation Step Size in register x46 x47 and x48
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 84: RAM4 – 0x49: Output Divider 3 Spread Modulation Rate Configuring Register

Bits	Default Value	Name	Function
D7	0	OD3_period[12:5]	13 bits used to configure spread modulation period in register x49 and x4A
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 85: RAM4 – 0x4A: Output Divider 3 Spread Modulation Rate Configuring Register

Bits	Default Value	Name	Function
D7	0	OD3_period[4:0]	13 bits used to configure spread modulation period in register x49 and x4A
D6	0		
D5	0		
D4	0		
D3	0		
D2	0	cnf_vreg_fod3<1:0>	cnf_vreg_fod3<1:0>: 00=1.2V, 10=1.3V, 11=1.33V
D1	0	Unused	Unused Factory Reserved Bit
D0	0	Unused	Unused Factory Reserved Bit

Table 86: RAM5 – 0x52: Output Divider 4 Fractional Settings

Bits	Default Value	Name	Function
D7	0	OD4_offset[29:6	30 bits to configure the fraction value of FOD4 in register addr. x52, x53, x54 and x55
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 87: RAM5 – 0x53: Output Divider 4 Fractional Settings

Bits	Default Value	Name	Function
D7	0	OD4_offset[29:6]	30 bits to configure the fraction value of FOD4 in register addr. X52, x53, x54 and x55
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 88: RAM5 – 0x54: Output Divider 4 Fractional Settings

Bits	Default Value	Name	Function
D7	0	OD4_offset[29:6]	30 bits to configure the fraction value of FOD4 in register addr. x52, x53, x54 and x55
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 89: RAM5 – 0x55: Output Divider 4 Fractional Settings

Bits	Default Value	Name	Function
D7	0	OD4_offset[5:0]	30 bits to configure the fraction value of FOD4 in register addr. x52, x53, x54 and x55
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0	OD1_ssce	Enable Spread Spectrum with center spread offset. Active High
D0	0	Unused bits	Unused Factory Reserved Bit

Table 90: RAM5 – 0x56: Output Divider 4 Step Spread Configuration Register

Bits	Default Value	Name	Function
D7	0	OD4_step[7:0]	24 bits used for Modulation Step Size in register x56 x57 and x58
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 91: RAM5 – 0x57: Output Divider 4 Step Spread Configuration Register

Bits	Default Value	Name	Function
D7	0	OD4_step[15:8]	24 bits used for Modulation Step Size in register x56 x57 and x58
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 92: RAM5 – 0x58: Output Divider 4 Step Spread Configuration Register

Bits	Default Value	Name	Function
D7	0	OD4_step[23:16]	24 bits used for Modulation Step Size in register x56 x57 and x58
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 93: RAM5 – 0x59: Output Divider 4 Spread Modulation Rate Configuring Register

Bits	Default Value	Name	Function
D7	0	OD4_period[12:5]	13 bits used to configure spread modulation period in register x59 and x5A
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 94: RAM5 – 0x5A: Output Divider 4 Spread Modulation Rate Configuring Register.

Bits	Default Value	Name	Function
D7	0	OD4_period[4:0]	13 bits used to configure spread modulation period in register x59 and x5A
D6	0		
D5	0		
D4	0		
D3	0		
D2	0	cnf_vreg_fod4<1:0>	cnf_vreg_fod4<1:0>: 00=1.2V, 10=1.3V, 11=1.33V
D1	0	Unused bits	Unused Factory Reserved Bit
D0	0	Unused bits	Unused Factory Reserved Bit

Skew

Skew is not implemented with a parallel load of the count of the output divider as is commonly done with non-fractional divides. Instead skew is accomplished by increasing the value of the fractional output divider for only the very first clock cycle. The divide is increased by the number of VCO cycles required to delay the completion of the first output clock cycle by the desired skew. For the second and all subsequent output cycles, hardware changes the output divider to the value for the proper steady state output frequency.

The integer and fractional components of skew are calculated as follows:

$$INT(Skew)(\text{dec}) = INT\left(\left[1 + \frac{Degrees\ of\ Skew}{360}\right] * N\right) - INT(N) \quad (11)$$

$$ODx\_intskew[11:0] = DEC2HEX\big(INT(Skew)\big) \quad (12)$$

$$FRAC(Skew)(\text{dec}) = \left[1 + \frac{Degrees\ of\ Skew}{360}\right] * N - INT(N) - INT(skew) \quad (13)$$

$$ODx\_frcskew[5:0] = DEC2HEX(INT[2^6 * FRAC(Skew)]) \quad (14)$$

There are 12 bits for an integer value and 6 bits for a fraction. The unit used for the skew is degrees of delay of the edge.

The VCO frequency is first divided by 2 before it goes to the Output Divider. The number programmed for skew is the amount of cycles of the VCO/2 frequency that is needed to achieve the skew amount.

Let's use an example of OUT1=100MHz, OUT2=100MHz and we want to delay OUT1 with 1.3ns versus OUT2. The total cycle is 10ns so 1.3ns represents 360×1.3/10=46.8° of skew. Let's also say that we used VCO=2800MHz so the Output Divider value N=(2800/2)/100=14. Each cycle of the VCO/2=1400MHz signal represents 360/14=25.7°. That means the skew number will be 46.8/25.7=1.82. The integer part of the skew will be 1 and the fractional setting will be INT(0.82×2^6)=116 or 74 hex.

The formulas for skew are as follows:

Formula for the integer value:

$$INT(Skew)(\text{dec}) = INT\left(\left[1 + \frac{Degrees\ of\ Skew}{360}\right] * N\right) - INT(N)$$

Formula for the fraction:

$$FRAC(Skew)(\text{dec}) = \left[1 + \frac{Degrees\ of\ Skew}{360}\right] * N - INT(N) - INT(skew)$$

INT(Skew) = INT((1+46.8/360)*14) - INT(14) = 15 - 14 = 1

FRAC(Skew) = (1+46.8/360)*14 - INT(14) - 1 = 0.82

Translating these two values to register settings:

$ODx\_intskew[11:0] = DEC2HEX\big(INT(Skew)\big)$ = 001 (hex)

$ODx\_frcskew[5:0] = DEC2HEX(INT[2^6 * FRAC(Skew)])$ = 74 (hex)

To apply the 1.3ns skew on OUT1 we need to write the following values:

Addr - Byte
0x2B - 00
0x2C - 10
0x2F - 74

After writing these values all counters need to be restarted to insert the 1.3ns delay in OUT1 versus the other outputs. The restarting can be done by toggling the I^2C global reset in bit 5 of register 0x76. First read register 0x76 to know the setting of all bits. Bit 5 will be "1" when the outputs are running. Commonly the value of 0x76 will be E3 (hex) and I am assuming this value in the example code below.

The full code to set the 1.3ns skew on the fly will look like this:

Addr - Byte
0x2B - 00 (OD1_intskew[11:4]=00, most likely it is already 00 and you could skip this line)
0x2C - 10 (OD1_intskew[3:0]=1)
0x2F - 74 (OD1_frskew[5:0]=74)
0x76 - C3 (Set I2C_Global_Reset)
0x76 - E3 (Release I2C_Global_Reset)

Removing the skew again:

0x2B - 00
0x2C - 00
0x2F - 00
0x76 - C3
0x76 - E3

After writing these values on the fly all counters need to be restarted to insert the 1.3ns delay in OUT1 versus the other outputs.

Output Divider Skew Integer and Fractional Part Registers Settings (Tables 95 to 107)

The 12 bits integer part of the skew are spread over 2 registers for each output divider and 6 bits are used to configure the fractional part of the skew.

Table 95: RAM2 – 0x2B: Output Divider 1 Skew Integer Part

Bits	Default Value	Name	Function
D7	0	OD1_intskew[11:4]	12 bits are used to set Output Divider 1 skew integer part in register x2B and x2C
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 96: RAM2 – 0x2C: Output Divider 1 Skew Integer Part

Bits	Default Value	Name	Function
D7	0	OD1_intskew[3:0]	12 bits are used to set Output Divider 1 skew integer part in register x2B and x2C
D6	0		
D5	0		
D4	0		
D3	0	Unused bits	Unused Factory Reserved Bit
D2	0	Unused bits	Unused Factory Reserved Bit
D1	0	Unused bits	Unused Factory Reserved Bit
D0	0	en_aux	Factory Reserved Bit

Table 97: RAM2 – 0x2F: Output Divider 1 Skew Fractional Part

Bits	Default Value	Name	Function
D7	0	Unused bits	Unused Factory Reserved Bit
D6	0	Unused bits	Unused Factory Reserved Bit
D5	0	OD1_frcskew[5:0]	6 bits are used to set Output Divider 1 Skew fractional part
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 98: RAM3 – 0x3B: Output Divider 2 Skew Integer Part

Bits	Default Value	Name	Function
D7	0	OD2_intskew[11:4]	12 bits are used to set Output Divider 2 skew integer part in register x3B and x3C
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 99: RAM3 – 0x3C: Output Divider 2 Skew Integer Part

Bits	Default Value	Name	Function
D7	0	OD2_intskew[3:0]	12 bits are used to set Output Divider2 skew integer part in register x3B and x3C
D6	0		
D5	0		
D4	0		
D3	0	Unused bits	Unused Factory Reserved Bit
D2	0	Unused bits	Unused Factory Reserved Bit
D1	0	Unused bits	Unused Factory Reserved Bit
D0	0	en_aux	Factory Reserved Bit

Table 100: RAM3 – 0x3F: Output Divider 2 Skew Fractional Part

Bits	Default Value	Name	Function
D7	0	Unused bits	Unused Factory Reserved Bit
D6	0	Unused bits	Unused Factory Reserved Bit
D5	0	OD2_frcskew[5:0]	6 bits are used to set Output Divider2 skew fractional part
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 101: RAM4 – 0x4B: Output Divider 3 Skew Integer Part

Bits	Default Value	Name	Function
D7	0	OD3_intskew[11:4]	12 bits are used to set Output Divider3 skew integer part in register x4B and x4C
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 102: RAM4 – 0x4C: Output Divider 3 Skew Integer Part

Bits	Default Value	Name	Function
D7	0	OD3_intskew[3:0]	12 bits are used to set Output Divider3 skew integer part in register x4B and x4C
D6	0		
D5	0		
D4	0		
D3	0	Unused bits	Unused Factory Reserved Bit
D2	0	Unused bits	Unused Factory Reserved Bit
D1	0	Unused bits	Unused Factory Reserved Bit
D0	0	en_aux	Factory Reserved Bit

Table 103: RAM4 – 0x4F: Output Divider 3 Skew Fractional Part

Bits	Default Value	Name	Function
D7	0	Unused bits	Unused Factory Reserved Bit
D6	0	Unused bits	Unused Factory Reserved Bit
D5	0	OD3_frcskew[5:0]	6 bits are used to set Output Divider3 skew fractional part
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 104: RAM5 – 0x50: Unused Factory Reserved Register

Bits	Default Value	Name	Function
D7	0	Unused Factory Reserved Bits	Unused Factory Reserved Bits
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 105: RAM5 – 0x5B: Output Divider 4 Skew Integer Part

Bits	Default Value	Name	Function
D7	0	OD4_intskew[11:4]	12 bits are used to set Output Divider4 skew integer part in register x5B and x5C
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 106: RAM5 – 0x5C: Output Divider 4 Skew Integer Part

Bits	Default Value	Name	Function
D7	0	OD4_intskew[3:0]	12 bits are used to set Output Divider4 skew integer part in register x5B and x5C
D6	0		
D5	0		
D4	0		
D3	0	Unused bits	Unused Factory Reserved Bit
D2	0	Unused bits	Unused Factory Reserved Bit
D1	0	Unused bits	Unused Factory Reserved Bit
D0	0	en_aux	Factory Reserved Bit

Table 107: RAM5 – 0x5F: Output Divider 4 Skew Fractional Part

Bits	Default Value	Name	Function
D7	0	Unused bits	Unused Factory Reserved Bit
D6	0	Unused bits	Unused Factory Reserved Bit
D5	0	OD4_frcskew[5:0]	6 bits are used to set Output Divider4 skew fractional part
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Clock Output Configurations Registers

In Clock Output Configuration registers described in the tables below, the CLKx_pwr_sel bits must be configured to match the clock outputs' supply voltages applied externally. The bits don't adjust the clock output signal swings. CMOSX2 provides two phase-coherent single ended CMOS outputs while CMOSD provides 2 signals out of phase by 180 degrees. In Clock2 Output Configuration, Bits are especially for disabling/enabling clock output/value and slew rate for differential outputs.

Table 108: RAM6 – 0x60: Clock1 Output Configuration

Bits	Default Value	Name	Function
D7	1	CLK1_cfg[2]	These bits give us the output type configuration mode. For D7,D6,D5 respectively: (D7,D6,D5)= 000 : low-voltage positive/pseudo emitter-coupled logic (LVPECL); (D7,D6,D5)= 001 : CMOS; (D7,D6,D5)= 010 : HCSL33; (D7,D6,D5)= 011: Low Voltage Differential Signal(LVDS); (D7,D6,D5)= 100: CMOS2; (D7,D6,D5)= 101: CMOSD; (D7,D6,D5)= 110: HCSL25;
D6	0	CLK1_cfg[1]	
D5	1	CLK1_cfg[0]	
D4	1	clk1_pwr_sel[1:0]	Output Drive Voltage is set by those bits. D4 D3 = 00 sets 1.8v D4 D3 = 10 sets 2.5v D4 D3 = 11 sets 3.3v
D3	1		
D2	0	Unused Bits	Factory reserved unused bits
D1	1	CLK1_slew[1]	It makes slew rate control for CMOS single ended D1 D0 = 00 then output slew rate is 0.8*Normal. D1 D0 = 01 then output slew rate indicates 0.85*Normal D1 D0 = 10 then output slew rate indicates 0.9*Normal D1 D0 = 11 then output slew rate indicates 1*Normal
D0	1	CLK1_slew[0]	

Table 109: RAM6 – 0x61: Clock1 Output Configuration

Bits	Default Value	Name	Function
D7	0	CLK1_slew_diff[5:0]	Unused Register Bits
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0	clk1_amuxen2	This bit is used to disable the output value. Active High (1) to disable output
D0	1	en_clkbuf1	This bit is used to enable the clock output. Active High (1) to enable the clock output

Table 110: RAM6 – 0x62: Clock2 Output Configuration

Bits	Default Value	Name	Function
D7	0	CLK2_cfg[2]	These bits give us the output type configuration mode. For D7,D6,D5 respectively: (D7,D6,D5)= 000 : low-voltage positive/pseudo emitter-coupled logic (LVPECL); (D7,D6,D5)= 001 : CMOS; (D7,D6,D5)= 010 : HCSL33; (D7,D6,D5)= 011: Low Voltage Differential Signal(LVDS); (D7,D6,D5)= 100: CMOS2; (D7,D6,D5)= 101: CMOSD; (D7,D6,D5)= 110: HCSL25;
D6	1	CLK2_cfg[1]	
D5	0	CLK2_cfg[0]	
D4	1	clk2_pwr_sel[1:0]	Output Drive Voltage is set by those bits. D4 D3 = 00 sets 1.8v D4 D3 = 10 sets 2.5v D4 D3 = 11 sets 3.3v
D3	1		
D2	0	Unused Bit	Unused Factory Reserved Bit
D1	1	CLK2_slew[1]	It makes slew rate control for CMOS single ended D1 D0 = 00 then output slew rate is 0.8*Normal. D1 D0 = 01 then output slew rate indicates 0.85*Normal D1 D0 = 10 then output slew rate indicates 0.9*Normal D1 D0 = 11 then output slew rate indicates 1*Normal
D0	1	CLK2_slew[0]	

Table 111: RAM6 – 0x63: Clock2 Output Configuration

Bits	Default Value	Name	Function
D7	0	CLK2_slew_diff[5:0]	Unused Register Bits
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0	clk2_amuxen2	This bit is used to disable the output value. Active High (1) to disable output
D0	0	en_clkbuf2	This bit is used to enable the clock output. Active High (1) to enable the clock output

Table 112: RAM6 – 0x64: Clock3 Output Configuration

Bits	Default Value	Name	Function
D7	0	CLK3_cfg[2]	These bits give us the output type configuration mode. For D7,D6,D5 respectively: (D7,D6,D5)= 000 : low-voltage positive/pseudo emitter-coupled logic (LVPECL); (D7,D6,D5)= 001 : CMOS; (D7,D6,D5)= 010 : HCSL33; (D7,D6,D5)= 011: Low Voltage Differential Signal(LVDS); (D7,D6,D5)= 100: CMOS2; (D7,D6,D5)= 101: CMOSD; (D7,D6,D5)= 110: HCSL25;
D6	1	CLK3_cfg[1]	
D5	1	CLK3_cfg[0]	
D4	1	clk3_pwr_sel[1:0]	Output Drive Voltage is set by those bits. D4 D3 = 00 sets 1.8v D4 D3 = 10 sets 2.5v D4 D3 = 11 sets 3.3v
D3	1		
D2	0	Unused Bit	Unused Factory Reserved Bit
D1	1	CLK3_slew[1]	It makes slew rate control for CMOS single ended D1 D0 = 00 then output slew rate is 0.8*Normal. D1 D0 = 01 then output slew rate indicates 0.85*Normal D1 D0 = 10 then output slew rate indicates 0.9*Normal D1 D0 = 11 then output slew rate indicates 1*Normal
D0	1	CLK3_slew[0]	

Table 113: RAM6 – 0x65: Clock3 Output Configuration

Bits	Default Value	Name	Function
D7	0	CLK3_slew_diff[5:0]	Unused Register Bits
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0	clk3_amuxen2	This bit is used to disable the output value. Active High (1) to disable output
D0	0	en_clkbuf3	This bit is used to enable the clock output. Active High (1) to enable the clock output

Table 114: RAM6 – 0x66: Clock4 Output Configuration

Bits	Default Value	Name	Function
D7	0	CLK4_cfg[2]	These bits give us the output type configuration mode. For D7,D6,D5 respectively: (D7,D6,D5)= 000 : low-voltage positive/pseudo emitter-coupled logic (LVPECL); (D7,D6,D5)= 001 : CMOS; (D7,D6,D5)= 010 : HCSL33; (D7,D6,D5)= 011: Low Voltage Differential Signal(LVDS); (D7,D6,D5)= 100: CMOS2; (D7,D6,D5)= 101: CMOSD; (D7,D6,D5)= 110: HCSL25;
D6	0	CLK4_cfg[1]	
D5	0	CLK4_cfg[0]	
D4	1	clk4_pwr_sel[1:0]	Output Drive Voltage is set by those bits. D4 D3 = 00 sets 1.8v D4 D3 = 10 sets 2.5v D4 D3 = 11 sets 3.3v
D3	1		
D2	0	Unused Bit	Unused Factory Reserved Bit
D1	1	CLK4_slew[1]	It makes slew rate control for CMOS single ended D1 D0 = 00 then output slew rate is 0.8*Normal. D1 D0 = 01 then output slew rate indicates 0.85*Normal D1 D0 = 10 then output slew rate indicates 0.9*Normal D1 D0 = 11 then output slew rate indicates 1*Normal
D0	1	CLK4_slew[0]	

Table 115: RAM6 – 0x67: Clock4 Output Configuration

Bits	Default Value	Name	Function
D7	0	CLK4_slew_diff[5:0]	Unused Register Bits
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0	clk4_amuxen2	This bit is used to disable the output value. Active High (1) to disable output
D0	0	en_clkbuf4	This bit is used to enable the clock output. Active High (1) to enable the clock output

Table 116: Unused Factory Reserved Registers

Registers	0x20	0x30	0x40	0x50

Revision History

Revision Date	Description of Change
May 29, 2019	Updated “When SP bit D1=1, SD/OE is active **low**”, to “When SP bit D1=1, SD/OE is active **high**” in the Shutdown Function section.
January 30, 2017	Initial release.

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