# RC32504A / RC22504A

The RC32504A / RC22504A evaluation board (EVB) is designed to help users evaluate the RC32504A and RC22504A Clock Generators, also known as FemtoClock 2. The RC32504A supports Jitter Attenuator and Synthesizer functionality, and the RC22504A supports only Synthesizer functionality.

When the evaluation board (EVB) is connected via USB to the user's computer running the Renesas' RICBox™ Software, FemtoClock 2 can be configured and programmed to generate frequencies with best-in-class performance. FemtoClock 2 has four output pairs that can be programmed to CMOS style, LVDS style, or HCSL style outputs.

## Features

- Develop configurations with Renesas RICBox software and upload to the EVB through USB
- Can be powered from the USB connection
- EVB is a combination evaluation with Renesas Low Noise power supply regulators and Renesas Low Noise fan-out buffer
- Clock output pairs are AC coupled and can be connected directly to test equipment through coax cables.

## Board Contents

- Renesas RS32504A ultra-low noise synthesizer and jitter attenuator
- Renesas RAA214020 low-noise power supply regulators
- Renesas 8P34S1208I low-noise fan-out buffer
- FTDI FT232HQ USB-to-I2C bridge

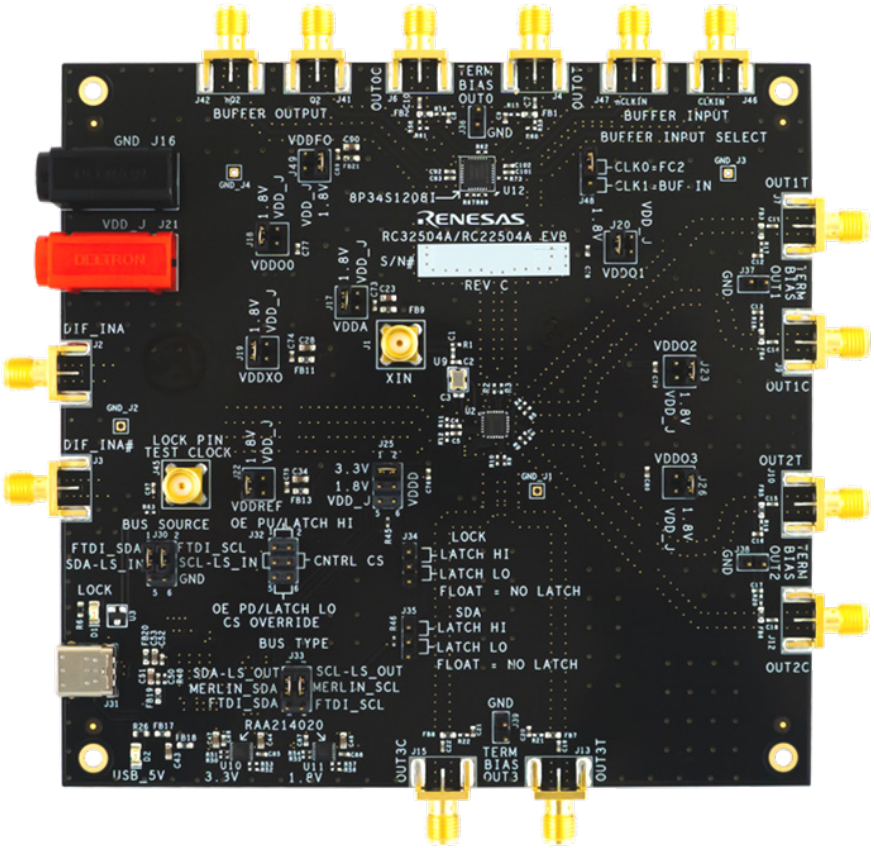



**Figure 1. RC32504A / RC22504A Board**

# Contents



# Figures

# 1. Functional Description

## 1.1 Connecting the Board to a Computer

The evaluation board can be connected to a computer via the USB connector (see Figure 4). This board has a USB-C type connector. The on-board USB-to-I2C bridge (FTDI chip) handles the data communication, and the +5V in the USB bus powers the on-board regulators. Using a bench power supply with the VDD jacks is optional. The board can fully function with just the USB cable to a computer.

Renesas' *RICBox Software* can control the RC32504A on the board. RICBox is compatible with both the on-board USB-to-I2C bridge and the Aardvark adapter. RICBox uses a software wizard for entering the overall configuration and has several tools to fine tune the configuration (e.g., block diagram GUI).

The Bus Source connector J30 can be used to select the source of the communication bus. The bus will be I2C for most communication but can also be SPI for specific tests. Pins 1 and 2 in J30 are SDA and SCL from the FTDI chip. Pins 3 and 4 pass the SDA and SCL to the I2C level shifter. To use the on-board FTDI chip, install jumpers on pins 1-3 and 2-4. The board will be shipped with these jumpers installed. Theoretically, any I2C adapter can be connected to pins 3 and 4 for SDA and SCL. Pin 6 can be used as the ground connection for the I2C connection. Pins 3, 4, 5, and 6 are arranged such that an Aardvark connector can be plugged onto pins 3, 4, 5, and 6 only (see Figure 5).

The Bus Type connector J33 is added to allow bypassing the I2C Level Shifter in case the connection type is SPI. For default I2C operation, jumpers are installed on pins 1-3 and 2-4.

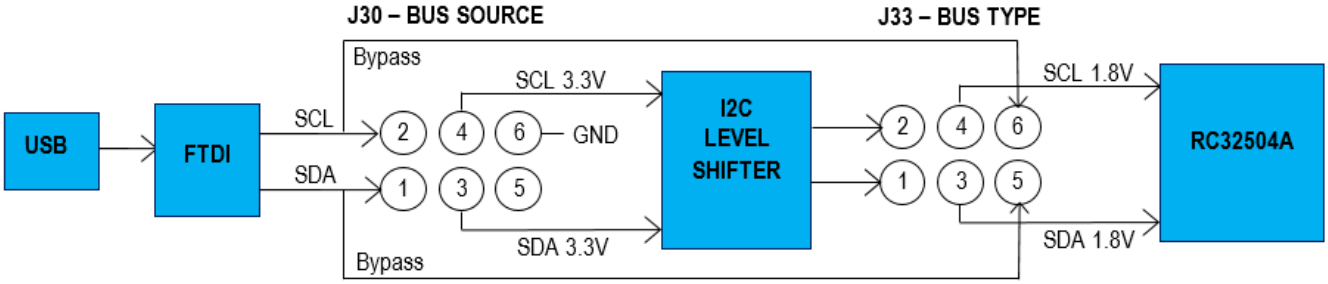



**Figure 4. Communication Path Block Diagram**

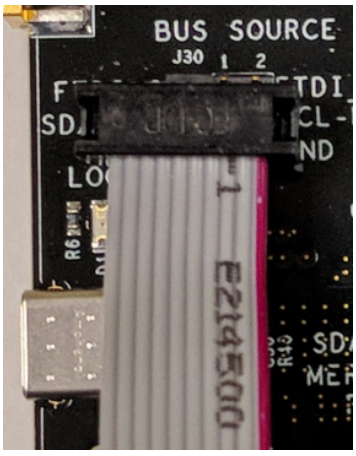



**Figure 5. Connect Aardvark Adapter to J30**

In Figure 14 the Aardvark adapter communicates with the RC32504A and the FTDI bridge chip is disconnected. USB can still be used to power the board.

## 1.2 Board Power Supply

The power source for each VDD pin can be selected with jumpers. The voltage for each pin, except one, is 1.8V. The exception is VDDD, which can be powered with 1.8V or 3.3V.

The power source can be either an on-board voltage regulator or the VDD_J jack. Most power source selectors have only two choices, 1.8V from the on-board 1.8V regulator or connect to the VDD_J J21 jack. The jack can connect to a bench supply; this connection can be useful, for example, to measure supply current into pins.

In Figure 2 the source for the pin VDDXO is chosen to be the on-board 1.8V regulator. The two pins on the bottom are both connected to the VDDXO pin through a power filter. The top left pin is connected to the on-board 1.8V regulator and the top right pin is connected to the VDD_J jack. `


**Figure 2. Power Source Selector Example**

In Figure 3 the source for the pin VDDD is chosen to be the on-board 3.3V regulator. J25 allows three choices for VDDD: 1.8V, 3.3V, or the VDD_J jack. The three pins on the right are all connected to the VDDD pin through a power filter. The top left pin is connected to the on-board 3.3V regulator, the mid left pin is connected to the on-board 1.8V regulator, and the bottom left pin is connected to the VDD_J Jack.


**Figure 3. Power Source Selector for VDDD**

## 1.3 Differential Output Termination Selectors

Each of the four differential output pairs can be programmed to LVDS, HCSL, or CMOS logic type. CMOS is a single-ended logic type and the output pair will essentially be two CMOS outputs of the same frequency. HCSL is the most versatile output because it can be customized. The HCSL driver is a current driver that simply turns a current on and off. Standard HCSL turns 15mA on and off to make 750mVpp swing in 50Ω termination.

The RC32504A HCSL driver can be programmed to drive 4mA to 19mA levels. When AC coupled, the HCSL driver can be compatible with LVDS, CML, and LVPECL signal swing requirements. Because of the output architecture, it needs a DC coupled termination to ground to drive the current into. The circuit at each output splits the termination into a DC part and an AC coupled RF part. The RF part is connected to the SMA edge connectors of each output and the DC part is controlled by the termination selectors.

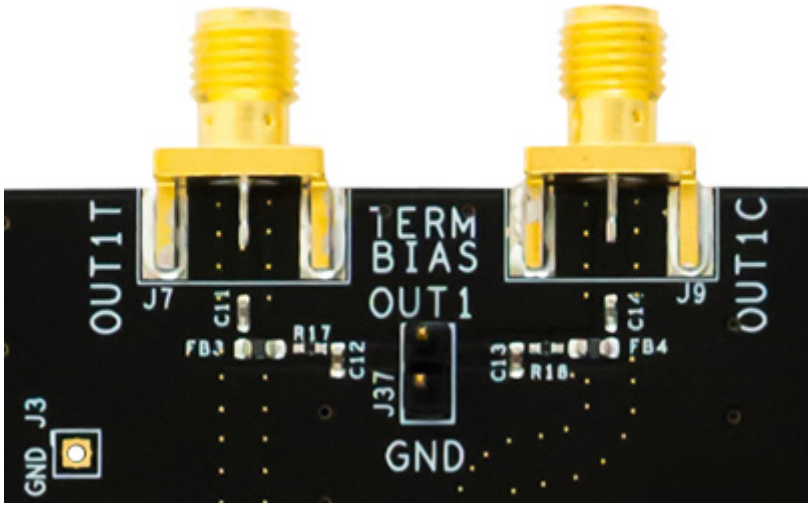



**Figure 4. Termination Bias Jumpers**

Figure 4 shows J36 for applying DC load to OUT0. When HCSL is selected and the on-chip termination is disabled, a jumper must be placed to provide the required DC load to ground. No jumper is needed for LVDS or LVCMOS, and when the on-chip termination is enabled with HCSL.

Separating DC load from AC coupled RF load helps increase the signal swing on the SMA connectors for better noise measurements. This method can also be used in the end application when the receiver input has on-chip termination, is AC coupled, and a large signal swing is required.

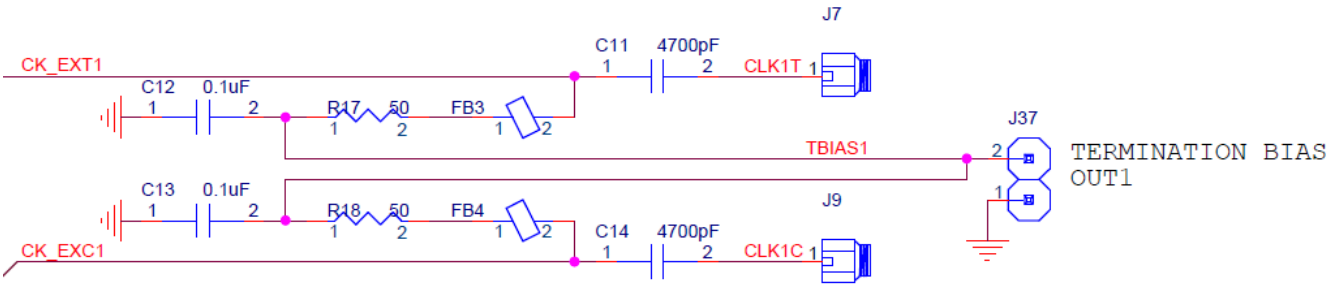



**Figure 5. Termination Bias Schematic**

## 1.4 Miscellaneous Selectors


**Figure 6. OE Pin Control**

J32 pins 2, 4, and 6 connect together to the OE pin of the RC32504A. Apply a jumper on pins 1 and 2 to pull the OE pin high or on 5 and 6 to pull the OE pin low. The RC32504A can be programmed to pull high or low on the chip so in most cases no jumpers are needed on J32.

A pull-up or pull-down jumper can also be used to latch a specific programmed configuration at power up.

When experimenting with SPI, a jumper can be applied to pins 3 and 4 to pass the CS (Chip Select) signal from the FTDI chip to the RC32504A.

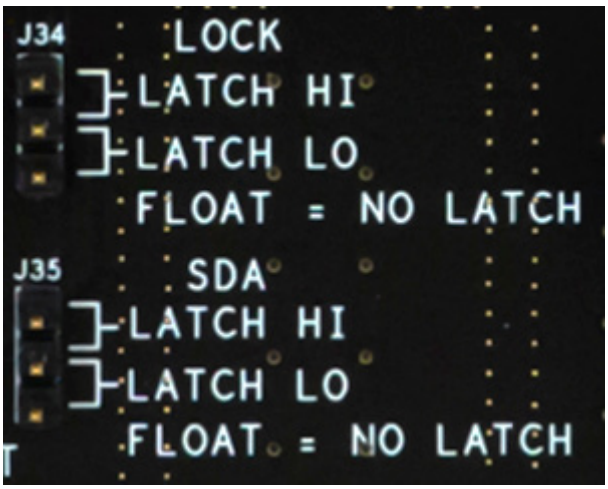



**Figure 7. Lock Pin and SDA Pin Latch Control**

J34 can be used to latch a specific level on the LOCK pin at power up. J35 can be used to latch a specific level on the SDA pin at power up.

Both are used to select a specific pre-programmed configuration. It is not needed to program OTP of the RC32504A on the evaluation board. Every possible configuration can be set up with RICBox in volatile registers. It is not recommended to attempt to program the OTP memory because of the risk that a mistake or error can destroy the chip.

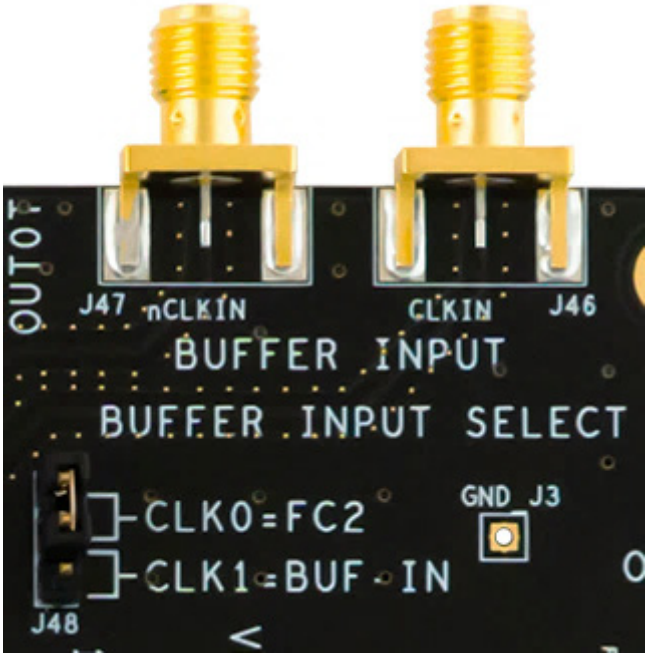



**Figure 8. Buffer Input Select**

J48 can be used to select the input source for the 8P34S1208I fan-out buffer. The CLK0 input pair on the buffer is connected to OUT0 of the FemtoClock 2, and the CLK1 input pair is connected to SMAs J46 and J47. By default, the jumper is on CLK0 for passing OUT0 of FC2 through the buffer. Changing the jumper to CLK1 and

another output can be passed through the buffer by connecting a pair of coax cables from that output to the buffer input SMA pair.

The CLK0 input is DC coupled to OUT0 on FC2 to demonstrate a connection with minimum components. OUT0 on FC2 must be configured as LVDS for this to work properly. The 8P34S1208I is an LVDS fan-out buffer.

The CLK1 input is AC coupled, using the buffer VREF for DC bias, to make that input compatible with any differential swing applied to the buffer input SMA pair.

## 1.5 On-Board Crystal

The evaluation board is assembled with a crystal. The default frequency for the crystal is 60MHz but Renesas can ship the board with a different crystal frequency to better match the specific application where the RC32504A will be used. The default 60MHz crystal is best suited for jitter attenuator applications. Synthesizer applications with output frequencies like 156.25MHz or 312.5MHz work better with a 62.5MHz crystal, or even better, with a 78.125MHz crystal. The crystal footprint U1 has a universal shape to allow assembly of 3.2 × 2.5 mm and 2.5 × 2.0 mm size crystals.

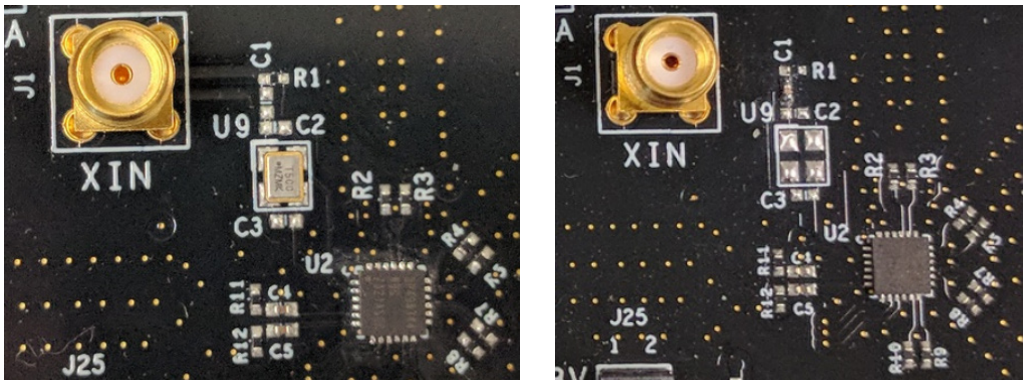



**Figure 9. Crystal and XIN Input**

## 1.6 Bypassing the Fan-Out Buffer at OUT0

Remove R60 and place at R59. Also remove R61 and place R58. The red rectangles are the new positions. These two resistors are 0Ω and the change will route the OUT0 clock to the J4 and J6 SMA connectors as opposed to the fan-out buffer input in the R60 and R61 positions.

When the fan-out buffer is not used, it is a good idea to remove jumper J49 (VDDFO) to remove power from the fan-out buffer.

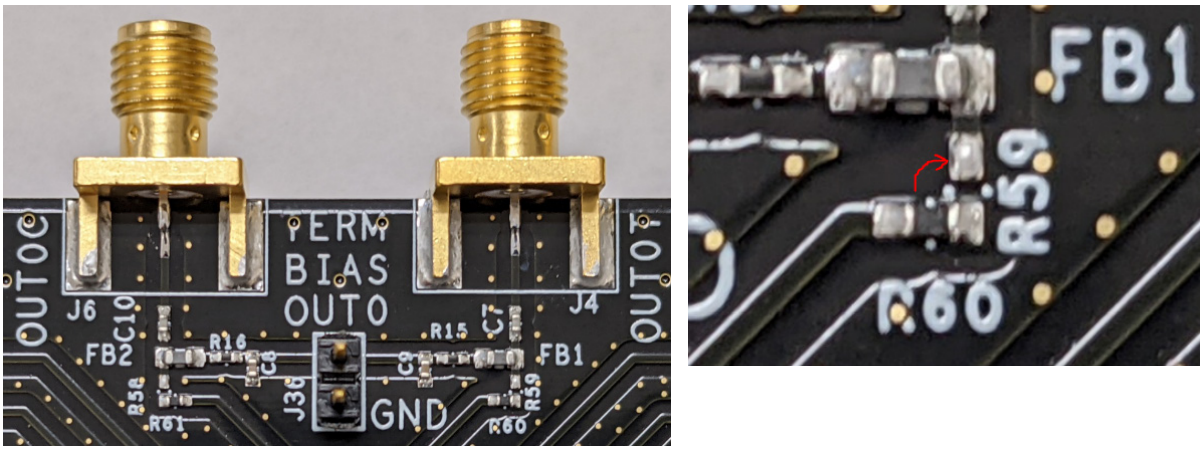
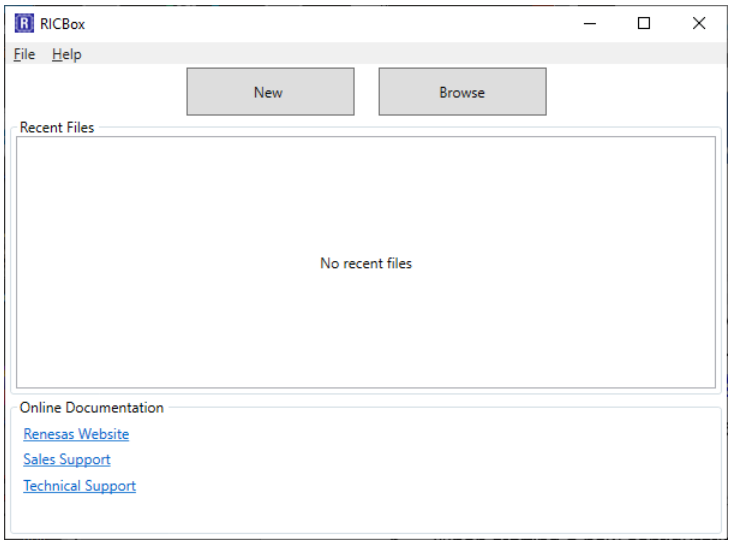



**Figure 10. OE Pin Control**

## 1.7 Setup and Configuration

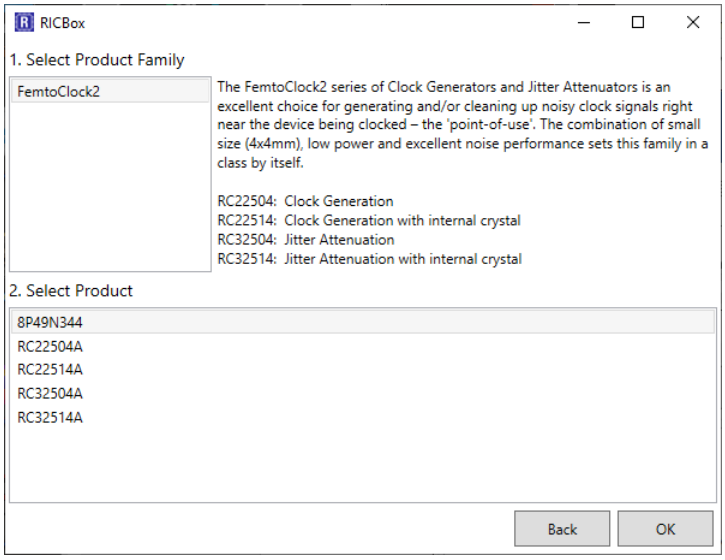
Complete the following steps to set up the RC32504A / RC22504A EVB using I2C and start the configuration of the board.

1. Connect J31 to a USB port of the user's computer using the USB cable supplied with the board.
2. Launch Renesas' *RICBox Software* according to the instructions in the *FemtoClock 2 RICBox User Guide*. The software and guide are downloadable from the RC32504A product page.
3. Following the "Getting Started" steps in the *RICBox Software*, an I2C connection is established between the GUI software and the RC32504A.
4. Open an existing settings file (click Browse) or start a new configuration (click New).



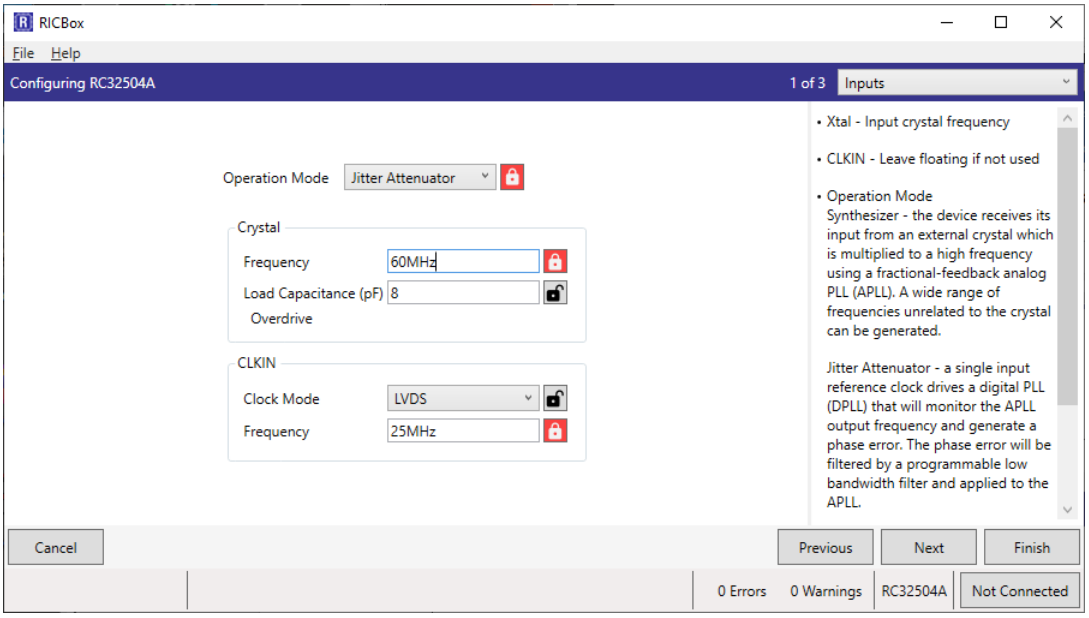

Configurations that were saved recently will show in the "Recent Files" box. Double-click on a file to load the configuration.

5. When starting a new configuration, the software first needs to know what product family to load the "Virtual Environment" for:



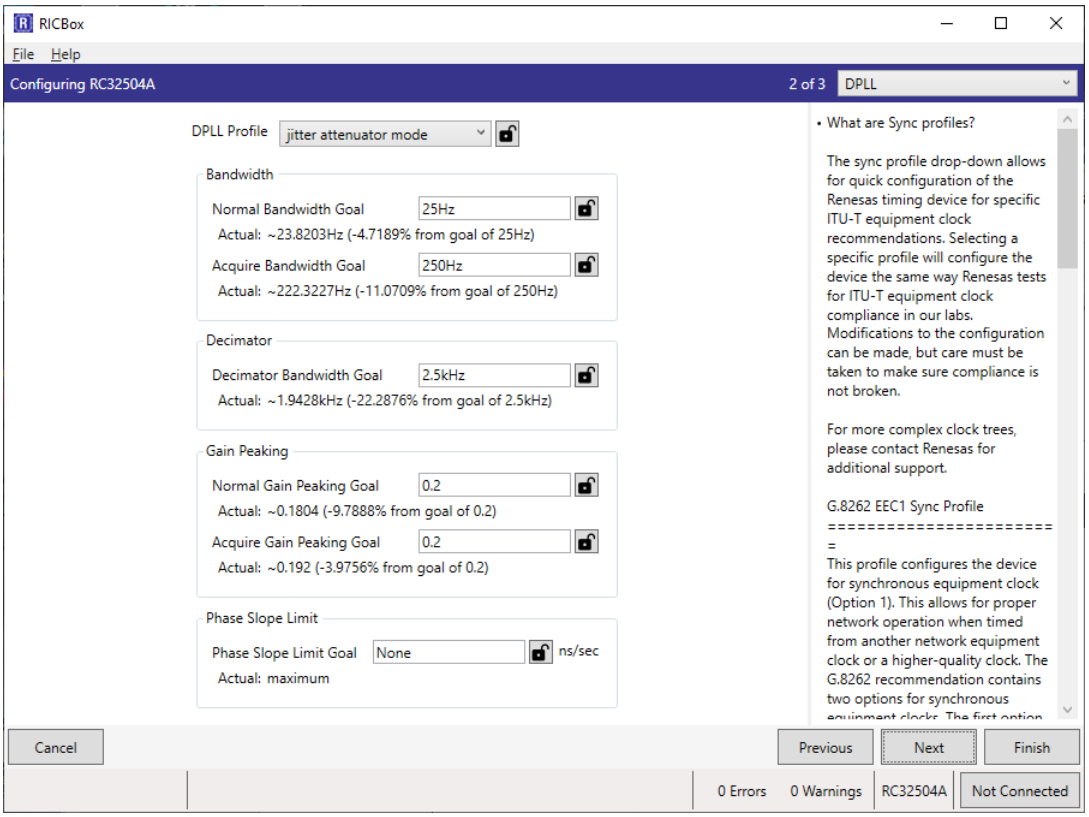

This screen shows only FemtoClock 2 but it is possible to install multiple Virtual Environments for various product families. At item 1, select FemtoClock 2 then select the specific product at item 2 and click "OK".

6. Select the “Operation Mode”: Synthesizer or Jitter Attenuator.

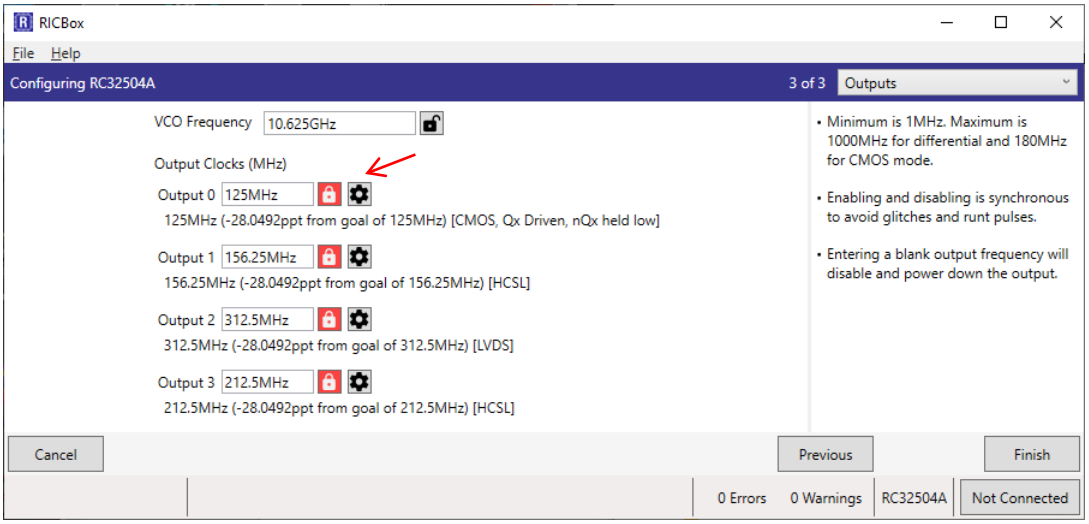



On the right are explanations and instructions. Click “Next” to go to the next screen.

7. Screen 2 has a list of Jitter Attenuator settings.



8. Screen 3 sets up the outputs.

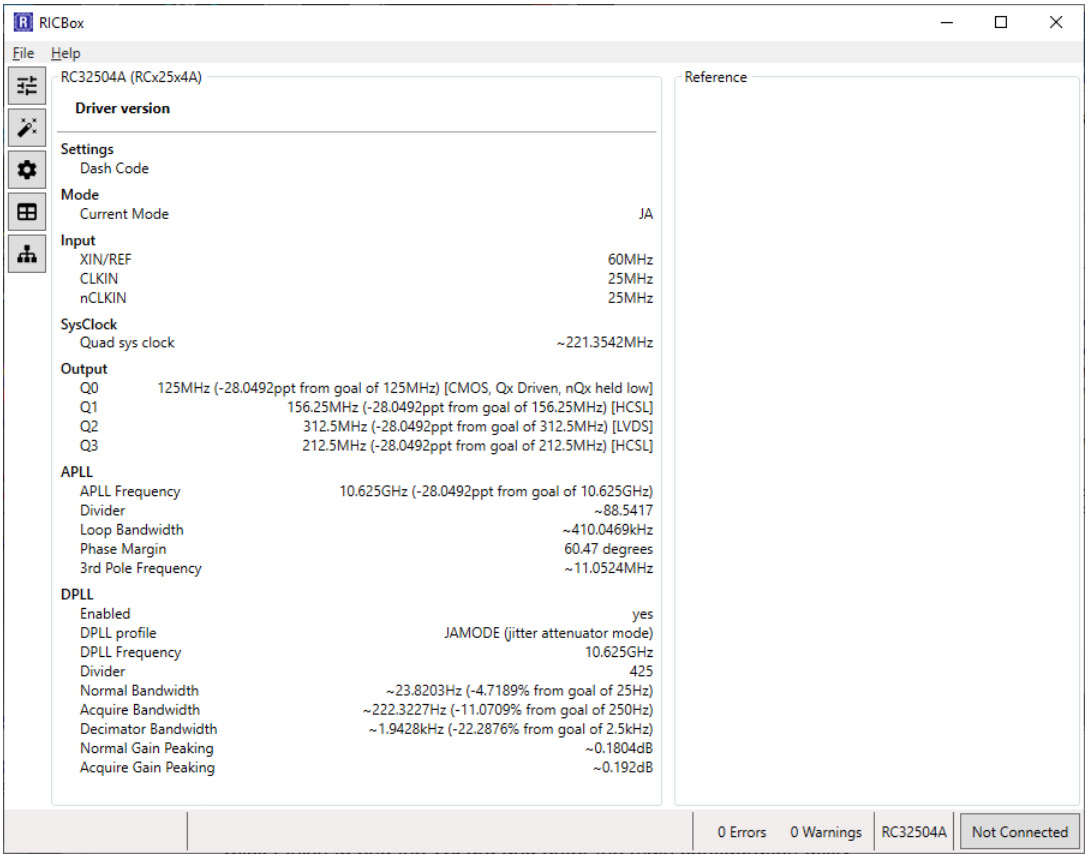



a. Fill in the desired output frequencies. Leave blank unused outputs.

b. Click on “Advanced Settings” at the red arrow to select Logic Type and Signal Amplitude.

c. Click “Finish” to end the Wizard and enter the main configuration utility.

9. The main configuration utility.

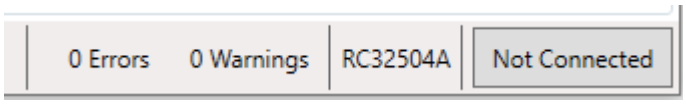



The buttons on the top left are Control Panel (the above screen), Wizard, Configuration, Registers, and Block Diagram.

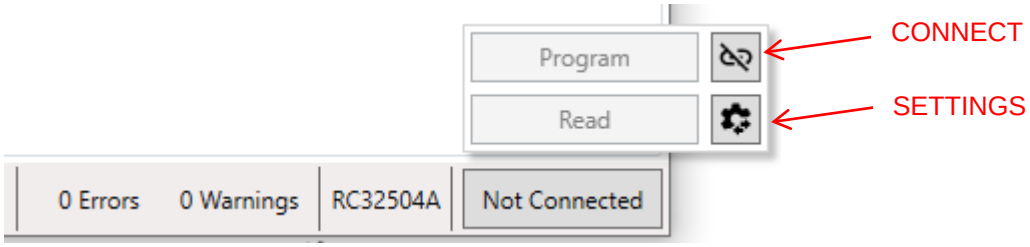
For more information, see the *FemtoClock 2 RICBox User Guide* located on the RC32504A product page.

10. Transfer the Configuration from RICBox into the FemtoClock 2 device:

    The bottom right of the screen has buttons to control the I2C connection with the device.

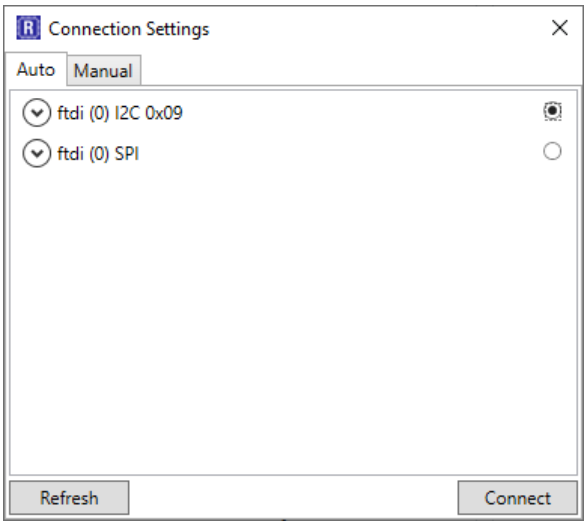



a. Click the “Not Connected” button to connect.



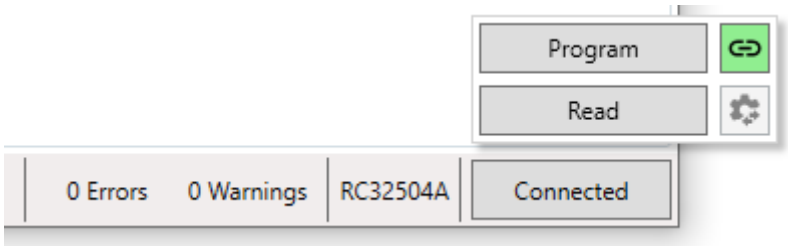

b. Click the small button to the right of “Program” to connect.

   The small button next to “Read” opens I2C settings and starts a search for connected devices.




The “Connection Settings” screen allows you to select a specific device and Connect.

After attempting to Connect:




The small Connect button turns green to indicate that the connection was successful. Now click “Program” to transfer all settings to the device.

# 2. Board Design

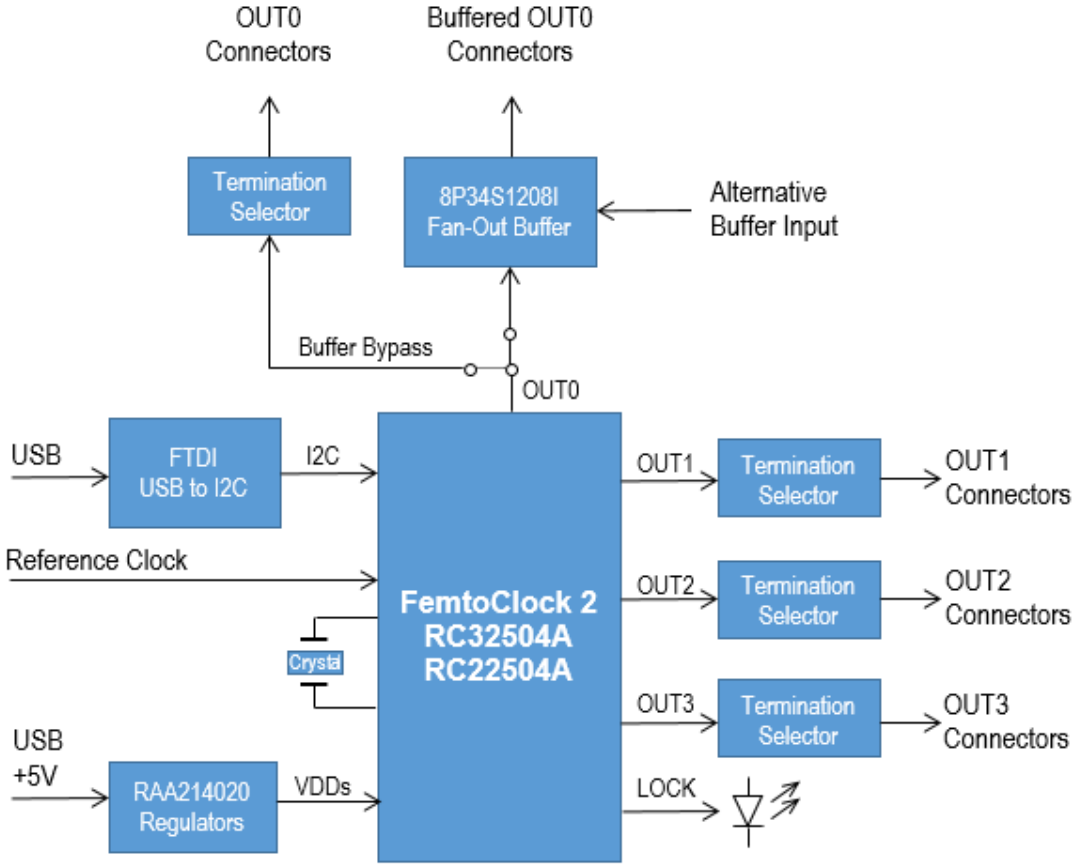



**Figure 11. RC32504A / RC22504 EVB – Block Diagram**

Each differential output clock is available on a pair of SMA connectors. Each pair of SMA connectors is AC coupled on the board. The termination selector can provide a DC path to ground for the HCSL output type when the on-chip termination is disabled.

Power is provided through the USB connection and regulated with RAA214020 low noise LDOs. Each power pin can also be switched to a banana plug jack for supply current measurements or other tests.

The board has an FTDI USB-to-I2C bridge for programming FemtoClock 2 from a computer. Renesas RICBox software is available for easy development of configurations and uploading these configurations to the FemtoClock 2 device.

To demonstrate the use of FemtoClock 2 with fan-out buffers, an 8P34S1208I is added at OUT0 of FemtoClock 2. When the buffer is not desired, the board can be easily modified by moving two 0Ω resistors to pass OUT0 to its own pair of SMA connectors, just like the other outputs. The buffer has one of its two inputs connected to OUT0 and the other connected to an SMA pair so the buffer can always be used to pass a clock from any output through a pair of coax cables.

The LOCK pin drives an LED and the LED lights up when the pin is high. Default function assigned to the LOCK pin is “APLL Lock” so the LED shows if the APLL is locked or not. Several other status items can be assigned to the LOCK pin.

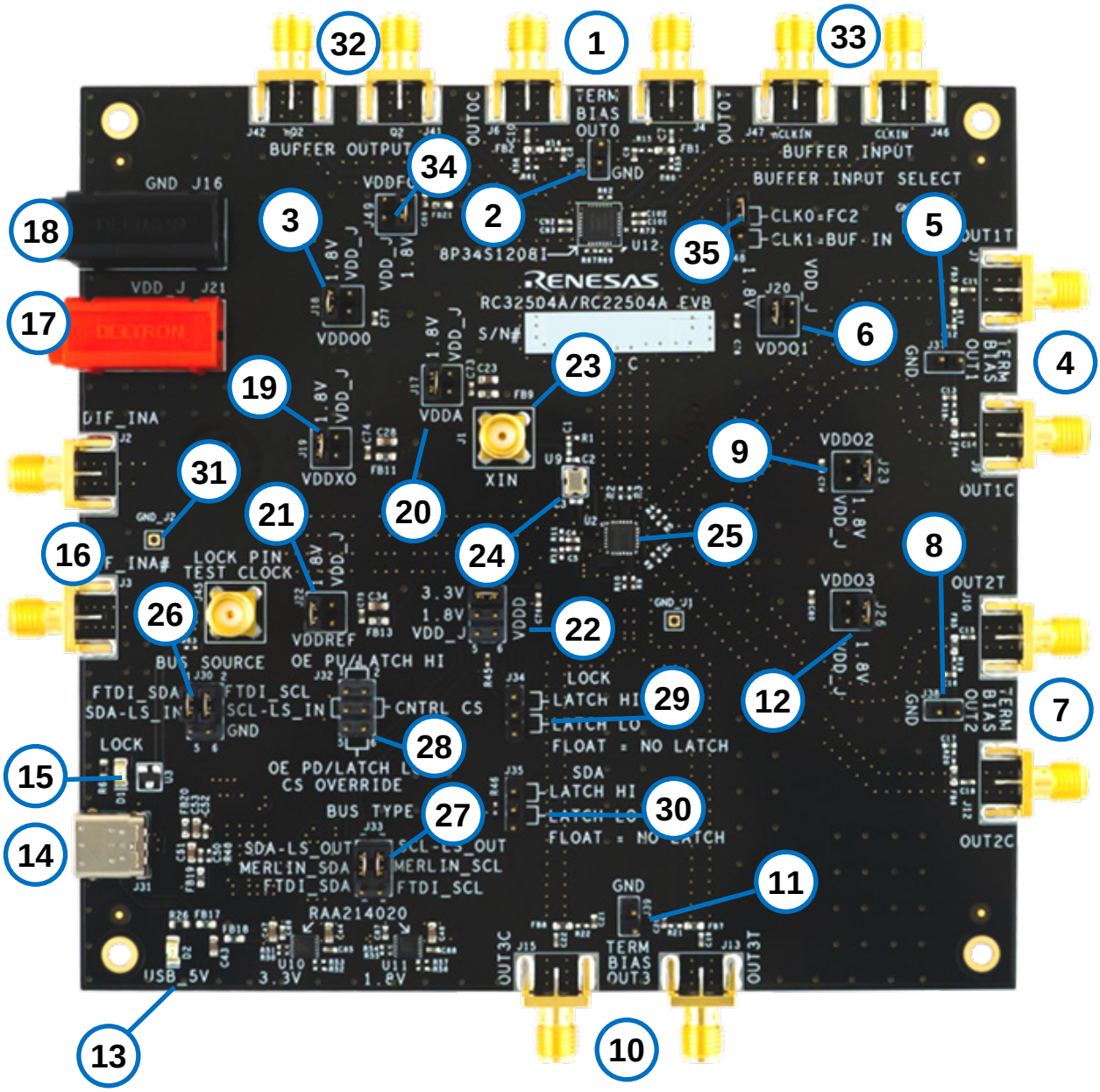



**Figure 12. RC32504A / RC22504A Board – Top View**

**Table 1. RC32504A / RC22504A – EVB Pins and Functions**

Note: See Figure 12 for reference numbers in the following table.

| Ref. | Name | On-Board Connector Label | Function |
|---|---|---|---|
| 1 | Output 0 | J4, J6 | Differential Clock Output 0 (not active with typical assembly) |
| 2 | Termination 0 | J36 | Termination Selector for Output 0 (not active with typical assembly) |
| 3 | VDDO0 | J18 | Power Source Selector for pin VDDO0 |
| 4 | Output 1 | J7, J9 | Differential Clock Output 1 |
| 5 | Termination 1 | J37 | Termination Selector for Output 1 |
| 6 | VDDO1 | J20 | Power Source Selector for pin VDDO1 |

| Ref. | Name | On-Board Connector Label | Function |
|---|---|---|---|
| 7 | Output 2 | J10, J12 | Differential Clock Output 2 |
| 8 | Termination 2 | J38 | Termination Selector for Output 2 |
| 9 | VDDO2 | J23 | Power Source Selector for pin VDDO2 |
| 10 | Output 3 | J13, J15 | Differential Clock Output 3 |
| 11 | Termination 3 | J39 | Termination Selector for Output 3 |
| 12 | VDDO3 | J26 | Power Source Selector for pin VDDO3 |
| 13 | LED_5V | D2 | LED lights when 5V USB Supply is present |
| 14 | USB Interface | J31 | USB-C Type Jack for connection with the user's computer and interaction with Renesas RICBox Software. |
| 15 | LOCK LED | D1 | LED lights up LOCK pin goes high. Default the LOCK pin signals APLL locking. |
| 16 | DIF_IN | J2, J3 | Differential Reference Clock Input |
| 17 | Power VDD Jack | J21 | External Power Supply, Positive Terminal |
| 18 | Power GND Jack | J16 | External Power Supply, Negative Terminal or Ground |
| 19 | VDDXO | J19 | Power Source Selector for pin VDDXO (Crystal Oscillator Power) |
| 20 | VDDA | J17 | Power Source Selector for pin VDDA (Analog Power) |
| 21 | VDDREF | J22 | Power Source Selector for pin VDDREF (Ref Clock Input Power) |
| 22 | VDDD | J25 | Power Source Selector for pin VDDD (Digital Power) |
| 23 | XIN | J1 | Overdrive XIN pin with External Clock |
| 24 | Crystal | U9 | Quartz Crystal |
| 25 | RC32504A | U2 | Evaluation Device. The RC32504A can also demonstrate RC22504A functionality. |
| 26 | Bus Source | J30 | Select Communication Bus Source |
| 27 | Bus Type | J33 | Select Communication Bus Type |
| 28 | OE / SPI CS | J32 | OE pin Pull-Up / -Down or Latch High / Low or Pass SPI Chip Select |
| 29 | LOCK Latch | J34 | Lock pin Latch High / Low |
| 30 | SDA Latch | J35 | SDA pin Latch High / Low |
| 31 | GND | GND_J1/2/3/4 | Miscellaneous Ground Points |
| 32 | OUT0 Buffer Output | J41, J42 | Differential Fan-Out Buffer Output |
| 33 | 2nd Buffer Input | J46, J47 | Alternative Fan-Out Buffer Input |
| 34 | VDDFO | J49 | Power Source Selector for 8P34S1208I Fan-Out Buffer |
| 35 | Buffer Input Select | J48 | Select between CLK0 = FemtoClock 2 OUT0 and CLK1 = Buffer Input SMA pair. |

## 2.1 Schematic Diagrams

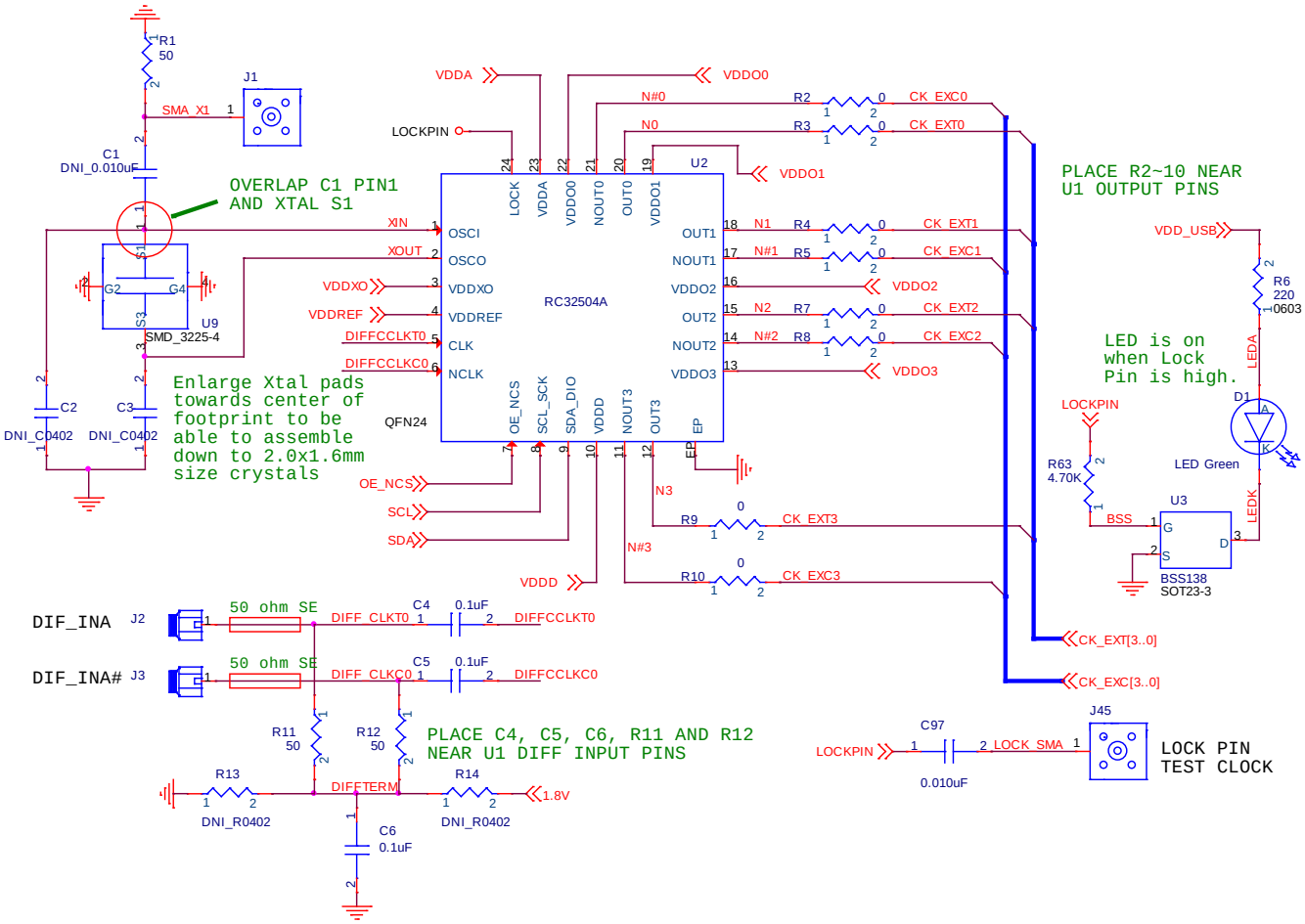



**Figure 13. RC32504A Evaluation Board Schematics – Page 1**

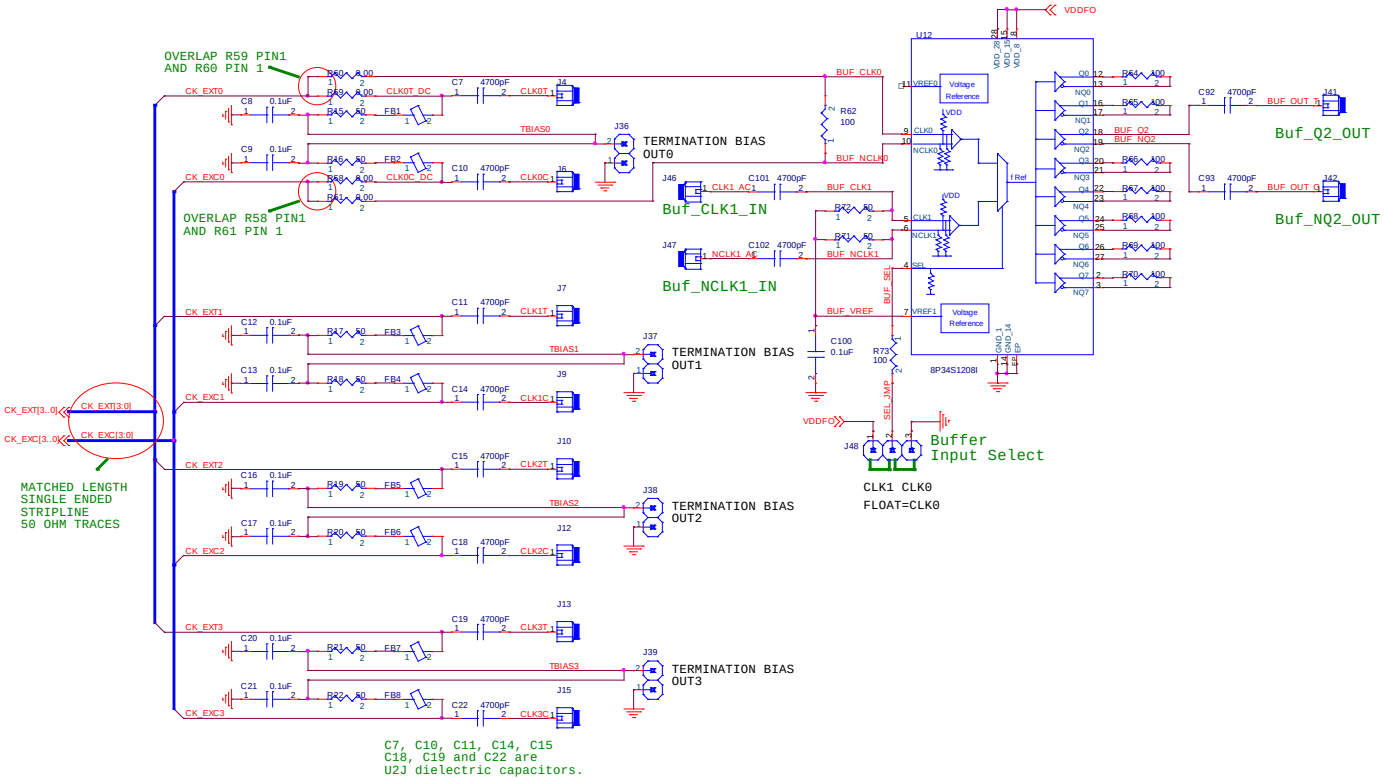



**Figure 14. RC32504A Evaluation Board Schematics – Page 2**

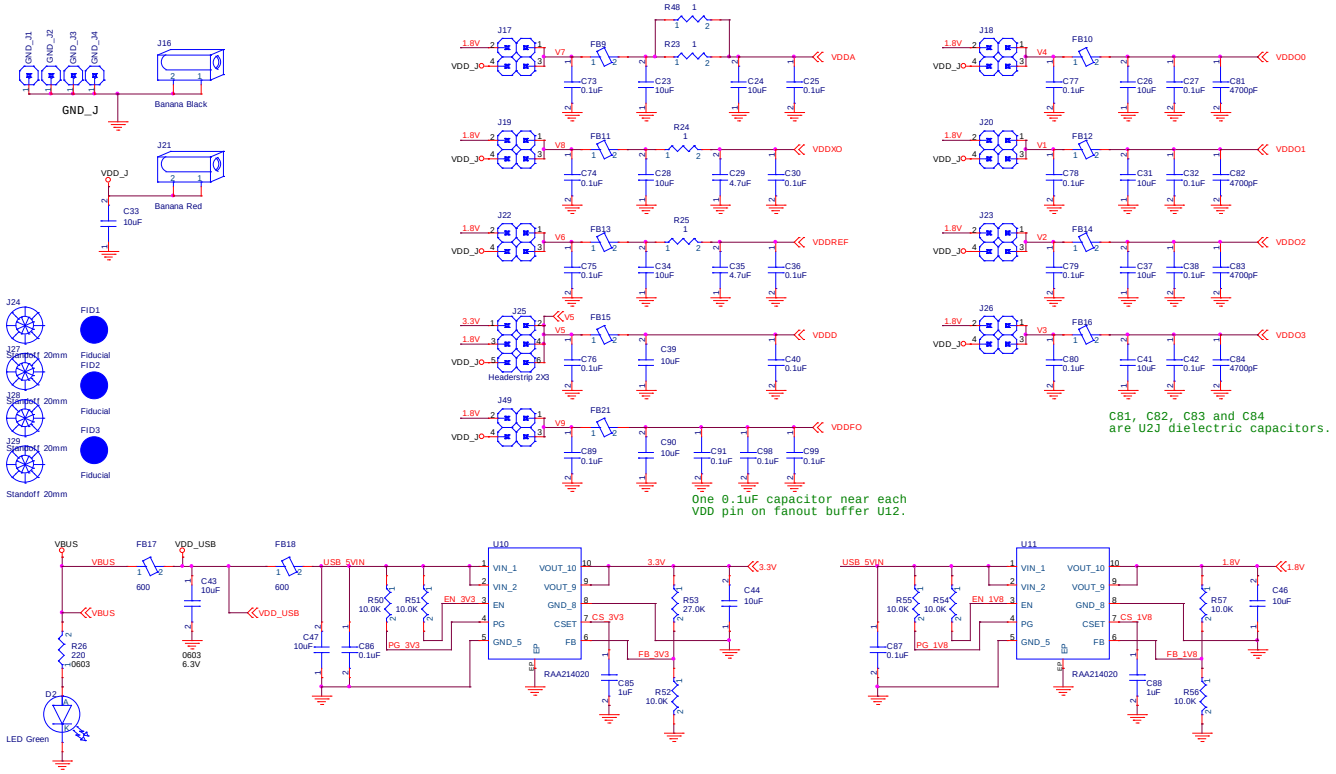



**Figure 15. RC32504A Evaluation Board Schematics – Page 3**

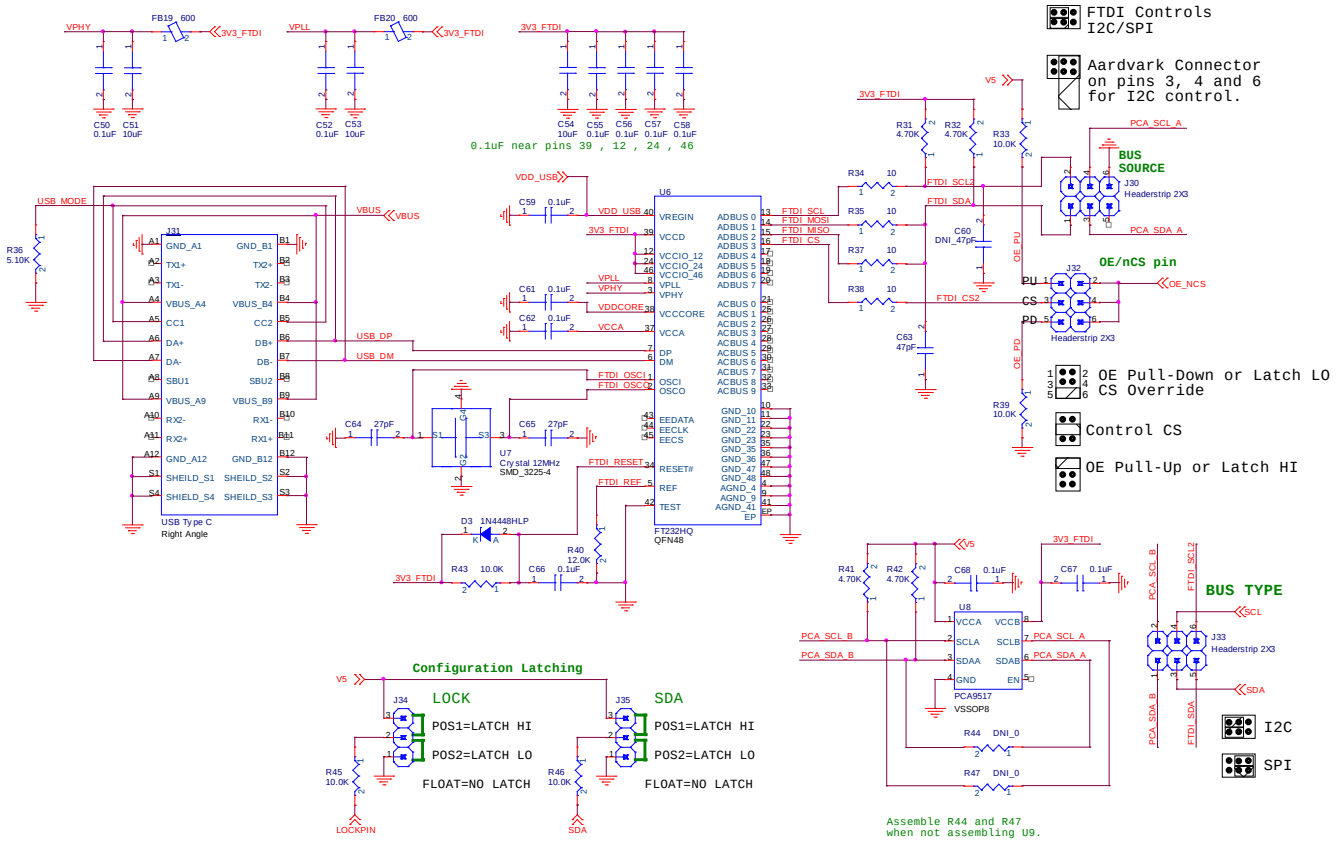



**Figure 16. RC32504A Evaluation Board Schematics – Page 4**

## 2.2 Bill of Materials

| Item | Qty | Reference | Value | Part Number | Manufacturer |
|---|---|---|---|---|---|
| 1 | 1 | C1 | DNI_0.010uF | GRM155R71E103J | |
| 2 | 2 | C2,C3 | DNI_C0402 | DNI_C0402 | |
| 3 | 46 | C4,C5,C6,C8,C9,C12,C13,C16,C17,C20,C21,C25,C27,C30,C32,C36,C38,C40,C42,C50,C52,C55,C56,C57,C58,C59,C61,C62,C66,C67,C68,C73,C74,C75,C76,C77,C78,C79,C80,C86,C87,C89,C91,C98,C99,C100 | 0.1uF | GRM155R71C104KA88D | Murata Electronics |
| 4 | 16 | C7,C10,C11,C14,C15,C18,C19,C22,C81,C82,C83,C84,C92,C93,C101,C102 | 4700pF | GRM1557U1A472JA01D | Murata Electronics |
| 5 | 18 | C23,C24,C26,C28,C31,C33,C34,C37,C39,C41,C43,C44,C46,C47,C51,C53,C54,C90 | 10uF | GRM188D70J106MA73D | Murata Electronics |
| 6 | 2 | C29,C35 | 4.7uF | ZRB15XR61A475ME01 | |
| 7 | 1 | C60 | DNI_47pF | GRM1555C1E470J | Murata Electronics |
| 8 | 1 | C63 | 47pF | GRM1555C1E470J | Murata Electronics |
| 9 | 2 | C64,C65 | 27pF | GRM1555C1E270J | Murata Electronics |

| Item | Qty | Reference | Value | Part Number | Manufacturer |
|---|---|---|---|---|---|
| 10 | 2 | C85,C88 | 1uF | GCM155C71A105KE38D | Murata Electronics |
| 11 | 1 | C97 | 0.010uF | GRM155R71E103J | Murata Electronics |
| 12 | 2 | D1,D2 | LED Green | APT3216CGCK | |
| 13 | 1 | D3 | 1N4448HLP | 1N4448HLP | |
| 14 | 21 | FB1,FB2,FB3,FB4,FB5,FB6,FB7,FB8,FB9,FB10,FB11,FB12,FB13,FB14,FB15,FB16,FB17,FB18,FB19,FB20,FB21 | 600 | BLM18AG601SN1D | Murata |
| 15 | 3 | FID1,FID2,FID3 | Fiducial | Fiducial DNI | |
| 16 | 4 | GND_J1,GND_J2,GND_J3,GND_J4 | DNI Headerstrip 1X1 | DNI 1x1 | |
| 17 | 2 | J1,J45 | SMA_JACK_STR_50 | 733910070 | Molex |
| 18 | 14 | J2,J3,J4,J6,J7,J9,J10,J12,J13,J15,J41,J42,J46,J47 | Cinch_142_0701_851 | 142_0701_851 | Johnson |
| 19 | 1 | J16 | Banana Black | 571-0100 | |
| 20 | 8 | J17,J18,J19,J20,J22,J23,J26,J49 | Header 2X2 | 499-10-202-10-009000 | |
| 21 | 1 | J21 | Banana Red | 571-0500 | |
| 22 | 4 | J24,J27,J28,J29 | Standoff 20mm | R30-1612000 | |
| 23 | 4 | J25,J30,J32,J33 | Headerstrip 2X3 | 10897062 | Molex |
| 24 | 1 | J31 | USB Type C | 12401598E4#2A | Amphenol |
| 25 | 3 | J34,J35,J48 | Headerstrip 1X3 | 22-28-4035 | Molex |
| 26 | 4 | J36,J37,J38,J39 | Headerstrip 1X2 | 22-28-4023 | Molex |
| 27 | 11 | R1,R15,R16,R17,R18,R19,R20,R21,R22,R71,R72 | 50 | ERA-2AEB49R9X | Panasonic |
| 28 | 8 | R2,R3,R4,R5,R7,R8,R9,R10 | 0 | ERJ-2GE0R00 | Panasonic |
| 29 | 2 | R6,R26 | 220 | CRCW0603220RFK | Vishay |
| 30 | 2 | R11,R12 | DNI_50 | ERA-2AEB49R9X | Panasonic |
| 31 | 2 | R13,R14 | DNI_R0402 | DNI_R0402 | |
| 32 | 4 | R23,R24,R25,R48 | 1 | RC0402FR-071RL | Yageo |
| 33 | 5 | R31,R32,R41,R42,R63 | 4.70K | CRCW04024K70FK | Vishay |
| 34 | 12 | R33,R39,R43,R45,R46,R50,R51,R52,R54,R55,R56,R57 | 10.0K | RCG040210K0FK | Yageo |
| 35 | 4 | R34,R35,R37,R38 | 10 | RC0402FR-0710RL | Yageo |
| 36 | 1 | R36 | 5.10K | CRCW04025K10FK | Vishay |
| 37 | 1 | R40 | 12.0K | CRCW040212K0FK | Vishay |

| Item | Qty | Reference | Value | Part Number | Manufacturer |
|---|---|---|---|---|---|
| 38 | 2 | R44,R47 | DNI_0 | ERJ-2GE0R00 | Panasonic |
| 39 | 1 | R53 | 27.0K | CRCW040227K0FK | Vishay |
| 40 | 2 | R58,R59 | DNI_0.00 | ERJ-2GE0R00 | Panasonic |
| 41 | 2 | R60,R61 | 0 | ERJ-2GE0R00 | Panasonic |
| 42 | 9 | R62,R64,R65,R66,R67,R68,R69,R70, R73 | 100 | CRCW0402100RFK | Vishay |
| 43 | 1 | U2 | RC32504A | RC32504A | Renesas |
| 44 | 1 | U3 | BSS138 | BSS138 | On Semi |
| 45 | 1 | U6 | FT232HQ | FT232HQ-REEL | FTDI |
| 46 | 1 | U7 | Crystal 12MHz | ABM8G-12.000MHZ-18-D2Y-T | Abracon |
| 47 | 1 | U8 | PCA9517 | PCA9517 | Texas Instruments |
| 48 | 1 | U9 | Crystal 50MHz | EXS00A-CG03550 | NDK America |
| 49 | 2 | U10,U11 | RAA214020 | RAA214020 | Renesas |
| 50 | 1 | U12 | 8P34S1208I | 8P34S1208I | Renesas |

# 3. Ordering Information

| Part Number | Description |
|---|---|
| RC32504A-EVK | RC32504A / RC22504A Evaluation Board; A-male to USB-C cable. |

# 4. Revision History

| Revision | Date | Description |
|---|---|---|
| 1.0 | Apr 21, 2021 | Initial release. |

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