ISL9122AIIN-EVZ, ISL9122AIRN-EVZ

The ISL9122AIIN-EVZ and ISL9122AIRN-EVZ platform allows quick evaluation of the high-performance features of the ISL9122A buck-boost regulator. The ISL9122A is a highly integrated non-inverting buck-boost switching regulator that accepts input voltages both above or below the regulated output voltage. It features an extremely low quiescent current consumption, excellent efficiency and an I^2C interface that allows you to access its internal registers, for output voltage and operation mode control.

Features

- Small, compact design
- I^2C interface for programmable V_{OUT}, slew rate and various operation modes (Forced Bypass, Auto-PFM, Forced PWM)
- Connectors, test points, and jumpers for easy probing

Specifications

The boards are designed to operate at the following operating conditions:

- Input voltage rating from 1.8V to 5.5V
- Programmable output voltage range of 1.8V to 5.375V and selectable transition slew rate through I^2C interface
- Up to 500mA output current (V_{IN} > V_{OUT} > 2.5V)
- Operating temperature range: -40°C to +85°C

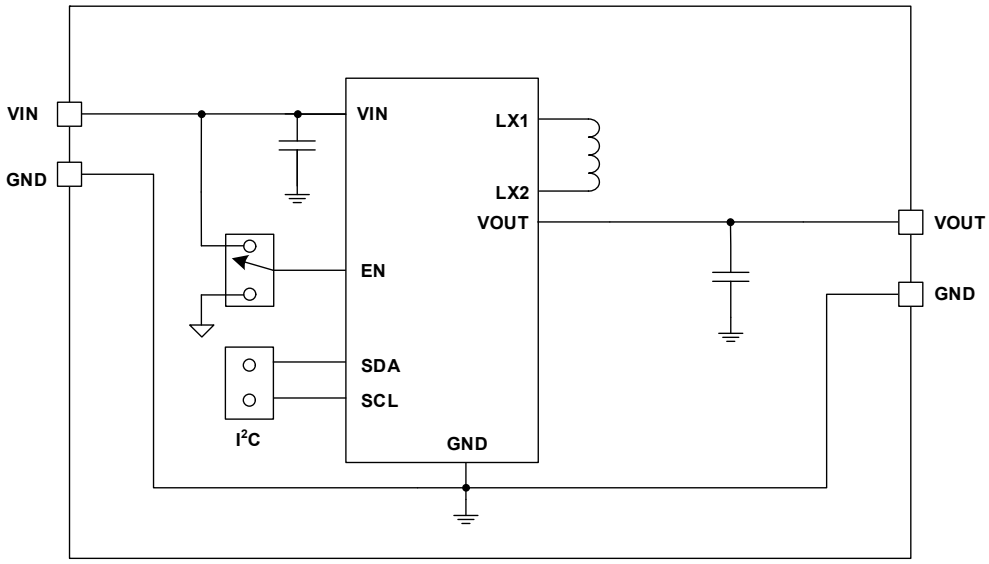

Figure 1. ISL9122AIIN-EVZ, ISL9122AIRN-EVZ Block Diagram

Contents

1. Functional Description

The ISL9122AIIN-EVZ and ISL9122AIRN-EVZ evaluation boards provide a simple platform to evaluate the feature-rich ISL9122A buck-boost regulator. Both boards have a 3.3V output after start-up and an output voltage that can be programmed by I^2C. Each evaluation board is optimized to best perform with the ISL9122A IC series. The input power and load connections are provided through multi-pin connectors for high-current operations.

The evaluation boards are shown in Figure 5 and Figure 6. Table 1 lists the test points and jumpers for the boards. The ISL9122A internal registers can be accessed by I^2C through the on-board jumper header J5, and its mode control register configures the part into the various operation modes. See the Evaluation Software Installation and Use to configure the board output voltage and operation modes.

Table 1. Description of Test Points and Jumpers

Test Points	Description
J1	Header for connecting input power
J2	Header for connecting external load
J4	Header for the EN pin J4 = GND disables the part output; J4 = V_{IN} enables the part output
J5	Header for connecting I^2C interface
J1 S+/S-	V_{IN} Kelvin connection for efficiency measurements
J2 S+/S-	V_{OUT} Kelvin connection for efficiency measurements
TP1	Through Hole Mount PCB test point for LX1 (Input side of power inductor)
TP2	Through Hole Mount PCB test point for LX2 (Output side of power inductor)
TP3	Through Hole Mount PCB test point for VOUT
TP4	Single Turret Terminal test point for VIN
TP5	Single Turret Terminal test point for VOUT
TP6	Single Turret Terminal test point for GND
TP7	Single Turret Terminal test point for GND

1.1 Operating Characteristics

The V_{IN} range of the boards is 1.8V to 5.5V while the adjustable V_{OUT} range is 1.8V to 5.375V. The I_{OUT} range of the boards is 0 to 500mA. The operating ambient temperature range is -40°C to +85°C.

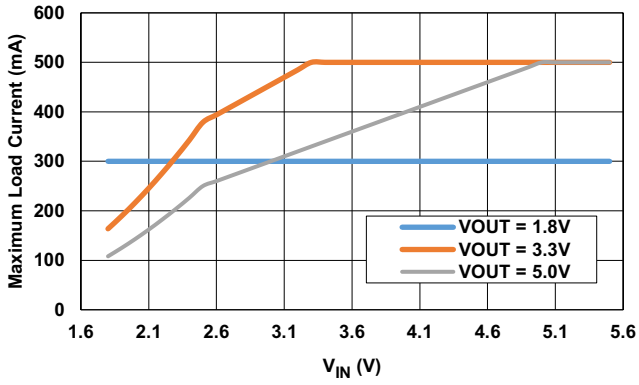

Figure 2. Maximum Load Current vs Input Voltage

1.2 Setup and Configuration

For both evaluation boards, the default output voltage is set at 3.3V. Use the following procedures to configure and power-up the board for proper operation. During the power-on process, the expected waveforms are shown in Figure 3.

1. Connect the power supply to J1, with voltage setting between 1.8V and 5.5V.
2. Connect the electronic load to J2.
3. Place the scope probes on VOUT test point and other test points of interest.
4. Ensure that the EN pin jumper (J4) is pulled up to V_{IN}.
5. Turn on the power supply. At the end of the soft start sequence, the ISL9122A is operating in Regulation mode by default with V_{OUT} = 3.3V. **Note**: A minimum effective output capacitance of 6µF is required. Therefore, depending on the performance specifications of the capacitor, an additional output capacitor might be required for higher output voltage settings.
6. Monitor the output voltage start-up sequence on the scope. The waveforms should look similar to those shown in Figure 3.
7. Turn on the electronic load.
8. Measure the output voltage with the voltmeter. The voltage should regulate within the datasheet specification limits.
9. To determine efficiency, measure input and output voltages at the Kelvin sense test points (S+ and S-), which are part of J1 and J2 headers. The bench power supply can be connected to the VIN and GND headers on J1. The electronic load can be connected to the VOUT and GND headers on J2. Measure the input and output currents. Calculate the efficiency based on these measurements.

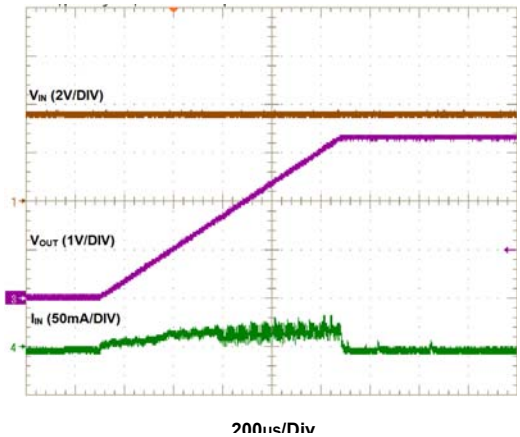

Figure 3. ISL9122A Start-Up with V_{IN} = 3.6V and V_{OUT} = 3.3V

1.3 Evaluation Software Installation and Use

The ISL9122 evaluation software and evaluation software guide are available for download from the Renesas website.

10. Save the evaluation software executable file and install the evaluation software (refer to the evaluation software manual). When the evaluation software launches, (refer to the Setup and Configuration and) connect the power supply, DC load, and other test equipment to the evaluation board; next, apply power.
11. The ISL9122A has five control registers. See the ISL9122 datasheet for detailed register descriptions.
12. Register **RO_REG1** (Address: 0x02) provides chip identification information. The **Get IC INFO_RO_REG1** button reads from this read-only register.
13. To change the output voltage, you can use the **VSET Control** slider in the **VSET** register (Address: 0x11) panel and perform a Write REG operation. The output voltage ramps up at the slew rate specified in the **DVSRATE**

setting of **CONV_CFG** register. If the modified output voltage is lower than the initial value, its ramp down rate depends on the applied load and output capacitance. The **Read REG** button provides the contents of the register, so adjust the slider accordingly.

14. Register **INTFLG_REG** (Address: 0x03) contains the fault flags. The background color changes from green to red: when (1) a fault occurs, and (2) this register is read using either the **Check Fault** button or the **READ ALL** button. Each bit is set by a fault event and cleared when read. When the bit is cleared after reading, the background color changes from red back to green.
15. Register **CONV_CFG** (Address: 0x12) contains crucial converter configuration bits. Selecting the **Write** (or **Read)** button writes (or reads) the entire **CONV_CFG** register in one go.
16. Use **EN_AND** bit to disable the converter through I^2C by toggling the **Soft Start EN_AND** button from **Soft Start enabled** to **Soft Start inhibit**.
17. Selecting the **Soft DSCHG enabled** button presents a soft discharge resistor on the output pin, when the converter is disabled through I^2C using the EN_AND bit and VIN is still HIGH. By default, the **Soft DSCHG disabled** button is selected.
18. Use the **DVSRATE** drop-down list to modify the dynamic voltage scaling rate for voltage ramp up, when output voltage is modified using the **VSET** register.
19. Use the **FMODE** drop-down list to select one of the forced operating modes: **Normal** (Auto-PFM, default), **Forced PWM**, and **Forced Bypass**.
20. Use the **CTRL Type** drop-down list to select the control mode between **Type I** and **Type II** error amplifier.
21. Register **INTFLG_MASK** (Address: 0x13) contains additional features influencing the part behavior. Selecting the **Write** (or **Read**) button writes (or reads) the entire **INTFLG_MASK** register in one go.
22. Use the **OC_FAULT** drop-down to select the over-current handling mechanism for the part. By default, the part is set to **Hiccup mode** during over-current, but this setting can be changed to **Shutdown mode** or **Current Limit mode** using this register.
23. Use the **EN_OR** drop-down list to enable a push-button ON functionality for the EN pin. By default, this feature is disabled.

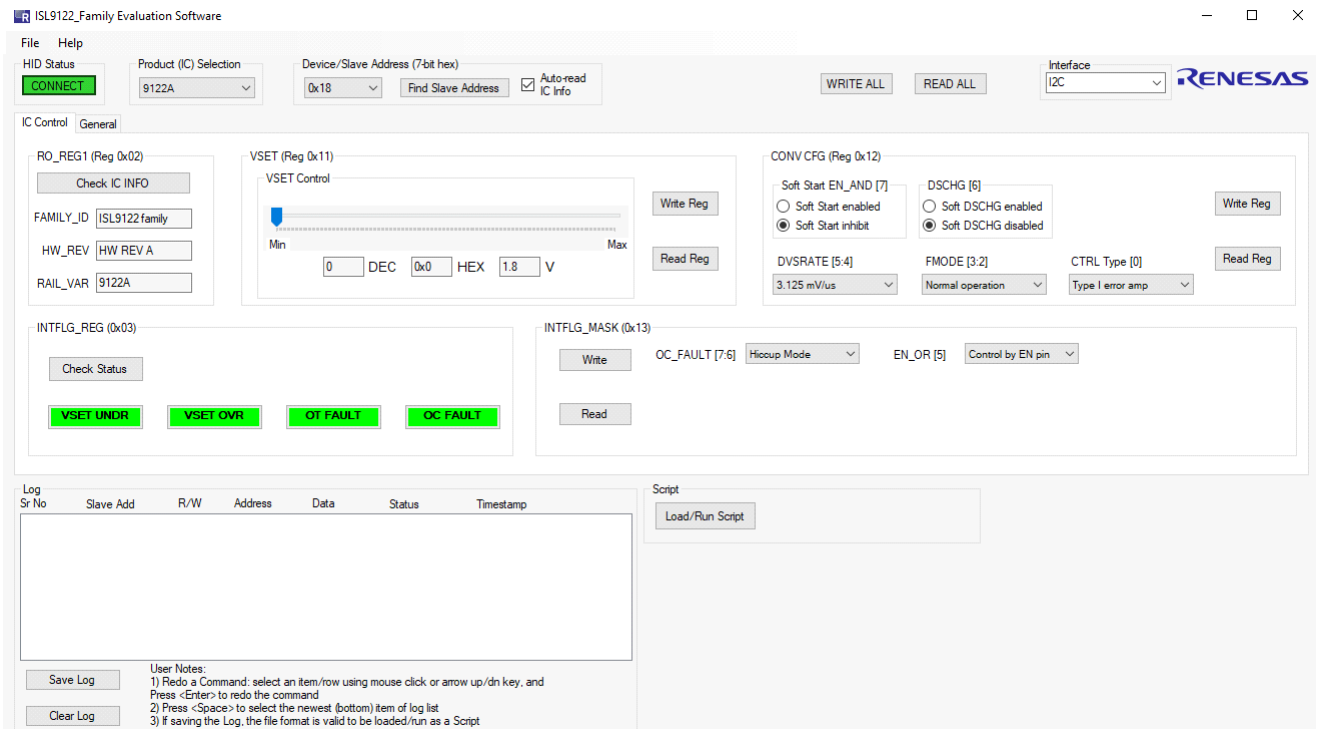

Figure 4. ISL9122 Evaluation Software Window

2. Board Design

2.1 ISL9122AIIN-EVZ Evaluation Board

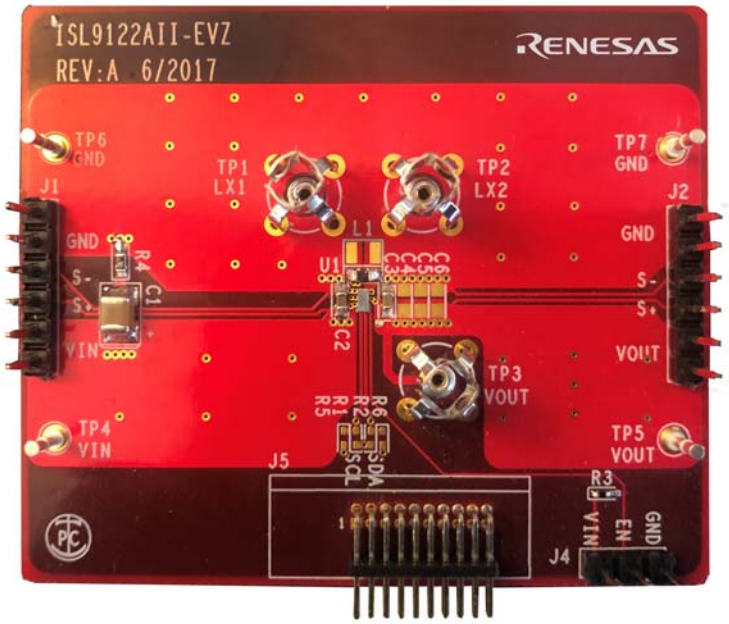

Figure 5. ISL9122AIIN-EVZ Evaluation Board (Top)

2.2 ISL9122AIRN-EVZ Evaluation Board

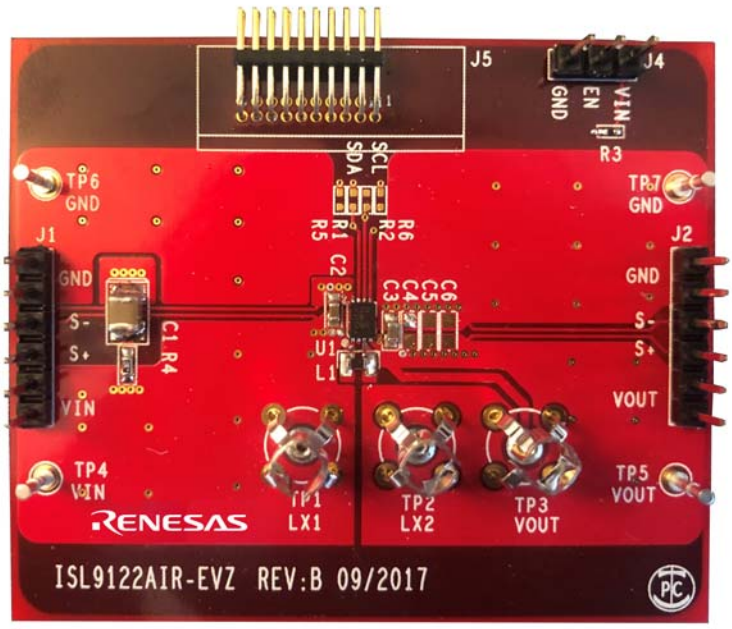

Figure 6. ISL9122AIRN-EVZ Evaluation Board (Top)

2.3 PCB Layout Guidelines

The ISL9122AIIN-EVZ and ISL9122AIRN-EVZ PCB layouts are optimized for electrical and thermal performance.

- The input and output capacitors should be positioned as close to the IC as possible. Both input and output currents can be discontinuous in a buck-boost converter; therefore, it is important to place both the input and output capacitors as close as possible.
- The ground connections of the input and output capacitors should be kept as short as possible and be on the component layer to avoid problems that are caused by high-switching currents flowing through PCB vias. If it is necessary to use the vias, use multiple vias to minimize the effective trace inductance.
- It is strongly advised that the second layer be a clean GND to mitigate problems that arise from long GND traces and subsequent parasitic inductive components. Also, a clean GND shields the intermediate layers from high power traces on the top layer.
- After placing short input and output loops, place an inductor as close as possible to the IC. While being cautious of any EMI concerns, ensure that the switch node traces (from LX1 and LX2 to the inductor) are short and wide.
- Finally, EN, SCL, SDA traces can be routed, but they should be routed away from high energy and high dV/dt traces to prevent mis-triggering. These traces can be routed through the intermediate layers.

Note: C1 and R4 are on the evaluation board to stabilize the input supply with long test leads. These are not required in actual system boards.

2.4 Schematic Diagrams

2.4.1 ISL9122AIIN-EVZ Circuit Schematic

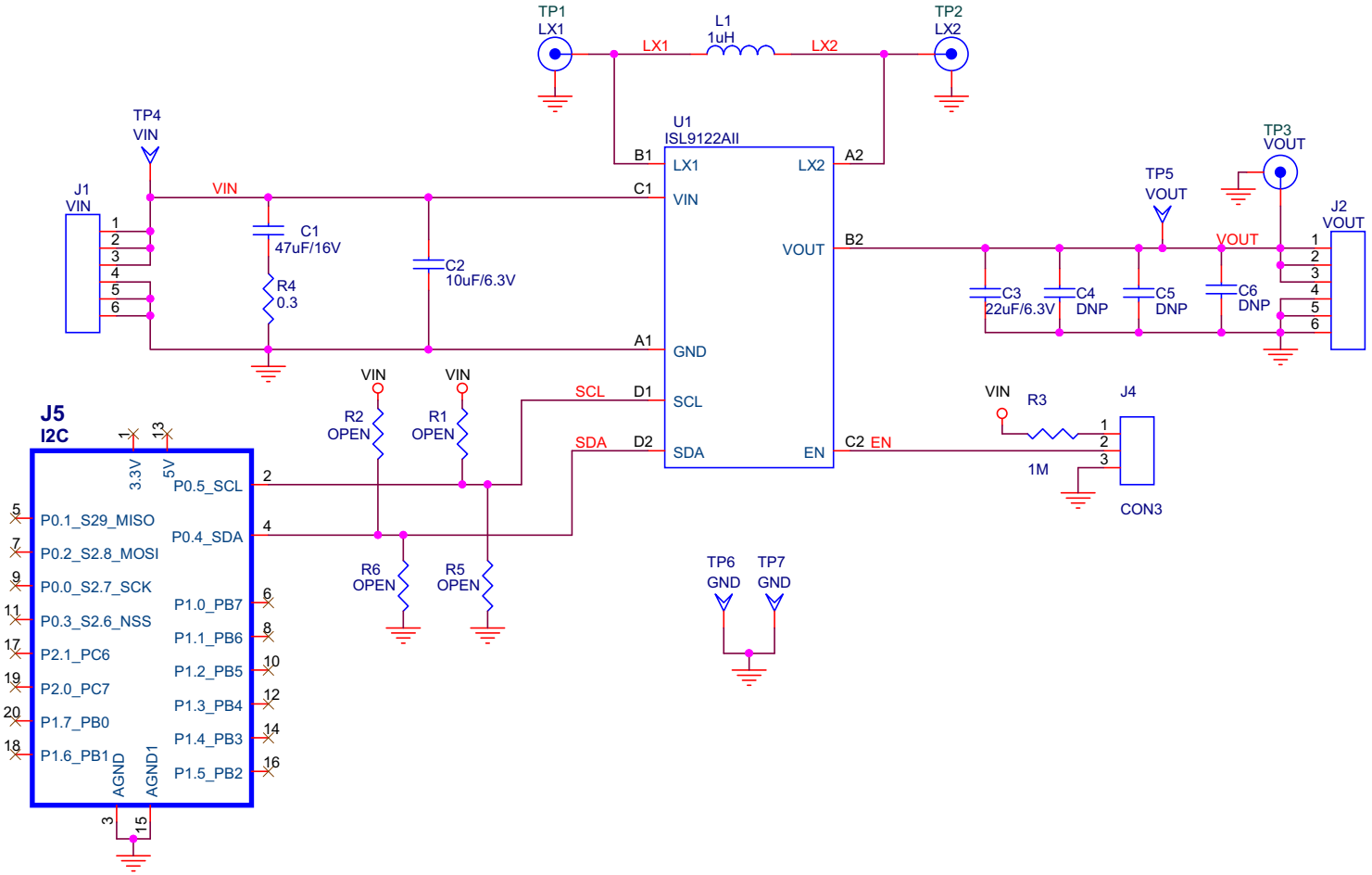

Figure 7. ISL9122AIIN-EVZ Circuit Schematic

2.4.2 ISL9122AIRN-EVZ Circuit Schematic

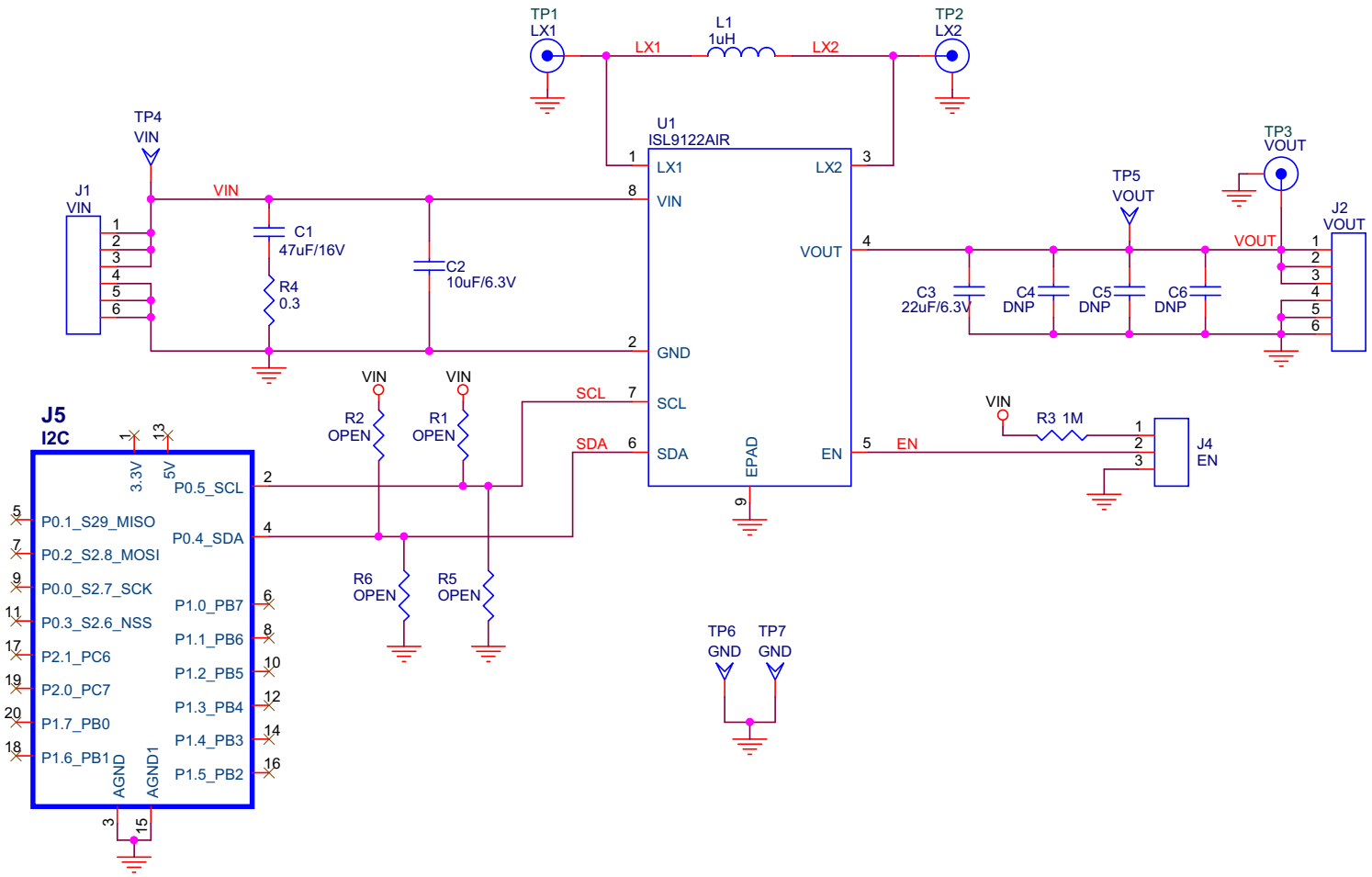

Figure 8. ISL9122AIRN-EVZ Circuit Schematic

2.5 Bill of Materials

2.5.1 ISL9122AIIN-EVZ Bill of Materials

Qty	Reference Designator	Part	PCB Footprint	Description	Manufacturer Part Number	Manufacturer
1	C1	47µF/16V	C_1210	CAP CER, X5R, SMD, ROHS, -55°C ~ 85°C	GRM32ER61C476ME15	Murata
1	C2	10µF/6.3V	C_0402	CAP CER, X5R, SMD, ROHS, -55°C ~ 85°C	GRM188R60J106ME84D	Murata
2	C3, C4[1]	22µF/6.3V (effective 6µF)	C_0603	CAP CER, X5R, SMD, ROHS, -55°C ~ 85°C	GRM188R60J226ME15D	Murata
2	C5, C6	DNP	C_0603		OPEN	Murata
1	J1	VIN	CON-1x6	BERGSTIK II 0.100" SR STRAIGHT	68000-236	FCI
1	J2	VOUT	CON-1x6	BERGSTIK II 0.100" SR STRAIGHT	68000-236	FCI
1	J4	EN	CON-1X3	BERGSTIK II 0.100" SR STRAIGHT	68000-236	FCI
1	J5	I^2C	USB_CONN_20	CONN HDR 1.27MM R/A AU 20POS	M50-3901042	Harwin Inc
1	L1	1µH	FERRITE_0603	FIXED IND 1µH 1.7A 128MΩ SMD	DFE18SAN1R0MG0L	Murata
4	R1, R2, R5, R6	OPEN	R_0402	RES SMD 1% 1/10W 0603	OPEN	Any
1	R3	1M	R_0402	RES SMD 1% 1/10W 0603	ANY	Any
1	R4	0.3	R_0603	RES SMD 1% 1/10W 0603	ANY	Any
1	TP1	LX1	TEK131-5031-00-PC	PCB Test Point, Through Hole Mount, 1.72 mm	131-5031-00	Mouser
1	TP2	LX2	TEK131-5031-00-PC	PCB Test Point, Through Hole Mount, 1.72 mm	131-5031-00	Mouser
1	TP3	VOUT	TEK131-5031-00-PC	PCB Test Point, Through Hole Mount, 1.72 mm	131-5031-00	Mouser
1	TP4	VIN	TP_PC	TERM TURRET SINGLE L = 5.84MM TIN	2110-2-00-80-00-00-07-0	Mill-Max
1	TP5	VOUT	TP_PC	TERM TURRET SINGLE L = 5.84MM TIN	2110-2-00-80-00-00-07-0	Mill-Max
2	TP6, TP7	GND	TP_PC	TERM TURRET SINGLE L = 5.84MM TIN	2110-2-00-80-00-00-07-0	Mill-Max
1	U1	ISL9122AIINZ-T	WLCSP8_39x71_157	Low I_Q Buck-Boost (WLCSP)	ISL9122AIINZ	Renesas Electronics
1	J4	Shunt installed between 1-2	2.54mm	Headers & Wire Housings Mini Jumper GF 6.0MM Close	151-8010-E	Kobiconn

1. C4 is DNP in default configuration. It is required to be populated if effective capacitance of C3 is less than 6µf at the operating output voltage.

2.5.2 ISL9122AIRN-EVZ Bill of Materials

Qty	Reference Designator	Part	PCB Footprint	Description	Manufacturer Part Number	Manufacturer
1	C1	47µF/16V	C_1210	CAP CER, X5R, SMD, RoHS, -55°C ~ 85°C	GRM32ER61C476ME15	Murata
1	C2	10µF/6.3V	C_0603	CAP CER, X5R, SMD, RoHS, -55°C ~ 85°C	GRM188R60J106ME84D	Murata
2	C3, C4[1]	22µF/6.3V (effective 6µF)	C_0603	CAP CER, X5R, SMD, RoHS, -55°C ~ 85°C	GRM188R60J226ME15D	Murata
2	C5, C6	DNP	C_0603	CAP CER, X5R, SMD, RoHS, -55°C ~ 85°C	OPEN	Murata
1	J1	VIN	CON-1x6	BERGSTIK II 0.100" SR STRAIGHT	68000-236	FCI
1	J2	VOUT	CON-1x6	BERGSTIK II 0.100" SR STRAIGHT	68000-236	FCI
1	J4	EN	CON-1X3	BERGSTIK II 0.100" SR STRAIGHT	68000-236	FCI
1	J5	I^2C	USB_CONN_20	CONN HDR 1.27MM R/A AU 20POS	M50-3901042	Harwin Inc
1	L1	1µH	FERRITE_0603	FIXED IND 1µH 950MA 200MΩ SMD	DFE18SAN1R0MG0L	Murata
4	R1, R2, R5, R6	OPEN	R_0402	RES, 1/10W, 0402, SMD,RoHS	OPEN	Any
1	R3	1M	R_0402	RES SMD 1% 1/10W 0603	ANY	Any
1	R4	0.3	R_0603	RES SMD 1% 1/10W 0603	ANY	Any
1	TP1	LX1	TEK131-5031-00-PC	PCB Test Point, Through Hole Mount, 1.72 mm	131-5031-00	Mouser
1	TP2	LX2	TEK131-5031-00-PC	PCB Test Point, Through Hole Mount, 1.72 mm	131-5031-00	Mouser
1	TP3	VOUT	TEK131-5031-00-PC	PCB Test Point, Through Hole Mount, 1.72 mm	131-5031-00	Mouser
1	TP4	VIN	TP_PC	TERM TURRET SINGLE L = 5.84MM TIN	2110-2-00-80-00-00-07-0	Mill-Max
1	TP5	VOUT	TP_PC	TERM TURRET SINGLE L = 5.84MM TIN	2110-2-00-80-00-00-07-0	Mill-Max
2	TP6, TP7	GND	TP_PC	TERM TURRET SINGLE L = 5.84MM TIN	2110-2-00-80-00-00-07-0	Mill-Max
1	U1	ISL9122AIRNZ-T	DFN8_79x118_197	Low I_Q Buck-Boost (DFN)	ISL9122AIRNZ	Renesas Electronics
1	J4	Shunt installed between 1-2	2.54mm	Headers & Wire Housings Mini Jumper GF 6.0MM Close	151-8010-E	Kobiconn

1. C4 is DNP in default configuration. It is required to be populated if effective capacitance of C3 is less than 6µf at the operating output voltage.

2.6 Board Layouts

2.6.1 ISL9122AIIN-EVZ Board Layout

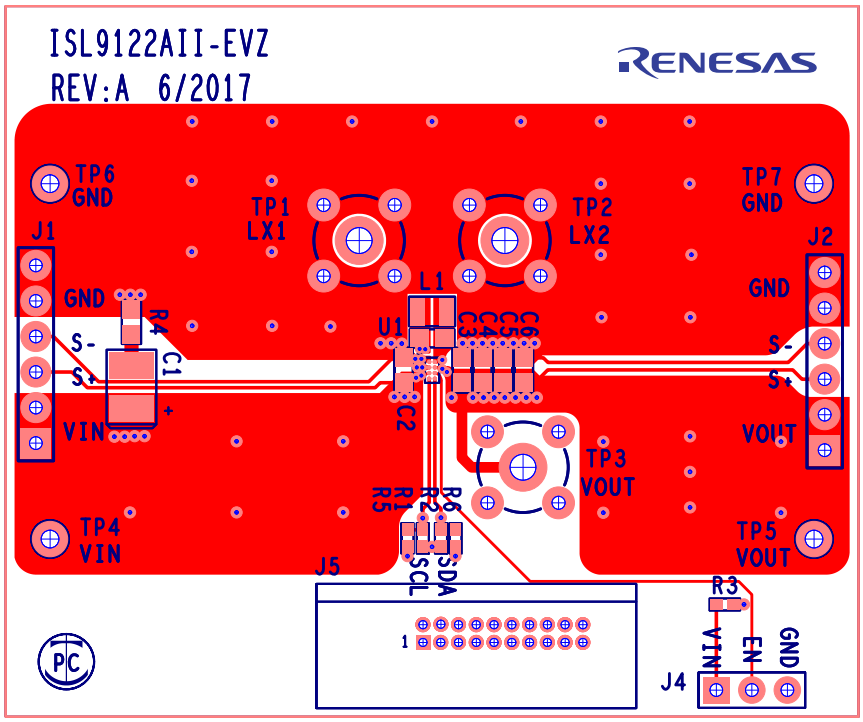

Figure 9. Top Layer Silk Screen

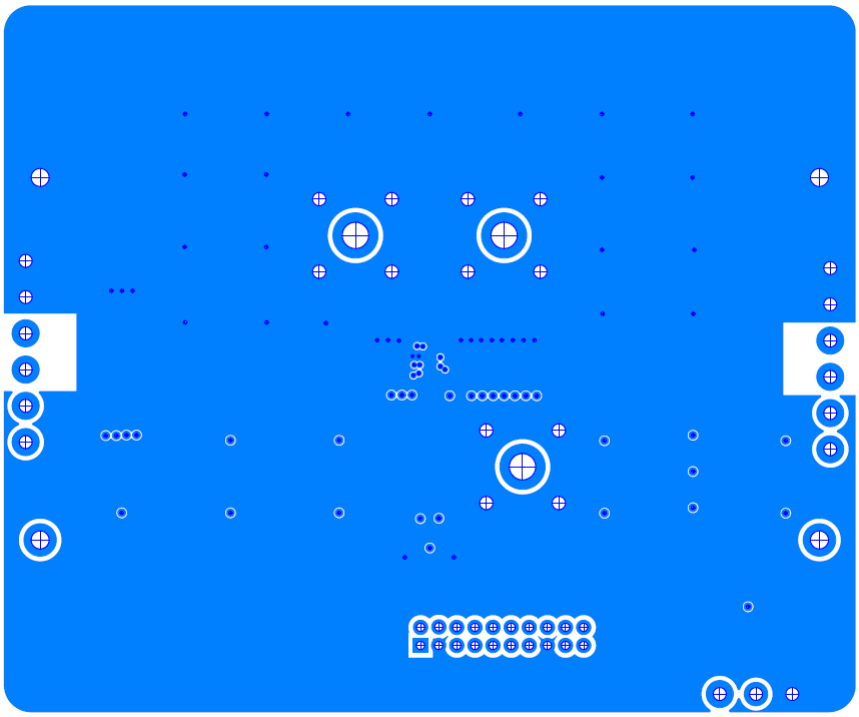

Figure 10. Inner Layer 2

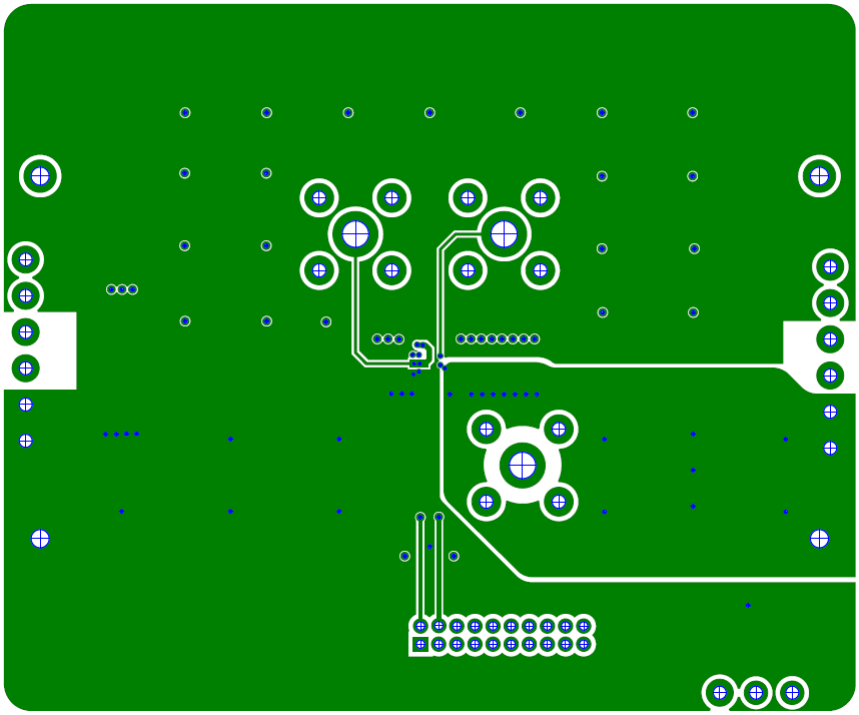

Figure 11. Inner Layer 3

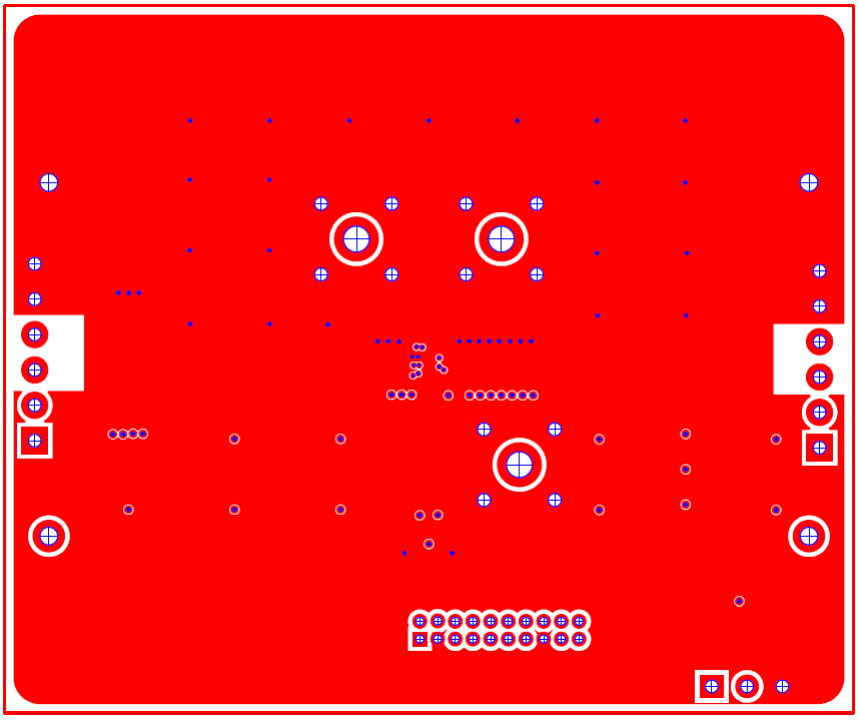

Figure 12. Bottom Layer Silk Screen

2.6.2 ISL9122AIRN-EVZ Board Layout

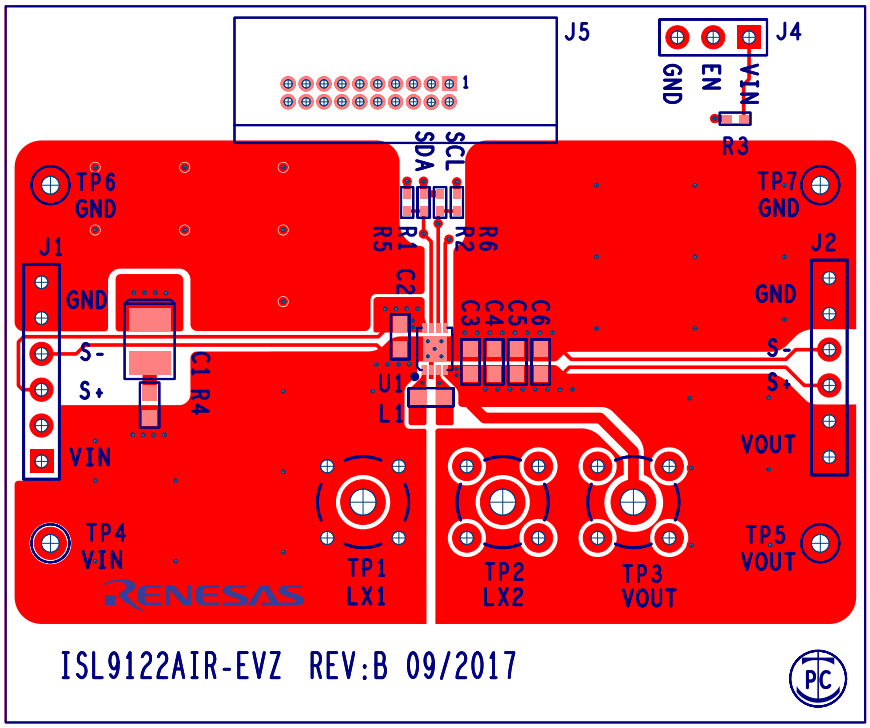

Figure 13. Top Layer Silk Screen

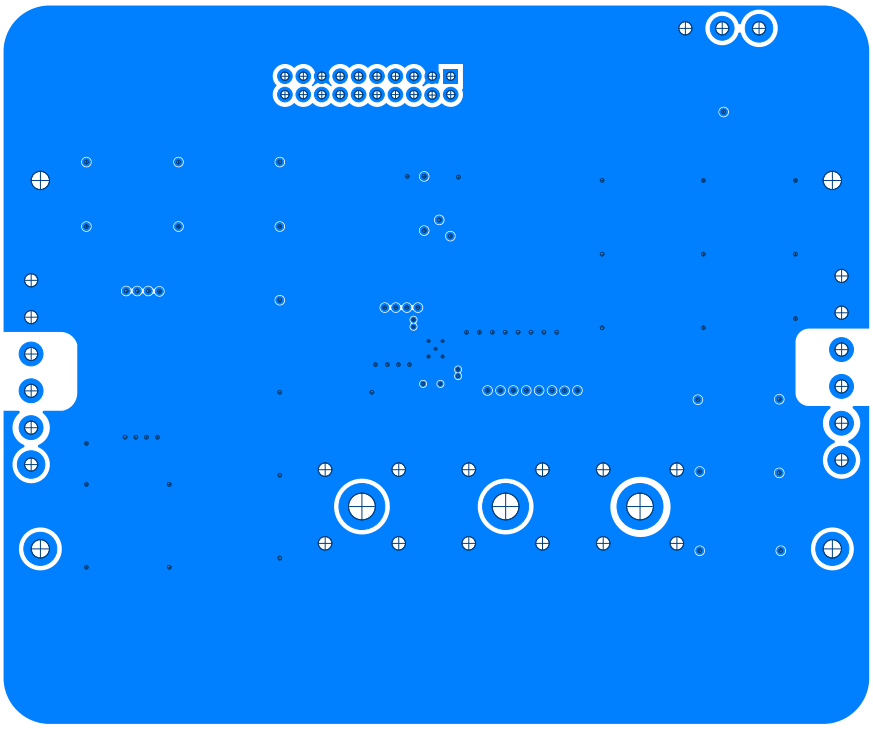

Figure 14. Inner Layer 2

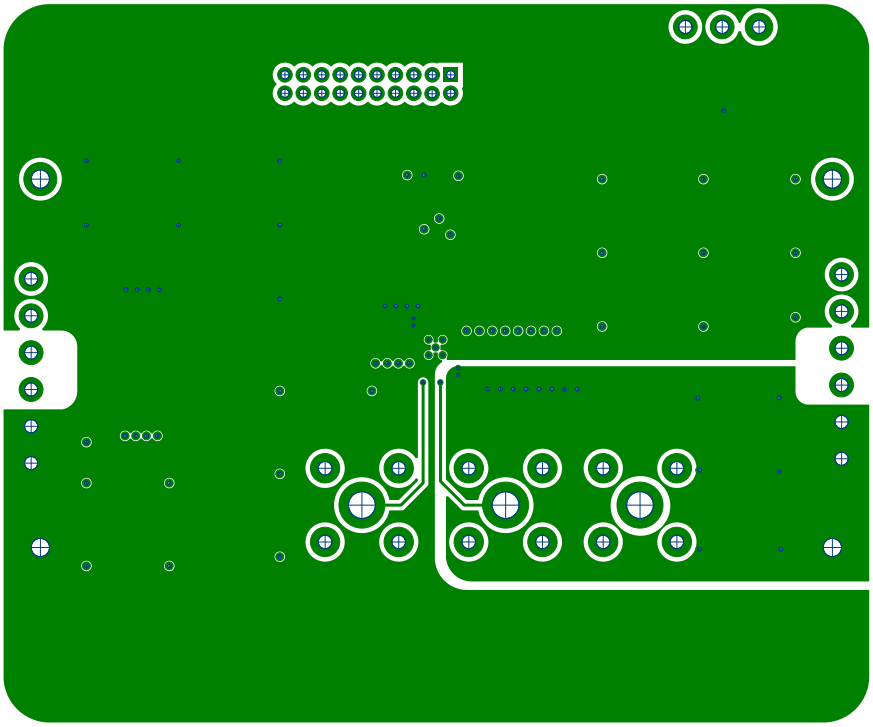

Figure 15. Inner Layer 3

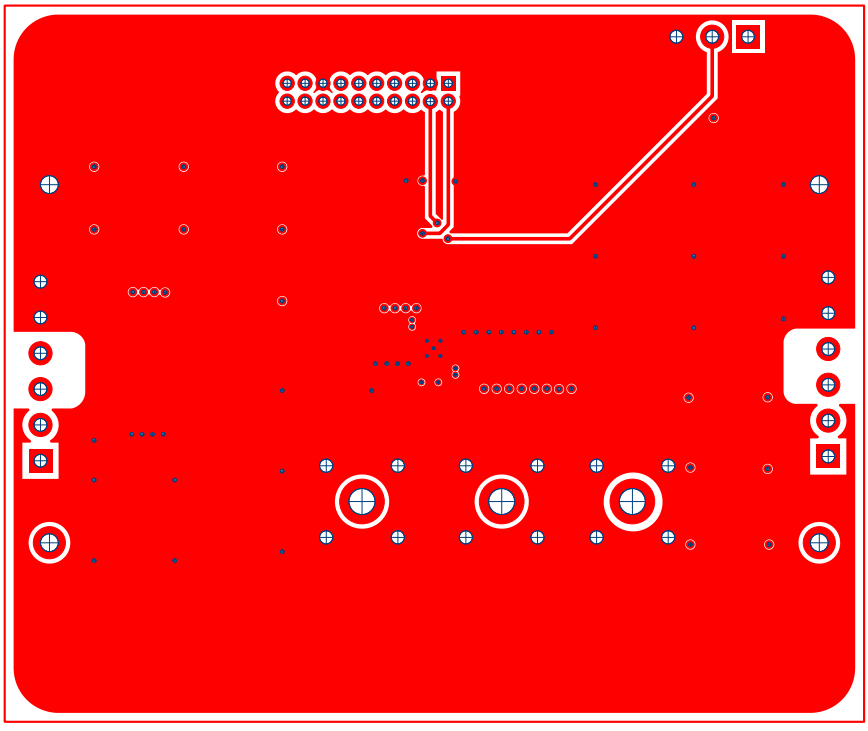

Figure 16. Bottom Layer Silk Screen

3. Ordering Information

Part Number	Description
ISL9122AIIN-EVZ	Evaluation board for ISL9122AIINZ
ISL9122AIRN-EVZ	Evaluation board for ISL9122AIRNZ

4. Revision History

Revision	Date	Description
1.02	Apr 1, 2022	Updated format to latest template. Updated Specification: Up to 500mA output current (V_{IN} > V_{OUT} > 2.5V) Added Figure 2. Updated section 1.2 and 1.3. Updated section 2, PCB Layout Guidelines. Updated schematics, Figure 7 and 8. Updated BOMs.
1.01	Oct 1, 2020	Updated Ordering Information table. Updated BOMs
1.00	Aug 18, 2020	Initial release

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