HIP4086 3-Phase Bridge Driver Configurations and Applications

Introduction

This application note describes the HIP4086 3-Phase MOSFET bridge driver, popular configurations in which the HIP4086 and the HIP4086 evaluation board can be used.

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Description

The HIP4086 is a 3-Phase Bridge N-Channel MOSFET driver IC. The HIP4086 is especially targeted at PWM motor control applications. The HIP4086 simplifies these designs without losing flexibility. The HIP4086 has a flexible input protocol for driving every possible switch combination. The user can even override the shoot-through protection, a feature needed when driving switched-reluctance motors. Compared to earlier parts in the HIP408x family such as the HIP4081A, the HIP4086's reduced output drive current of 0.5A and its wide range of programmable dead-time (0.25ms to 4.5ms) makes it ideal for motor control applications in the DC to 100kHz range. It even sports programmable undervoltage set point.

Key Features

Feature Summary

The HIP4086 includes an enhanced superset of features common to earlier members of the HIP408x family adding flexibility to meet the needs of both motor control and power supply applications.

The HIP4086 refresh start-up pulse duration and the undervoltage shutdown threshold levels are now adjustable. Both upper and lower MOSFET switches can now be turned on simultaneously (useful in double forward converter applications). As with other HIP408x family parts, a suitable 'dead-time' can be programmed using an external resistor.

Starting with the HIP4086, the use of negative logic for the high-side input control allows both high and low-side MOSFETs of a phase leg to be controlled without added external logic.

Undervoltage Shutdown

Undervoltage shutdown prevents the power MOSFETs from being turned on if the bias supply voltage is below the level set by the UVLO pin. There are several ways to program the UVLO pin. Leaving the UVLO pin open results in an undervoltage trip setting of approximately 6.6V. Tying the UVLO pin to V_{DD} sets the trip level to approximately 6.2V. Hysteresis in this configuration is disabled.

For higher trip settings, tie a resistor between V_{SS} and UVLO. A 50kΩ resistor, for example, will provide a trip voltage of approximately 8.5V. See Figure 19 of the HIP4086 [1] datasheet, for details.

Input Logic Flexibility

You can drive the input control logic of the HIP4086 by TTL or CMOS logic. The threshold voltages for input control of the HIP4086 is a guaranteed "one" at or above 2.7V and a guaranteed "zero" at or below 0.8V.

The HIP4086 inputs source approximately 100µA through an internal pull-up when the inputs are held low. With 5V or more at the logic inputs, the input current drops to less than 1µA.

Disable (DIS) Function

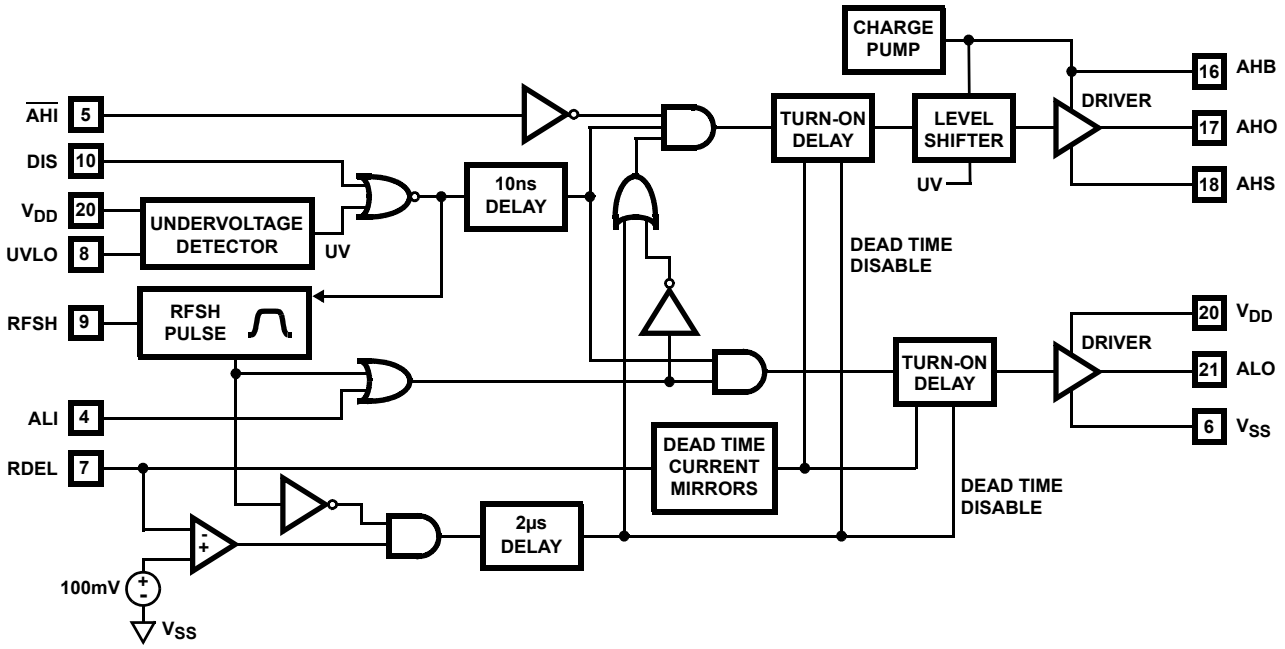
A logical "one" applied to the DIS pin turns off all MOSFETs and overrides all inputs. To enable the HIP4086 the 100µA internal pull-up must be pulled down externally. After a short delay the gate control inputs are again re-enabled. During the delay, the lower MOSFETs are turned on to refresh the upper bootstrap capacitors. See "Description of Operation" "Input Timing" on page 5.

TABLE 1. TRUTH TABLE

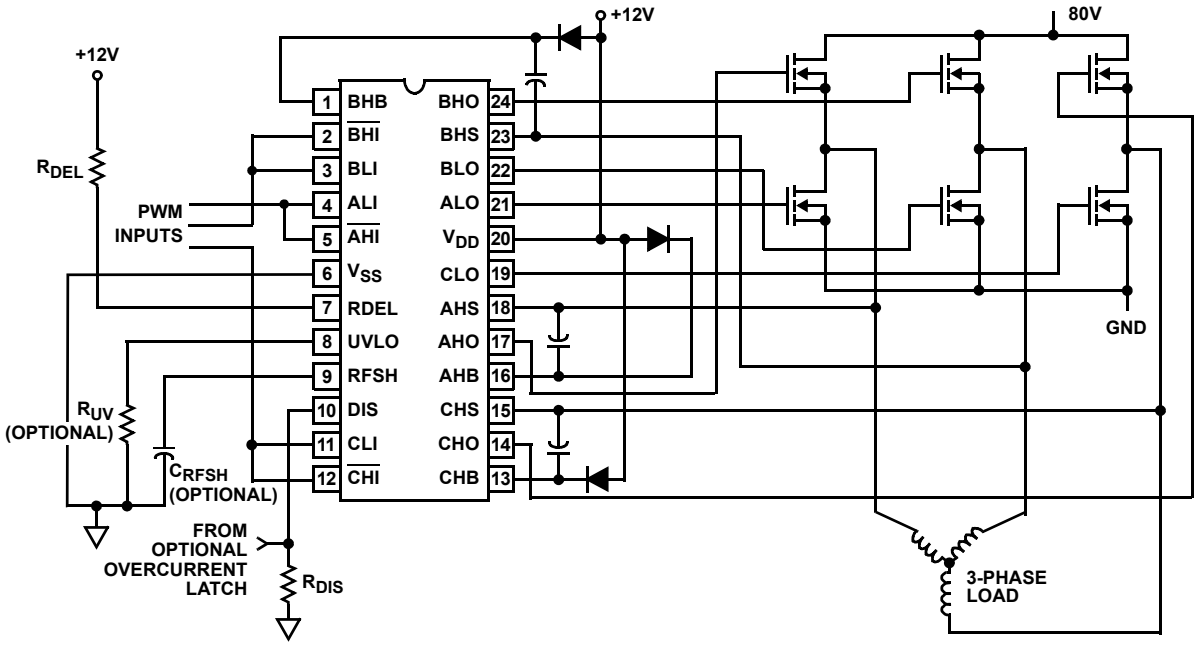
INPUT					OUTPUT	
ALI, BLI, CLI	$\overline{AHI}$, $\overline{BHI}$, $\overline{CHI}$	UV	DIS	RDEL	ALO, BLO, CLO	AHO, BHO, CHO
X	X	X	1	X	0	0
X	X	1	X	X	0	0
1	X	0	0	>100mV	1	0
0	0	0	0	X	0	1
0	1	0	0	X	0	0
1	0	0	0	<100mV	1	1

NOTE: X signifies that input can be either a "1" or "0".

Functional Block Diagram (1/3 of HIP4086)



Typical Application (PWM Mode Switching)



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
16 1 13	AHB BHB CHB (xHB)	High-side Bootstrap supplies. One external bootstrap diode and one capacitor are required for each. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to each xHB pin.
5 2 12	$\overline{AHI}$ $\overline{BHI}$ $\overline{CHI}$ ($\overline{xHI}$)	High-side Logic Level Inputs. Logic at these three pins controls the three high-side output drivers, AHO (Pin 17), BHO (Pin 24) and CHO (Pin 14). When $\overline{xHI}$ is low, xHO is high. When $\overline{xHI}$ is high, xHO is low. Unless the dead time is disabled by connecting RDEL (Pin 7) to ground, the low-side input of each phase will override the corresponding high-side input on that phase (see "TRUTH TABLE" on page 1). If RDEL is tied to ground, dead time is disabled and the outputs follow the inputs. Care must be taken to avoid shoot-through in this application. DIS (Pin 10) also overrides the high-side inputs. $\overline{xHI}$ can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
4 3 11	ALI BLI CLI (xLI)	Low-side Logic Level Inputs. Logic at these three pins controls the three low-side output drivers ALO (Pin 21), BLO (Pin 22) and CLO (Pin 19). If the upper inputs are grounded then the lower inputs control both xLO and xHO drivers, with the dead time set by the resistor at RDEL (Pin 7). DIS (Pin 10) high level input overrides xLI, forcing all outputs low. xLI can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
6	V_{SS}	Ground. Connect the sources of the Low-Side power MOSFETs to this pin.
7	RDEL	Dead Time Setting. Connect a resistor from this pin to V_{DD} to set timing current that defines the dead time between drivers - see Figure 18 of HIP4086 [1]. All drivers turn-off with no adjustable delay, so the RDEL resistor guarantees no shoot-through by delaying the turn-on of all drivers. When RDEL is tied to V_{SS}, both upper and lowers can be commanded on simultaneously. While not necessary in most applications, a decoupling capacitor of 0.1µF or smaller may be connected between RDEL and V_{SS}.
8	UVLO	Undervoltage Setting. A resistor can be connected between this pin and V_{SS} to program the undervoltage set point, see Figure 19 of HIP4086 [1]. With this pin not connected, the undervoltage disable is typically 6.6V. When this pin is tied to V_{DD}, the undervoltage disable is typically 6.2V.
9	RFSH	Refresh Pulse Setting. An external capacitor can be connected from this pin to V_{SS} to increase the length of the start-up refresh pulse - see Figure 17 of HIP4086 [1]. If this pin is not connected, the refresh pulse is typically 1.5µs.
10	DIS	Disable Input. Logic level input that when taken high sets all six outputs low. DIS high overrides all other inputs. With DIS low, the outputs are controlled by the other inputs. DIS can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
17 24 14	AHO BHO CHO (xHO)	High-side Outputs. Connect to the gates of the High-Side power MOSFETs in each phase.
18 23 15	AHS BHS CHS (xHS)	High-side Source Connection. Connect the sources of the High-side power MOSFETs to these pins. The negative side of the bootstrap capacitors should also be connected to these pins.
20	V_{DD}	Positive Supply. Decouple this pin to V_{SS} (Pin 6).
21 22 19	ALO BLO CLO (xLO)	Low-side Outputs. Connect the gates of the Low-side power MOSFETs to these pins.

NOTE: x = A, B and C.

Charge Pumps

The charge pumps are designed to maintain floating supply bias voltage when the upper MOSFETs are turned on and the lower MOSFETs are turned off. The upper charge pump is turned off whenever the lower MOSFET in that phase is turned on. When a lower MOSFET is turned on, the bootstrap capacitor for that phase is refreshed through its V_{DD} supply and bootstrap diode eliminating the need for charge pumping during these periods. The total chip bias current, ICC, is reduced by 1.0mA for each phase's charge pump which is turned off.

When both upper and lower switches are turned off, the charge pumps continue to operate, but the off level-shift current (typically 800µA) overcomes that of the charge pump (typically 125µA) and the bootstrap capacitor will discharge. In order to refresh the bootstrap capacitor for subsequent upper turn-on, that phase's lower must first be turned on. As long as the lower MOSFETs are continually being pulse-width-modulated at a reasonably high frequency, the bootstrap capacitors in each phase will remain charged up.

When both upper and lower MOSFETs are commanded on simultaneously (switched-reluctance motor drive or other double-forward converter applications) the charge pump deactivates because the lower MOSFET is turned on. Since the upper MOSFET is also on, the bootstrap capacitor will eventually discharge. To maintain bootstrap supply in this situation, the upper/lower pairs must be constantly PWMed. Refreshing of the bootstrap supply will occur automatically during the period when

both upper and lower MOSFETs are off. This happens because the load current will continue to flow during the 'off' part of the PWM cycle forcing the converter's flyback diodes to conduct. The conducting flyback diodes will cause the xHS terminals to be pulled a diode drop below V_{SS}, which will refresh the bootstrap capacitors.

Good practice always dictates the use of a bootstrap diode and capacitor for maintaining upper bias voltage. Do not assume that the charge pump can always maintain the required bias. When connecting one of the upper drivers as a low-side driver, do not use the bootstrap diode and capacitor. Rather, connect that phase's xHB terminal to V_{CC} and the xHS terminal to V_{SS}.

An excellent treatise on bootstrap circuit design and charge pump operation can be found in application notes AN9404 [2] or AN9405 [3], under Applications Considerations.

Shoot-Through Avoidance

Shoot-through or cross conduction is eliminated by connecting a resistor from the RDEL pin to V_{DD} ranging from 2kΩ to 100kΩ, which provides for a dead-time range of approximately 0.1µs to 4.5µs. Dead-time varies directly with RDEL resistance above 0.1µs as shown in Figure 1.

In double-forward and/or switched-reluctance driver applications where simultaneous conduction in both upper and lower MOSFETs, the phase legs are desired or where dead time will be externally controlled, tie the RDEL pin to V_{SS}. This disables the dead time delay circuitry and allows direct control of both upper and lower MOSFETs without regard to prior conduction states.

Very small propagation delays associated with both upper and lower MOSFETs, typically 50ns, remain even with RDEL tied to V_{SS}.

Programmable Refresh

The start-up refresh pulse duration is controlled by the size of the refresh capacitor tied to the RFSH pin as shown in Figure 2. The start-up refresh pulse initializes the charge on the bootstrap capacitors of the three high-side drivers when power is first applied to the HIP4086. The charge pump can supply only enough charge to maintain the gate voltage applied to an upper MOSFET in the on-state position.

The duration of the start-up refresh pulse will be at least 1µs with no external capacitor connected between the RFSH and the V_{SS} pins. The start-up refresh pulse duration can be extended beyond 1µs by connecting a small capacitor between pin 9 (RFSH) and pin 6 (V_{SS}). For example, a 100pF capacitor extends the refresh time to about 16µs. which is more than long enough for most applications.

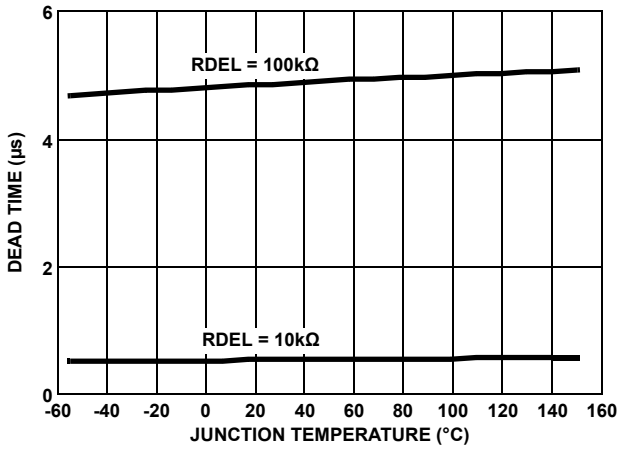


FIGURE 1. DEAD-TIME vs RDEL RESISTANCE

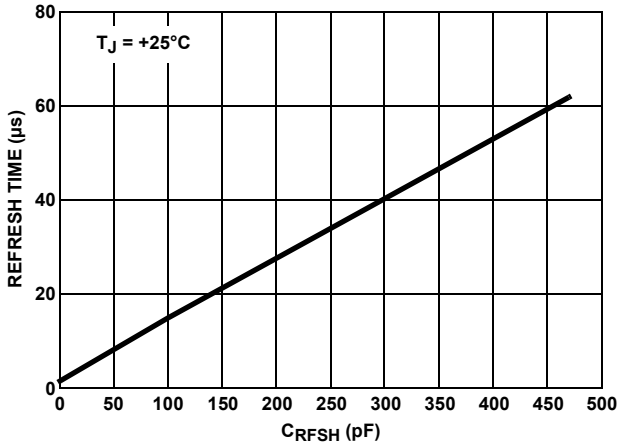


FIGURE 2. REFRESH CAPACITANCE vs REFRESH TIME

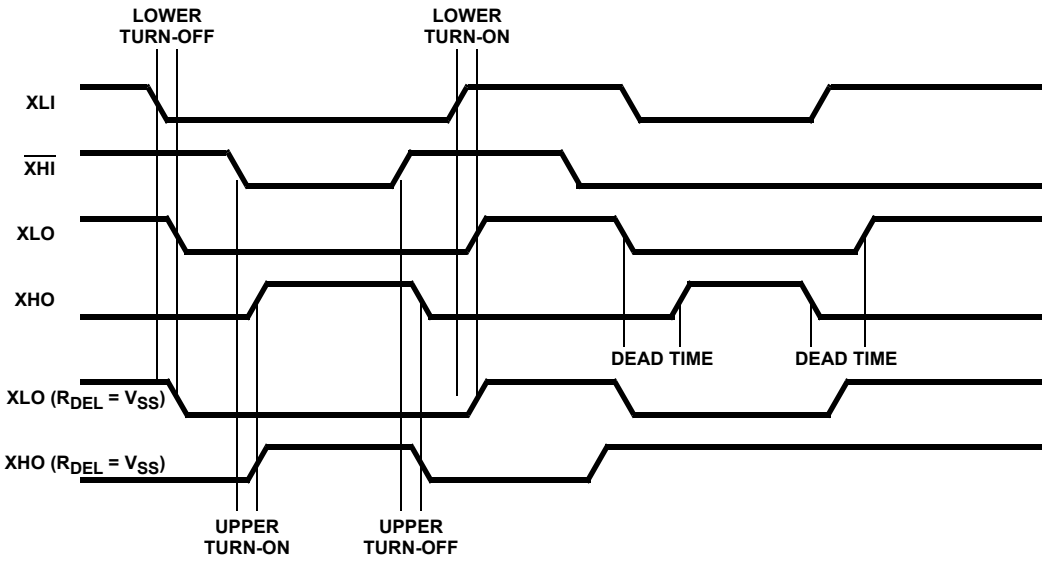
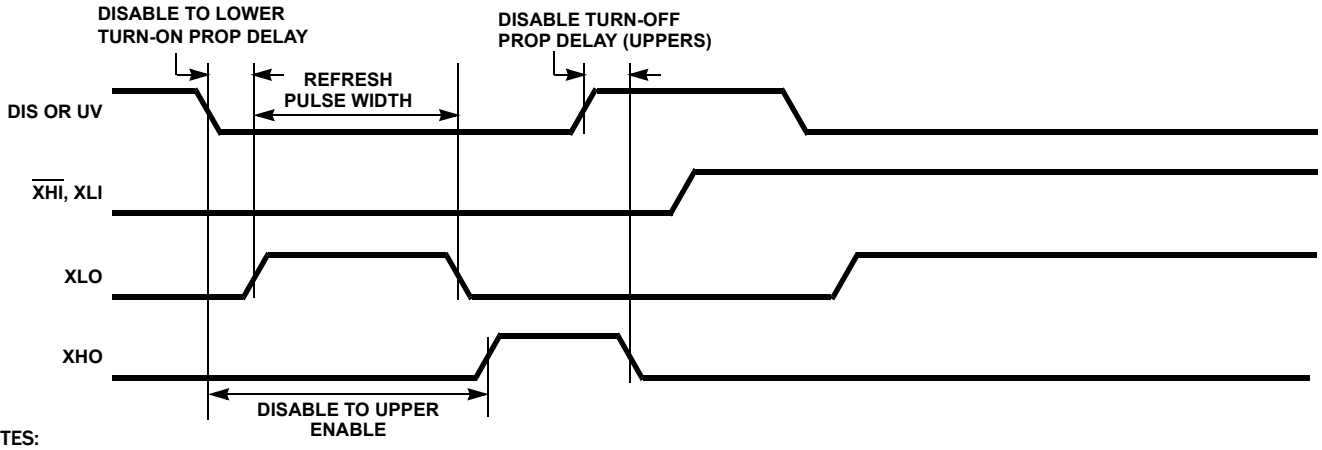


FIGURE 3. TIMING DIAGRAMS



NOTES:

1. X means any “A”, “B”, or “C” phase.
2. With RDEL resistor tied to V_{DD}, lowers and uppers cannot be turned on at the same time. Low-side logic overrides high-side logic unless RDEL is < 100mV.

FIGURE 4. DISABLE FUNCTION

Description of Operation

Input Timing

The timing diagrams of Figures 3 and 4 show the switching relationships between the inputs and their respective outputs in standard bridge mode (RDEL tied to V_{DD} through a programming resistor) and in simultaneous-conduction mode (RDEL tied to V_{SS}). Note that RDEL should never be left open.

Since the HIP4086 upper input logic is inverted, the upper devices will be OFF if the upper inputs are pulled high. For full bridge operation the upper input control pins should be connected to the lower control input pins thus minimizing additional external logic. For double-forward and switched-reluctance operating modes (simultaneous conduction mode) either the upper or lower inputs must be inverted with respect to each other.

The Dead Time as shown in Figure 3 actually represents the turn-on delay time associated with turning on that device in response to that device’s input command. Simultaneously, a turn-off command is issued to the opposite device in the same phase leg, but the actual turn-off is only delayed by the natural IC propagation delay. In other words, there is no added delay involved in turning off the switches, other than their natural transport delays (approximately 45ns to 75ns) plus the time it takes the driver to pull enough charge out of the power MOSFET gate to turn it off.

The Dead Time, or more appropriately, the turn-on delay time is tailored to specific application by adjusting the value of the RDEL resistor as discussed previously in “Shoot-Through Avoidance” on page 4 and characterized by Figure 1 on page 4.

Figure 4 indicates how the Undervoltage sensor, U/V, and the DIS, disable, pin affect the states of the gate driver outputs. Two

conditions must be satisfied to allow a lower refresh pulse to be initiated. First, the V_{DD} voltage must be above the U/V trip level and second, the DIS pin must be pulled low (chip enable). The refresh function was discussed previously in "Programmable Refresh" on page 4 and is characterized in Figure 2 on page 4. Long refresh times may be necessary when MOSFETs with very large gate turn-on charge requirements are used or when several large MOSFETs are paralleled to drive heavy loads that a single MOSFET cannot drive.

Level-Shift Operation

The level-shift function for the HIP4086 operates exactly like the HIP4082 level-shifter described more fully in application note AN9611 [4].

The continuous on/off level-shift technique uses no latches in the floating logic section of the IC and avoids the possibility that an on/off latch could inadvertently change states. The only down-side of the continuous on/off level-shift technique is that higher level-shift power dissipation can occur under certain modes of operation, for example, when the upper MOSFETs are off throughout most of the duty cycle. See application note AN9611 [4] for more detail.

Power Dissipation

See Power Dissipation [2, 3] and Thermal Design under Power Dissipation the Easy Way [2, 3] for a very good discussion on determining IC power dissipation based upon the switching frequency, IC supply voltage and switching frequency.

HIP4086 Applications Configurations

The HIP4086 can drive up to 6 independent power MOSFETs. Three of the HIP4086's gate drivers must be used to drive low-side, N-Channel MOSFETs. That is, MOSFETs which have their sources tied to the most negative power bus rail or very close to it through a low valued resistive shunt.

The three remaining drivers' negative references float, since they are intended for driving high-side, N-Channel MOSFETs. However, they can also be configured to drive low-side MOSFETs by externally tying the drivers' negative references, AHS, BHS and CHS to the HIP4086's V_{SS} potential.

The 3-phase bridge configuration, one of the most common motor drive configurations, employs 3 low-side and 3 high-side drivers as shown in Figure 5. The load is connected between the points marked "Phase A", "Phase B" and "Phase C". The 3-phase bridge configuration is used for controlling PM brushless DC (BDC) motors.

A high-side driver paired with a low-side driver is referred to as a half-bridge, three of which are used in the 3-phase bridge configuration. The half-bridge is the basic building block for driving most brush and brushless motor drives. Normally, the MOSFETs body diodes are used to recirculate inductive load current in configurations comprised of one or more half-bridges.

Note that the 3 "floating" drivers incorporated in the HIP4086, can control up to 6 independent low-side MOSFET switches for driving various loads, (i.e., relays and single quadrant brush motors).

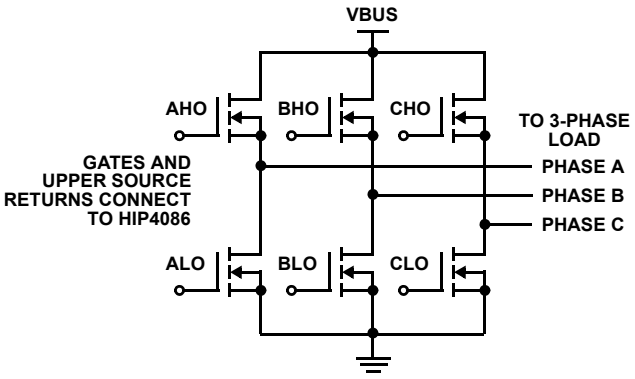


FIGURE 5. 3-PHASE BRIDGE CONFIGURATION

The HIP4086 can provide up to 3 separate high-side switch drivers for driving grounded loads or it can drive all high-side connected loads as shown in Figure 6. Appropriate freewheeling diodes must be added as shown. The 3 remaining non-floating, ground-referenced gate drivers must be used as low-side drivers. The low-side driver outputs are distinguished by their ALO, BLO and CLO pin designations.

Another basic building block, repeated 3 times in Figure 7 is referred to as a double-forward converter. In the double-forward converter the load is connected between the upper and lower MOSFETs. This configuration is a basic building block for many two-switch forward converter (power supplies), switched reluctance motors, and automotive fuel injectors. In this configuration, one MOSFET can be used to commutate the current in the windings while the other can be pulse-with-modulated to regulate current. Note in Figure 7 that diodes must be added for recirculating current. When MOSFETs are used as high-side switches, a current of 1mA flows into the load from each of the pins, AHS, BHS and CHS when the upper MOSFET(s) is off.

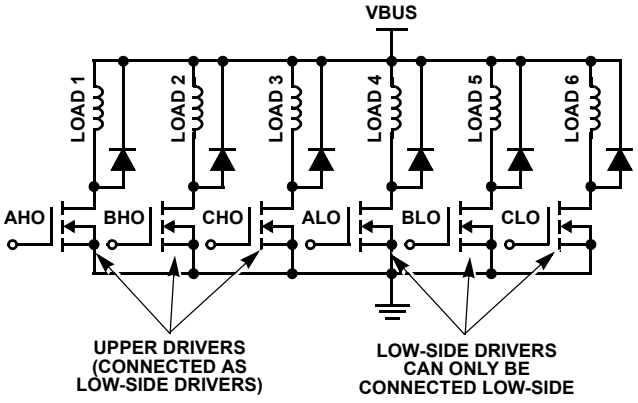


FIGURE 6. 6-LOWER CONFIGURATION

It is possible to share the current regulation MOSFET that is pulse-width-modulated for multiple loads as shown in Figure 8. This minimizes the number of MOSFETs required to drive the loads. To allow both upper and lower MOSFETs to be turned on simultaneously, the RDEL pin of the HIP4086 is tied to V_{SS}. This disables the 'on-delay' feature also known as "dead-time".

Of course, there are many other possibilities. For example, the three-phase bridge configuration can drive three independent DC brush motors in two-quadrant mode, which means that each motor can have one polarity of voltage impressed across it, but with current flowing either into or out of the motor. In two quadrant mode, motors may be controlled in one direction with both accelerating or braking torque control.

Another possibility is to drive one DC brush motor in 4-quadrant mode (this requires a full H-bridge) and a second in 2-quadrant mode as discussed previously. In 4-quadrant mode the motor's torque and rotational direction can be controlled in both directions. The 4-quadrant motor would be connected between any two of the phase terminals as shown in Figure 9 and a 2-quadrant motor would be connected between the remaining phase terminal and either the bus or the power ground.

Since the phases are truly independent, a synchronous boost regulator could be made using one of the three MOSFET bridge legs with the resulting DC output used to supply the bus for the other two MOSFET bridge legs, either making these two independently controlled half-bridges or an H-bridge as shown in Figure 9. In the figure a boost regulator was chosen with the upper MOSFET of phase A being used as the diode. Phases B and C function as an H-Bridge to control the load voltage.

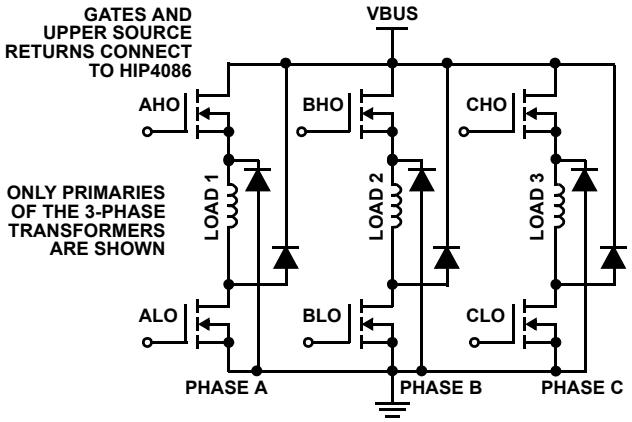


FIGURE 7. DOUBLE-FORWARD CONVERTER BRIDGE CONFIGURATION

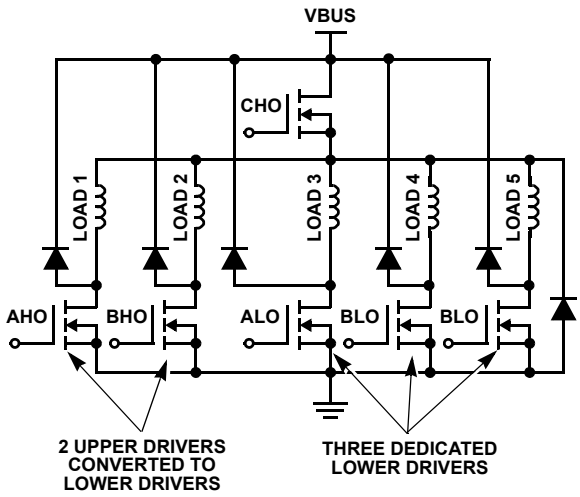


FIGURE 8. MULTIPLE LOADS WITH UPPER MODULATED SWITCH FOR CONTROL

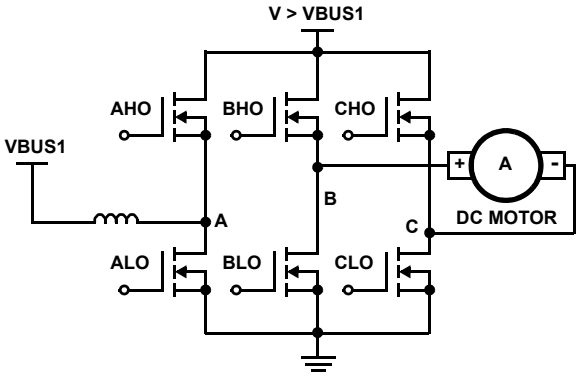


FIGURE 9. SYNCHRONOUS BOOST WITH HIGHER VOLTAGE FOR DRIVING LOAD

In summary, the HIP4086 drives six independent N-Channel MOSFETs. Three of these drivers must drive low-side MOSFETs, but the other three floating drivers can be used to drive high or low- side MOSFETs. The outputs can be configured in many ways to drive a variety of motors, relays, injectors, speakers and two-switch forward converter (power supplies). The HIP4086 allows the designer great flexibility. The details of this flexibility pertains not only to configuration versatility, but also to the HIP4086's many features, which will be discussed in the following section.

HIP4086 Evaluation PC Board

The HIP4086 Evaluation PC Board provides a fast and efficient way for users to evaluate performance of the HIP4086 without having to design and build their own board. In fact, the evaluation printed circuit board was used to characterize the propagation and dead time parameters included in the HIP4086 datasheet.

The evaluation PC board has been designed to enable users to quickly try different power circuit configurations, such as 3-phase full wave bridge. The switched reluctance and double-forward converter configurations can also be configured with the HIP4086 Evaluation PC Board. For the latter, fast recovery power rectifiers have been included for allowing freewheeling currents to flow in the inductive load.

Evaluation Printed Circuit Board Features

The evaluation printed circuit board provides the following features and conveniences:

- 6 RFP22N10 Power MOSFETs, 2 RURG3010 power rectifiers and 5 RURP1510 power rectifiers to provide circuitry for changing quickly between different circuit configurations. 11 banana jacks for fast connection of external circuits and power supplies and for changing configurations.
- 3 Kelvin shunts, 0.1Ω, 3W for current sensing. Two are located in the upper MOSFET source to phase connections (1 in each of two phases) and the third is located between the common source connections of the lower MOSFETs and power ground.
- A four terminal header to access the upper shunt signals and a 28 pin header to provide access to the HIP4086 gate control inputs and to customize signals coming from the on-board PWM distribution network.
- On-board PWM distribution network with potentiometer to change duty cycle. An access test-point is available to dynamically control duty-cycle if desired from an external source.
- 24 test points to monitor waveforms at representative points on the HIP4086 and bridge inverter.
- All necessary bootstrap components, bypass capacitors, gate resistors and source return resistors are included. Provision for tailoring refresh start-up pulse width, undervoltage set-point and dead-time are included.
- Color-coded banana jacks for connecting Bias supply and Bus supply voltages.

Setting Up the HIP4086 Evaluation Printed Circuit Board

Since the HIP4086 can drive floating as well as ground-referenced N-Channel MOSFETs, the power circuit configurations shown in Figures 5 through 9 can be driven by the HIP4086. Please refer to the full schematic located in the appendix to this application note. The HIP4086EVAL board can be configured to implement the configurations shown in Figures 5 through 9, with the exception that, in Figure 8, only four low-side MOSFETs can be implemented.

Connect power to the HIP4086EVAL board, +12VDC to BJ1 with ground of this supply to BJ11 (the common ground for logic and power). The Power Bus (up to +80 VDC Max) is tied to BJ2 with its ground tied to BJ11. The Power and Control power can be driven from the same 12V supply if desired.

If desired, the internal current sensor can be used to latch upon sensing an overcurrent in the shunt resistor, SH3. This is a 3W, 0.1Ω, 1% resistor mounted on the heat sink which also cools the power MOSFETs. To use the internal overcurrent latch, pins 1 and 2 of JP1 must be jumpered. Two other shunts, identical to SH3, are located in the source paths of two upper MOSFETs, Q1 and Q2. The Kelvin sense leads of these have been brought to JP2 pins 1 and 2 and pins 3 and 4, respectively. These shunts may be sensed by a users external sense amplifiers or comparators as desired. If they will be used in lieu of SH3 or if overcurrent latchout is not desired, the jumper connecting JP1 pins 1 and 2 should be removed, allowing the DIS pin on the HIP4086 to be held low by resistor, R11.

Potentiometer, P1, may be used to adjust the duty cycle of the pulse width modulator, PWM. This is a simple PWM modulator made by comparing a triangle wave (from the ICM7555 timer) with a DC level from the wiper of P1. Three individual DC levels may be compared to the triangle wave if the jumpers between pins 3 to 4, 5 to 6 and 7 to 8 of JP1 are removed and appropriate user-supplied signals are applied to pins 3, 5 and 7 to control the modulation index of phases B, C and A respectively.

Tables 2, 3, and 4 have been prepared to simplify the task of connecting all of the jumpers for the different configurations possible with the HIP4086EVAL board. Table 2 deals with the setting of the JP1 jumpers to implement several of the configurations possible with the HIP4086EVAL board. Probably the most popular configuration is the 3-phase bridge configuration. For this reason the HIP4086 was designed to allow bringing in only one control signal for each of the A, B and C half-bridges. This is accomplished by jumpering the xLI input to the same xHI input. In this configuration, when an upper is to be on, a lower is to be off and face-savers. The upper input control signals are designed to cause each upper switch to be on when its corresponding input signal is low (a logical inversion). The JP1 jumpers provide for either bringing the same control signal to the xLI and xHI inputs or for inverting one of them. The former provides the proper input polarities for conventional 3-Phase bridges, whereas the latter provides the proper input polarities for implementing double-forward converter configurations.

Table 3 deals with PWM stimulus and overcurrent shutdown provisions. When a user wants to supply external control signals for the driver, the HIP4086 provides a means for bringing in separate external PWM stimuli. This is accomplished through JP1 jumpers across terminals 3-4, 5-6 and 7-8. The single low-side connected shunt, SH3, triggers the U5B comparator with latching hysteresis added. The output of the comparator will drive the HIP4086 DIS pin if JP1 pin 1 is jumpered to JP1 pin 2. This jumper can be pulled when the user wishes to employ external current sense through use of the current-sensing shunts.

Table 4 shows how to connect the loads for the different configurations shown. Please refer to the schematic in Figure 10.

Printed Circuit Board Layout

Eventually you will want to produce your own printed circuit board layout. As with any high frequency circuit, short wire runs within the power circuit, good ground plane techniques, and proper bias supply and high voltage bus bypassing techniques are important. The section, Layout Problems and Effects, in AN9405 [3] is a good resource as the comments therein apply generally to all IC MOSFET gate drivers.

References

For Intersil documents available on the internet, see web site www.intersil.com/

[1] HIP4086 Data Sheet, Intersil Corporation

[2] AN9404 "HIP4080A, 80V High Frequency H-Bridge Driver", Intersil Corp., March, 1995.

[3] AN9405 "HIP4081A, 80V High Frequency H-Bridge Driver", Intersil Corp., March, 1995.

[4] AN9611 "A DC-AC Isolated Battery Inverter Using the HIP4082", Intersil Corp., May, 1996.

TABLE 2.

CONFIGURATION	ON BOARD PWM STIMULUS	LOW-SIDE			HIGH-SIDE		
		A	B	C	A	B	C
3-Phase Bridge (Figure 5)	Yes	25-26	19-20	13-14	23-24	17-18	11-12
3-Upper, 3-Lower (Figure 5)	Yes	25-26	19-20	13-14	23-24	17-18	11-12
3-Double Forward Converter (Figure 7)	Yes	25-26	19-20	13-14	21-22	15-16	9-10
Multiple Load Drive (Figure 8)	Yes	25-26	19-20	13-14	21-22	15-16	9-10
All Configurations	No	EXT-26	EXT-20	EXT-14	EXT-24	EXT-18	EXT-12

NOTES:

3. JP1 is shown in Figure 12 schematic.
4. "EXT" refers to external logic level stimulus supplied by user.
5. The "3-Upper/3-Lower" configuration can also be jumpered like the 3-double-forward converter configuration.
6. When both upper and lower MOSFETs are to be simultaneously on, tie the RDEL pin to V_{SS}.

TABLE 3.

FUNCTION	JP1 CONNECTIONS				
	LOW AND HIGH A	LOW AND HIGH B	LOW AND HIGH C	LOW-SIDE CURRENT SENSE (SH3)	HIGH-SIDE CURRENT SENSE (SH1, SH2)
On Board PWM Stimulus	7-8	3-4	5-6		
On Board Overcurrent Shutdown				1-2	
Off Board Overcurrent Shutdown				Note 8	Note 9

NOTES:

7. Use Potentiometer, P1, to control PWM pulse width.
8. Off board current sense amplifier input connected to pin 3 and 2 of SH1. Remove jumper, JP1, pins 1-2.
9. Off board current sense amplifier input connected to pins 1 and 2 of JP2 (SH1) or JP2 pins 3 and 4 (SH2). Off board control circuit controls upper FET PWM for current control in multiple drive or double forward configurations.

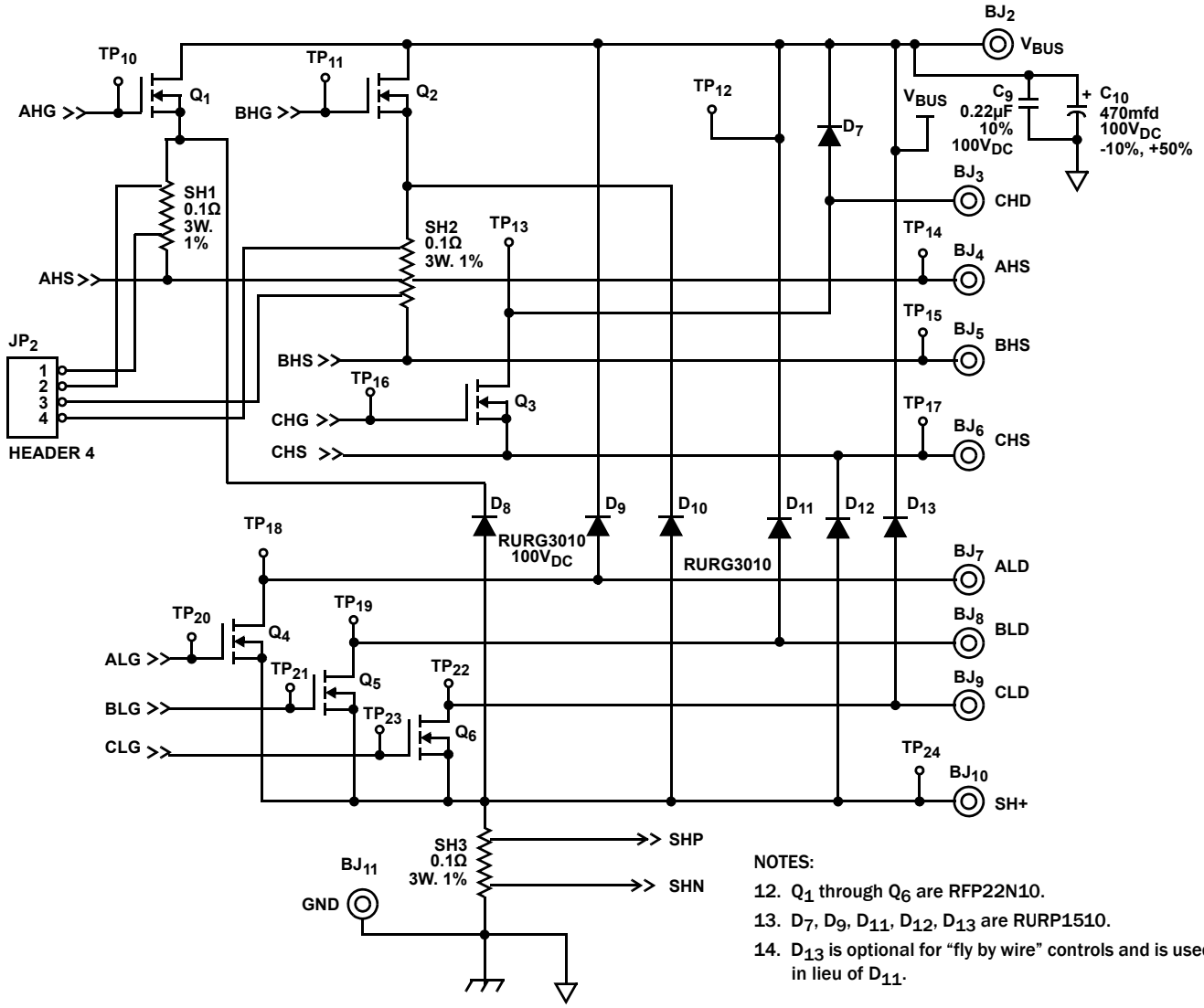
TABLE 4.

CONFIGURATION	LOAD CONNECTION					
	LOAD 1	LOAD 2	LOAD 3	LOAD 4	LOAD 5	LOAD 6
3-Upper, 3-Lower	BJ4 - BJ11	BJ4 - BJ11	BJ6 - BJ11	BJ7 - BJ2	BJ8 - BJ2	BJ9 - BJ2
3-Phase Bridge (Note 10)	BJ4 to BJ5	BJ5 to BJ6	BJ6 to BJ4	NA	NA	NA
3-Double Forward Converter	BJ4 - BJ7	BJ8 - BJ5	BJ9 - BJ6	NA	NA	NA
Multiple Load Drive (Note 11)	BJ7 - BJ4	BJ8 - BJ4	BJ9 - BJ4	BJ3 - BJ4	NA	NA

NOTES:

10. Before connecting loads, jumper BJ4 to BJ7, BJ5 to BJ8 and BJ6 to BJ9 and BJ2 to BJ3.
11. Maximum of 4 low-side FETs can be driven with this EVAL BD. In addition to connecting loads as shown in the table, jumper BJ6 to BJ10. Q2 is not used and Q3 becomes a low-side switch.

Appendix



NOTES:

12. Q_1 through Q_6 are RFP22N10.
13. D_7, D_9, D_{11}, D_{12}, D_{13} are RURP1510.
14. D_{13} is optional for “fly by wire” controls and is used in lieu of D_{11}.

FIGURE 10.

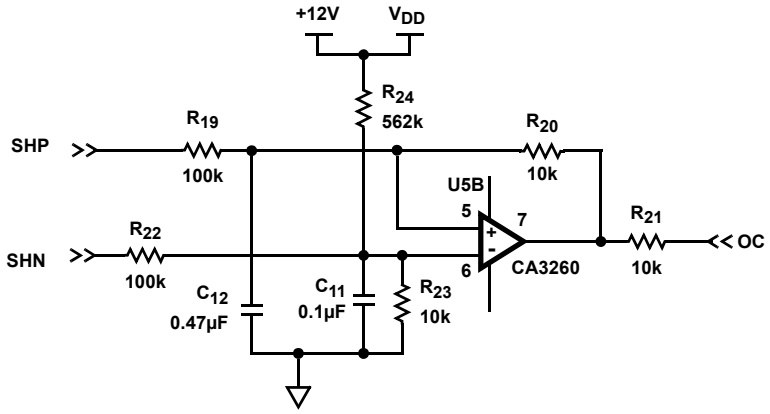
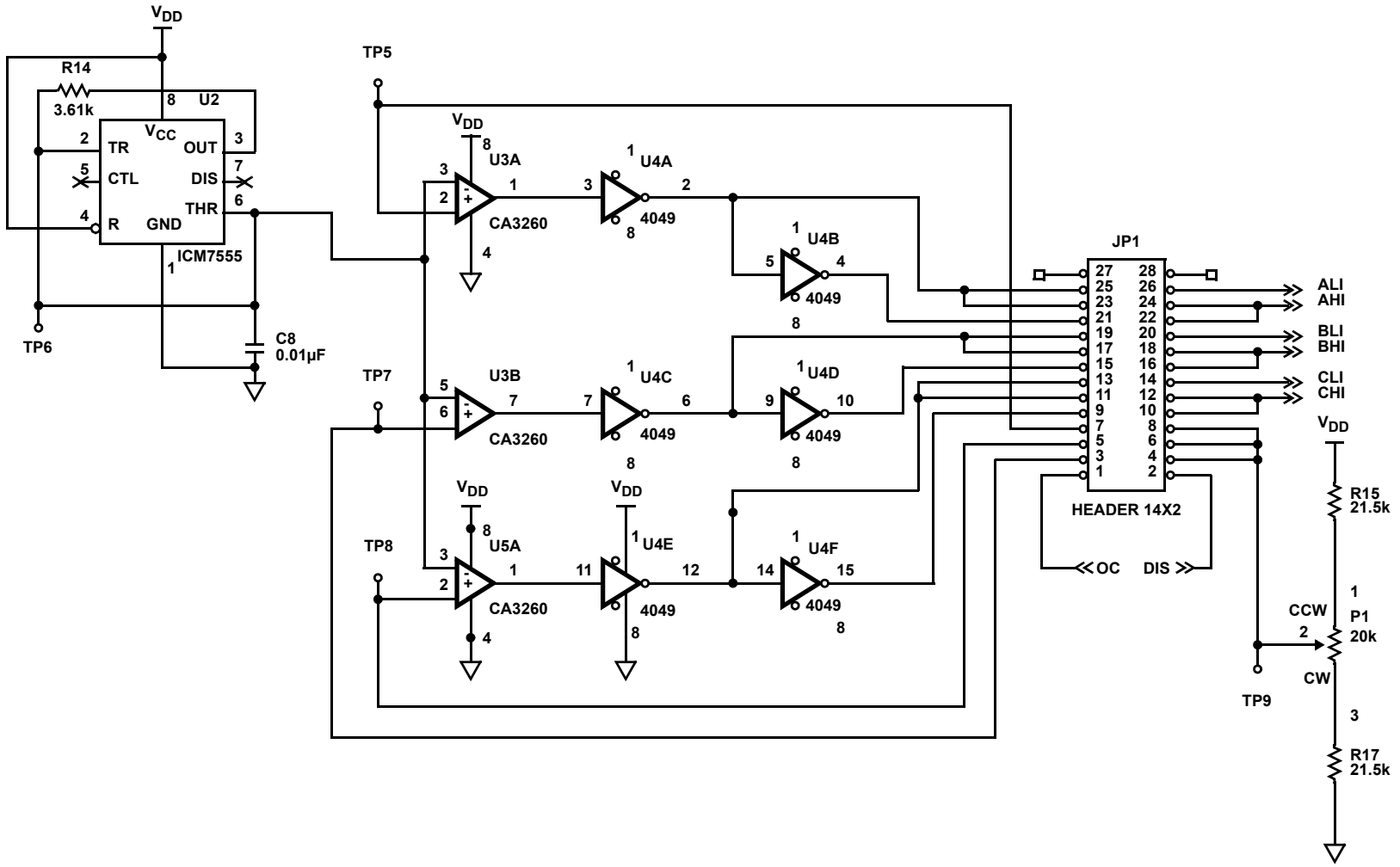


FIGURE 11.

Appendix (Continued)



NOTES:

15. Insert 20k resistor in JP1 pin 13 to 14 for UVLO setting.
16. Insert 100pF capacitor in JP1 pin 17 to 18 for refresh adjustment.
17. Jumper JP1, pin 19 to 20 to activate O/C shutdown.

FIGURE 12.

Appendix (Continued)

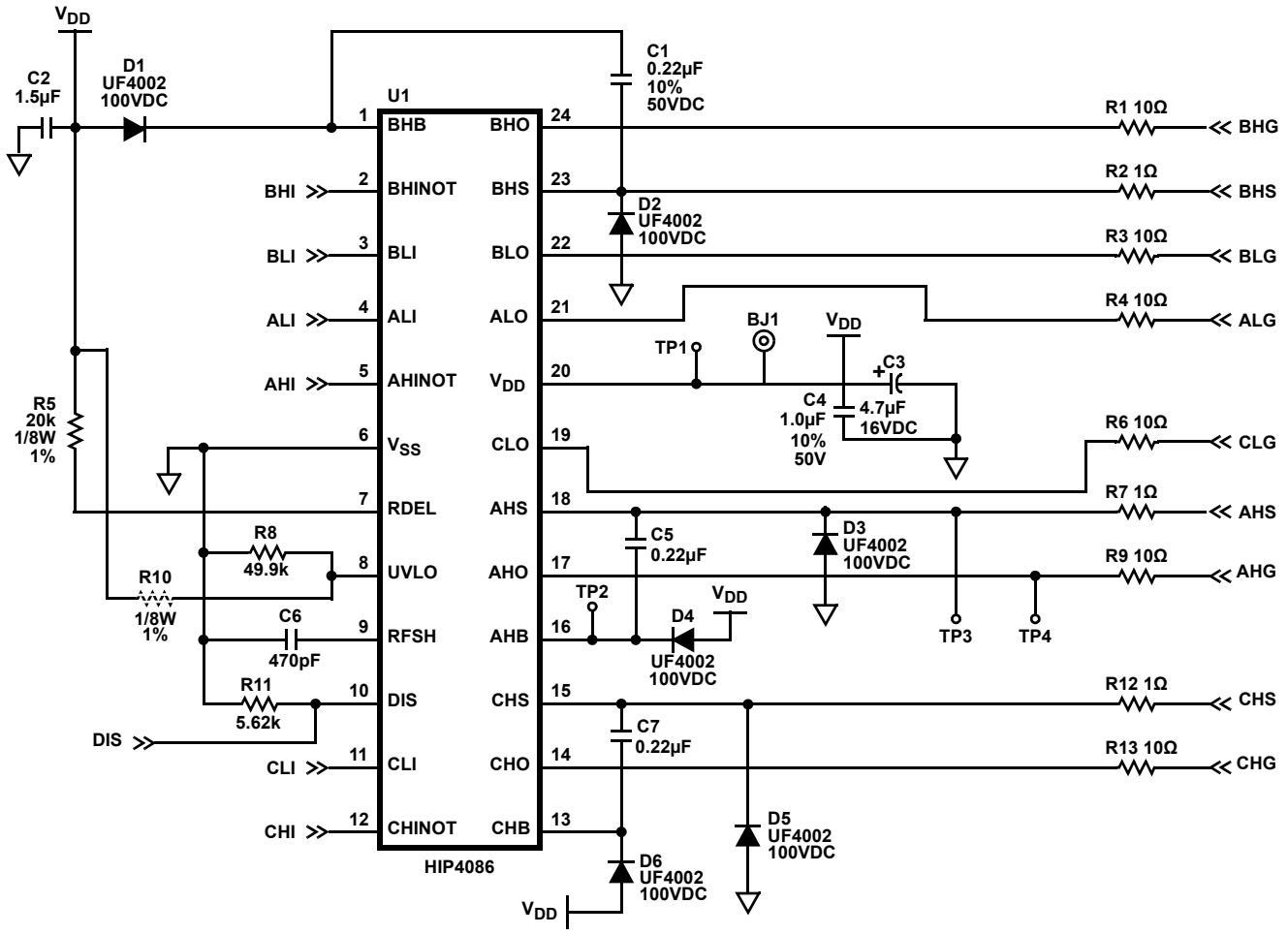


FIGURE 13.