9.8 mΩ, Nanopower Mobile 6 A Load Switch with Discharge

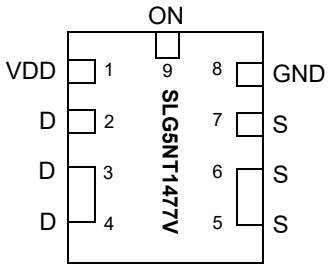
General Description

The SLG5NT1477V is a 9.8 mΩ, 6 A single-channel load switch that is able to switch 0.85 V to 3.3 V power rails. The product is packaged in an ultra-small 1.5 x 2.0 mm package.

Features

- 1.5 x 2.0 mm FC-TDFN 9L package (2 fused pins for drain and 2 fused pins for source)
- Logic level ON pin capable of supporting 0.85 V CMOS Logic
- Discharged Load when off
- Fast Turn On time
- Low RDS_{ON} while supporting 6 A
- Pb-Free / Halogen-Free / RoHS compliant
- Operating Temperature: -40 °C to 85 °C
- Operating Voltage: 3.0 V to 5.25 V

Pin Configuration

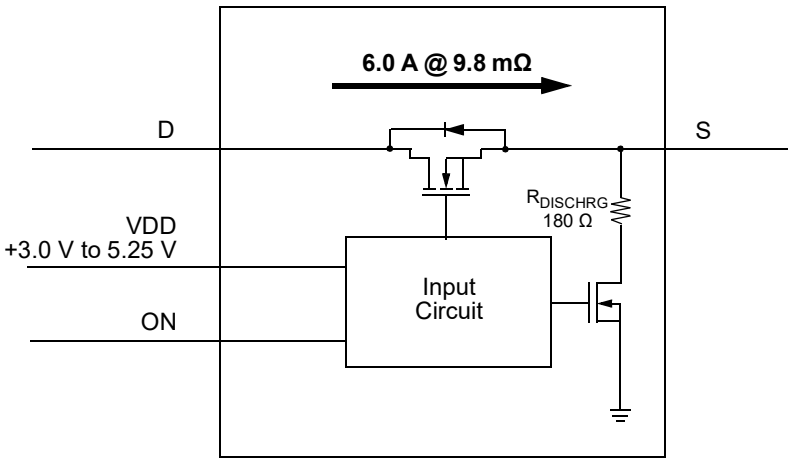


9-pin FC-TDFN
(Top View)

Applications

- Watch Power Rail Switching
- Tablet Power Rail Switching
- Smartphone Power Rail Switching
- Notebook Power Rail Switching

Block Diagram



RoHS Compliant
Directive
2002/95/EC

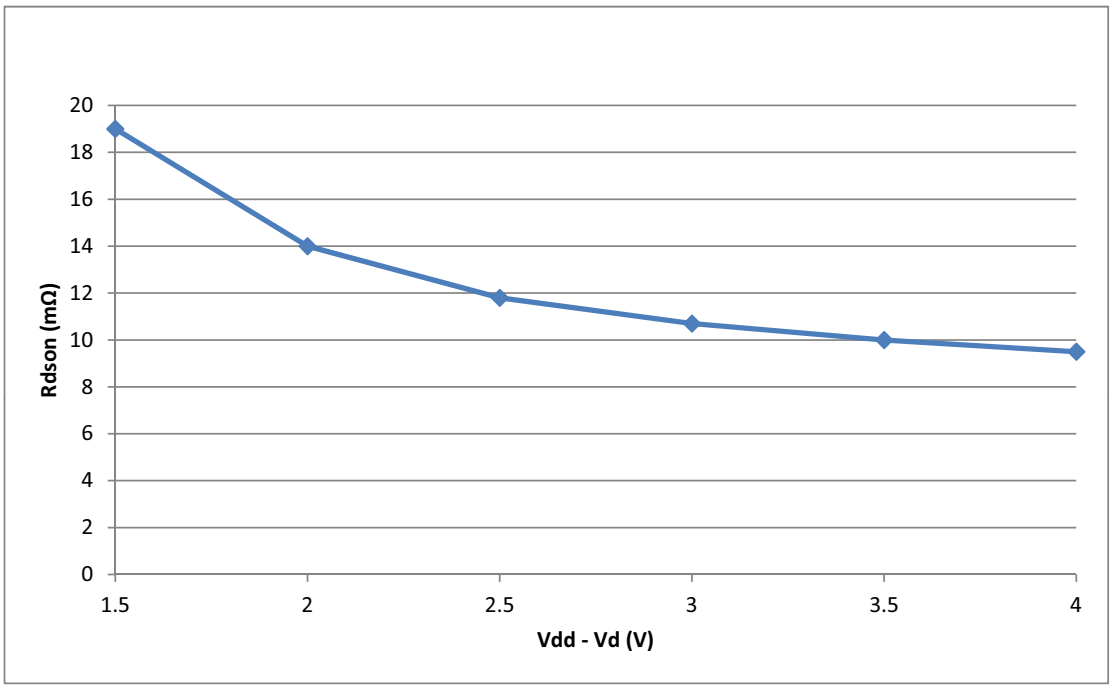
Pin Description

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	VDD power for load switch control (3.0 V to 5.25 V)
2	D	MOSFET	Drain of Power MOSFET
3	D	MOSFET	Drain of Power MOSFET (fused with pin 4)
4	D	MOSFET	Drain of Power MOSFET (fused with pin 3)
5	S	MOSFET	Source of Power MOSFET (fused with pin 6)
6	S	MOSFET	Source of Power MOSFET (fused with pin 5)
7	S	MOSFET	Source of Power MOSFET
8	GND	GND	Ground
9	ON	Input	Turns MOSFET ON (4 MΩ pull down resistor) CMOS input with ON_V_{IL} < 0.2 V, ON_V_{IH} > 0.85 V

Ordering Information

Part Number	Type	Production Flow
SLG5NT1477V	FC-TDFN 9L	Industrial, -40 °C to 85 °C
SLG5NT1477VTR	FC-TDFN 9L (Tape and Reel)	Industrial, -40 °C to 85 °C

SLG5NT1477V RDS_{ON}



Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply		--	--	7	V
T_S	Storage Temperature		-65	--	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
MSL	Moisture Sensitivity Level		1			
W_{DIS}	Package Power Dissipation		--	--	1.0	W
MOSFET IDS_{PK}	Peak Current from Drain to Source	For no more than 1 ms with 1% duty cycle	--	--	9	A

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

T_A = -40 °C to 85 °C (unless otherwise noted)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage	-40 °C to 85 °C	3.0	--	5.25	V
I_{DD}	Power Supply Current (PIN 1) [1]	when OFF, T_A = 25 °C	--	30	60	nA
		when ON, No load, ON = V_{DD}, T_A = 25 °C	--	35	70	nA
		when OFF, T_A = 70 °C	--	100	900	nA
		when ON, No load, ON = V_{DD}, T_A = 70 °C	--	200	900	nA
RDS_{ON}	ON Resistance	T_A = 25 °C; I_{DS} = 300 mA, V_{DD} - V_D = 1.5 V	--	16.2	18.6	mΩ
		T_A = 25 °C; I_{DS} = 300 mA, V_{DD} - V_D = 2.0 V	--	11.5	13.2	mΩ
		T_A = 25 °C; I_{DS} = 300 mA, V_{DD} - V_D = 2.5 V	--	9.5	10.9	mΩ
		T_A = 25 °C; I_{DS} = 300 mA, V_{DD} - V_D = 3.0 V	--	8.5	9.8	mΩ
		T_A = 25 °C; I_{DS} = 300 mA, V_{DD} - V_D = 3.5 V	--	7.9	9.1	mΩ
		T_A = 25 °C; I_{DS} = 300 mA, V_{DD} - V_D = 4.0 V	--	7.4	8.5	mΩ
RDS_{ON}	ON Resistance	T_A = 70 °C; I_{DS} = 300 mA, V_{DD} - V_D = 1.5 V	--	19.2	22.1	mΩ
		T_A = 70 °C; I_{DS} = 300 mA, V_{DD} - V_D = 2.0 V	--	14.1	16.2	mΩ
		T_A = 70 °C; I_{DS} = 300 mA, V_{DD} - V_D = 2.5 V	--	11.7	13.5	mΩ
		T_A = 70 °C; I_{DS} = 300 mA, V_{DD} - V_D = 3.0 V	--	10.5	12.1	mΩ
		T_A = 70 °C; I_{DS} = 300 mA, V_{DD} - V_D = 3.5 V	--	9.7	11.2	mΩ
		T_A = 70 °C; I_{DS} = 300 mA, V_{DD} - V_D = 4.0 V	--	9.2	10.6	mΩ
RDS_{ON}	ON Resistance	T_A = 85 °C; I_{DS} = 300 mA, V_{DD} - V_D = 1.5 V	--	24.96	28.73	mΩ
		T_A = 85 °C; I_{DS} = 300 mA, V_{DD} - V_D = 2.0 V	--	18.33	21.06	mΩ
		T_A = 85 °C; I_{DS} = 300 mA, V_{DD} - V_D = 2.5 V	--	15.21	17.55	mΩ
		T_A = 85 °C; I_{DS} = 300 mA, V_{DD} - V_D = 3.0 V	--	13.65	15.73	mΩ
		T_A = 85 °C; I_{DS} = 300 mA, V_{DD} - V_D = 3.5 V	--	12.61	14.56	mΩ
		T_A = 85 °C; I_{DS} = 300 mA, V_{DD} - V_D = 4.0 V	--	11.96	13.78	mΩ
MOSFET IDS	Current from D to S	Continuous	--	--	6	A
V_D	Drain Voltage		0.85	--	V_{DD} - 1.5	V

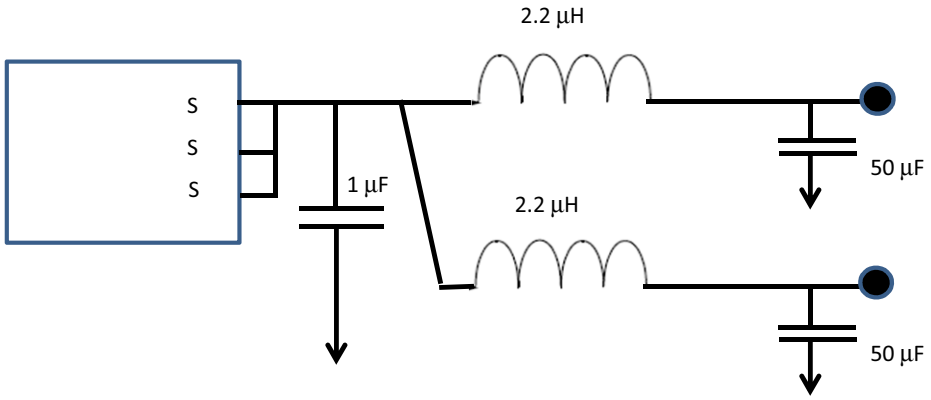
Electrical Characteristics (continued)

T_A = -40 °C to 85 °C (unless otherwise noted)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
T_{Total_ON}	Total Turn On Time	50% ON to 90% V_S, V_{DD} = 5.25 V, V_D = 1.0 V, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω	7	9	12	µs
		50% ON to 90% V_S, V_{DD} = 5.25 V, V_D = 1.0 V, C_{LOAD} = 2 µF, R_{LOAD} = 20 Ω	8	10	12	µs
		50% ON to 90% V_S, V_{DD} = 5 V, V_D = 1.0 V, C_{LOAD} = 2 x (50 µF + 2.2 µH Inductor) [2]	30	42	50	µs
$V_{S(SR)}$	V_S Slew Rate	10% V_S to 90% V_S, V_{DD} = 5.25 V, V_D = 1.0 V, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω	130	160	190	V/ms
		10% V_S to 90% V_S, V_{DD} = 5.25 V, V_D = 1.0 V, C_{LOAD} = 2 µF, R_{LOAD} = 20 Ω	150	176	200	V/ms
		10% V_S to 90% V_S, V_{DD} = 5 V, V_D = 1.0 V, R_{LOAD} = 20 Ω, C_{LOAD} = 2 x (50 µF + 2.2 µH Inductor) [2]	20	26	35	V/ms
C_{LOAD}	Output Load Capacitance	C_{LOAD} connected from S to GND	--	--	10	µF
$R_{DISCHRG}$	Discharge Resistance		100	180	300	Ω
ON_V_{IH}	High Input Voltage on ON pin		0.85	--	V_{DD}	V
ON_V_{IL}	Low Input Voltage on ON pin		-0.3	0	0.2	V
T_{OFF_Delay}	OFF Delay Time	50% ON to V_S Fall Start ↓, V_{DD} = 5.25 V, V_D = 1.0 V, R_{LOAD} = 20 Ω, no C_{LOAD}	--	--	60	µs
T_{FALL}	V_S Fall Time	90% V_S to 10% V_S, V_{DD} = 5.25 V, V_D = 1.0 V, R_{LOAD} = 20 Ω, no C_{LOAD}	--	15	--	µs

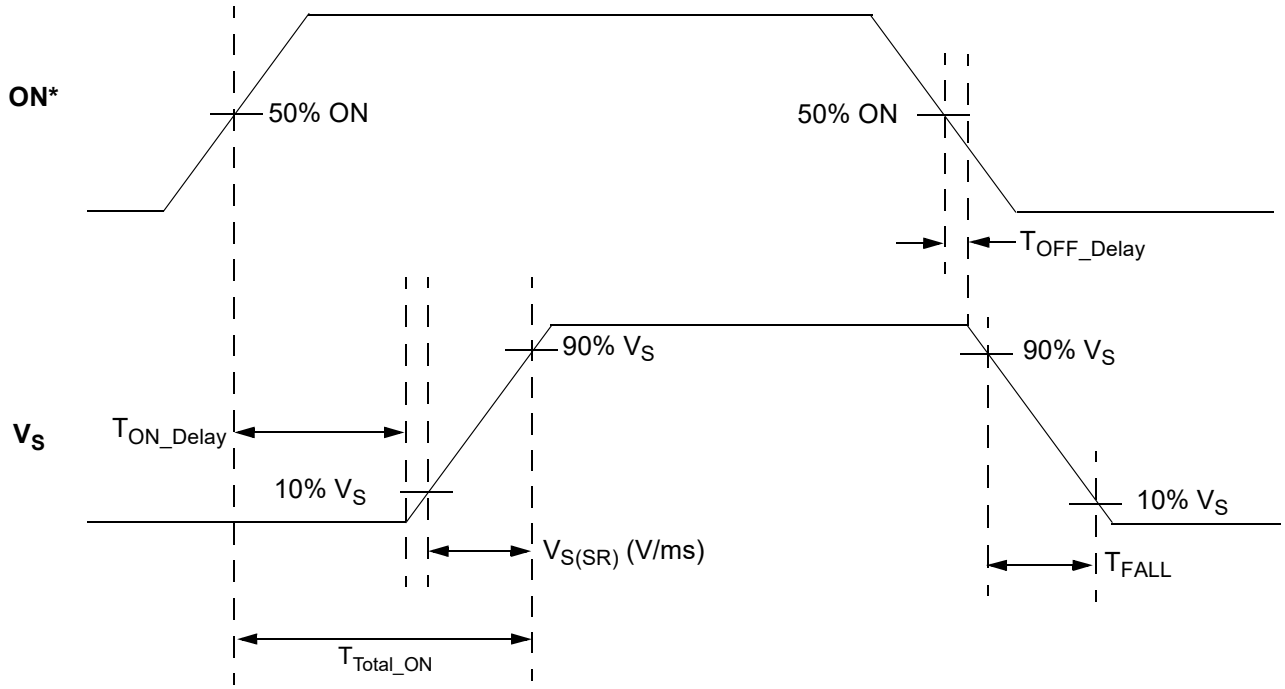
Notes:
1. Guaranteed by design and characterization
2. See Application Diagram below regarding C_{LOAD} = 2 x (50 µF + 2.2 µH).

Application Diagram (Source loading > 10 µF)



Capacitive loads > 10 µF directly on the S pin may result in nonlinear output ramping. In cases where > 10 µF load capacitance is required, we recommend decoupling the load(s) with 2.2 µH inductors while putting a 1 µF capacitor on S as shown above in order to guarantee linear ramping and inrush current limiting.

T_{Total_ON}, T_{ON_Delay} and Slew Rate Measurement



*Rise and Fall Times of the ON Signal are 100 ns

Layout Guidelines:

1. The VDD pin needs a 0.1 µF and 10 µF external capacitors to smooth pulses from the power supply. Locate these capacitors as close as possible to the SLG5NT1477V's PIN1.

2. Since the D and S pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with absolute minimum widths of 15 mils (0.381 mm) per Ampere. A representative layout, shown in Figure 1, illustrates proper techniques for heat to transfer as efficiently as possible out of the device;

3. To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input C_{IN} and output C_{LOAD} low-ESR capacitors as close as possible to the SLG5NT1477V's D and S pins;

4. The GND pin should be connected to system analog or power ground plane.

5. 2 oz. copper is recommended for high current operation.

SLG5NT1477V Evaluation Board:

A GreenFET Evaluation Board for SLG5NT1477V is designed according to the statements above and is illustrated on Figure 1. Please note that evaluation board has D_Sense and S_Sense pads. They cannot carry high currents and dedicated only for RDS_{ON} evaluation.

Please solder your SLG5NT1477V here

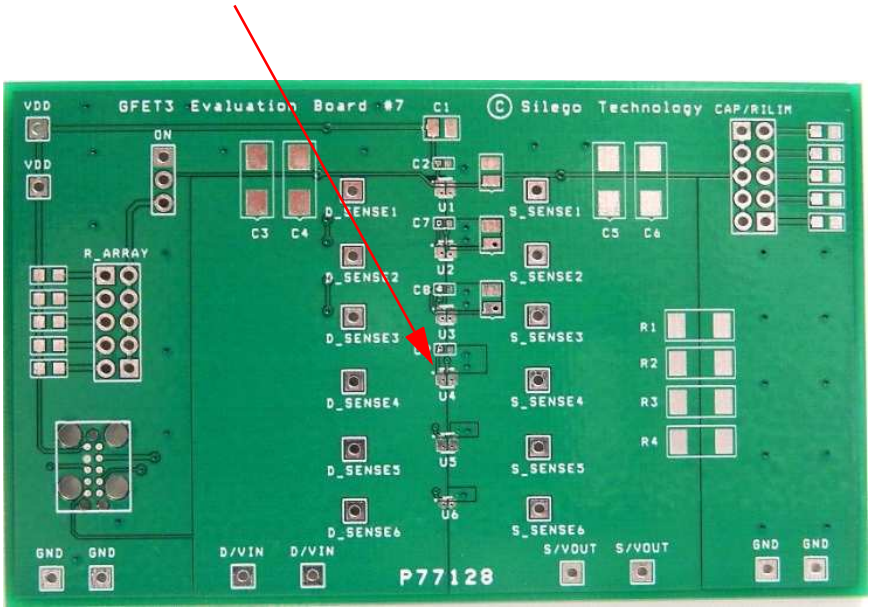


Figure 1. SLG5NT1477V Evaluation Board

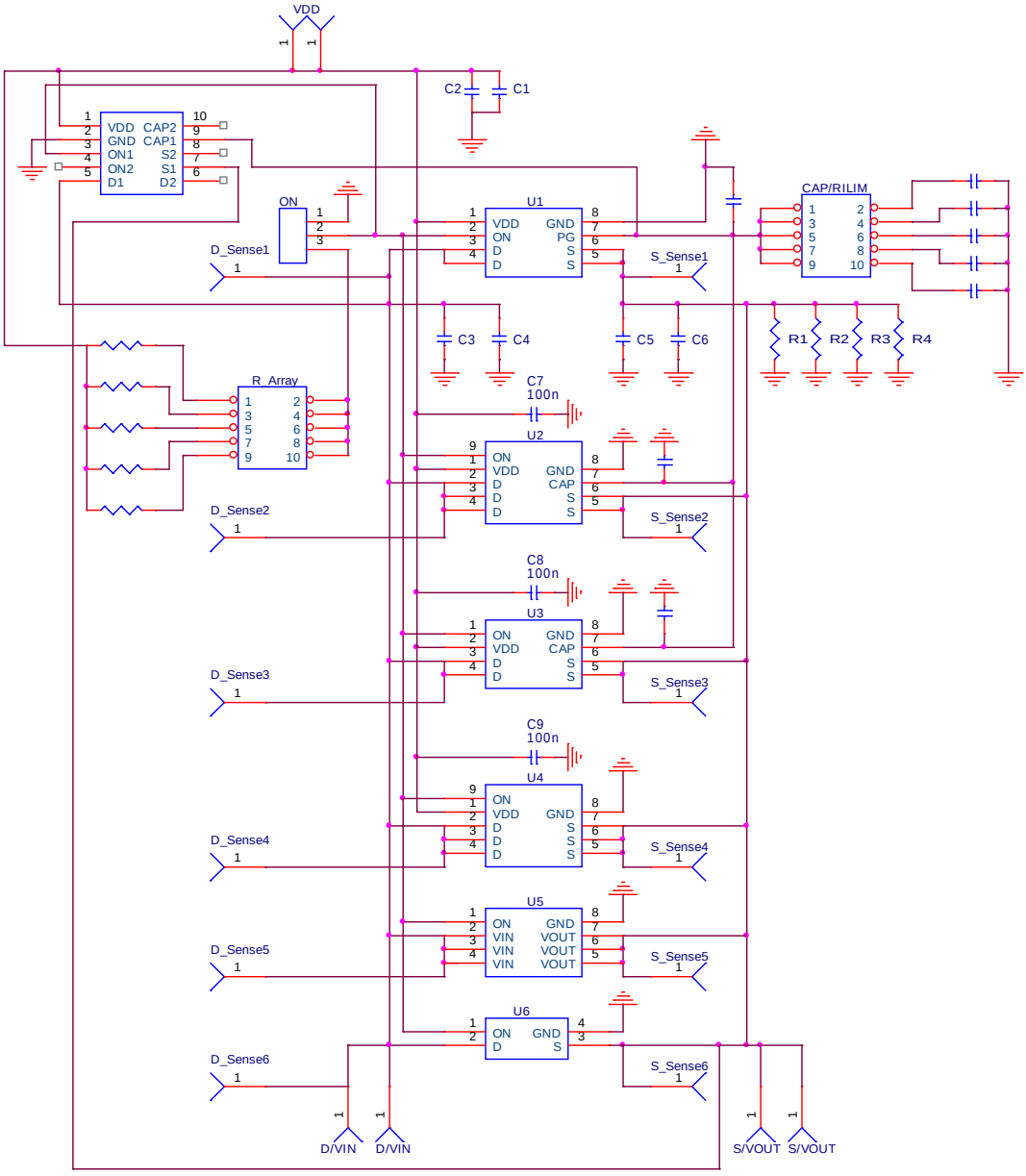


Figure 2. SLG5NT1477V Evaluation Board Connection Circuit

Basic Test Setup and Connections

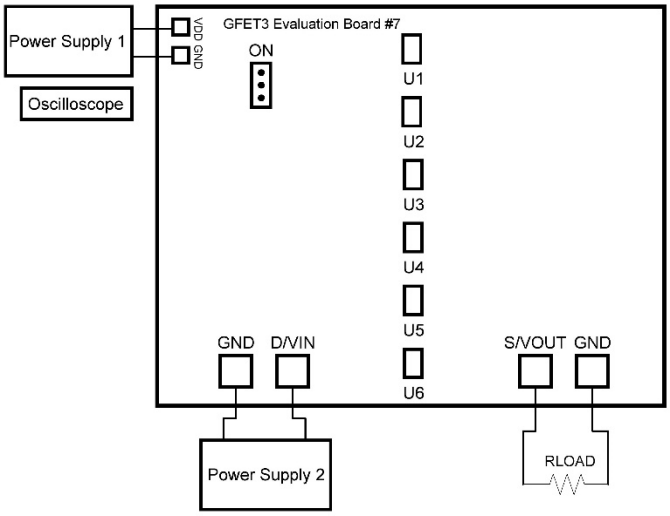
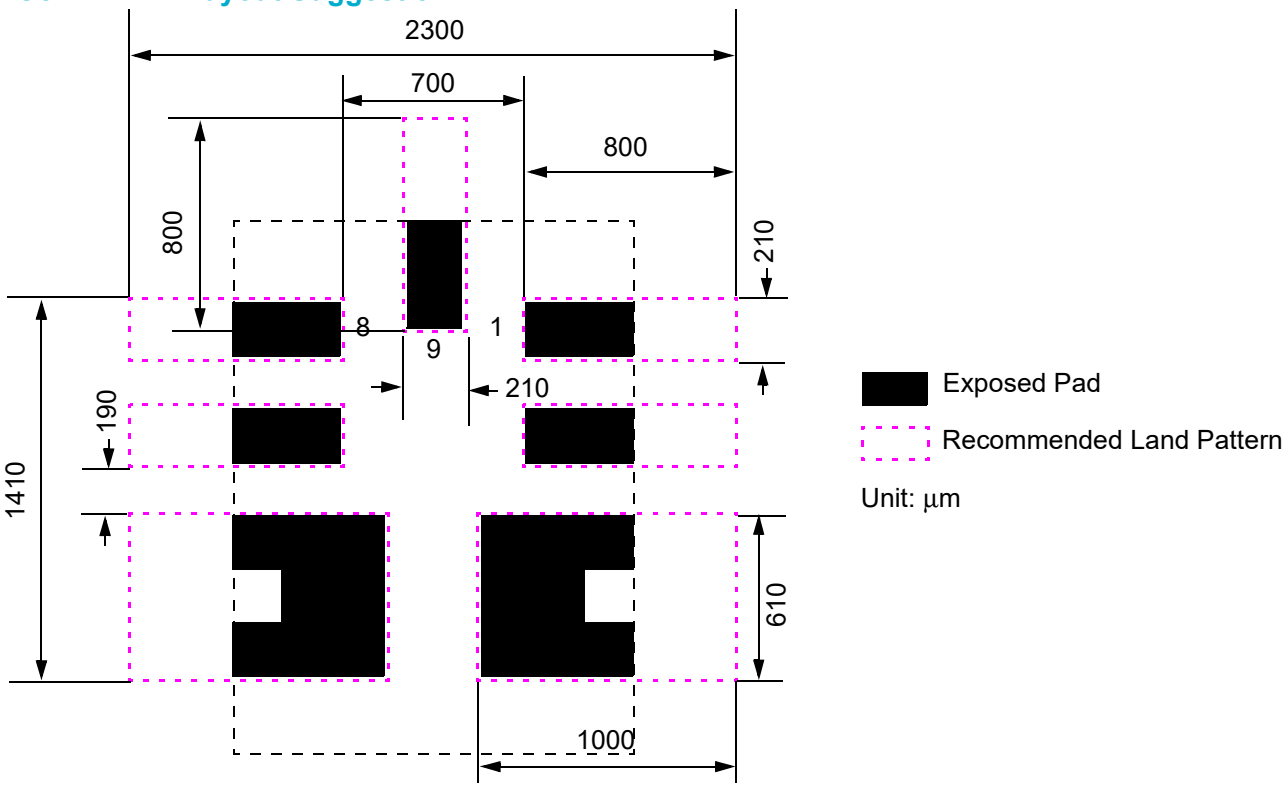


Figure 3. SLG5NT1477V Evaluation Board Connection Circuit

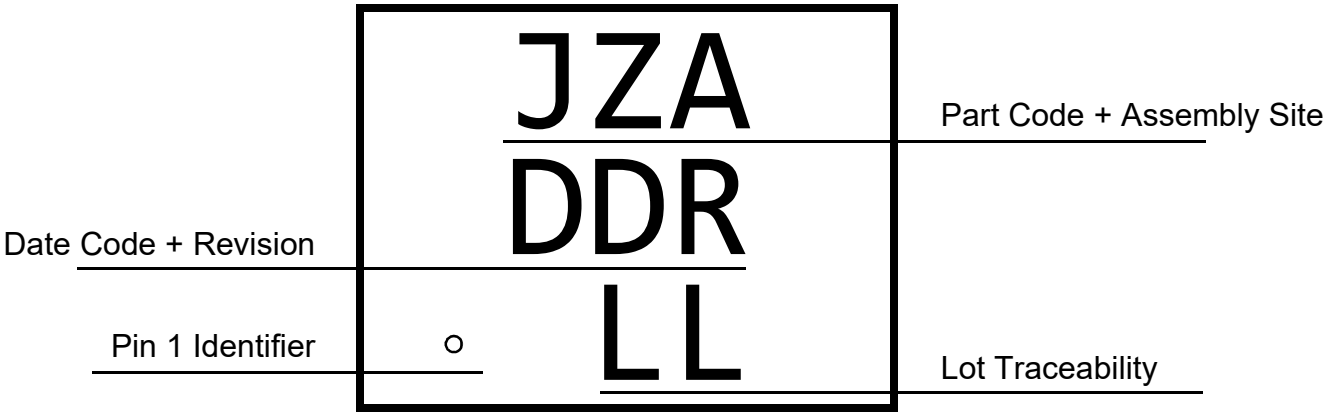
EVB Configuration

1. Connect oscilloscope probes to D/VIN, S/VOUT, ON, etc.;
2. Turn on Power Supply 1 and set desired V_{DD} from 3 V…5.25 V range;
3. Turn on Power Supply 2 and set desired V_D from 0.85 V…V_{DD} - 1.5 V range;
4. Toggle the ON signal High or Low to observe SLG5NT1477V operation.

SLG5NT1477V Layout Suggestion



Package Top Marking System Definition

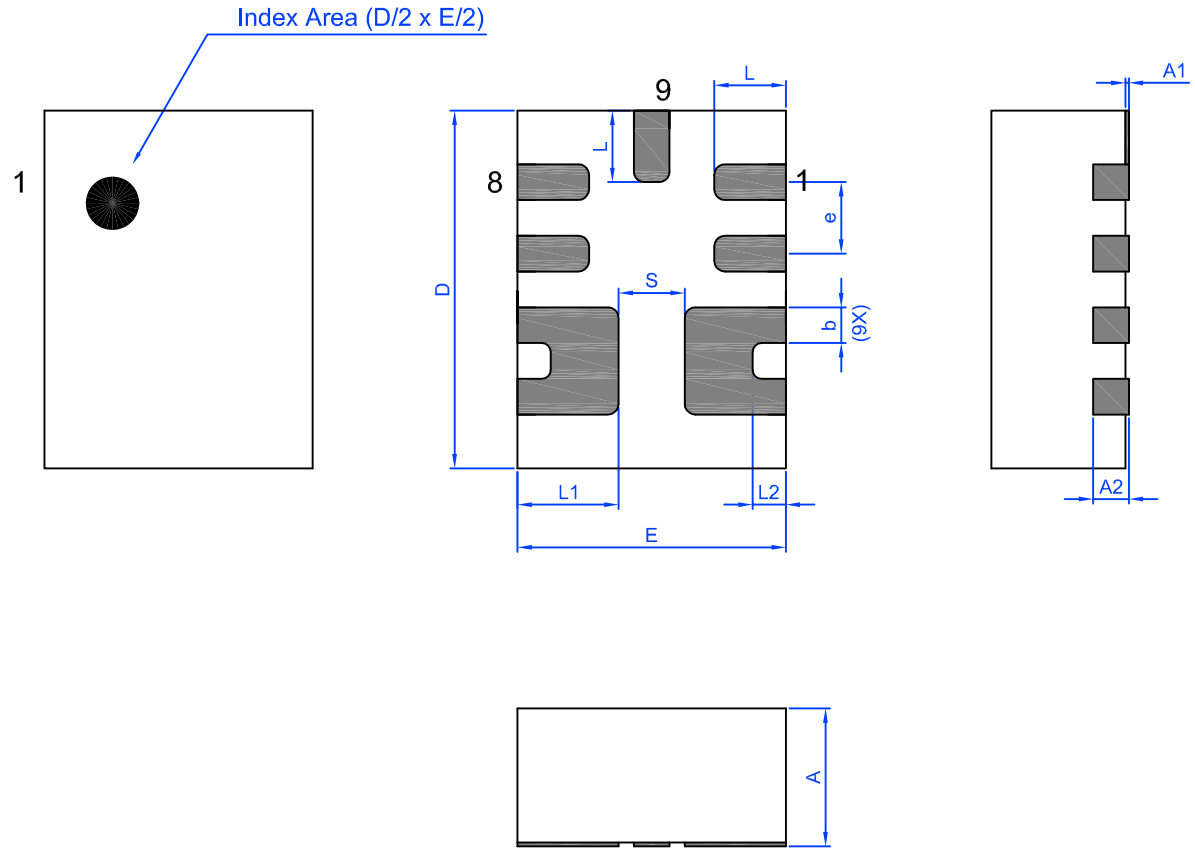


JZ - Part Code[1]
A - Assembly Site Code Field[2]
DD - Date Code Field[1]
R - Part Revision Code Field[2]
LL - Lot Traceability Field[1]

Note 1: Each character in code field can be alphanumeric A-Z and 0-9
Note 2: Character in code field can be alphabetic A-Z

Package Drawing and Dimensions

9 Lead TDFN FC Package 1.5 x 2.0 mm (Fused Lead)
JEDEC MO-252, Variation W2015D



Unit: mm

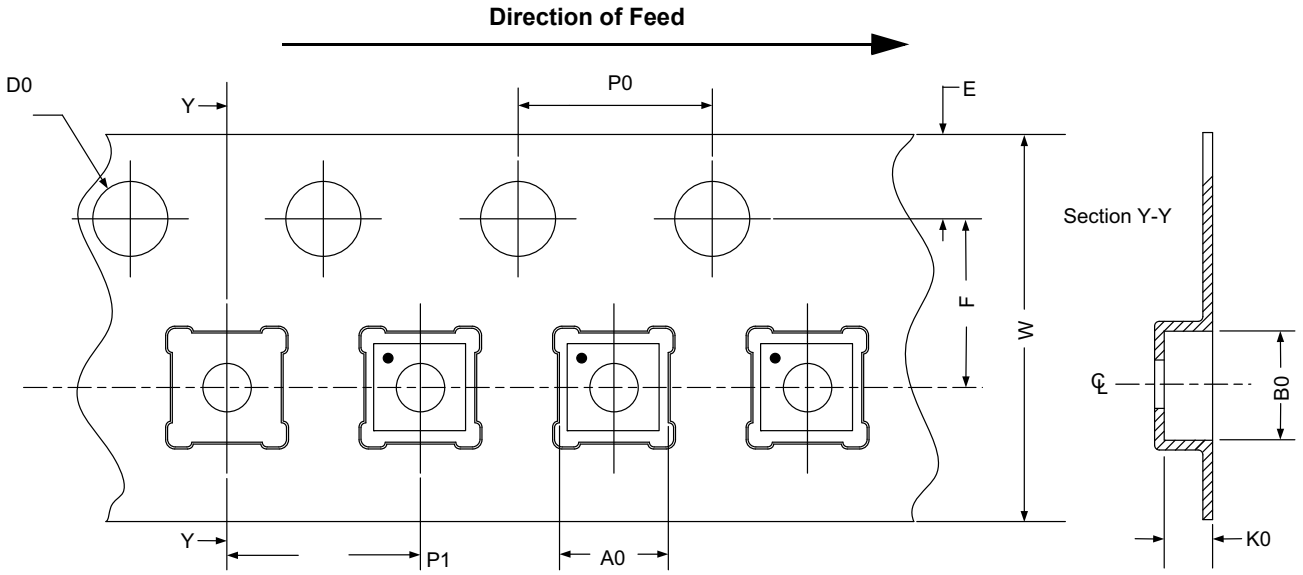
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.70	0.75	0.80	L	0.35	0.40	0.45
A1	0.005	-	0.060	L1	0.515	0.565	0.615
A2	0.15	0.20	0.25	L2	0.135	0.185	0.235
b	0.15	0.20	0.25	e	0.40 BSC		
D	1.95	2.00	2.05	S	0.37 REF		
E	1.45	1.50	1.55				

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
TDFN 9L FC Green	9	1.5 x 2.0 x 0.75	3000	3000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
TDFN 9L FC Green	1.70 ±0.05 mm	2.20 ±0.05 mm	0.95 +0.10 mm -0.05 mm	4	4	1.5	1.75	3.5	8



Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.25 mm^3 (nominal). More information can be found at www.jedec.org.

Revision History

Date	Version	Change
2/2/2022	1.29	Updated Company name and logo Fixed typos
11/3/2020	1.28	Updated Carrier Tape Drawing and Dimensions
6/5/2020	1.27	Updated style and formatting Added Layout Guidelines Add Tape and Reel Feed Direction Fixed typos
9/8/2016	1.26	Updated T_{Total_ON}, $V_{OUT(SR)}$, T_{OFF_Delay}, T_{FALL} specs Updated Application Diagram Notes Updated Formating and Parameter Names for clarity
4/26/2016	1.25	Added MSL 1 Added Part Code Marking Information
9/04/2015	1.24	Fixed T_A conditions in Electrical Characteristics

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