

## NP29N04QUK

40 V – 30 A – Dual N-channel Power MOS FET Application: Automotive

R07DS1329EJ0200 Rev. 2.00 May 24, 2018

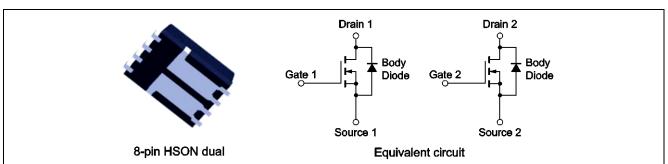
### **Description**

NP29N04QUK is a dual N-channel MOS Field Effect Transistor designed for high current switching applications.

#### **Features**

- Super low on-state resistance
  - $R_{DS(on)} = 10.1 \text{ m}\Omega \text{ MAX.} (V_{GS} = 10 \text{ V}, I_D = 15 \text{ A})$
- Low  $C_{iss}$ :  $C_{iss} = 1000 \text{ pF TYP.} (V_{DS} = 25 \text{ V})$
- Designed for automotive application and AEC-Q101 qualified
- Small size package 8-pin HSON dual

### **Outline**



Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

### **Ordering Information**

Part No.	Lead Plating	Pac	Package	
NP29N04QUK-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	8-pin HSON dual
NP29N04QUK -E2-AY *1			Taping (E2 type)	

Note: \*1. Pb-free (This product does not contain Pb in the external electrode)

### **Absolute Maximum Ratings** (T<sub>A</sub> = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	40	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	±20	V
Drain Current (DC) (T <sub>C</sub> = 25°C) *4	I <sub>D(DC)</sub>	±30	Α
Drain Current (pulse) *1, 4, 5	I <sub>D(pulse)</sub>	±60	Α
Total Power Dissipation (T <sub>C</sub> = 25°C) *4	P <sub>T1</sub>	44	W
Total Power Dissipation (T <sub>A</sub> = 25°C) *2,4	P <sub>T2</sub>	1.0	W
Channel Temperature	T <sub>ch</sub>	175	°C
Storage Temperature	T <sub>stg</sub>	−55 to +175	°C
Repetitive Avalanche Current *3, 5	I <sub>AR</sub>	17	Α
Repetitive Avalanche Energy *3,5	E <sub>AR</sub>	30	mJ

### **Thermal Resistance**

Notes: \*1.  $T_C$  = 25°C, PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1%

<sup>\*2.</sup> Mounted on glass epoxy substrate of 40 mm  $\times$  40 mm  $\times$  1.6 mmt with 4% copper area (35  $\mu\text{m})$ 

<sup>\*3.</sup> Rg = 25  $\Omega$ , Vgs = 20 V  $\rightarrow$  0 V

<sup>\*4.</sup> One channel operation

<sup>\*5.</sup> Not subject of production test. Verified by design/characterization.

## **Electrical Characteristics** (T<sub>A</sub> = 25°C)

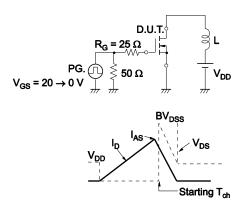
Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I <sub>DSS</sub>			1	μΑ	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$
Gate Leakage Current	I <sub>GSS</sub>			±100	nA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	2.0	3.0	4.0	V	$V_{DS} = V_{GS}, I_D = 250 \mu A$
Forward Transfer Admittance *1	y <sub>fs</sub>	10	17		S	$V_{DS} = 5 \text{ V}, I_{D} = 15 \text{ A}$
Drain to Source On-state Resistance *1	R <sub>DS(on)1</sub>		8.5	10.1	mΩ	$V_{GS} = 10 \text{ V}, I_D = 15 \text{ A}$
Input Capacitance *2	C <sub>iss</sub>		1000	1500	pF	$V_{DS} = 25 V$ ,
Output Capacitance *2	Coss		150	230	pF	$V_{GS} = 0 V$ ,
Reverse Transfer Capacitance *2	C <sub>rss</sub>		70	130	pF	f = 1 MHz
Turn-on Delay Time *2	t <sub>d(on)</sub>		14	28	ns	$V_{DD} = 20 \text{ V}, I_D = 15 \text{ A},$
Rise Time *2	t <sub>r</sub>		4	10	ns	$V_{GS} = 10 \text{ V},$
Turn-off Delay Time *2	t <sub>d(off)</sub>		30	60	ns	$R_G = 0 \Omega$
Fall Time *2	t <sub>f</sub>		6	15	ns	
Total Gate Charge *2	Q <sub>G</sub>		19	29	nC	$V_{DD} = 32 \text{ V},$
Gate to Source Charge	Q <sub>GS</sub>		6		nC	$V_{GS} = 10 \text{ V},$
Gate to Drain Charge	Q <sub>GD</sub>		5		nC	I <sub>D</sub> = 30 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$		0.9	1.5	V	I <sub>F</sub> = 30 A, V <sub>GS</sub> = 0 V
Reverse Recovery Time	t <sub>rr</sub>		30		ns	I <sub>F</sub> = 30 A, V <sub>GS</sub> = 0 V,
Reverse Recovery Charge	Qrr		31		nC	di/dt = 100 A/μs

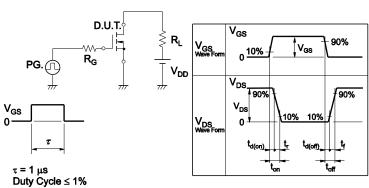
Note: \*1. Pulsed test

Note: \*2. Not subject of production test. Verified by design/characterization.

### **TEST CIRCUIT 1 AVALANCHE CAPABILITY**

## TEST CIRCUIT 2 SWITCHING TIME

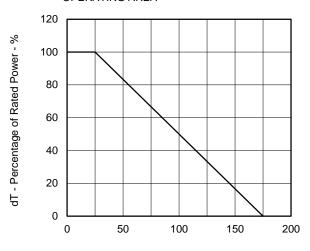




### **TEST CIRCUIT 3 GATE CHARGE**

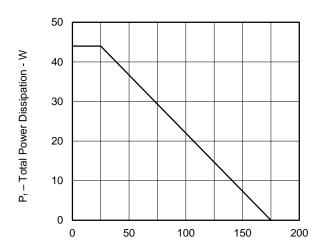
## **Typical Characteristics** (T<sub>A</sub> = 25°C)

# DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



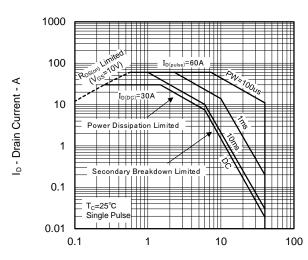
T<sub>C</sub> - Case Temperature - °C

## TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



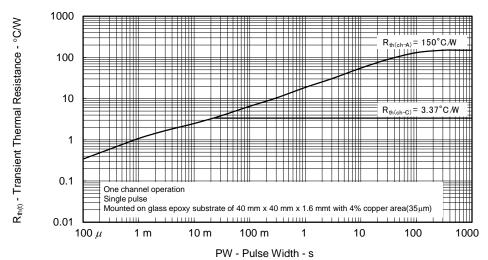
T<sub>C</sub> - Case Temperature - °C

#### FORWARD BIAS SAFE OPERATING AREA

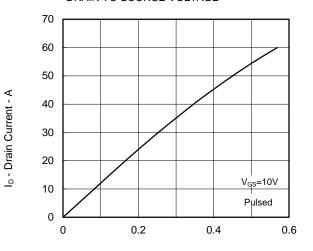


 $V_{\text{DS}}$  - Drain to Source Voltage  $-\,V$ 

#### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

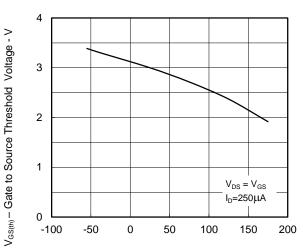


## DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



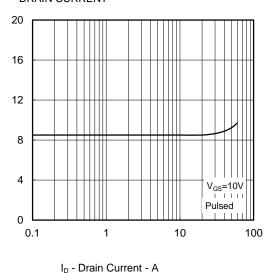
V<sub>DS</sub> - Drain to Source Voltage - V

# GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

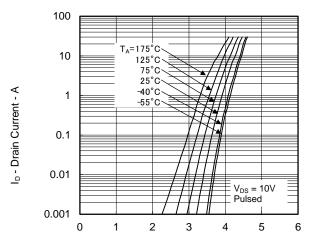


 $T_{\text{ch}}$  - Channel Temperature -  $^{\circ}C$ 

# DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

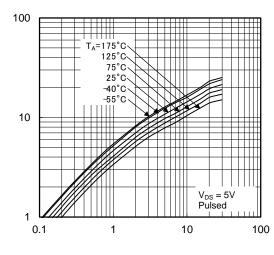


#### FORWARD TRANSFER CHARACTERISTICS



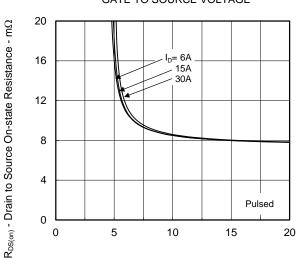
V<sub>GS</sub> - Gate to Source Voltage - V

# FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



I<sub>D</sub> - Drain Current - A

# DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



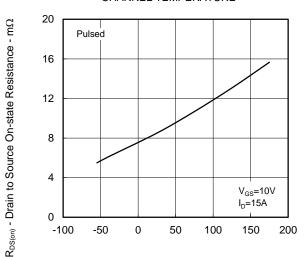
 $V_{\text{GS}}$  - Gate to Source Voltage - V

 $R_{\text{DS(on)}}$  - Drain to Source On-state Resistance -  $m\Omega$ 

| y<sub>fs</sub> | - Forward Transfer Admittance - S

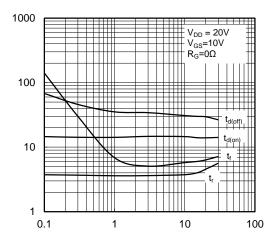
td(on),tr,td(off),tr - Switching Time - ns

## DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



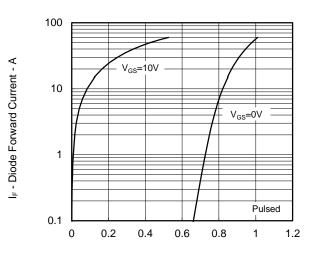
T<sub>ch</sub> - Channel Temperature - °C

#### SWITCHING CHARACTERISTICS



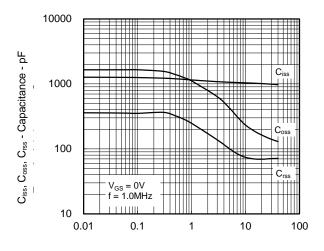
I<sub>D</sub> - Drain Current - A

#### SOURCE TO DRAIN DIODE FORWARD VOLTAGE



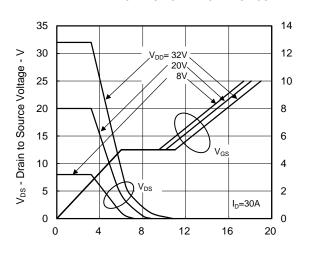
 $V_{F(S-D)}$  - Source to Drain Voltage - V

#### CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



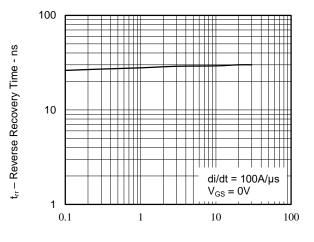
V<sub>DS</sub> - Drain to Source Voltage - V

#### DYNAMIC INPUT CHARACTERISTICS



Q<sub>G</sub> - Gate Charge - nC

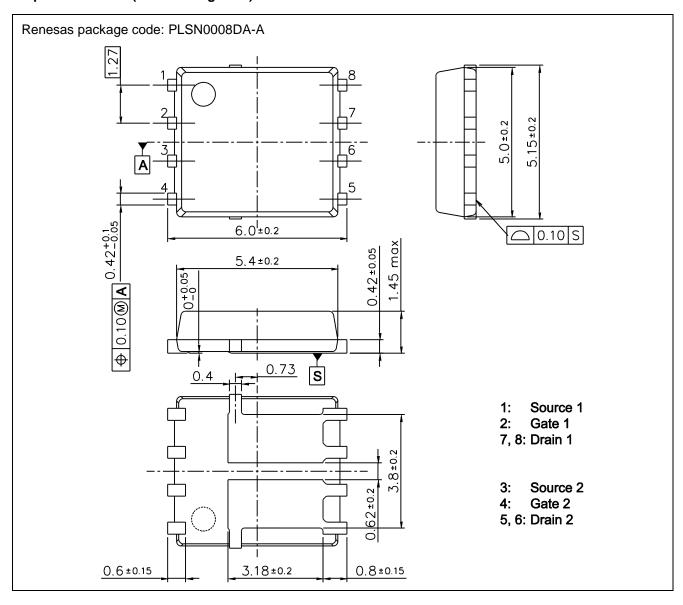
# REVERSE RECOVERY TIME vs. DRAIN CURRENT



IF - Drain Current - A

## Package Drawings (Unit: mm)

### 8-pin HSON Dual (Mass: 0.12 g TYP.)



**Revision History** 

## NP29N04QUK Data Sheet

		Description		
Rev.	Date	Page	Summary	
1.00	Mar 28, 2016	_	First Edition Issued	
2.00	May 24,2018	2	Note 5 was added	
		3	Note 2 was added	

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Renesas Electronics America Inc.

| Murphy Ranch Road, Milpitas, CA 95035, U.S.A. +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited 9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3 Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH

Arcadiastrasse 10, 40472 Düsseldorf, Germar Tel: +49-211-6503-0, Fax: +49-211-6503-132

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd. Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.

13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
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Renesas Electronics India Pvt. Ltd. No.777C, 100 Feet Road, HAL 2nd St

No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd. 17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea Tel: +82-2-558-3737, Fax: +82-2-558-5338