ISL80510

High Performance 1A LDO

FN8767
Rev 0.00
July 28, 2015

The ISL80510 is a single output Low Dropout voltage regulator (LDO) capable of sourcing up to 1A output current. This LDO operates from input voltages of 2.2V to 6V. The output voltage of ISL80510 can be programmed from 0.8V to 5.5V.

A submicron BiCMOS process is utilized for this product family to deliver the best in class analog performance and overall value. This CMOS LDO consumes significantly lower quiescent current as a function of load compared to bipolar LDOs, which translates into higher efficiency and packages with smaller footprints.

State-of-the-art internal compensation achieves a very fast load transient response and excellent PSRR. The ISL80510 provides an output accuracy of ±1.8% V_{OUT} accuracy over all load, line and temperature variation (T_J = -40°C to +125°C). An external capacitor on the soft-start pin provides an adjustable soft starting of the output voltage ramp to control the inrush current. The ENABLE feature allows the part to be placed into a low quiescent current shutdown mode.

Table 1 shows the differences between the ISL80510 and others in its family.

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART NUMBER	MAX OUTPUT CURRENT
ISL80510	1.0A
ISL80505	0.5A

Features

- ±1.8% V_{OUT} accuracy guaranteed over line, load and T_J = -40°C to +125°C
- Very low 130mV dropout voltage at V_{OUT} = 2.5V
- Stable with a 4.7µF output ceramic capacitor
- Very fast transient response
- Programmable output soft-start time
- Excellent PSRR over wide frequency range
- Current limit protection
- Thermal shutdown function
- Available in an 8 Ld DFN package
- Pb-free (RoHS compliant)

Applications

- Noise-sensitive instrumentation systems
- Post regulation of switched mode power supplies
- Industrial systems
- Medical equipment
- Telecommunications and networking equipment
- Servers
- Hard disk drives (HD/HDD)

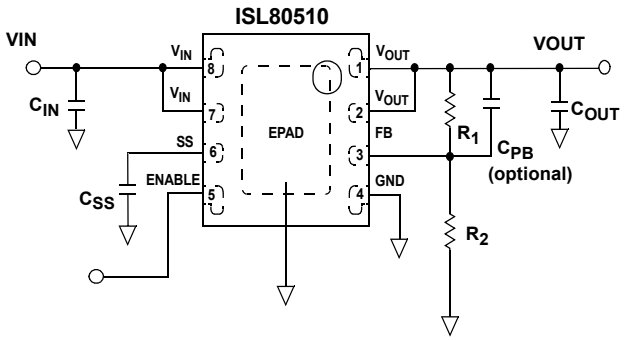


FIGURE 1. TYPICAL APPLICATION CIRCUIT

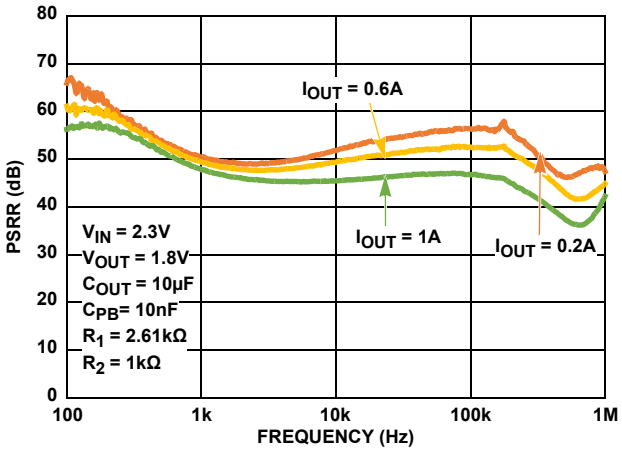


FIGURE 2. PSRR

Block Diagram

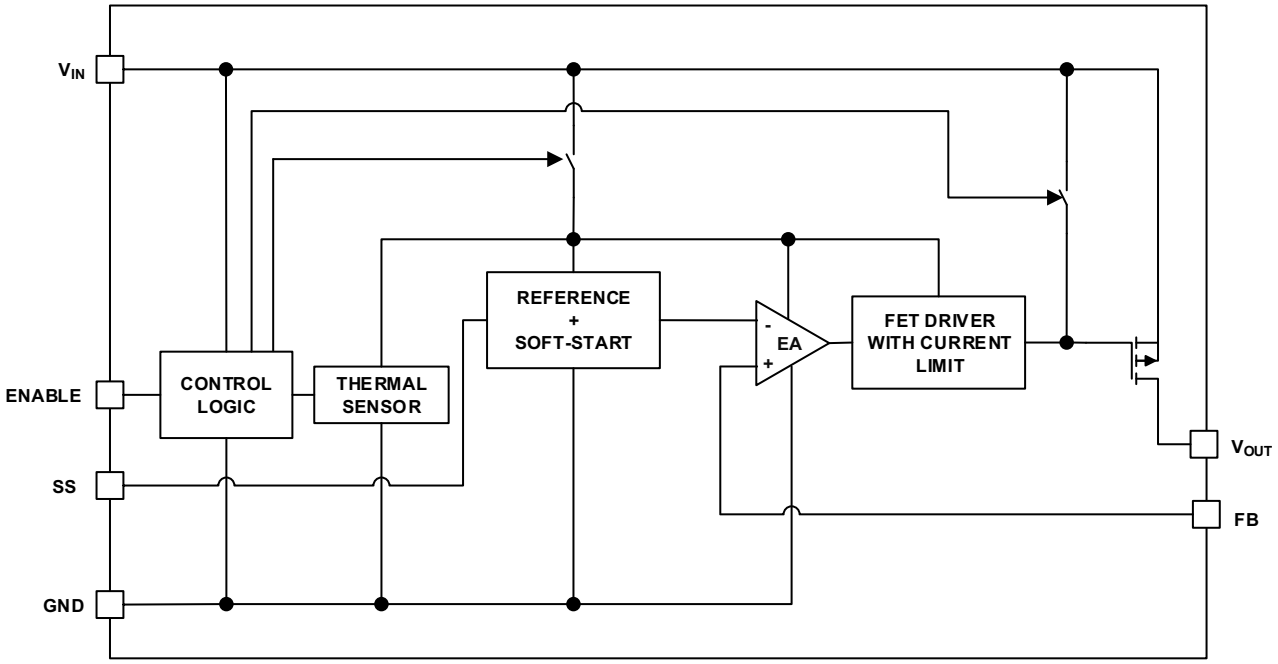


FIGURE 3. BLOCK DIAGRAM

Ordering Information

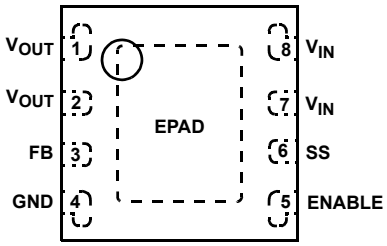
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG DWG. #
ISL80510IRAJZ	0510	-40 to +125	8 Ld 3x3 DFN	L8.3X3J
ISL80510EVAL1Z	Evaluation Board			

NOTES:

1. Add "-T*" for Tape and Reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL80510. For more information on MSL please see Technical Brief TB363.

Pin Configuration

ISL80510
(8 LD 3x3 DFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1, 2	V_{OUT}	Regulated output voltage. A minimum 4.7µF X5R/X7R output capacitor is required for stability. See "External Capacitor Requirements" on page 10 for more details.
3	FB	This pin is the input to the control loop error amplifier and is used to set the output voltage of the LDO.
4	GND	Ground
5	ENABLE	V_{IN} independent chip enable. TTL and CMOS compatible.
6	SS	External capacitor on this pin adjusts start-up ramp and controls inrush current.
7, 8	V_{IN}	Input supply; A minimum of 4.7µF X5R/X7R input capacitor is required for proper operation. See "External Capacitor Requirements" on page 10 for more details.
-	EPAD	EPAD at ground potential; It is recommended to solder the EPAD to the ground plane.

Absolute Maximum Ratings

V_{IN} Relative to GND (Note 4) . . . . . -0.3V to +6.5V
V_{OUT} Relative to GND (Note 4) . . . . . -0.3V to +6.5V
ENABLE, FB, SS
Relative to GND (Note 4) . . . . . -0.3V to +6.5V
ESD Rating
Human Body Model (Tested per JESD22-A114F) 2.5kV
Machine Model (Tested per JESD22-A115C) 250V
Charge Device Model (Tested per JESD22-C101C) 2kV
Latch-up (Tested per JESD78C, Class 2, Level A) . . . . . ±100mA at +85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld DFN Package (Notes 5, 6)	48	7

Storage Temperature Range . . . . . -65°C to +150°C
Junction Temperature . . . . . +150°C
Pb-free Reflow Profile . . . . . see TB493

Recommended Operating Conditions (Notes 7, 8)

Junction Temperature Range (TJ) (Note 7) . . . . . -40°C to +125°C
V_{IN} Relative to GND . . . . . 2.2V to 6V
V_{OUT} Range . . . . . 800mV to 5.5V
ENABLE, FB, SS relative to GND . . . . . 0V to 6V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. Absolute maximum voltage rating is defined as the voltage applied for a lifetime average duty cycle above 6V of 1%.
5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
6. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
7. Extended operation at these conditions may compromise reliability. Exceeding these limits will result in damage. Recommended operating conditions define limits where specifications are guaranteed.
8. Electromigration specification defined as lifetime average junction temperature of +110°C where max rated DC current = lifetime average current.

Electrical Specifications

Unless otherwise noted, 2.2V < V_{IN} < 6V, V_{OUT} = 0.5V, T_J = +25°C. Applications must follow thermal guidelines of the package to determine worst case junction temperature. Please refer to “Applications Information” on page 10 and Tech Brief TB379. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
DC CHARACTERISTICS						
Feedback Pin Voltage	V_{FB}	2.2V < V_{IN} < 6V; 0A < I_{LOAD} < 1A	**491**	500	**509**	mV
Feedback Input Current		V_{FB} = 0.5V		0.01	**1**	µA
Line Regulation	($V_{OUT(LOW\ LINE)}$ - $V_{OUT(HIGH\ LINE)}$)/$V_{OUT(LOW\ LINE)}$	V_{IN} = 2.2V to 6V; I_{LOAD} = 100mA	**-0.9**		**0.9**	%
Load Regulation	($V_{OUT(NO\ LOAD)}$ - $V_{OUT(FULL\ LOAD)}$)/$V_{OUT(NO\ LOAD)}$	V_{IN} = 2.2V; I_{LOAD} = 0A to 1A	**-0.9**		**0.9**	%
Ground Pin Current	I_Q	I_{LOAD} = 0A, V_{IN} = 2.2V		2.2	**4.6**	mA
		I_{LOAD} = 1A, V_{IN} = 2.2V		2.8	**5.7**	mA
Ground Pin Current in Shutdown	I_{SHDN}	ENABLE Pin = 0V, V_{IN} = 6V		0.2	**12**	µA
Dropout Voltage (Note 10)	V_{DO}	I_{LOAD} = 1A, V_{OUT} = 2.5V		130	**212**	mV
Output Short-circuit Current	OCP	V_{OUT} = 0V	**1.35**	1.75	**2.15**	A
Thermal Shutdown Temperature	TSD			160		°C
Thermal Shutdown Hysteresis	TSDn			30		°C
AC CHARACTERISTICS						
Input Supply Ripple Rejection	PSRR	f = 1kHz, I_{LOAD} = 1A; V_{IN} = 2.2V; V_{OUT} = 1.8V		48		dB
		f = 120Hz, I_{LOAD} = 1A; V_{IN} = 2.2V; V_{OUT} = 1.8V		58		dB
Output Noise Voltage		V_{IN} = 2.2V; V_{OUT} = 1.8V; I_{LOAD} = 1A, BW = 100Hz < f < 100kHz		75		μV_{RMS}

Electrical Specifications

Unless otherwise noted, 2.2V < V_{IN} < 6V, V_{OUT} = 0.5V, T_J = +25°C. Applications must follow thermal guidelines of the package to determine worst case junction temperature. Please refer to "Applications Information" on page 10 and Tech Brief TB379. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
ENABLE PIN CHARACTERISTICS						
Turn-on Threshold			**0.5**	0.8	**1**	V
Hysteresis			**10**	80	**200**	mV
ENABLE Pin Turn-on Delay		C_{OUT} = 4.7µF, I_{LOAD} = 1A		100		µs
ENABLE Pin Leakage Current		V_{IN} = 6V, ENABLE = 3V			**1**	µA
SOFT-START CHARACTERISTICS						
SS Pin Currents (Note 11)	I_{PD}	V_{IN} = 3.5V, ENABLE = 0V, SS = 1V	**0.5**	1	**1.3**	mA
	I_{CHG}		**-3.3**	-2	**-0.8**	µA

NOTES:

9. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
10. Dropout is defined as the difference in supply V_{IN} and V_{OUT} when the output is below its nominal regulation.
11. I_{PD} is the internal pull-down current that discharges the external SS capacitor on disable. I_{CHG} is the current from the SS pin that charges the external SS capacitor during start-up.

Typical Operating Performance

Unless otherwise noted: V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A.

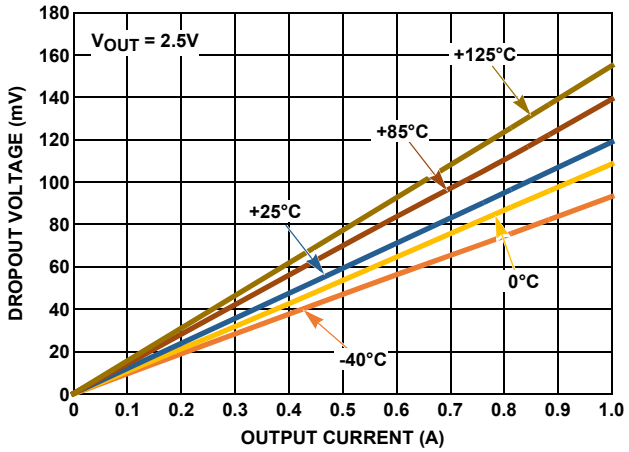


FIGURE 4. DROPOUT vs OUTPUT CURRENT

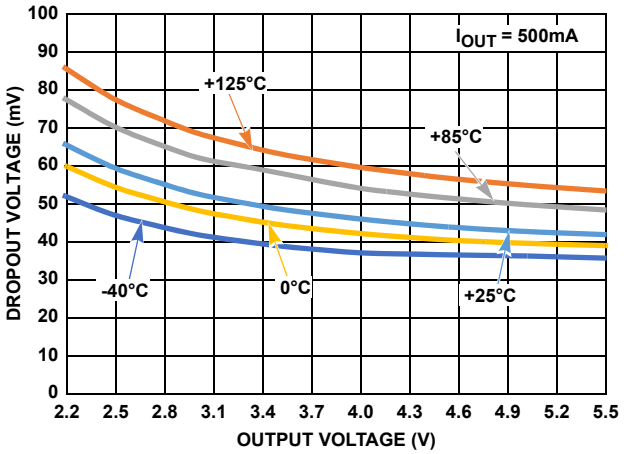


FIGURE 5. DROPOUT vs OUTPUT VOLTAGE

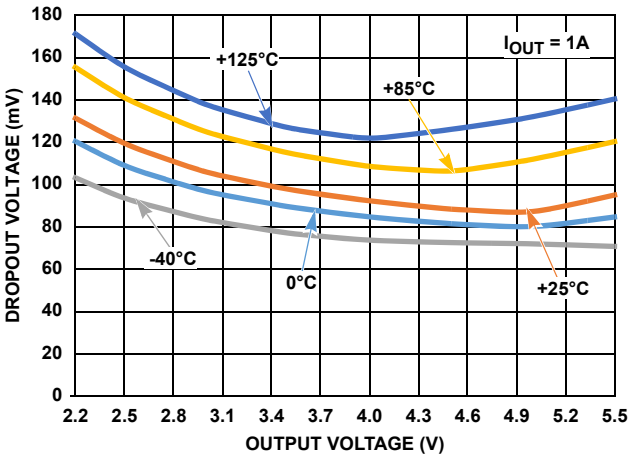


FIGURE 6. DROPOUT vs OUTPUT VOLTAGE

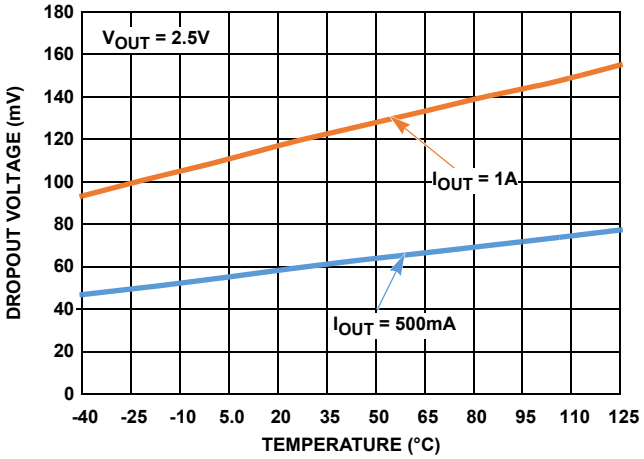


FIGURE 7. DROPOUT vs TEMPERATURE

Typical Operating Performance

Unless otherwise noted: V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A. **(Continued)**

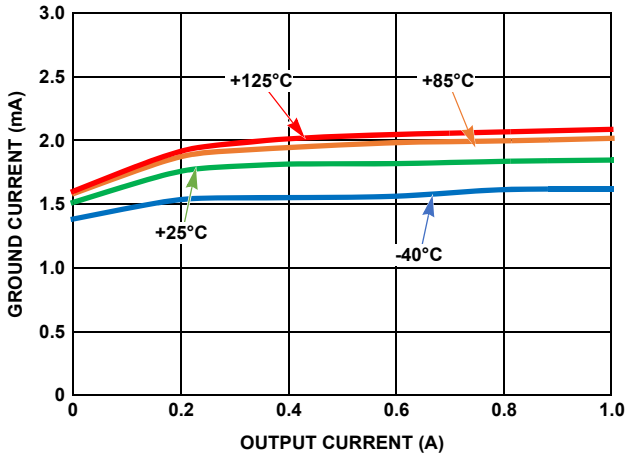


FIGURE 8. GROUND CURRENT vs OUTPUT CURRENT

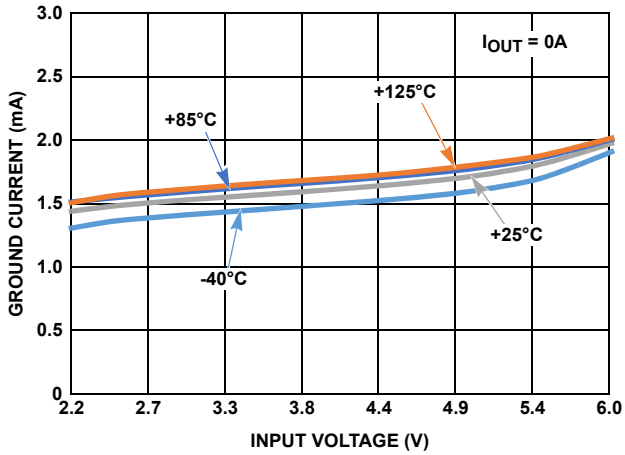


FIGURE 9. GROUND CURRENT vs INPUT VOLTAGE

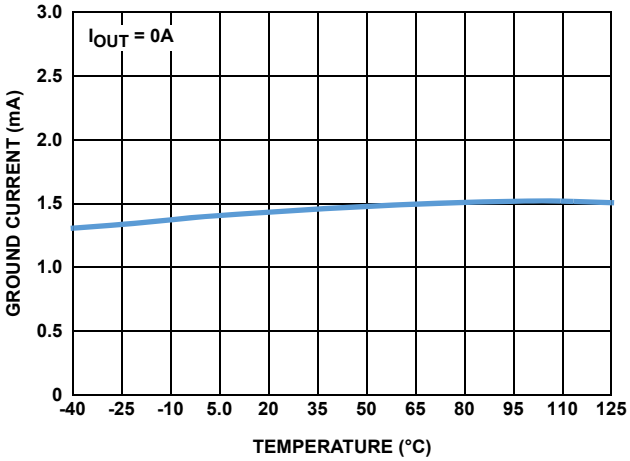


FIGURE 10. GROUND CURRENT vs TEMPERATURE

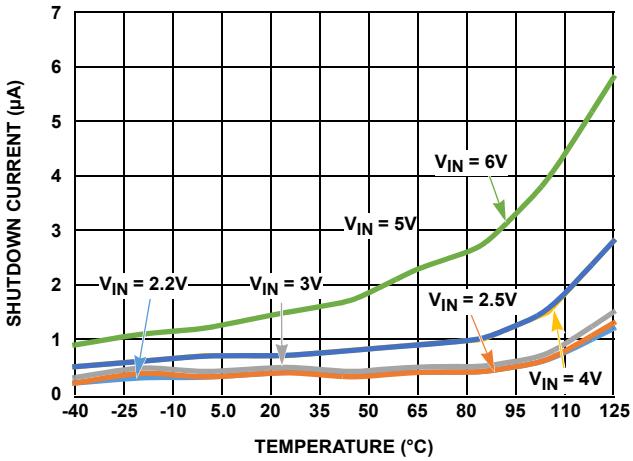


FIGURE 11. SHUTDOWN CURRENT vs TEMPERATURE

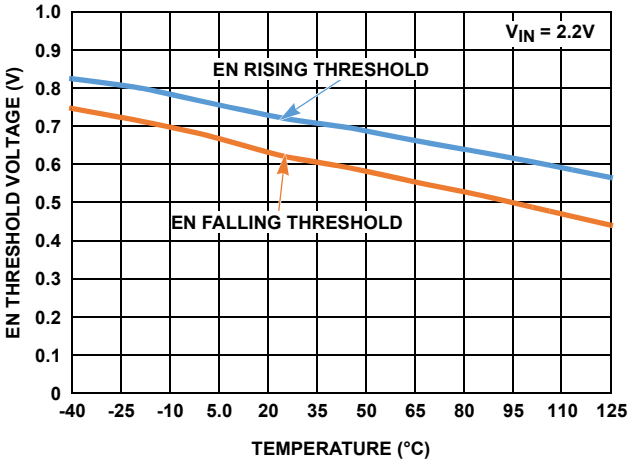


FIGURE 12. EN THRESHOLDS vs TEMPERATURE

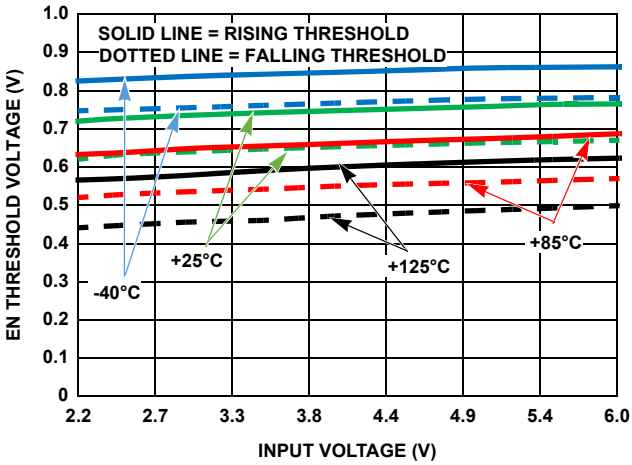


FIGURE 13. EN THRESHOLDS vs INPUT VOLTAGE

Typical Operating Performance

Unless otherwise noted: V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A. **(Continued)**

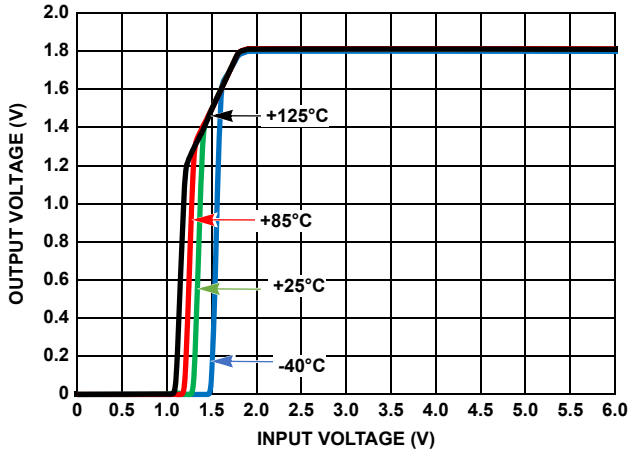


FIGURE 14. OUTPUT VOLTAGE vs INPUT VOLTAGE

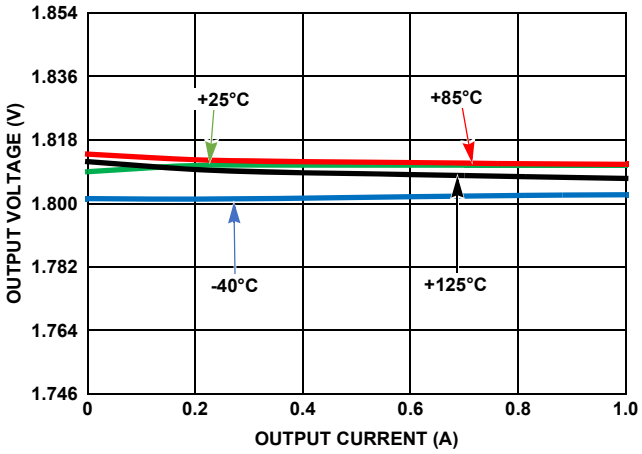


FIGURE 15. OUTPUT VOLTAGE vs OUTPUT CURRENT

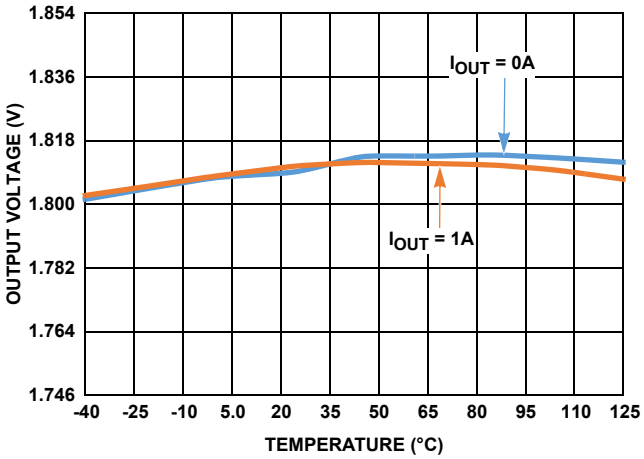


FIGURE 16. OUTPUT VOLTAGE vs TEMPERATURE

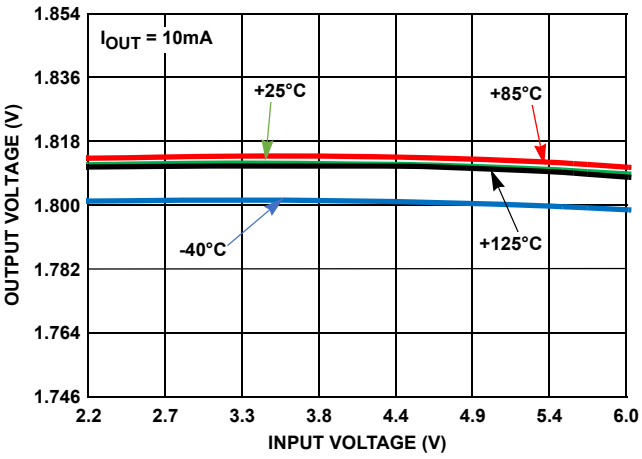


FIGURE 17. OUTPUT VOLTAGE vs INPUT VOLTAGE

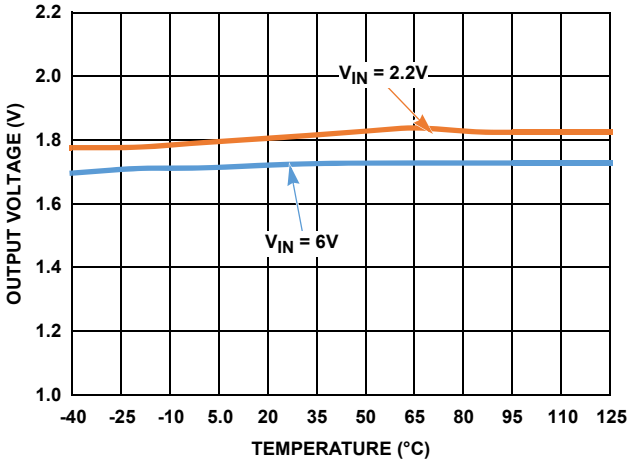


FIGURE 18. CURRENT LIMIT vs TEMPERATURE

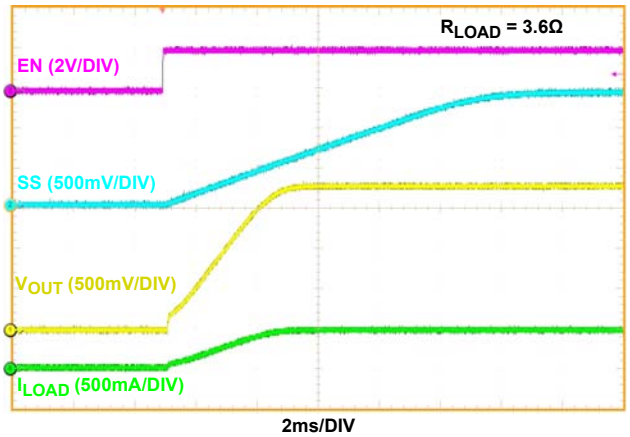


FIGURE 19. ENABLE START-UP (C_{SS} = 10nF)

Typical Operating Performance

Unless otherwise noted: V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A. **(Continued)**

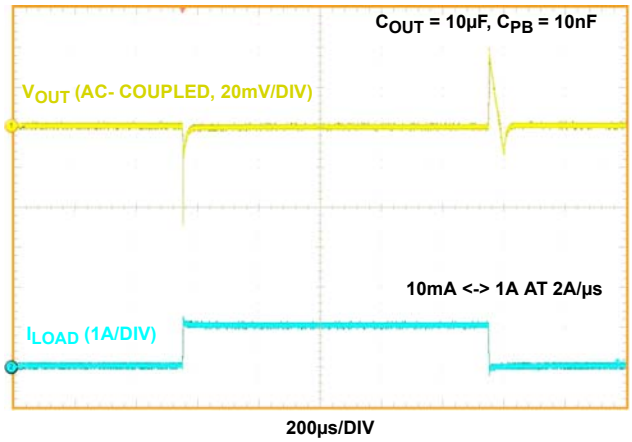


FIGURE 20. LOAD TRANSIENT RESPONSE

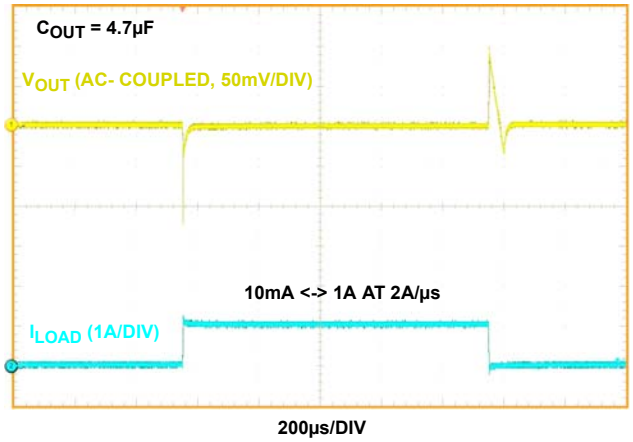


FIGURE 21. LOAD TRANSIENT RESPONSE

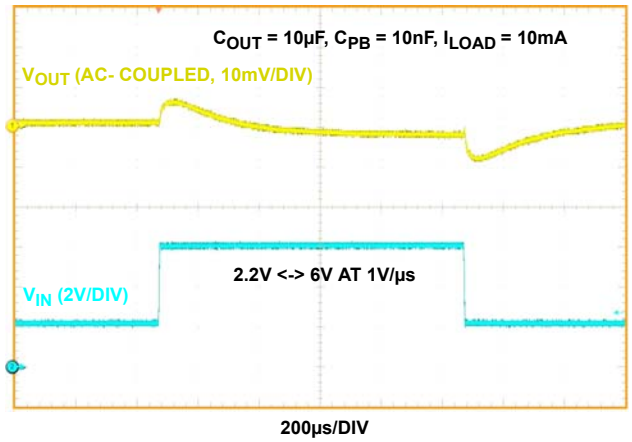


FIGURE 22. LINE TRANSIENT RESPONSE

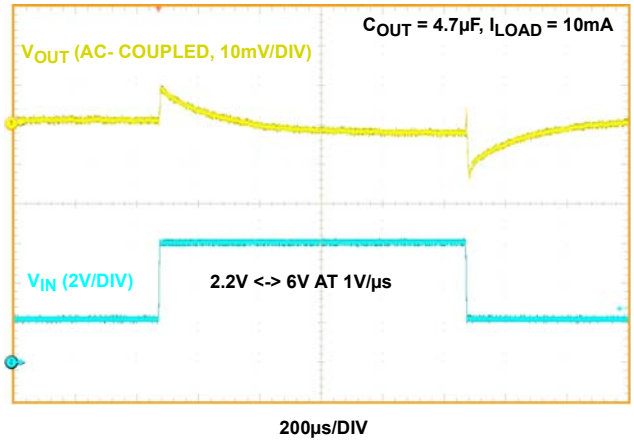


FIGURE 23. LINE TRANSIENT RESPONSE

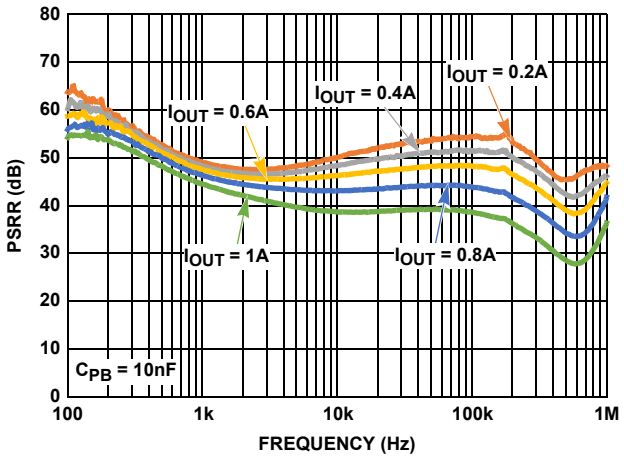


FIGURE 24. PSRR vs FREQUENCY

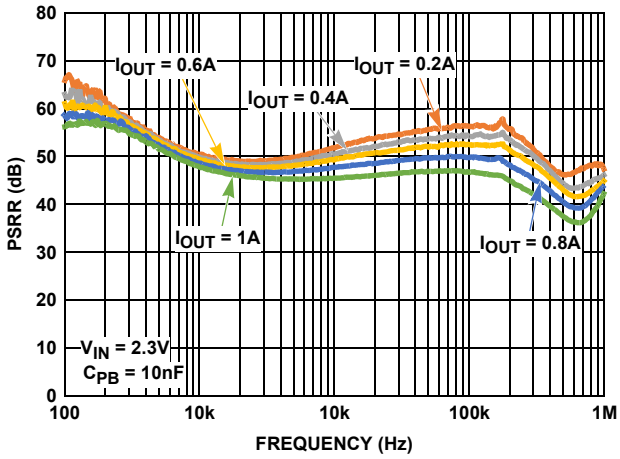


FIGURE 25. PSRR vs FREQUENCY

Typical Operating Performance

Unless otherwise noted: V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A. **(Continued)**

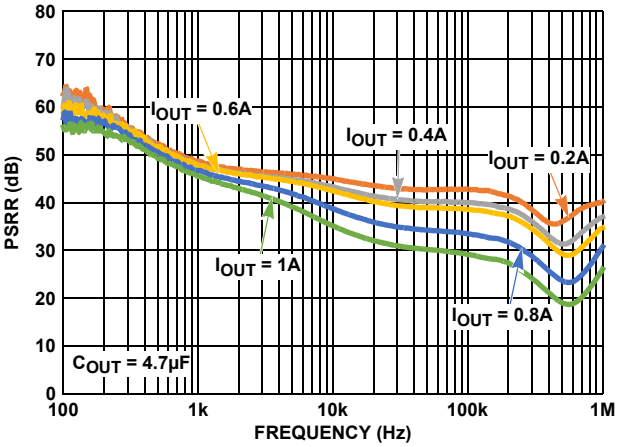


FIGURE 26. PSRR vs FREQUENCY (C_{OUT} = 4.7µF)

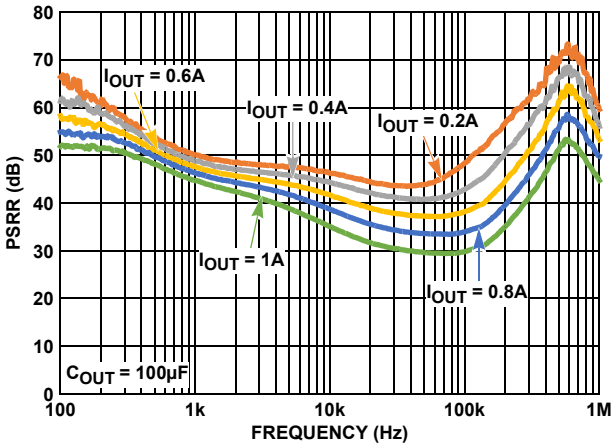


FIGURE 27. PSRR vs FREQUENCY (C_{OUT} = 100µF)

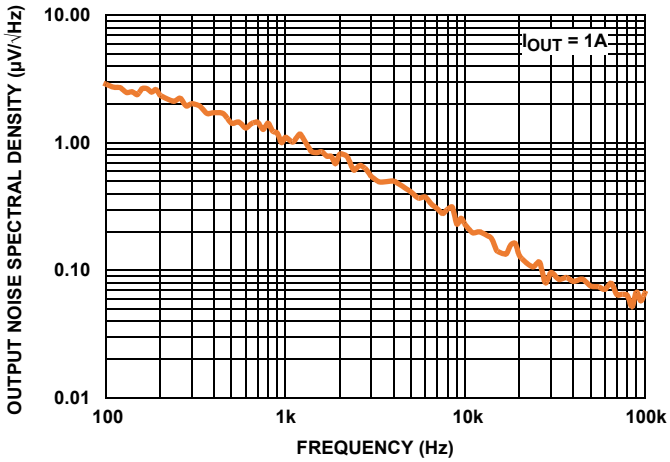


FIGURE 28. OUTPUT NOISE SPECTRAL DENSITY

Applications Information

Input Voltage Requirements

The ISL80510 is a linear voltage regulator operating from 2.2V to 6V input voltage and regulates output voltage between 0.8V to 5.5V, a maximum 1A output current.

Due to the nature of an LDO, V_{IN} must be some margin higher than V_{OUT} plus dropout at the maximum rated current of the application if active filtering (PSRR) is expected from V_{IN} to V_{OUT}. The generous dropout specification of this family of LDOs allows applications to design a level of efficiency.

Enable Operation

The ENABLE turn-on threshold is typically 800mV with 80mV of hysteresis. An internal pull-up or pull-down resistor to change these values is available upon request. As a result, this pin must not be left floating, and should be tied to V_{IN} if not used. A 1kΩ to 10kΩ pull-up resistor is required for applications that use open collector or open-drain outputs to control the ENABLE pin. The ENABLE pin may be connected directly to V_{IN} for applications with outputs that are always on.

Output Voltage

The output voltage can be set to be an external resistor divider network. The values of resistors R_1 and R_2 can be calculated by using Equation 1.

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{0.5} - 1\right) \quad \text{(EQ. 1)}$$

Soft-start Operation

The soft-start circuit controls the rate at which the output voltage rises up to regulation at power-up or LDO enable. This start-up ramp time can be set by adding an external capacitor from the SS pin to ground. An internal 2µA current source charges up the C_{SS} and the feedback reference voltage is clamped to the voltage across it. The start-up time is set by Equation 2.

$$t_{start} = \frac{C_{SS} x 0.5}{2\mu A} \quad \text{(EQ. 2)}$$

Equation 3 determines the C_{SS} required for a specific start-up inrush current, where V_{OUT} is the output voltage, C_{OUT} is the total capacitance on the output and I_{INRUSH} is the desired inrush current.

$$C_{SS} = \frac{V_{OUT} x C_{OUT} x 2\mu A}{I_{INRUSH} x 0.5V} \quad \text{(EQ. 3)}$$

The external capacitor is always discharged to ground at the beginning of start-up or enabling.

External Capacitor Requirements

External capacitors are required for proper operation. Careful attention must be paid to the layout guidelines and selection of capacitor type and value to ensure optimal performance.

OUTPUT CAPACITOR

The ISL80510 applies state-of-the-art internal compensation to keep the selection of the output capacitor simple for the customer. Stable operation over full temperature, V_{IN} range, V_{OUT} range and load extremes are guaranteed for all capacitor types and values assuming a minimum of 4.7µF X5R/X7R is used for local bypass on V_{OUT}. This output capacitor must be connected to the V_{OUT} and GND pins of the LDO with PCB traces no longer than 0.5cm.

There is a growing trend to use very low ESR Multilayer Ceramic Capacitors (MLCC) because they can support fast load transients and also bypass very high frequency noise from other sources. However, the effective capacitance of MLCCs drops with applied voltage, age and temperature. X7R and X5R dielectric ceramic capacitors are strongly recommended as they typically maintain a capacitance range within ±20% of nominal voltage over full operating ratings of temperature and voltage.

Additional capacitors of any value in ceramic, POSCAP, alum/tantalum electrolytic types may be placed in parallel to improve PSRR at higher frequencies and/or load transient AC output voltage tolerances.

INPUT CAPACITOR

For proper operation, a minimum capacitance of 4.7µF X5R/X7R is required at the input. This ceramic input capacitor must be connected to the V_{IN} and GND pins of the LDO with PCB traces no longer than 0.5cm.

PHASE BOOST CAPACITOR (CPB)

A small phase boost capacitor, C_{PB}, can be placed across the top resistor, R_1, in the feedback resistor divider network in order to improve the AC performances of the LDO for the applications where the output capacitor is 10µF or larger. For 10µF output capacitor, the recommended C_{PB} value can be calculated by using Equation 4.

$$C_{PB} = \frac{1}{2\pi x 6000 x R_1} \quad \text{(EQ. 4)}$$

This zero increases the crossover frequency of the LDO and provides additional phase resulting in faster load transient response

Power Dissipation and Thermals

The junction temperature must not exceed the range specified in the "Recommended Operating Conditions (Notes 7, 8)" on page 4. The power dissipation can be calculated by using Equation 5:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad \text{(EQ. 5)}$$

The maximum allowable junction temperature, $T_{J(MAX)}$ and the maximum expected ambient temperature, $T_{A(MAX)}$ determine the maximum allowable power dissipation, as shown in Equation 6:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA} \quad \text{(EQ. 6)}$$

θ_{JA} is the junction-to-ambient thermal resistance.

For safe operation, ensure that the power dissipation P_D, calculated from Equation 5, is less than the maximum allowable power dissipation $P_{D(MAX)}$.

The DFN package uses the copper area on the PCB as a heatsink. The EPAD of this package must be soldered to the copper plane (GND plane) for effective heat dissipation. Figure 29 shows a curve for the θ_{JA} of the DFN package for different copper area sizes.

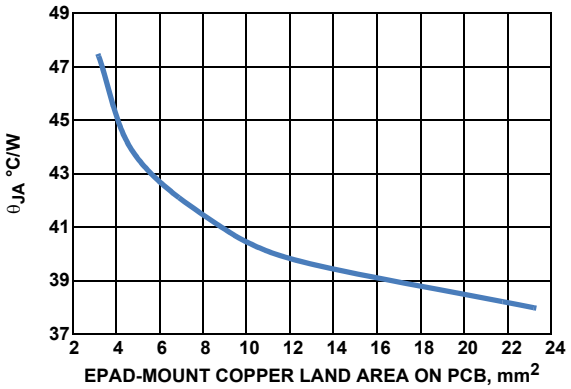


FIGURE 29. 3mmx3mm-10 PIN DFN ON 4-LAYER PCB WITH THERMAL VIAS θ_{JA} vs EPAD-MOUNT COPPER LAND AREA ON PCB

Thermal Fault Protection

The power level and the thermal impedance of the package (+48°C/W for DFN) determine when the junction temperature exceeds the thermal shutdown temperature. In the event that the die temperature exceeds around +160°C, the output of the LDO will shut down until the die temperature cools down to about +130°C.

Current Limit Protection

The ISL80510 LDO incorporates protection against overcurrent due to any short or overload condition applied to the output pin. The LDO performs as a constant current source when the output current exceeds the current limit threshold noted in the “Electrical Specifications” table on page 4. If the short or overload condition is removed from V_{OUT}, then the output returns to normal voltage regulation mode. In the event of an overload condition, the LDO may begin to cycle on and off due to the die temperature exceeding thermal fault condition and subsequently cooling down after the power device is turned off.

PC Board Layout

The performances of this LDO depend greatly on the care taken in designing the PC board. The following are recommendations to achieve optimum performance.

- A minimum capacitance of 4.7µF X5R/X7R ceramic input capacitor must be placed to the VIN and GND pins of the LDO with PCB traces no longer than 0.5cm.
- A minimum capacitance of 4.7µF X5R/X7R ceramic output capacitor must be placed to the VOUT and GND pins of the LDO with PCB traces no longer than 0.5cm.
- Connect the EPAD to the ground plane with low-thermal resistance vias.

Figure 30 shows an example for 2-layer PCB layout. The bottom layer is the ground plane

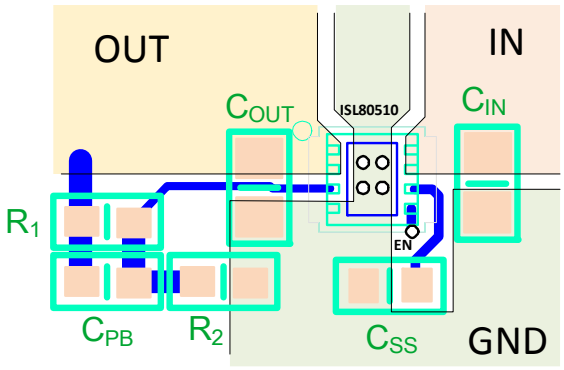


FIGURE 30. EXAMPLE FOR PCB LAYOUT

General PowerPAD Design Considerations

The following is an example of how to use via’s to remove heat from the IC.

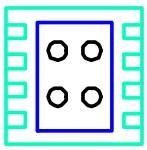


FIGURE 31. PCB VIA PATTERN

A minimum of 4 vias evenly distributed to fill the thermal pad footprint is recommended. Keep the vias small but not so small that their inside diameter prevents solder wicking through the holes during reflow.

Connect all vias to the ground plane. It is important the vias have a low thermal resistance for efficient heat transfer. Do not use “thermal relief” patterns to connect the vias. It is important to have a complete connection of the plated through-hole to each plane.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
July 28, 2015	FN8767.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

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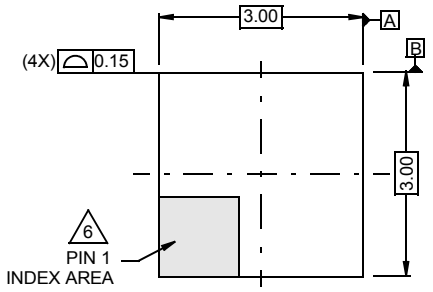
Package Outline Drawing

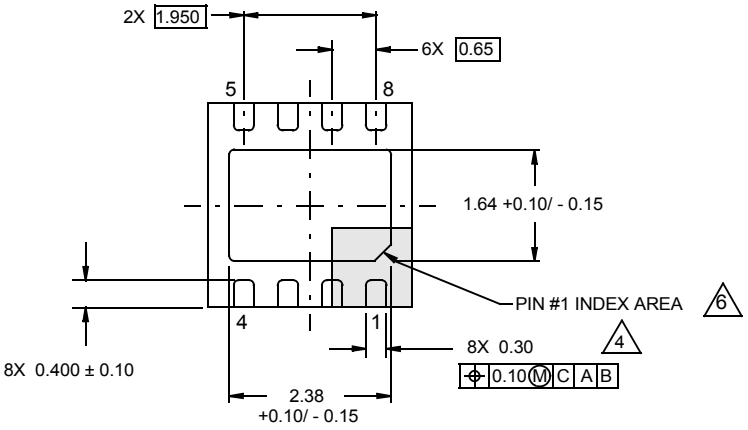
L8.3x3J

8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

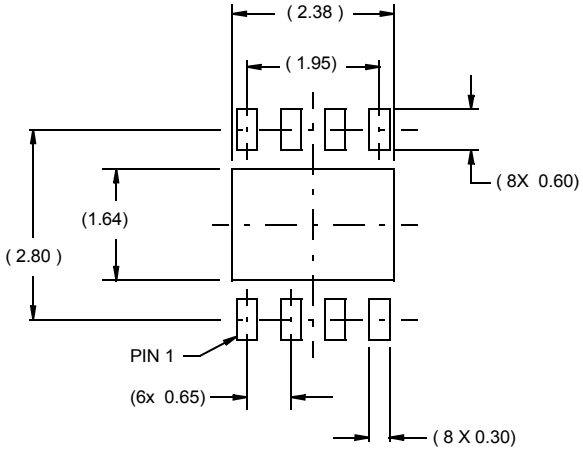
Rev 1 3/15



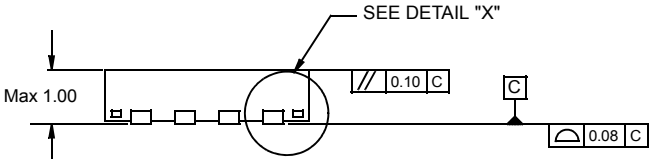
TOP VIEW



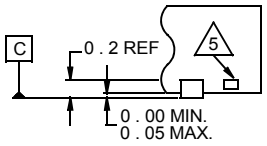
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.