

Description

The ICS501A LOCO™ is the most cost effective way to generate a high quality, high frequency clock output from a lower frequency crystal or clock input. The name LOCO stands for Low Cost Oscillator, as it is designed to replace crystal oscillators in most electronic systems. Using Phase-Locked Loop (PLL) techniques, the device uses a standard fundamental mode, inexpensive crystal to produce output clocks up to 200 MHz.

Stored in the chip's ROM is the ability to generate nine different multiplication factors, allowing one chip to output many common frequencies (see table on page 2).

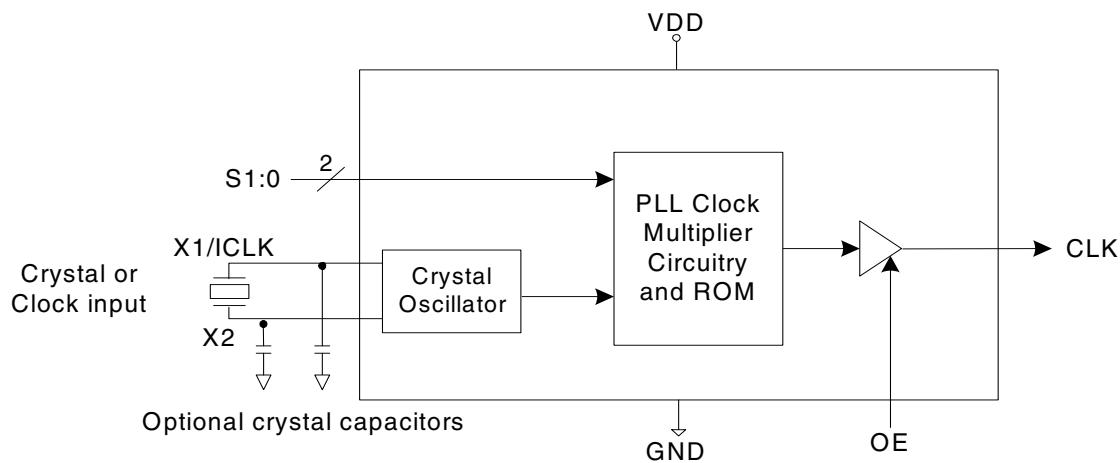
The device also has an output enable pin which tri-states the clock output when the OE pin is taken low.

This product is intended for clock generation. It has low output jitter (variation in the output period), but input to output skew and jitter are not defined or guaranteed. For applications which require defined input to output skew, use the ICS570B.

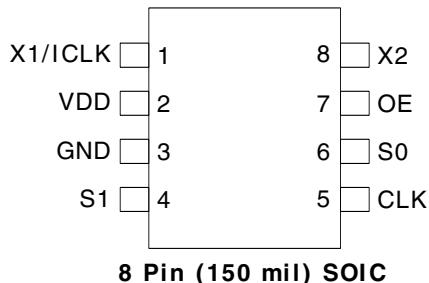
Features

- Packaged as 8-pin SOIC (Pb-free) or die
- IDT's lowest cost PLL clock
- Zero ppm multiplication error
- Input crystal frequency of up to 27 MHz
- Input clock frequency of up to 50 MHz
- Output clock frequencies up to 200 MHz
- Extremely low jitter of 25 ps (one sigma)
- Compatible with all popular CPUs
- Duty cycle of 45/55 up to 200 MHz
- Nine selectable frequencies
- Operating voltage of 3.3 V
- Tri-state output for board level testing
- 25 mA drive capability at TTL levels
- Ideal for oscillator replacement
- Optimized for output frequencies of up to 200 MHz (166 MHz maximum for industrial temperature version)
- Industrial temperature version available
- Advanced, low power CMOS process

Block Diagram



Pin Assignment



Clock Output Table

S1	S0	CLK	Minimum Input (MHz)
0	0	4X input	15
0	M	5.333X input	12
0	1	5X input	12
M	0	10X input	6
M	M	2X input	30
M	1	12X input	5
1	0	6X input	10
1	M	3X input	20
1	1	8X input	10

0 = connect directly to ground

1 = connect directly to VDD

M = leave unconnected (floating)

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	XI/ICLK	Input	Crystal connection or clock input.
2	VDD	Power	Connect to +3.3 V.
3	GND	Power	Connect to ground.
4	S1	Tri-level Input	Select 1 for output clock. Connect to GND or VDD or float.
5	CLK	Output	Clock output per table above.
6	S0	Tri-level Input	Select 0 for output clock. Connect to GND or VDD or float.
7	OE	Input	Output enable. Tri-states CLK output when low. Internal pull-up resistor.
8	X2	Output	Crystal connection. Leave unconnected for clock input.

External Components

Decoupling Capacitor

As with any high-performance mixed-signal IC, the ICS501A must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of $0.01\mu\text{F}$ must be connected between VDD and the GND. It must be connected close to the ICS501A to minimize lead inductance. No external power supply filtering is required for the ICS501A.

Series Termination Resistor

A 33Ω terminating resistor can be used next to the CLK pin for trace lengths over one inch.

Crystal Load Capacitors

The total on-chip capacitance is approximately 12 pF . A

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS501A. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	-40 to +85°C
Storage Temperature	-65 to +150°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.0		+3.6	V

parallel resonant, fundamental mode crystal should be used. The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors, if needed, must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal $(C_L - 12\text{ pF}) * 2$. In this equation, C_L = crystal load capacitance in pF. Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 8 pF $[(16-12) \times 2 = 8]$.

DC Electrical Characteristics

VDD=3.3 V $\pm 10\%$, Ambient temperature -40 to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		3.6	V
Input High Voltage, ICLK only	V _{IH}	ICLK (pin 1)	(VDD/2)+1			V
Input Low Voltage, ICLK only	V _{IL}	ICLK (pin 1)			(VDD/2)-1	V
Input High Voltage	V _{IH}	OE (pin 7)	2.0			V
Input Low Voltage	V _{IL}	OE (pin 7)			0.8	V
Input High Voltage	V _{IH}	S0, S1	VDD-0.5			V
Input Low Voltage	V _{IL}	S0, S1			0.5	V
Output High Voltage	V _{OH}	I _{OH} = -12 mA	2.4			V
Output Low Voltage	V _{OL}	I _{OL} = 12 mA			0.4	V
IDD Operating Supply Current, 20		No load, 100M		20		mA
Short Circuit Current		CLK output		± 70		mA
On-Chip Pull-up Resistor		Pin 7		270		k Ω
Input Capacitance, S1, S0, and OE		Pins 4, 6, 7		4		pF
Nominal Output Impedance				20		Ω

AC Electrical Characteristics

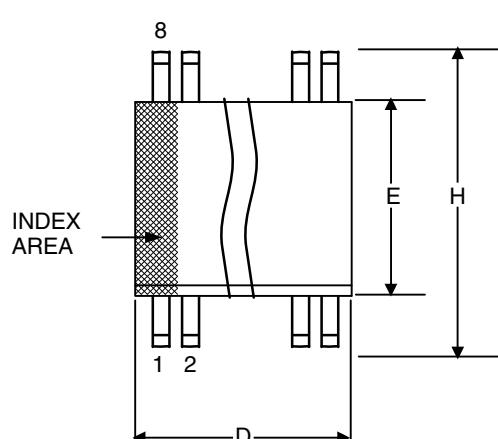
VDD = 3.3 V $\pm 10\%$, Ambient Temperature -40 to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency, crystal input	F _{IN}	see page 2			27	MHz
Input Frequency, clock input	F _{IN}	see page 2			50	MHz
Output Frequency, VDD = 3.0 to 3.6 V	F _{OUT}	0°C to +70°C			200	MHz
		-40°C to +85°C			166	MHz
Output Clock Rise Time	t _{OR}	0.8 to 2.0 V, Note 1		1		ns
Output Clock Fall Time	t _{OF}	2.0 to 8.0 V, Note 1		1		ns
Output Clock Duty Cycle	t _{OD}	1.5 V, up to 160 MHz	45	49-51	55	%
PLL Bandwidth			120			kHz
Output Enable Time, OE high to output on				50		ns
Output Disable Time, OE low to tri-state				50		ns
Absolute Clock Period Jitter	t _{ja}	Deviation from mean		± 70		ps
One Sigma Clock Period Jitter	t _{js}			25		ps

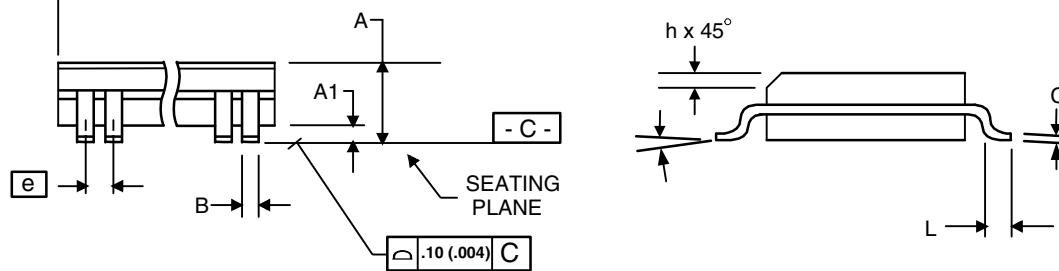
Note 1: Measured with 15 pF load.

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
501AMLF	501AMLF	Tubes	8-pin SOIC	0 to +70° C
501AMLFT	501AMLF	Tape and Reel	8-pin SOIC	0 to +70° C
501AMILF	501AMILF	Tubes	8-pin SOIC	-40 to +85° C
501AMILFT	501AMILF	Tape and Reel	8-pin SOIC	-40 to +85° C
501A-DWF	-	Die on uncut, probed wafers		0 to +70° C
501A-DPK	-	Tested die in waffle pack		0 to +70° C

“LF” suffix to the part number denotes Pb configuration, RoHS compliant.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

ICS501A

LOCO™ PLL CLOCK MULTIPLIER

CLOCK MULTIPLIER

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.