Contents

List of Figures

List of Tables

1. Introduction

In the circuit design described in this application note, the analog output voltage of the ZSC31050 is shifted into the range of 0 to 10 VDC by external circuitry creating a voltage-to-current-to-voltage converter consisting of four resistors (R5, R6, R7, and RC2), a capacitor (RC1), and two bipolar transistors (T2 and T3) as shown in Figure 1.

T2 is a common NPN-type transistor (e.g., BC817-40); there are no special requirements to be considered. T3 is a PNP-type transistor; the type depends on the power dissipation at the maximum ambient temperature T_{AMB_max} with the maximum supply voltage V_{SUPP_max}, the maximum output load current I_{OUT_max}, and the output voltage V_{OUT}. The required power dissipation rating for T3 at T_{AMB_max} can be calculated using equation (1).

$$P_{T3\_max}\left(T_{AMB\_max}\right) \geq \left(I_{OUT\_max} + \frac{V_{OUT\_max}}{R7 + RC2}\right) * \left(V_{SUPP\_max} - V_{OUT\_max}\right) \qquad (1)$$

Figure 1 provides the basic schematic for this application. VOUT_NR is the non-ratiometric output voltage. See Table 1 for details for external components. Note that component values vary depending on the output configuration.

With the current loop output, the analog 2-wire-interface is connected to V+ and V-. The ZACwire™ (one-wire; OWI) interface communicates via VOUT referenced to VSS using an isolated communication module with a pull-up resistor at VOUT, which is supplied by a voltage equal to VDDA. For more details regarding current-loop applications and the ZACwire™ interface, refer to the *ZSC31050 Application Note – Two-Wire Current Loop Output*.

With all analog voltage output configurations, V- is shorted to VSS via R3 = 0 Ω.

For protection against reverse polarity at low voltage drops, a PMOS-enhancement transistor with sufficient gate-to-source voltage could be used instead of D1 or R1.

Figure 1. Ratiometric, 0V to 10V Analog Output, and 4 to 20mA Current Loop Schematic

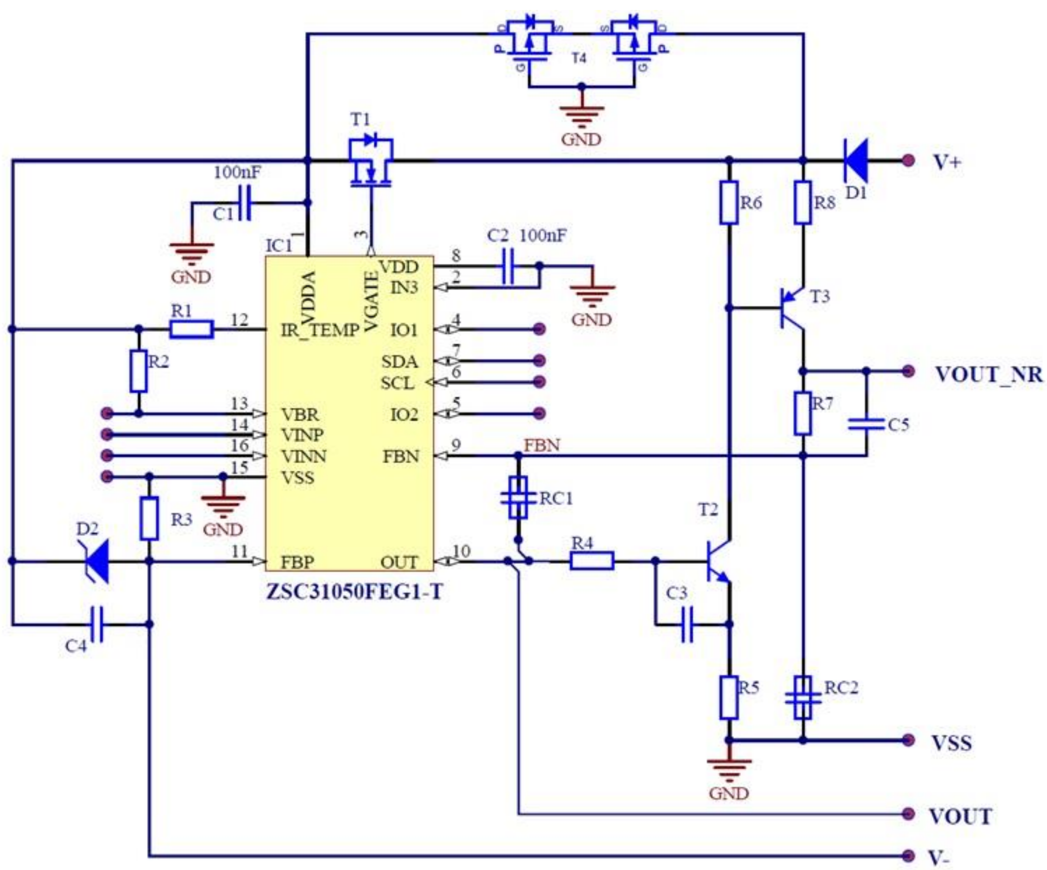


Table 1. Parameters for External Components depending on Output Configuration

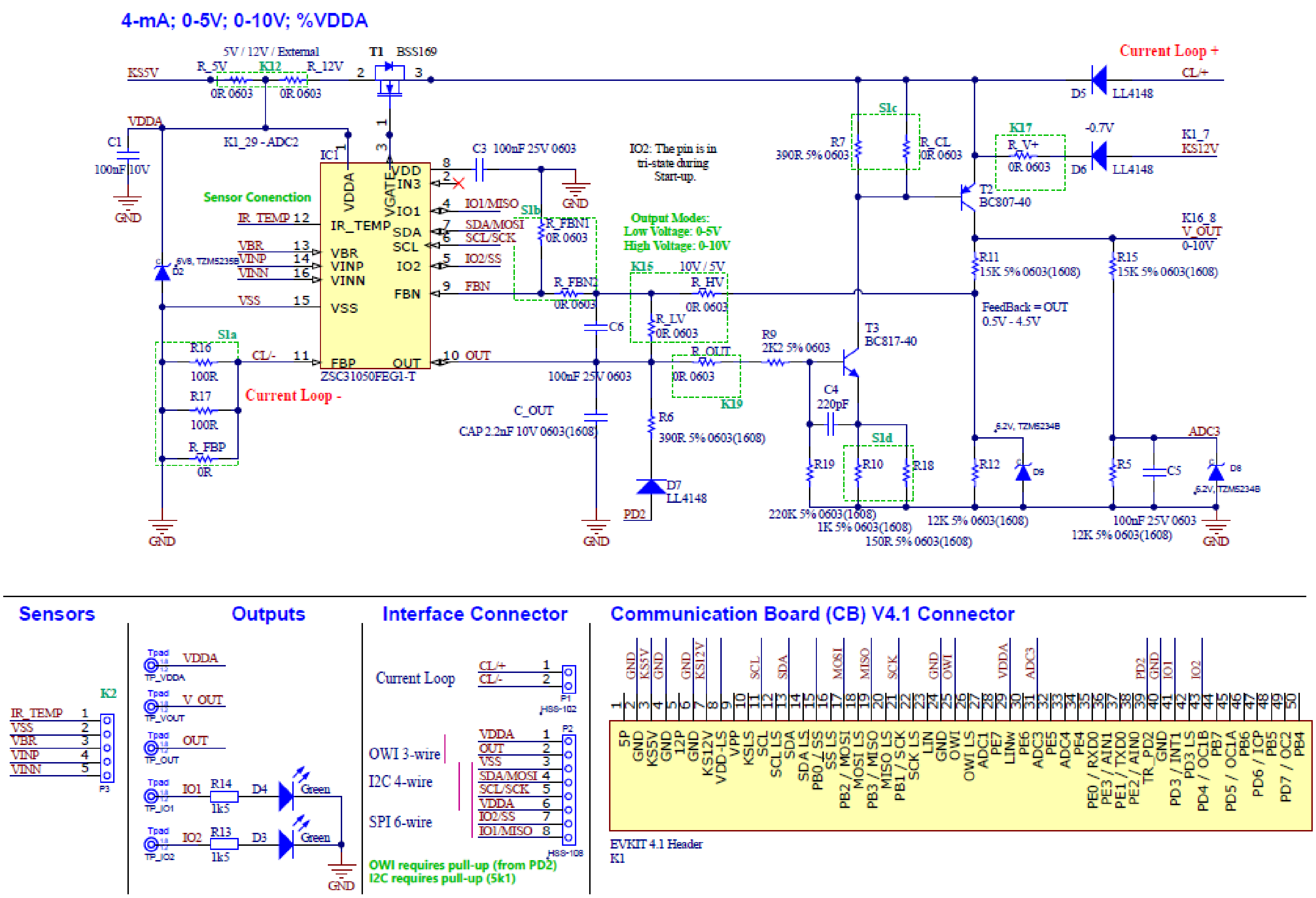
Part ID	Ratiometric Output	Non-ratiometric Output (0V to 10V)	4 to 20mA Current Loop
R1	For bridge in current excitation mode only		
R2	For bridge in voltage excitation (from VDDA) mode only		
R3	0Ω	0Ω	50Ω
R4	Not placed	2.2kΩ	2.2kΩ
R5	Not placed	1kΩ	150Ω
R6	Not placed	390Ω	0Ω
R7	0Ω	2.2kΩ	Not placed
R8	Not placed	Typical 150 Ω (for current limitation)	Not placed
RC1	0Ω	100nF	Not placed
RC2	15nF	2kΩ	0Ω
C1	100nF		
C2	100nF		
C3	Not placed	220pF	220pF
C4	Not placed	10nF	10nF
C5	Not placed	100nF	Not placed
D1	Not placed	LL4148	LL4148
D2	Not placed	BZV55C6V8	BZV55B7V5
T1	Not placed	BSS169N	BSS169N
T2	Not placed	BC817-40 (SOT23)	BC817-40 (SOT23)
T3	Not placed	BC807-40 (SOT23)	Not placed
T4	FDC6306P	Not placed	Not placed

2. Application Configuration

The configuration is determined by the programming of the ZSC31050 and by the placement and value of the external parts given in the schematics in Figure 1 and Table 1. The ZSC31050 SSC Evaluation Kit can be used to program the ZSC31050 as needed for one of the output configurations. The SSC Communication Board included in the ZSC31050 SSC Evaluation Kit can be connected to the application circuit shown in Figure 1 to provide a communication interface for programming the ZSC31050. For full details for connections, programming and configuration of the ZSC31050 with the SSC Evaluation Kit, see the *ZSC31050 Evaluation Kit Description*.

Figure 2 provides a schematic that is equivalent to the Evaluation Board schematic provided in the *ZSC31050 Evaluation Kit Description*. Jumpers and switches are replaced with resistors for easier tests and prototyping.

Figure 2. ZSC31050 Evaluation Kit Equivalent Schematic



2.1 Output Voltage Adjustment V_{OUT}

The following procedures will compensate components' parameter variations in order to achieve the desired output voltage range of 0 to 10V.

- Calibration and coefficient calculation (initial targets: 10% and 90%)
- Analog output measurement
- Re-adjustment of target values (manual calculation via equation (2)) and limit values and then calculation of the new coefficients

$$New\_Target = Initial\_Target - \left(\frac{V_{OUT} - V_{SET}}{V_{SET\_MAX} - V_{SET\_MIN}} \right) * (Target\_max\% - Target\_min\%) \qquad (2)$$

Where

V_{OUT} = the measured voltage

V_{SET} = the target voltage

V_{SET_MAX} = the target maximum voltage

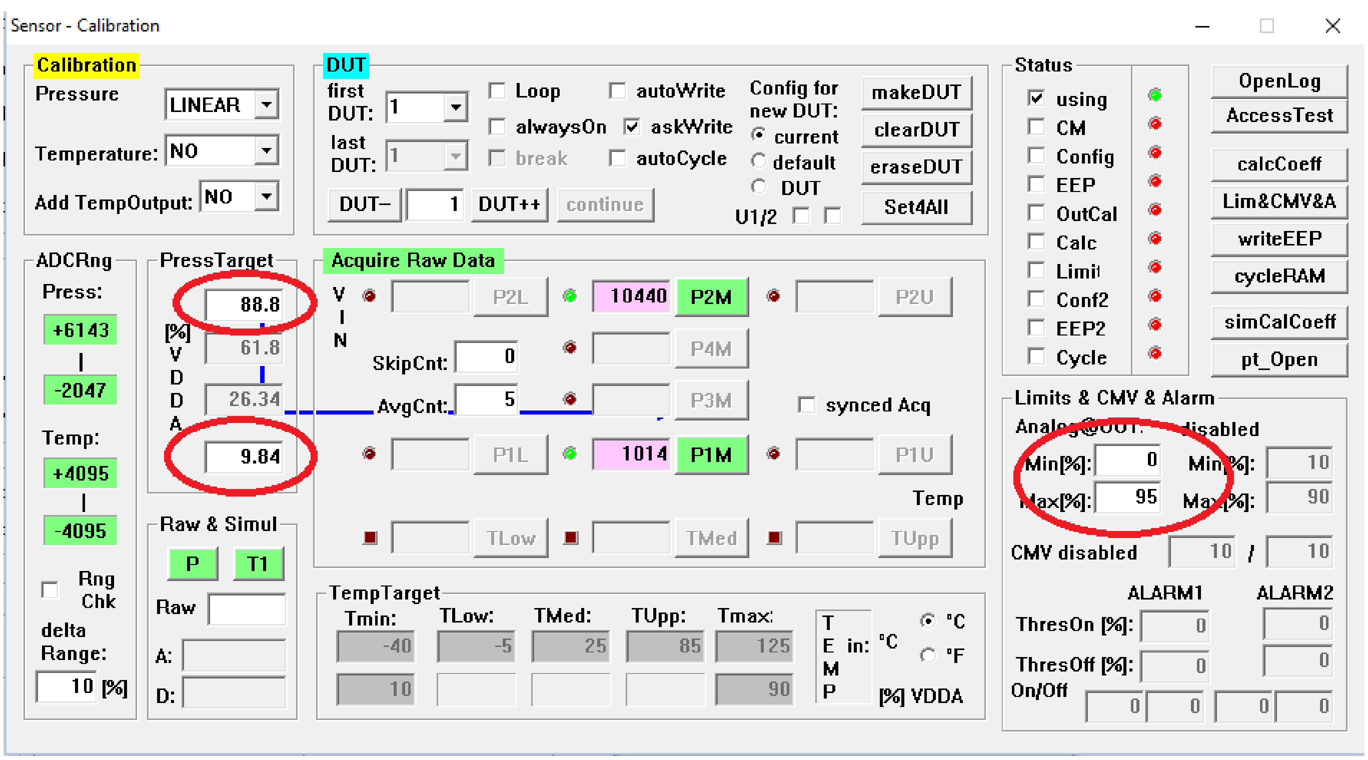
V_{SET_MIN} = target minimum voltage

For example, re-calculation of the maximum target can be done based on the measured output 10.15V and initial calibration targets 10% and 90% as demonstrated in equation (3):

$$New\_Target = 90\% - \left(\frac{10.15V - 10V}{10V - 0V} \right) * (90\% - 10\%) = 88.8\% \qquad (3)$$

Calibrating with a target of 0% (0V) is not reliable in practice; therefore, to adjust the minimum calibration target, the sensor signal can be set to a level that results in a 10% output (measured as 1.11V in this example). After raw data acquisition, equation (2) for calculating the adjusted targets can be applied for fine-tuning the output.

Figure 3. Calibration Window

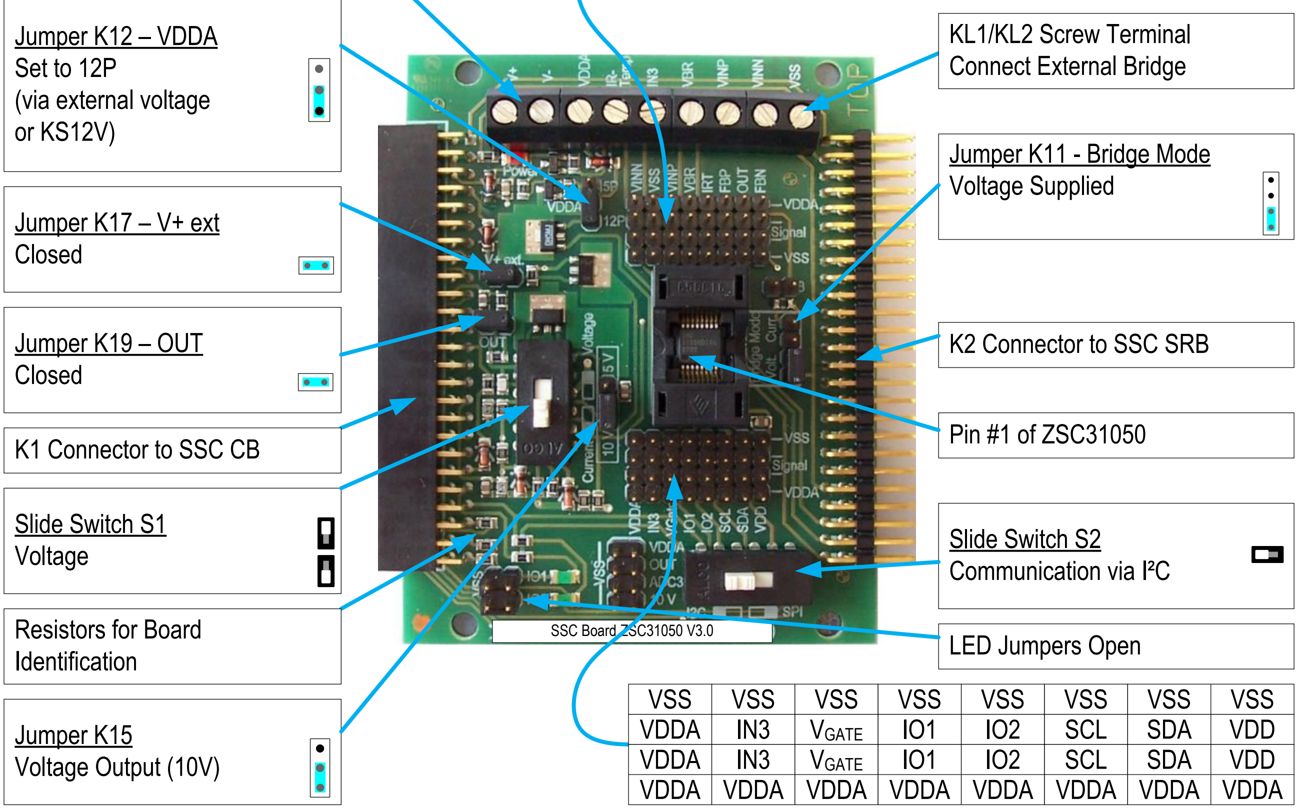


2.2 Setup for the ZSC31050 Evaluation Board

Set the switches and jumpers on the SSC Evaluation Board according to Figure 4.

Figure 4. ZSC31050 Evaluation Board Settings

VDDA	VDDA	VDDA	VDDA	VDDA	VDDA	VDDA	VDDA
VINN	VSS	VINP	VBR	IRT	FBP	OUT	FBN
VINN	VSS	VINP	VBR	IRT	FBP	OUT	FBN
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS



VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
VDDA	IN3	V_{GATE}	IO1	IO2	SCL	SDA	VDD
VDDA	IN3	V_{GATE}	IO1	IO2	SCL	SDA	VDD
VDDA	VDDA	VDDA	VDDA	VDDA	VDDA	VDDA	VDDA

3. Document Revision History

Revision Date	Description of Change
August 22, 2017	▪ Removal of content regarding the configuration for 3-wire 0-10V output with OWI applications, which will be provided in a pending separate document. ▪ Addition of Figure 2 and introductory text. ▪ Minor edits.
April 26, 2017	Changed to IDT branding.
October 14, 2013 (Revision 2.10)	Addition of sections 2.3, 2.4, and 2.5 Update to “Related Documents” section to add example Gerber files available on the IDT website. Update for Figure 2.3. Update for Table 3.1. Minor edits for clarity.
May 22, 2013 (Revision 2.00)	Schematic for three-wire operation added. Update for contact information, imagery for cover and headers.
April 5, 2011 (Revision 1.10)	Changed ZACwire™ description to OneWire; update for template. Updated contact information. Renamed ZMD31050 to ZSC31050.
April 8, 2010 (Revision 1.01)	Update for template.
September 21, 2009 (Revision 1.00)	First release.

Notice

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks