SH72A/SH72A2 Group

LIN Application note

R01AN1186EC0100
Rev.1.00
May. 15, 2012

Abstract

In this application note, four examples of LIN basic communication are shown.

Products

MCUs: SH72A2 Group
SH72A0 Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

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1. Specifications

This application note describes four LIN basic communications.

- Frame transmission (Non-frame separate mode)
- Frame reception
- Wake-up transmission
- Wake-up reception

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	SH72A2 Group, SH72A0 Group
Operating frequency	External input clock 10MHz, CPU clock 100MHz, Bus clock 50MHz, LIN clock 25MHz
Operating voltage	5 V
Integrated development environment	Renesas Electronics products High-performance Embedded Workshop V.4.08.011
C compiler	Renesas Electronics products SuperH RISC engine Standard Toolchain V.9.4.0.0
Operating mode	Single-chip mode

Table 2.2 shows the allocation of the sections used in this application.

Section Name	Description	Area	Start Address
DVECTTBL	Reset vector table	ROM	0x00000000
DINTTBL	Interrupt vector table	ROM	
PResetPRG	Reset programs	ROM	0x00000800
PIntPRG	Interrupt programs	ROM	
P	Program area	ROM	0x00001000
C	Constant area	ROM	
C$BSEC	Structure for uninitialized data area addresses	ROM	
C$DSEC	Structure for initialized data area addresses	ROM	
D	Initialized data(initial values)	ROM	
B	Uninitialized data area	RAM	0xFFF80000
R	Initialized data area	RAM	
S	Stack area	RAM	0xFFF83800

3. Reference Application Note

None

4. Hardware

4.1 Pins Used

Table 4.1 lists the used pins and their functions.

Table 4.1 Pins Used and Their Functions

Pin Name	I/O	Function
PD05	Input	LIN reception port
PD04	Output	LIN transmission port
PK00	Output	Transceiver sleep control, HIGH level constantly
PK01	Output	Transceiver wake-up output control, HIGH level constantly

4.2 Reference Connection

Figure 4.1 shows a connection example in this application note.

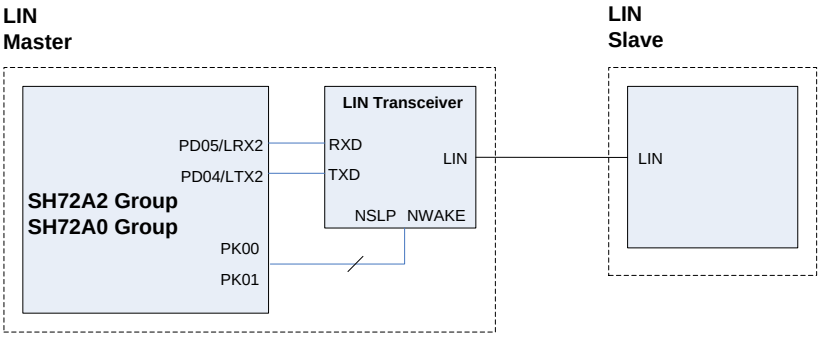


Figure 4.1 Connection Example

5. Software

5.1 Operation Overview

5.1.1 Initial settings

There are 2 parts about initial settings.

One part is about system clock settings.

The other part is about LIN communication settings.

System clock settings are including:

- Set f(CPU) division, here set as No division
- Set f(BUS) division, here set as division by 2
- Set f(PBB)* division, here set as division by 4.
- Supply the LIN bus clock

* f(PBB) is as LIN bus clock.

LIN communication settings are including:

- Set LIN function pins and LIN transceiver control pins.
  Here, PD05 is as LRX2, PD04 is as LTX2.

  PK00 is used to control NSLP pin, PK01 is used to control NWAKE pin.
- Set LIN communication clock source.
  Here, f(SYS) divided by 4 is used as LIN communication clock source.
- Set LIN communication baud rate. Figure 5.1 shows baud rate generation block example.

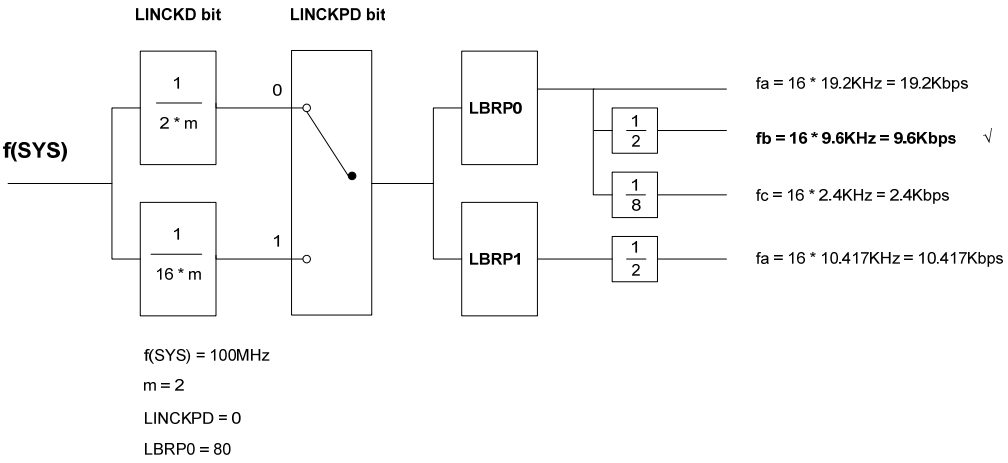


Figure 5.1 Baud rate Generation Block Example

5.1.2 Frame transmission (Non–frame separate mode)

- Specification

LIN master sends frame in non-frame separate mode.

LIN slave can do process after it received the frame.

Table 5.1 lists the communication settings

Table 5.1 Communication Settings Example (Frame Transmission)

Item	Setting
Baud rate	9600bps
Break width	13Tbits
Break delimiter width	1Tbit
Inter byte space (header) /Response space	0Tbit
Inter byte space (response)	0Tbit
Frame separate mode	Non-frame separate mode
Checksum type	Classic
Response field data length	8 data bytes
ID&IDP	0xF5
Data[0] ~ Data[7]	0x00, 0x01, 0x02, 0x03, 0x10, 0x11, 0x12, 0x13

- Register being used description

Table 5.2 Register being used

Register	Address	Setting	Description
LIN Baud Rate Prescaler 0 Register (LBRP0)	H'FF61 0002	H'50	Set LIN baud rate prescaler LBRP0 = "H'50": The peripheral clock is divided by (80+1)
LIN2 Mode Register (L2MD)	H'FF61 0048	H'04	Select LIN system clock LCKS = "B'01": "fb" is selected
LIN2 Break Field Setting Register (L2BRK)	H'FF61 0049	H'00	Set Break delimiter transmission BDT = "B'00": 1 Tbit is set Set Break transmission BLT = "B'0000": 13 Tbits is set
LIN2 Space Setting Register (L2SPC)	H'FF61 004A	H'00	Set Interbyte space IBS = "B'00": 0 Tbit is set Set Interbyte space (Header)/Response space IBSH = "B'000": 0 Tbit is set
LIN2 Interrupt Enable Register (L2IE)	H'FF61 004C	H'00	Set LIN interrupt enable bits ERRIE = "B'0": Disable Error detection interrupt FRCIE = "B'0": Disable Frame/Wake-up receive completion interrupt FTCIE = "B'0": Disable Frame/Wake-up transmit completion interrupt
LIN2 Error Detection Enable Register (L2EDE)	H'FF61 004D	H'0F	Set LIN Error detection enable bits FERE = "B'1": Enable Framing error detection FTERE = "B'1": Enable Frame timeout error detection PBERE = "B'1": Enable Physical bus error detection BERE = "B'1": Enable Bit error detection
LIN2 Response Field Setting Register (L2RFC)	H'FF61 0054	H'18	Set Frame separate mode FSM = "B'0": Non-frame separate mode is selected Set Check sum mode CSM = "B'0": Classic check sum is selected Set Response field Transmit/Receive direction RFT = "B'1": Transmission direction is set Set Response field data length RFDL = "B'1000": 8 bytes + check sum is set
LIN2 ID Buffer Register (L2IDB)	H'FF61 0055	H'F5	Set Parity bits IDP = "B'11" Set ID bits ID = "B'110101"

Register	Address	Setting	Description
LIN2 Data 1 Buffer Register (L2DB1)	H'FF61 0058	H'00	Set data 1 to be transmitted L2DB1 = H'00
LIN2 Data 2 Buffer Register (L2DB2)	H'FF61 0059	H'01	Set data 2 to be transmitted L2DB2 = H'01
LIN2 Data 3 Buffer Register (L2DB3)	H'FF61 005A	H'02	Set data 3 to be transmitted L2DB3 = H'02
LIN2 Data 4 Buffer Register (L2DB4)	H'FF61 005B	H'03	Set data 4 to be transmitted L2DB4 = H'03
LIN2 Data 5 Buffer Register (L2DB5)	H'FF61 005C	H'10	Set data 5 to be transmitted L2DB5 = H'10
LIN2 Data 6 Buffer Register (L2DB6)	H'FF61 005D	H'11	Set data 6 to be transmitted L2DB6 = H'11
LIN2 Data 7 Buffer Register (L2DB7)	H'FF61 005E	H'12	Set data 7 to be transmitted L2DB7 = H'12
LIN2 Data 8 Buffer Register (L2DB8)	H'FF61 005F	H'13	Set data 8 to be transmitted L2DB8 = H'13

5.1.3 Frame reception

- Specification

LIN master sends header.

LIN slave must return response with correct checksum, 8 response data field and classic checksum is required in this example.

Table 5.3 lists the communication settings

Table 5.3 Communication Settings Example (Frame Reception)

Item	Setting
Baud rate	9600bps
Break width	13Tbits
Break delimiter width	1Tbit
Inter byte space (header)	0Tbit
Checksum type	Classic
Response field data length	8 data bytes
ID&IDP	0x76

- Register being used description

Table 5.4 Register being used

Register	Address	Setting	Description
LIN Baud Rate Prescaler 0 Register (LBRP0)	H'FF61 0002	H'50	Set LIN baud rate prescaler LBRP0 = "H'50": The peripheral clock is divided by (80+1)
LIN2 Mode Register (L2MD)	H'FF61 0048	H'04	Select LIN system clock LCKS = "B'01": "fb" is selected
LIN2 Break Field Setting Register (L2BRK)	H'FF61 0049	H'00	Set Break delimiter transmission BDT = "B'00": 1 Tbit is set Set Break transmission BLT = "B'0000": 13 Tbits is set
LIN2 Space Setting Register (L2SPC)	H'FF61 004A	H'00	Set Interbyte space IBS = "B'00": 0 Tbit is set Set Interbyte space (Header)/Response space IBSH = "B'000": 0 Tbit is set
LIN2 Interrupt Enable Register (L2IE)	H'FF61 004C	H'00	Set LIN interrupt enable bits ERRIE = "B'0": Disable Error detection interrupt FRCIE = "B'0": Disable Frame/Wake-up receive completion interrupt FTCIE = "B'0": Disable Frame/Wake-up transmit completion interrupt
LIN2 Error Detection Enable Register (L2EDE)	H'FF61 004D	H'0F	Set LIN Error detection enable bits FERE = "B'1": Enable Framing error detection FTERE = "B'1": Enable Frame timeout error detection PBERE = "B'1": Enable Physical bus error detection BERE = "B'1": Enable Bit error detection
LIN2 Response Field Setting Register (L2RFC)	H'FF61 0054	H'08	Set Frame separate mode FSM = "B'0": Non-frame separate mode is selected Set Check sum mode CSM = "B'0": Classic check sum is selected Set Response field Transmit/Receive direction RFT = "B'0": Reception direction is set Set Response field data length RFDL = "B'1000": 8 bytes + check sum is set
LIN2 ID Buffer Register (L2IDB)	H'FF61 0055	H'76	Set Parity bits IDP = "B'01" Set ID bits ID = "B'110110"

5.1.4 Wake–up transmission

- Specification

LIN master sends Wake-up signal with specified width.

Table 5.5 lists the communication settings

Table 5.5 Communication Settings Example (Wake-up Transmission)

Item	Setting
Baud rate	9600bps
Wake-up signal width	3Tbits

- Register being used description

Table 5.6 Register being used

Register	Address	Setting	Description
LIN Baud Rate Prescaler 0 Register (LBRP0)	H'FF61 0002	H'50	Set LIN baud rate prescaler LBRP0 = "H'50": The peripheral clock is divided by (80+1)
LIN2 Mode Register (L2MD)	H'FF61 0048	H'04	Select LIN system clock LCKS = "B'01": "fb" is selected
LIN2 Wake-up Setting Register (L2WUP)	H'FF61 004B	H'20	Set Wake-up transmission low time pulse width WUTL = "B'0010": 3 Tbits
LIN2 Interrupt Enable Register (L2IE)	H'FF61 004C	H'00	Set LIN interrupt enable bits ERRIE = "B'0": Disable Error detection interrupt FRCIE = "B'0": Disable Frame/Wake-up receive completion interrupt FTCIE = "B'0": Disable Frame/Wake-up transmit completion interrupt
LIN2 Error Detection Enable Register (L2EDE)	H'FF61 004D	H'0F	Set LIN Error detection enable bits FERE = "B'1": Enable Framing error detection FTERE = "B'1": Enable Frame timeout error detection PBERE = "B'1": Enable Physical bus error detection BERE = "B'1": Enable Bit error detection
LIN2 Response Field Setting Register (L2RFC)	H'FF61 0054	H'10	Set Frame separate mode FSM = "B'0": Non-frame separate mode is selected(* not valid here) Set Check sum mode CSM = "B'0": Classic check sum is selected (* not valid here) Set Response field Transmit/Receive direction RFT = "B'1": Transmission direction is set Set Response field data length RFDL = "B'0000": 8 bytes + check sum is set (* not valid here)

5.1.5 Wake–up reception

- Specification

LIN master waits Wake-up signal input with specified width.

LIN slave must send signal low time to be 125μs or more in this example.

- Register being used description

Table 5.7 Register being used

Register	Address	Setting	Description
LIN Wake-up Baud Rate Select Register (LWBR)	H'FF61 0001	H'01	Set Wake-up baud rate LWBR0 = "B'1": When LIN 2.0 and 2.1 used. This allows the input signal Low time to be measured 125 μs or more.
LIN Baud Rate Prescaler 0 Register (LBRP0)	H'FF61 0002	H'50	Set LIN baud rate prescaler LBRP0 = "H'50": The peripheral clock is divided by (80+1)
LIN2 Interrupt Enable Register (L2IE)	H'FF61 004C	H'00	Set LIN interrupt enable bits ERRIE = "B'0": Disable Error detection interrupt FRCIE = "B'0": Disable Frame/Wake-up receive completion interrupt FTCIE = "B'0": Disable Frame/Wake-up transmit completion interrupt
LIN2 Error Detection Enable Register (L2EDE)	H'FF61 004D	H'0F	Set LIN Error detection enable bits FERE = "B'1": Enable Framing error detection FTERE = "B'1": Enable Frame timeout error detection PBERE = "B'1": Enable Physical bus error detection BERE = "B'1": Enable Bit error detection
LIN2 Response Field Setting Register (L2RFC)	H'FF61 0054	H'00	Set Frame separate mode FSM = "B'0": Non-frame separate mode is selected(* not valid here) Set Check sum mode CSM = "B'0": Classic check sum is selected (* not valid here) Set Response field Transmit/Receive direction RFT = "B'0": Reception direction is set Set Response field data length RFDL = "B'0000": 8 bytes + check sum is set (* not valid here)

5.2 Required Memory Size

Table 5.8 lists the required memory size.

Table 5.8 Required Memory Size

Memory Used	Size	Remarks
ROM	2449 Bytes	SH RISC Complier 9.4.0.0, Optimization OFF
RAM	4 Bytes	
Maximum user stack	1024 Bytes	

The required memory size varies depending on the C compiler version and compiler options.

5.3 Invariable Table

Table 5.9 lists the invariables used in the sample code.

Table 5.9 Invariables Used in the Sample Code

Invariable Name	Setting Value	Description
FALSE	0	False
TRUE	1	True
CUR_LIN_CH	0x02	Current LIN channel number

5.4 Function Table

Table 5.10 lists the functions.

Table 5.10 Functions

Function Name	Description
initSysClock	Initialize system clock
LINInit	Initialize LIN communication source
LINSetClockSource	Set LIN communication clock source
LINSetPins	Set LIN pins used
LINResetMode	Set specified LIN channel to Reset mode
LINOperateMode	Set specified LIN channel to Operate mode
LINWakeupMode	Set specified LIN channel to Wake-up mode
LINSetBaudrate	Set LIN communication baud rate
LINFrameTxNotSeparate	Frame transmission (not-frame separate mode)
LINFrameRx	Frame reception
LINWupTx	Wake-up transmission
LINWupRx	Wake-up reception
main	main function

5.5 Function Specifications

The following tables list the sample code function specifications.

initSysClock	
Outline	Initialize system clock
Header	None
Declaration	static void initSysClock(void)
Description	Initialize system clock as 100MHz
Argument	None
Returned value	None

LINInit	
Outline	Initialization for LIN communication
Header	None
Declaration	static void LINInit (void)
Description	Initialize LIN communication clock source, pins, baud rate call LINSetPins (), call LINSetClockSource (), call LINSetBaudrate (),
Argument	None
Returned value	None

LINSetClockSource	
Outline	Set LIN communication clock source
Header	None
Declaration	static void LINSetClockSource(void)
Description	Set LIN communication clock source f(LIN) = f(SYS)/4 = 100 MHz / 4 = 25 MHz,
Argument	None
Returned value	None

LINSetPins	
Outline	Set LIN pins used
Header	None
Declaration	static void LINSetPins(void)
Description	Set LIN pins used PD05 is as for LRX2 PD04 is as for LTX2
Argument	None
Returned value	None

LINResetMode	
Outline	Set specified LIN channel to Reset mode
Header	None
Declaration	static void LINResetMode(U8 LINchannel)
Description	Set specified LIN channel to Reset mode
Argument	LINchannel, specified LIN channel
Returned value	None

LINOperateMode	
Outline	Set specified LIN channel to Operate mode
Header	None
Declaration	static void LINOperateMode(U8 LINchannel)
Description	Set specified LIN channel to Operate mode
Argument	LINchannel, specified LIN channel
Returned value	None

LINWakeupMode	
Outline	Set specified LIN channel to Wake-up mode
Header	None
Declaration	static void LINWakeupMode(U8 LINchannel)
Description	Set specified LIN channel to Wake-up mode
Argument	LINchannel, specified LIN channel
Returned value	None

LINSetBaudrate	
Outline	Set LIN communication baud rate
Header	None
Declaration	static void LINSetBaudrate(U8 LINchannel)
Description	Set LIN communication baud rate as 9600bps
Argument	LINchannel, specified LIN channel
Returned value	None

LINFrameTxNotSeparate	
Outline	Frame transmission (not-frame separate mode)
Header	None
Declaration	static void LINFrameTxNotSeparate(void)
Description	LIN frame transmission (not-frame separate mode)
Argument	None
Returned value	None

LINFrameRx	
Outline	Frame reception
Header	None
Declaration	static void LINFrameRx(void)
Description	LIN frame reception
Argument	None
Returned value	None

LINWupTx	
Outline	Wake-up transmission
Header	None
Declaration	static void LINWupTx(void)
Description	LIN Wake-up transmission
Argument	None
Returned value	None

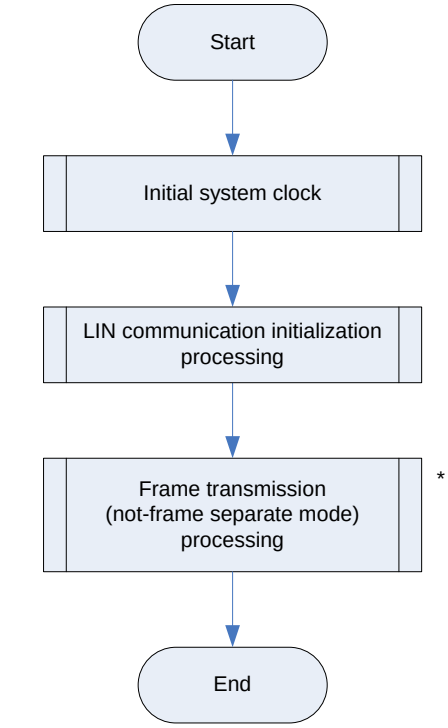
LINWupRx	
Outline	Wake-up reception
Header	None
Declaration	static void LINWupRx(void)
Description	LIN Wake-up reception
Argument	None
Returned value	None

main	
Outline	main function
Header	None
Declaration	void main(void)
Description	main function call initSysClock(), call LINInit(), call LINFrameTxNotSeparate(), call LINFrameRx(), call LINWupTx(), call LINWupRx()
Argument	None
Returned value	None

5.6 Flowchart

5.6.1 Main Processing

Figure 5.2 shows the main processing.



* LIN communication process is selected based on different compile macro definition.

Figure 5.2 Main Processing

5.6.2 System Clock Initialization Processing

Figure 5.3 shows the system clock initialization processing

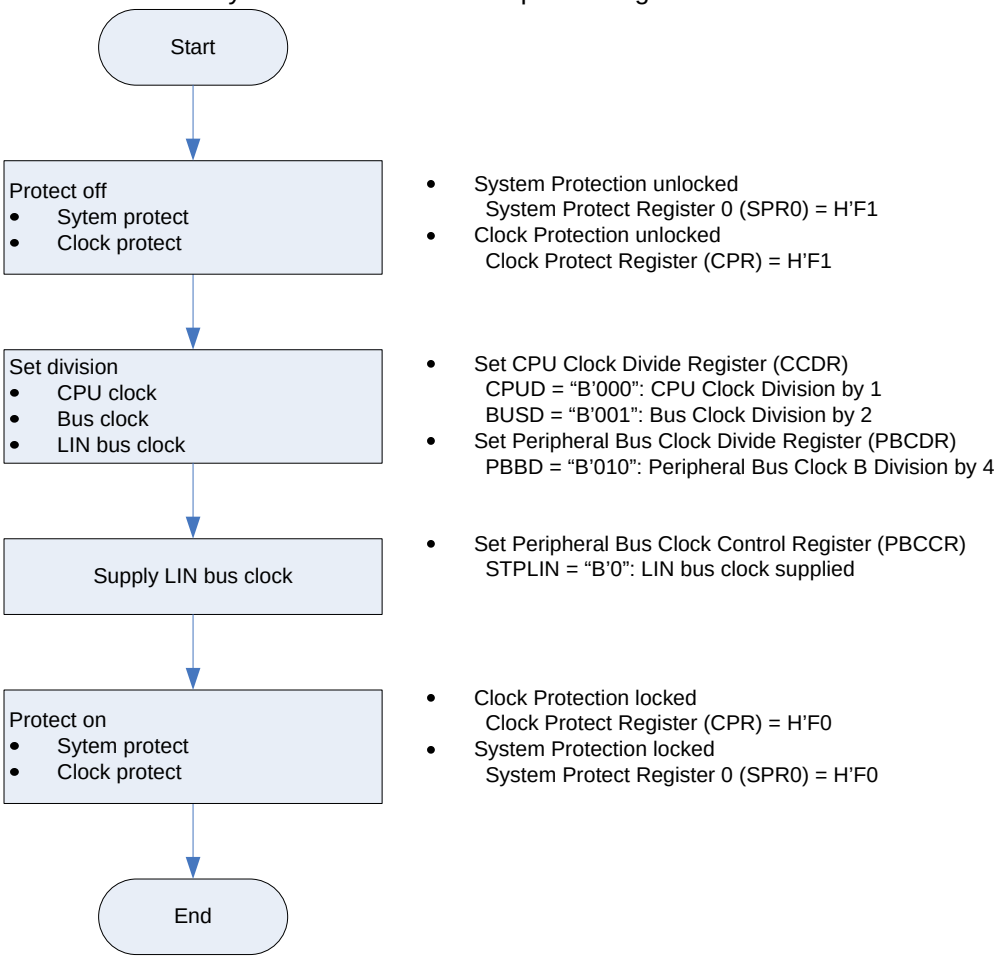


Figure 5.3 System Clock Initialization Processing

5.6.3 LIN Initialization Processing

Figure 5.4 shows the LIN initialization processing.
Figure 5.5 shows the LIN communication pins setting processing.
Figure 5.6 shows the LIN communication clock source setting processing.
Figure 5.7 shows the LIN communication baud rate setting processing.

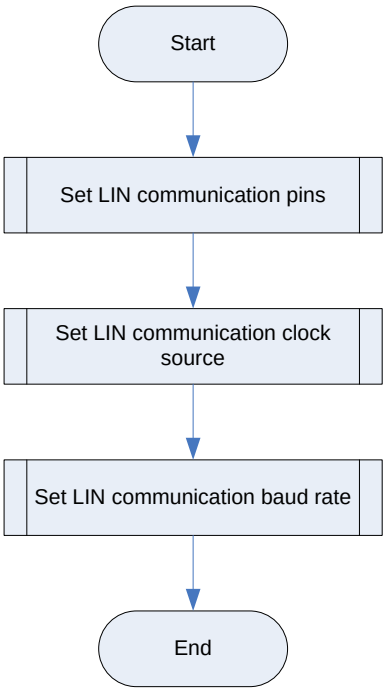


Figure 5.4 LIN Communication Initialization Processing

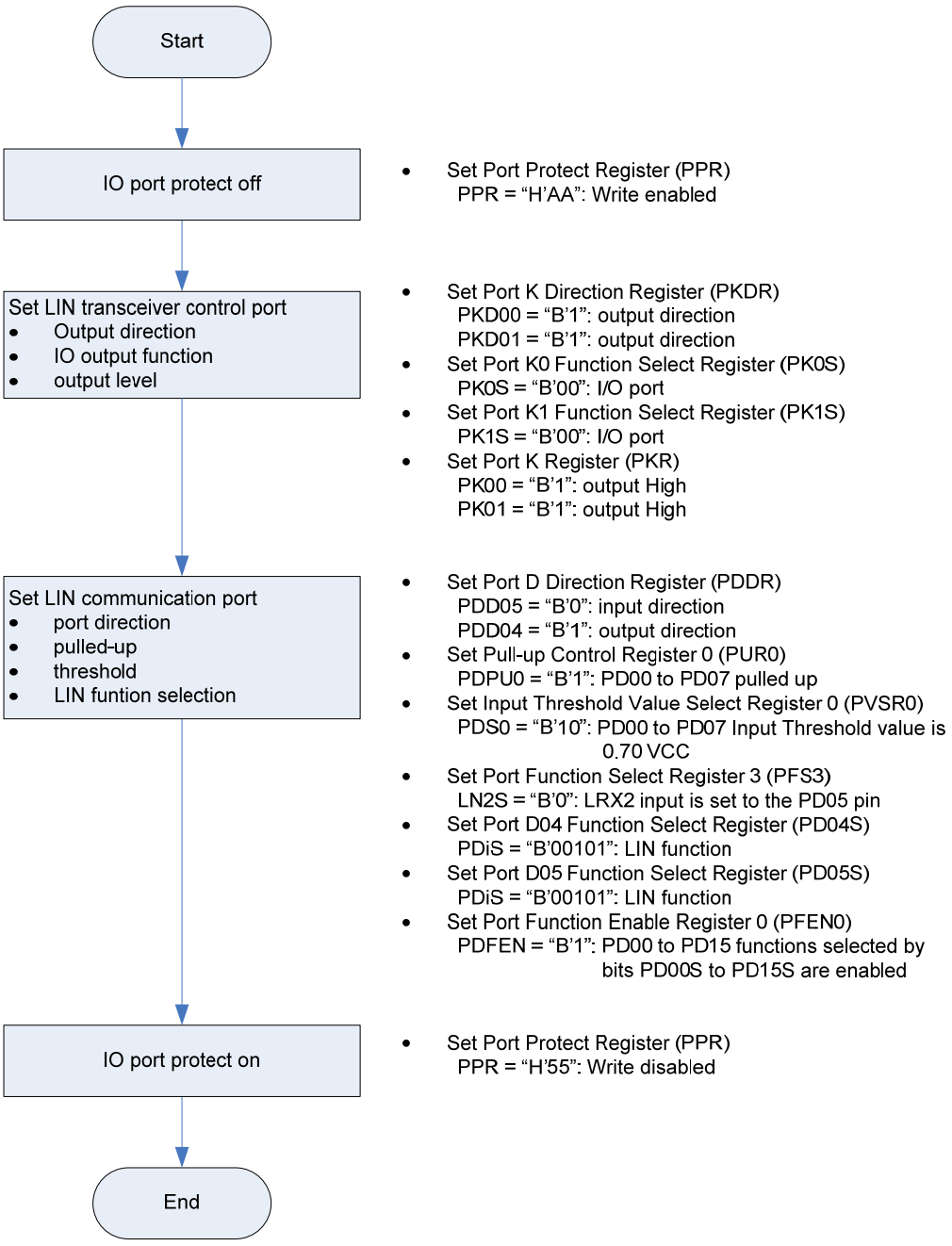


Figure 5.5 LIN Communication Pins Setting Processing

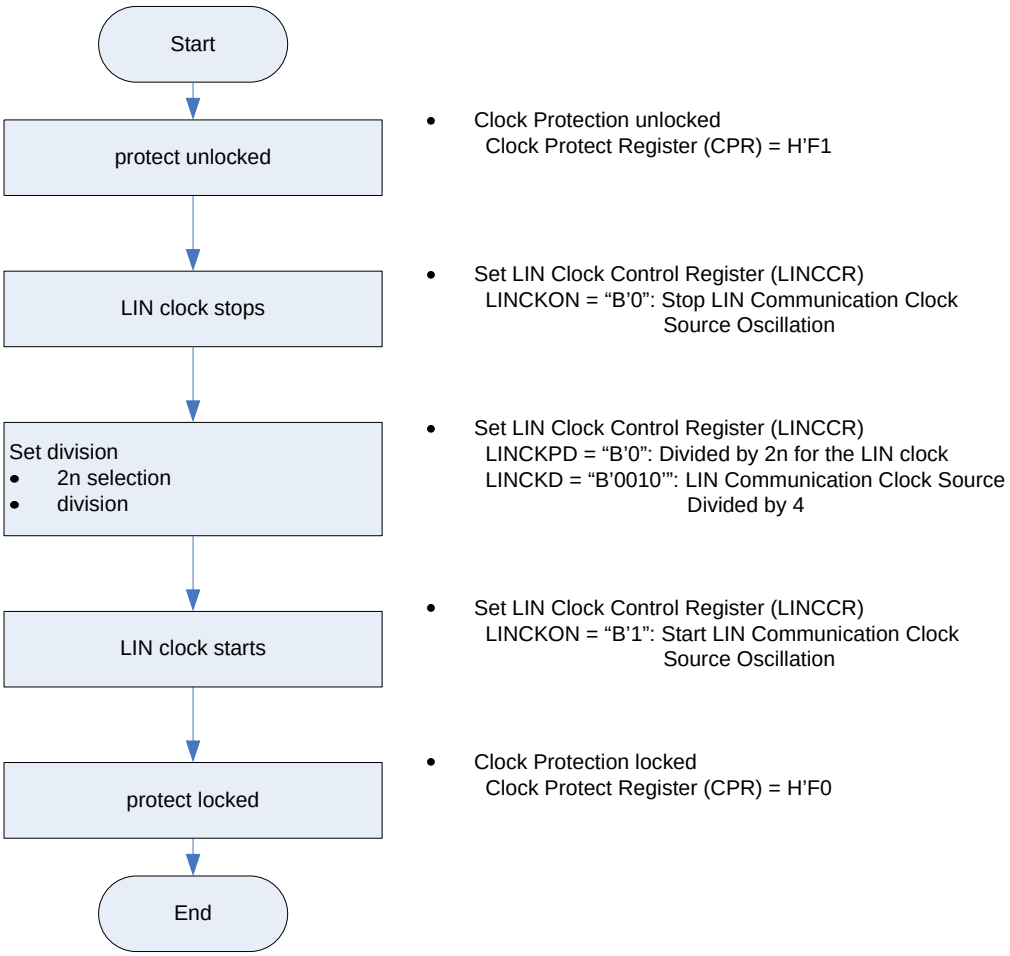
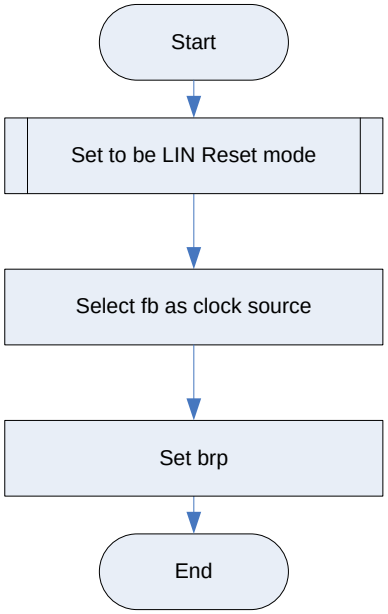


Figure 5.6 LIN Communication Clock Source Setting Processing

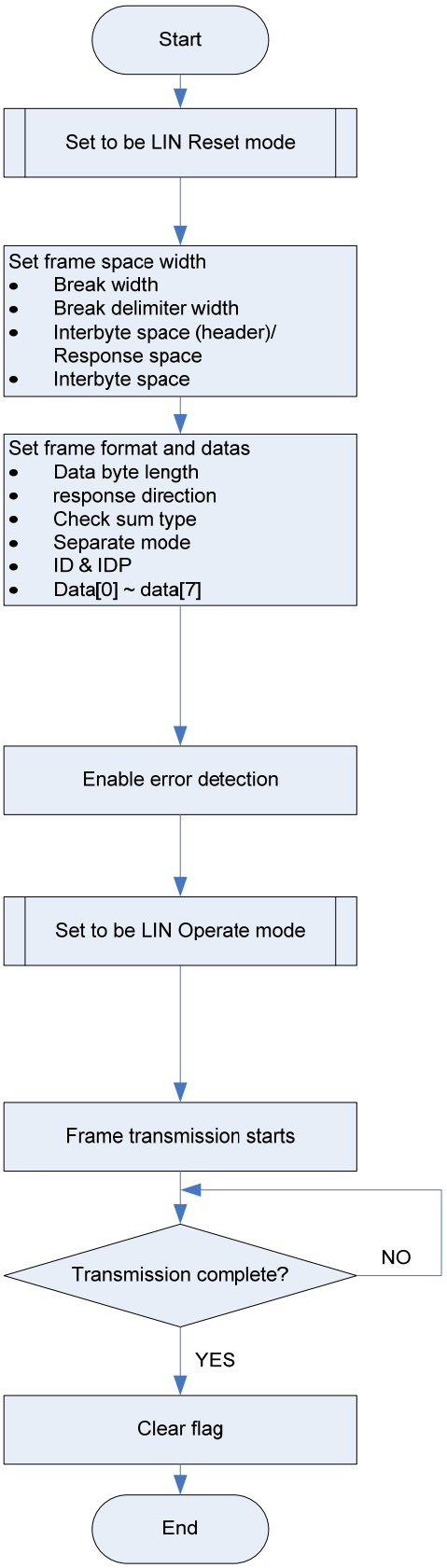


- Set to LIN Reset mode
  Set LIN2 Control Register (L2C)
  OM0 = “B’0”: LIN reset mode
  and, check until LIN2 Mode Status Register (L2MST)’s
  OMM0 == “B’0” (LIN2 is reset mode)
- Set LIN2 Mode Register (L2MD)
  LCKS = “B’01”: select “fb” as LIN System Clock
- Set LIN Baud Rate Prescaler 0 Register (LBRP0)
  LBRP0 = “H’50”: The peripheral clock is divided by (80+1)

Figure 5.7 LIN Communication Baud rate Setting Processing

5.6.4 Frame Transmission (Non-frame separate mode) Processing

Figure 5.8 shows Frame transmission (Non–frame separate mode) Processing.

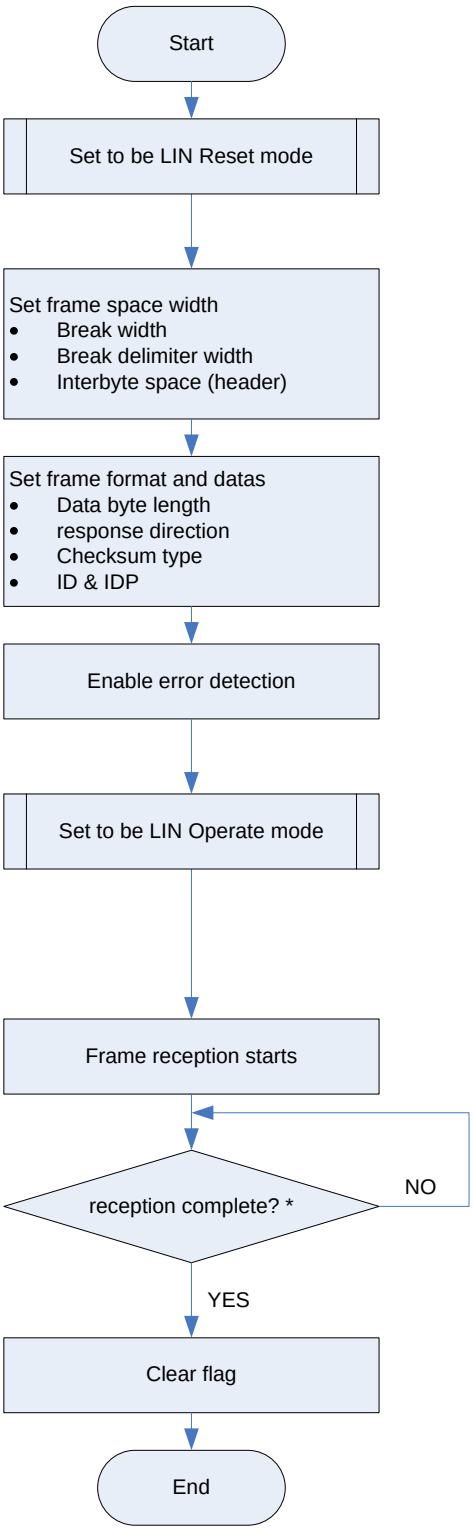


- Set to LIN Reset mode
  Set LIN2 Control Register (L2C)
  OM0 = “B’0”: LIN reset mode
  and, check until LIN2 Mode Status Register (L2MST)’s
  OMM0 == “B’0” (LIN2 is reset mode)
- Set LIN2 Break Field Setting Register (L2BRK)
  BLT = “B’0000”: 13 Tbits Break Transmission
  BDT = “B’00”: 1 Tbit Break Delimiter Transmission
- Set LIN2 Space Setting Register (L2SPC)
  IBSH = “B’000”: 0 Tbit Interbyte Space (Header) /Response Space
  IBS = “B’00”: 0 Tbit Interbyte Space
- Set LIN2 Reponse Field Setting Register (L2RFC)
  RFDL = “B’1000”: 8 bytes + checksum
  RFT = “B’1”: Transmission
  CSM = “B’0”: Classic check sum
  FSM = “B’0”: Non-frame separate mode
- Set LIN2 ID Buffer Register (LIN2IDB)
  IDP = “B’11”
  ID = “B’110101”
- Set LIN2 Data 1 to Data 8 (L2DB1 to L2DB8)
  L2DB1 = “H’00”, L2DB2 = “H’01”,
  L2DB3 = “H’02”, L2DB4 = “H’03”,
  L2DB5 = “H’10”, L2DB6 = “H’11”,
  L2DB7 = “H’12”, L2DB8 = “H’13”,
- Set LIN2 Error Detection Enable Register (L2EDE)
  FERE = “B’1”: Enable Framing Error Detection
  FTERE = “B’1”: Enable Frame Timeout Error Detection
  PBERE = “B’1”: Enable Physical Bus Error Detection
  BERE = “B’1”: Enable Bit Error Detection
- Set to LIN Operation mode
  Set LIN2 Control Register (L2C)
  OM0 = “B’1”
  and, check until LIN2 Mode Status Register (L2MST)’s
  OMM0 == “B’1”
  OM1 = “B’1”
  and, check until LIN2 Mode Status Register (L2MST)’s
  OMM1 == “B’1”
- Set LIN2 Transmission Control Register (L2TC)
  FTS = “B’1”: Start frame transmission
- Check LIN2 Status Register (L2ST)
  until FTC == “B’1” (Frame transmission has been completed)
- Clear Frame Transmit Complete Flag
  LIN2 Status Register (L2ST)
  FTC = “B’0”

Figure 5.8 Frame Transmission (Non–frame separate mode) Processing

5.6.5 Frame Reception Processing

Figure 5.9 shows the Frame reception Processing.



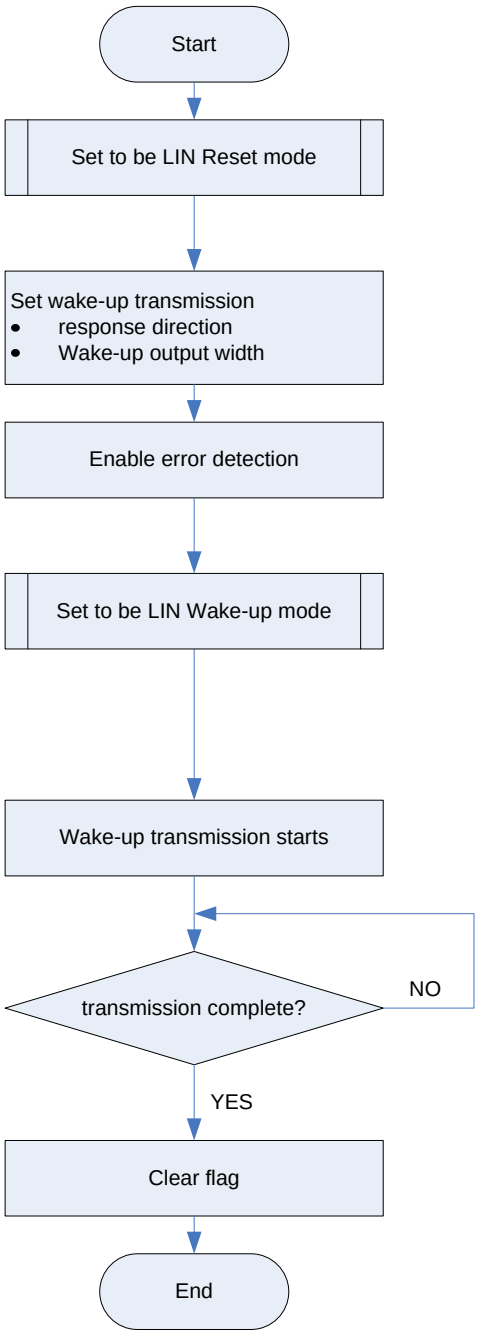
- Set to LIN Reset mode
  Set LIN2 Control Register (L2C)
  OM0 = “B’0”: LIN reset mode
  and, check until LIN2 Mode Status Register (L2MST)’s
  OMM0 == “B’0” (LIN2 is reset mode)
- Set LIN2 Break Field Setting Register (L2BRK)
  BLT = “B’0000”: 13 Tbits Break Transmission
  BDT = “B’00”: 1 Tbit Break Delimiter Transmission
- Set LIN2 Space Setting Register (L2SPC)
  IBSH = “B’000”: 0 Tbit Interbyte Space (Header) /Response Space
- Set LIN2 Reponse Field Setting Register (L2RFC)
  RFDL = “B’1000”: 8 bytes + checksum
  RFT = “B’0”: Reception
  CSM = “B’0”: Classic check sum
- Set LIN2 ID Buffer Register (LIN2IDB)
  IDP = “B’01”
  ID = “B’110110”
- Set LIN2 Error Detection Enable Register (L2EDE)
  FERE = “B’1”: Enable Framing Error Detection
  FTERE = “B’1”: Enable Frame Timeout Error Detection
  PBERE = “B’1”: Enable Physical Bus Error Detection
  BERE = “B’1”: Enable Bit Error Detection
- Set to LIN Operation mode
  Set LIN2 Control Register (L2C)
  OM0 = “B’1”
  and, check until LIN2 Mode Status Register (L2MST)’s
  OMM0 == “B’1”
  OM1 = “B’1”
  and, check until LIN2 Mode Status Register (L2MST)’s
  OMM1 == “B’1”
- Set LIN2 Transmission Control Register (L2TC)
  FTS = “B’1”: Start frame reception
- Check LIN2 Status Register (L2ST)
  until FRC == “B’1” (Frame Reception has been completed)
- Clear Frame Receive Complete Flag
  LIN2 Status Register (L2ST)
  FRC = “B’0”

* LIN slave should check ID & IDP from master and returns response, 8 data bytes and classic checksum is required in this example.

Figure 5.9 Frame Reception Processing

5.6.6 Wake-up Transmission Processing

Figure 5.10 shows the Wake-up transmission Processing.

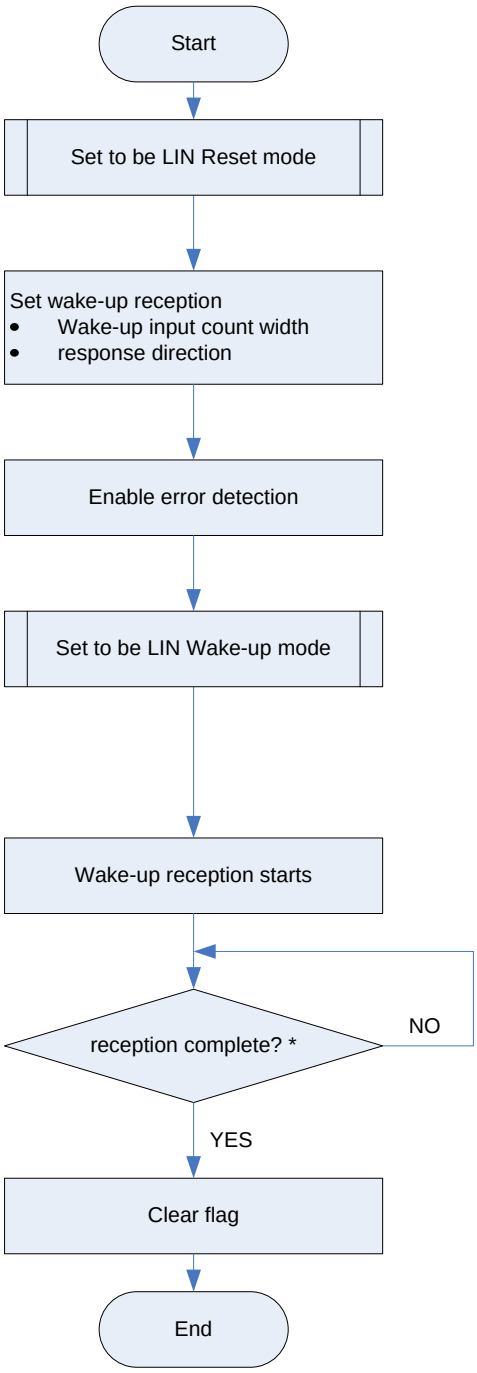


- Set to LIN Reset mode
  Set LIN2 Control Register (L2C)
  OM0 = “B’0”: LIN reset mode
  and, check until LIN2 Mode Status Register (L2MST)’s
  OMM0 == “B’0” (LIN2 is reset mode)
- Set LIN2 Reponse Field Setting Register (L2RFC)
  RFT = “B’1”: Transmission
- Set LIN2 Wake-up Setting Register (L2WUP)
  WUTL = “B’0010”: 3 Tbits Wake-up Transmission Low Time Pulse
- Set LIN2 Error Detection Enable Register (L2EDE)
  FERE = “B’1”: Enable Framing Error Detection
  FTERE = “B’1”: Enable Frame Timeout Error Detection
  PBERE = “B’1”: Enable Physical Bus Error Detection
  BERE = “B’1”: Enable Bit Error Detection
- Set to LIN Wake-up mode
  Set LIN2 Control Register (L2C)
  OM0 = “B’1”
  and, check until LIN2 Mode Status Register (L2MST)’s
  OMM0 == “B’1”
  OM1 = “B’0”
  and, check until LIN2 Mode Status Register (L2MST)’s
  OMM1 == “B’0”
- Set LIN2 Transmission Control Register (L2TC)
  FTS = “B’1”: Start Wake-up transmission
- Check LIN2 Status Register (L2ST)
  until FTC == “B’1” (Wake-up Transmission has been completed)
- Clear Wake-up Transmit Complete Flag
  LIN2 Status Register (L2ST)
  FTC = “B’0”

Figure 5.10 Wake-up Transmission Processing

5.6.7 Wake-up Reception Processing

Figure 5.11 shows the Wake-up reception Processing.



- Set to LIN Reset mode
  Set LIN2 Control Register (L2C)
  OM0 = “B’0”: LIN reset mode
  and, check until LIN2 Mode Status Register (L2MST)’s
  OMM0 == “B’0” (LIN2 is reset mode)
- Set LIN Wake-up Baud Rate Select Register (LWBR)
  LWBR0 = “B’1”: When LIN 2.0 and 2.1 used.
  This allows the input signal Low time to be measured 125us or more.
- Set LIN2 Reponse Field Setting Register (L2RFC)
  RFT = “B’0”: Reception
- Set LIN2 Error Detection Enable Register (L2EDE)
  FERE = “B’1”: Enable Framing Error Detection
  FTERE = “B’1”: Enable Frame Timeout Error Detection
  PBERE = “B’1”: Enable Physical Bus Error Detection
  BERE = “B’1”: Enable Bit Error Detection
- Set to LIN Wake-up mode
  Set LIN2 Control Register (L2C)
  OM0 = “B’1”
  and, check until LIN2 Mode Status Register (L2MST)’s
  OMM0 == “B’1”
  OM1 = “B’0”
  and, check until LIN2 Mode Status Register (L2MST)’s
  OMM1 == “B’0”
- Set LIN2 Transmission Control Register (L2TC)
  FTS = “B’1”: Start Wake-up reception
- Check LIN2 Status Register (L2ST)
  until FRC == “B’1” (Wake-up Reception has been completed)
- Clear Wake-up Receive Complete Flag
  LIN2 Status Register (L2ST)
  FRC = “B’0”

* LIN slave should send specified width wake-up signal. 125 µs or more is required in this example.

Figure 5.11 Wake-up Reception Processing

REVISION HISTORY	SH72A0/SH72A2 Group LIN Application note

Rev.	Date	Description	
		Page	Summary
1.00	May. 15, 2012	—	First edition issued

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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