RZ/T1 Group

Independent Watchdog Timer (IWDTA)

R01AN2579EJ0140
Rev.1.40
Jun. 07, 2018

Introduction

This application notes describes a sample program that performs reset control of the independent watchdog timer (IWDTA).

The major features of the program are listed below:

- After the IWDTA starts operating, refreshing operations are triggered at 273-ms intervals by using a compare match timer (CMT).
- Generation of a software wait in response to the external interrupt (IRQ5) stops refreshing operations, which leads to the generation of a reset. After the reset is generated, LED2 is turned on.

Target Devices for Operation Checking

RZ/T1 Group

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

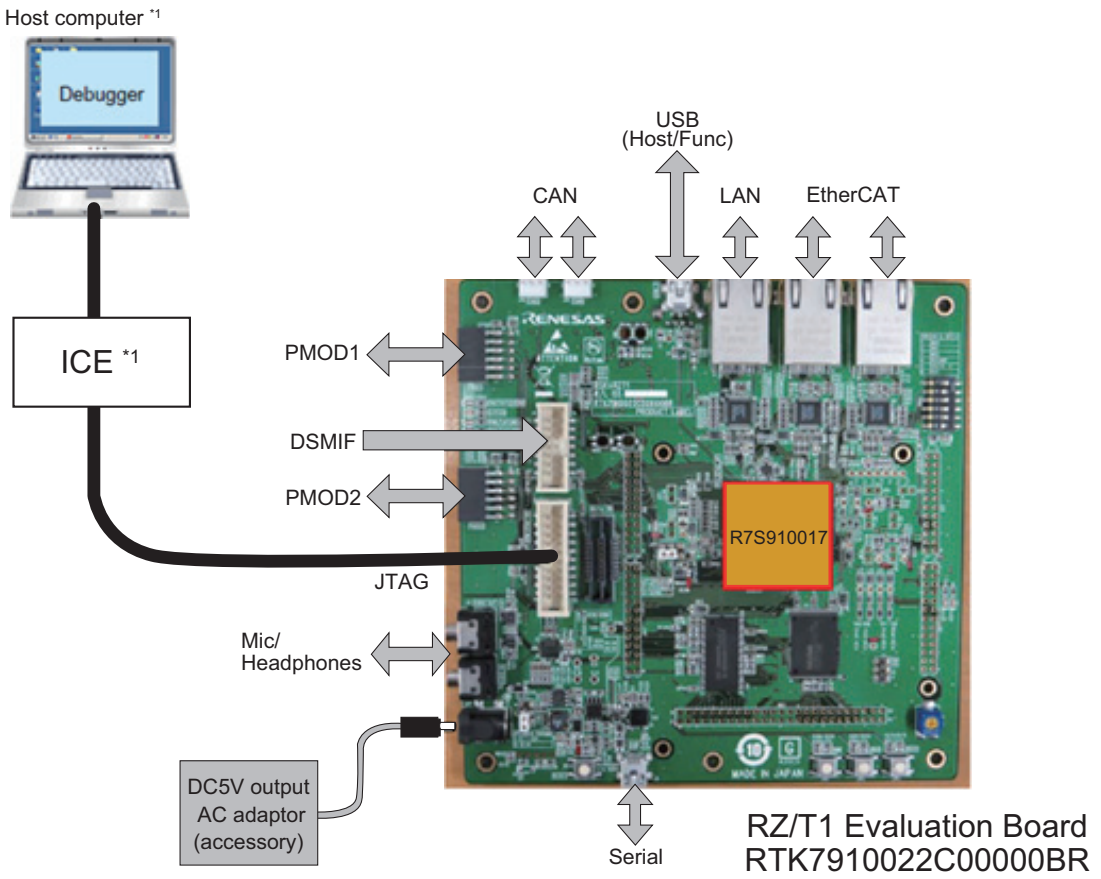
Table of Contents

1. Specifications

Table 1.1 lists the peripheral functions to be used and their applications and Figure 1.1 shows the operating environment.

Table 1.1 Peripheral Functions and Applications

Peripheral Function	Application
Clock Pulse Generator (CPG)	The CPG produces the CPU clock and low-speed on-chip oscillator clock signals
Interrupt Control Unit A (ICUA)	The ICUA is used for the external interrupt input pin (IRQ5) and compare match timer interrupt (CMI0)
Compare Match Timer (CMT)	The CMT is used for cycle counting of a compare match timer.
Independent Watchdog Timer A (IWDTA)	The IWDTA operates with a timeout period of 546.1 ms and control must applied to refresh its counter at regular intervals. An ECM reset is generated in response to an underflow of or error in refreshing the IWDT counter.
Error Control Module (ECM)	The ECM is used to initialize the ERROROUT# pins and to indicate underflows of or errors in refreshing the IWDTA.
General I/O port	The general I/O port is used to control pins for turning the LEDs on and off.



Note 1. Indicates the device that the user needs to prepare.

Figure 1.1 Operating Environment

2. Operating Environment

The sample program of this application is for the environment below.

Table 2.1 Operating Environment

Item	Description
Microcomputer	RZ/T1 Group
Operating frequency	CPUCLK = 450 MHz
Operating voltage	3.3 V
Integrated development environment	Manufactured by IAR Systems Embedded Workbench® for Arm Version 8.20.2 Manufactured by Arm DS-5™ 5.26.2 Manufactured by RENESAS e2studio 6.1.0
Operating modes	SPI boot mode 16-bit bus boot mode
Board	RZ/T1 Evaluation board (RTK7910022C00000BR)
Devices (functions to be used on the board)	• NOR flash memory (connected to CS0/CS1 space) Manufacturer: Macronix International Co. Ltd. Model: MX29GL512FLT2I-10Q • SDRAM (connected to CS2/CS3 space) Manufacturer: Integrated Silicon Solution Inc. Model: IS42S16320D-7TL • Serial flash memory Manufacturer: Macronix International Co. Ltd. Model: MX25L51245G

3. Related Application Notes

Refer to the relevant application notes listed below.

- RZ/T1 Group Initial Settings
- RZ/T1 Group Compare Match Timer (CMT)

4. Peripheral Functions

For the basics of the clock pulse generator (CPG), independent watchdog timer (IWDTA), compare match timer (CMT), interrupt control unit A (ICUA), error control module (ECM), general input/output port, refer to the RZ/T1 Group User's Manual: Hardware.

5. Hardware

5.1 Example of Hardware Configuration

Figure 5.1 shows an example of hardware configuration.

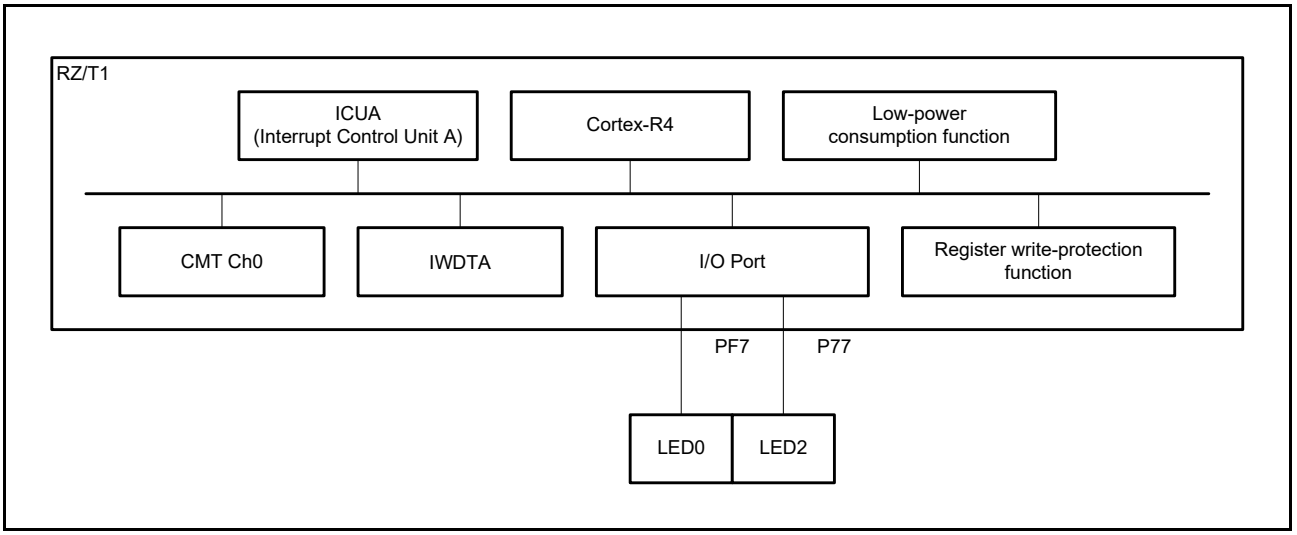


Figure 5.1 Example of Hardware Configuration

5.2 Pins

Table 5.1 shows pins to be used and their functions.

Table 5.1 Pins and Pin Functions

Pin Name	I/O	Function
MD0	Input	Selection of operating modes MD0 = L, MD1 = L, MD2 = L (SPI boot mode) MD0 = L, MD1 = H, MD2 = L (16-bit bus boot mode)
MD1	Input	
MD2	Input	
IRQ5	Input	SW2 (IRQ pin interrupt)
PF7	Output	Turning LED0 on and off
P77	Output	Turning LED2 on and off

6. Software

6.1 Operation Overview

The sample program makes the initial settings of the independent watchdog timer (IWDTA), and then performs refreshing operations at regular intervals by using interval interrupts of the compare match timer.

Pressing SW2 down generates an external pin interrupt 5 and a software wait proceeds during the interrupt processing. During this period, as CMT interval interrupts are held, the IWDTA stops refreshing operations. Thus, the value of the counter of the IWDTA underflows and this leads to notification of an error to the ECM and then to generation of an ECM reset. LED2 is turned on based on the reset judgment after reset release.

Table 6.1 shows the functional overview of the sample program and Figure 6.1 shows the timing diagram.

Table 6.1 Functional Overview

Function	Description
Clock	IWDTCLK/64 (= 120 kHz/64)
Timeout	1024 cycles (= 546.1 ms)
Window	Start: 100% End: 0%
Notification of errors to ECM	Enabled

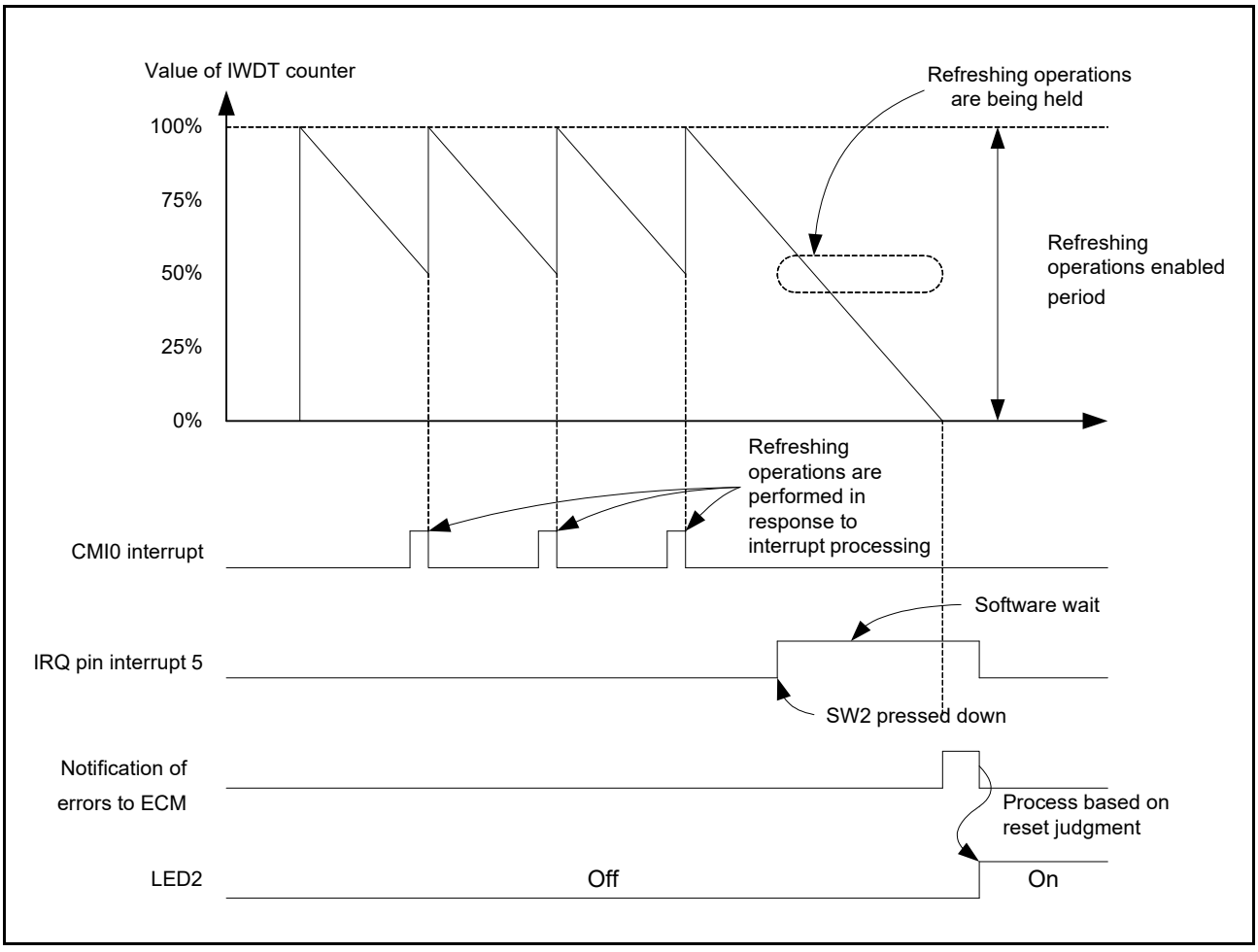


Figure 6.1 Timing Diagram

6.1.1 Project Settings

For the settings of the project to be used on the EWARM for development environment, refer to the Application Note: RZ/T1 Group Initial Settings.

6.2 Memory Map

For the address space of the RZ/T1 Group and a memory map of the RZ/T1 evaluation board, refer to the Application Note: RZ/T1 Group Initial Settings.

6.2.1 Assignment to Sections of Sample Program

Refer to the Application Note: RZ/T1 Group Initial Settings for the sections to be used in the sample program, assignment to sections (loading view) of the sample program in its initial state, and assignment to sections of the sample program following the application of scatter loading (execution view).

6.2.2 MPU Settings

Refer to the Application Note: RZ/T1 Group Initial Settings for MPU settings.

6.2.3 Exception Processing Vector Table

Refer to the Application Note: RZ/T1 Group Initial Settings for the vector table for exception processing.

6.3 Interrupts

Table 6.2 shows interrupts to be used in the sample program.

Table 6.2 Interrupts for Sample Program

Interrupt (Source ID)	Priority	Processing
IRQ pin interrupt 5 (IRQ9)	0	Pressing SW2 down causes an underflow without refreshing of the IWDTA and generates an ECM reset. Based on the reset judgment after reset release, LED2 is turned on.
Compare match interrupt_ch0 (CMI0)	15	Every time an interval period (273-ms interval) is generated, refreshing operations of the IWDTA are performed.

6.4 Fixed-Width Integer Types

Table 6.3 shows fixed width integers to be used in the sample program.

Table 6.3 Fixed-Width Integers for Sample Program

Symbol	Description
int8_t	8-bit signed integer (defined in the standard library)
int16_t	16-bit signed integer (defined in the standard library)
int32_t	32-bit signed integer (defined in the standard library)
int64_t	64-bit signed integer (defined in the standard library)
uint8_t	8-bit unsigned integer (defined in the standard library)
uint16_t	16-bit unsigned integer (defined in the standard library)
uint32_t	32-bit unsigned integer (defined in the standard library)
uint64_t	64-bit unsigned integer (defined in the standard library)

6.5 Constants/Error Codes

Table 6.4 shows constants to be used in the sample program.

Table 6.4 Constants for Sample Program

Constant Name	Setting Value	Description
IWDT_STAT_REFRESH_ERR_MASK	(0x8000)	A definition to acquire a refreshing error flag from the IWDT status.
IWDT_STAT_UNDERFLOW_ERR_MASK	(0x4000)	A definition to acquire an underflow flag from the IWDT status.
IWDT_STAT_ERROR_MASK	(0xC000)	A definition to acquire a refreshing error flag and underflow flag from the IWDT status.
IWDT_STAT_COUNTER_MASK	(0x3FFF)	A definition to acquire a counter value from the IWDT status.
IWDT_CFG_PARAM_CHECKING_ENABLE	(1)	The API function of IWDTA indicates enabling (1) or disabling (0) of parameter checking.

6.6 Structures/Unions/Enumerated Types

Figure 6.2 to Figure 6.4 show the structures, unions, and enumerated types to be used in the sample program.

```
typedef enum e_iwdt_err            // IWDT API error codes
{
    IWDT_SUCCESS=0,
    IWDT_ERR_OPEN_IGNORED,      // The module has already been Open()ed
    IWDT_ERR_INVALID_ARG,       // Argument is not valid for parameter
    IWDT_ERR_NULL_PTR,          // Received null pointer or missing required argument
    IWDT_ERR_NOT_OPENED         // Open function has not yet been called
} iwdt_err_t;

/* Open() DEFINITIONS */
typedef enum e_iwdt_timeout                    // IWDT Time-Out Period
{
    IWDT_TIMEOUT_1024 =0x0000u,              // 1024 (cycles)
    IWDT_TIMEOUT_4096 =0x0001u,              // 4096 (cycles)
    IWDT_TIMEOUT_8192 =0x0002u,              // 8192 (cycles)
    IWDT_TIMEOUT_16384=0x0003u,              // 16,384 (cycles)
    IWDT_NUM_TIMEOUTS
} iwdt_timeout_t;

typedef enum e_iwdt_clock_div              // IWDT Clock Division Ratio
{
    IWDT_CLOCK_DIV_1  =0x0000u,            // IWDTCLK/1
    IWDT_CLOCK_DIV_16 =0x0020u,            // IWDTCLK/16
    IWDT_CLOCK_DIV_32 =0x0030u,            // IWDTCLK/32
    IWDT_CLOCK_DIV_64 =0x0040u,            // IWDTCLK/64
    IWDT_CLOCK_DIV_128=0x00F0u,            // IWDTCLK/128
    IWDT_CLOCK_DIV_256=0x0050u             // IWDTCLK/256
} iwdt_clock_div_t;
```

Figure 6.2 Structures/Unions/Enumerated Types for Sample Program

```
typedef enum e_iwdt_window_end                  // Window End Position
{
    IWDT_WINDOW_END_75=0x0000u,             // 75%
    IWDT_WINDOW_END_50=0x0100u,             // 50%
    IWDT_WINDOW_END_25=0x0200u,             // 25%
    IWDT_WINDOW_END_0 =0x0300u              // 0% (window end position is not specified)
} iwdt_window_end_t;

typedef enum e_iwdt_window_start                // Window Start Position
{
    IWDT_WINDOW_START_25 =0x0000u,      // 25%
    IWDT_WINDOW_START_50 =0x1000u,      // 50%
    IWDT_WINDOW_START_75 =0x2000u,      // 75%
    IWDT_WINDOW_START_100=0x3000u       // 100% (window start position is not specified)
} iwdt_window_start_t;

typedef enum e_iwdt_timeout_control     // Signal control when Time-out and Refresh error
{
    IWDT_ERROR_ENABLE =0x00u,       // Error output is enebled
    IWDT_ERROR_DISABLE=0x80u        // Error output is disabled
} iwdt_timeout_control_t;

typedef struct st_iwdt_config                   // IWDT configuration options used in Open function
{
    iwdt_timeout_t          timeout;                    // Time-out period
    iwdt_clock_div_t        iwdtclk_div;            // IWDT clock division ratio
    iwdt_window_start_t     window_start;           // Window start position
    iwdt_window_end_t       window_end;             // Window end position
    iwdt_timeout_control_t  timeout_control;    // ERROR output when time-out
 } iwdt_config_t;
```

Figure 6.3 Structures/Unions/Enumerated Types for Sample Program

```
/* Control() DEFINITIONS */

typedef enum e_iwdt_cmd                         // Command used in Control and GetStatus function
{
    IWDT_CMD_GET_STATUS,                        // Get IWDT status
    IWDT_CMD_REFRESH_COUNTING,          // Refresh the counter
    IWDT_CMD_NO_ACTION,
} iwdt_cmd_t;
```

Figure 6.4 Structures/Unions/Enumerated Types for Sample Program

6.7 Functions

Table 6.5 lists functions to be used.

Table 6.5 Functions

Function	Page Number
main	13
iwdt_init	13
R_IWDT_Open	14
R_IWDT_Control	15
R_IRQ9_isr	15
R_IRQ21_isr	15

6.8 Specifications of Functions

6.8.1 main

main	
Synopsis	Main processing
Declaration	int main (void)
Description	This function makes initial settings for the ports, ECM, CMT, ICU, and IWDT, and starts operation of CMT0. After that, the main loop of the function repeatedly alternates between LED0 on and off.
Arguments	None
Return value	None
Supplement	None

6.8.2 iwdt_init

iwdt_init	
Synopsis	Initializing IWDT
Declaration	void iwdt_init (void)
Description	This function initializes the IWDT and starts counting operation of the IWDT.
Arguments	None
Return value	None
Supplement	None

6.8.3 R_IWDT_Open

R_IWDT_Open		
Synopsis	IWDTA open	
Header	r_iwdt_if.h	
Declaration	iwdt_err_t R_IWDT_Open (void * const p_cfg)	
Description	This function initializes IWDTA-related registers and sets the options of the IWDT counter.	
Arguments	uint16_t channel	This specifies the WDT channels Setting range: (0, 1)
	void * const p_cfg	The pointer that stores the data group to be set in the IWDTA-related registers Timeout period IWDT_TIMEOUT_1024 IWDT_TIMEOUT_4096 IWDT_TIMEOUT_8192 IWDT_TIMEOUT_16384 Clock division ratio IWDT_CLOCK_DIV_1 IWDT_CLOCK_DIV_16 IWDT_CLOCK_DIV_32 IWDT_CLOCK_DIV_64 IWDT_CLOCK_DIV_128 IWDT_CLOCK_DIV_256 Window stop IWDT_WINDOW_END_75 IWDT_WINDOW_END_50 IWDT_WINDOW_END_25 IWDT_WINDOW_END_0 Window start IWDT_WINDOW_START_25 IWDT_WINDOW_START_50 IWDT_WINDOW_START_75 IWDT_WINDOW_START_100 Notification of ECM errors IWDT_ERROR_ENABLE IWDT_ERROR_DISABLE
Return value	Execution result of the open function IWDT_SUCCESS: IWDT initialized IWDT_ERR_OPEN_IGNORED: Module already opened IWDT_ERR_INVALID_ARG: Invalid values included in the element of the p_cfg structure. IWDT_ERR_NULL_PTR: p_cfg pointer null	
Supplement	Setting IWDT_CFG_PARAM_CHECKING_ENABLE that is defined by r_iwdt_config.h to 1 enables checking of the parameters of the arguments.	

6.8.4 R_IWDT_Control

R_IWDT_Control		
Synopsis	Controlling IWDTA	
Header	r_iwdt_if.h	
Declaration	iwdt_err_t R_IWDT_Control (iwdt_cmd_t const cmd, uint16_t * p_status)	
Description	This function reads the state of the IWDT and refreshes the down counter of the IWDT.	
Arguments	iwdt_cmd_t const cmd	Specifies the command to be executed IWDT_CMD_GET_STATUS IWDT_CMD_REFRESH_COUNTING
	uint16_t * p_status	The pointer to the storage positions of the counter and status flag
Return value	Execution result of the control function IWDT_SUCCESS: Command completed IWDT_ERR_INVALID_ARG: Argument value invalid IWDT_ERR_NULL_PTR: p_status null. IWDT_ERR_NOT_OPEND: Open unread	
Supplement	Setting IWDT_CFG_PARAM_CHECKING_ENABLE that is defined by r_iwdt_config.h to 1 enables checking of the parameters of the argument.	

6.8.5 R_IRQ9_isr

R_IRQ9_isr	
Synopsis	IRQ9 interrupt (IRQ pin interrupt 5) processing
Declaration	void R_IRQ9_isr (void)
Description	This function executes software wait processing (approx. 3 seconds). During this period, it causes an underflow of the independent watchdog timer and generates an ECM reset. It also turns LED2 on based on the reset judgment after reset release.
Arguments	None
Return value	None
Supplement	None

6.8.6 R_IRQ21_isr

R_IRQ21_isr	
Synopsis	IRQ21 interrupt (compare match timer (CMI0)) processing
Declaration	void R_IRQ21_isr (void)
Description	This functions performs refreshing operations of the independent watchdog timer.
Arguments	None
Return value	None
Supplement	None

6.9 Flowcharts

6.9.1 Main Processing

Figure 6.5 shows a flowchart of main processing.

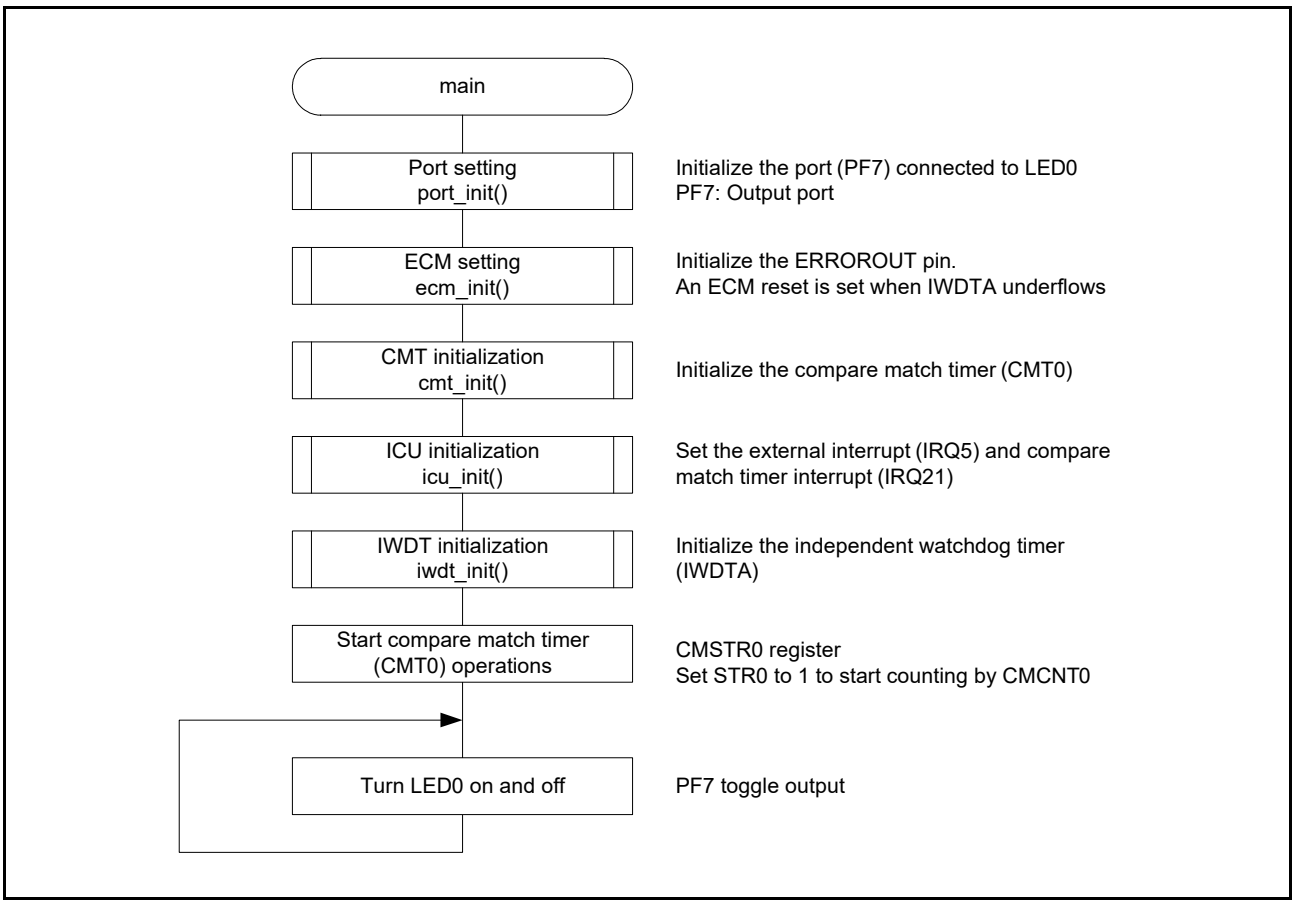


Figure 6.5 Main Processing

6.9.2 IWDT Initialization

Figure 6.6 show a flowchart of IWDT initialization.

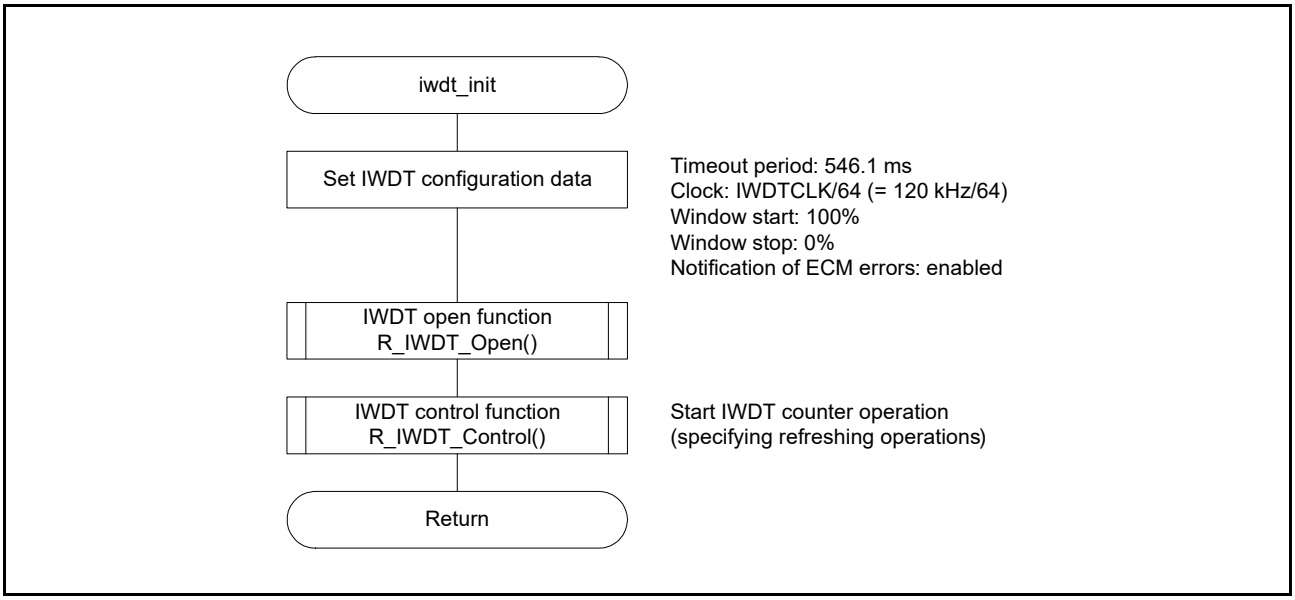
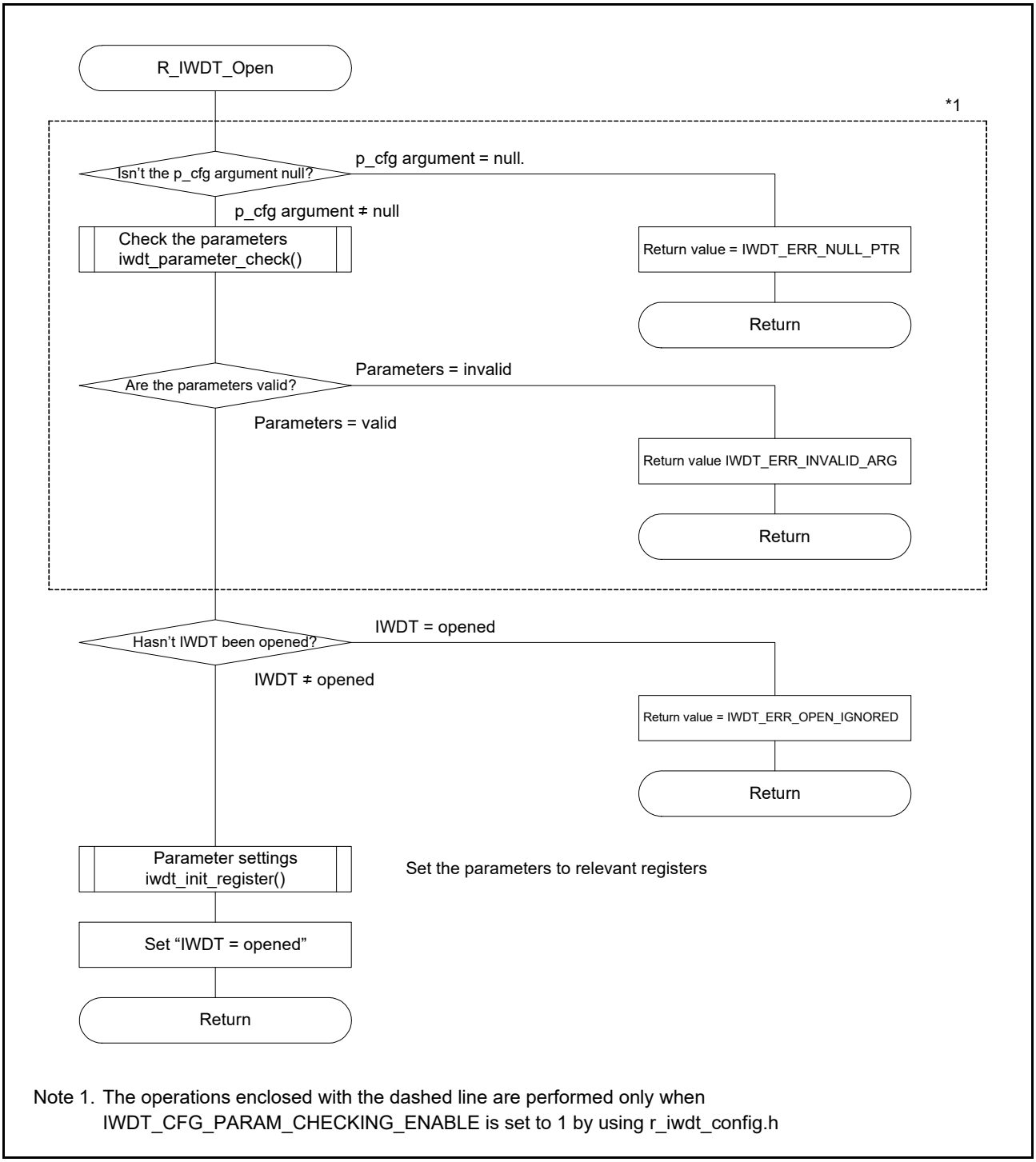


Figure 6.6 IWDT Initialization

6.9.3 IWDT Open Function

Figure 6.7 shows a flowchart of IWDT open function.

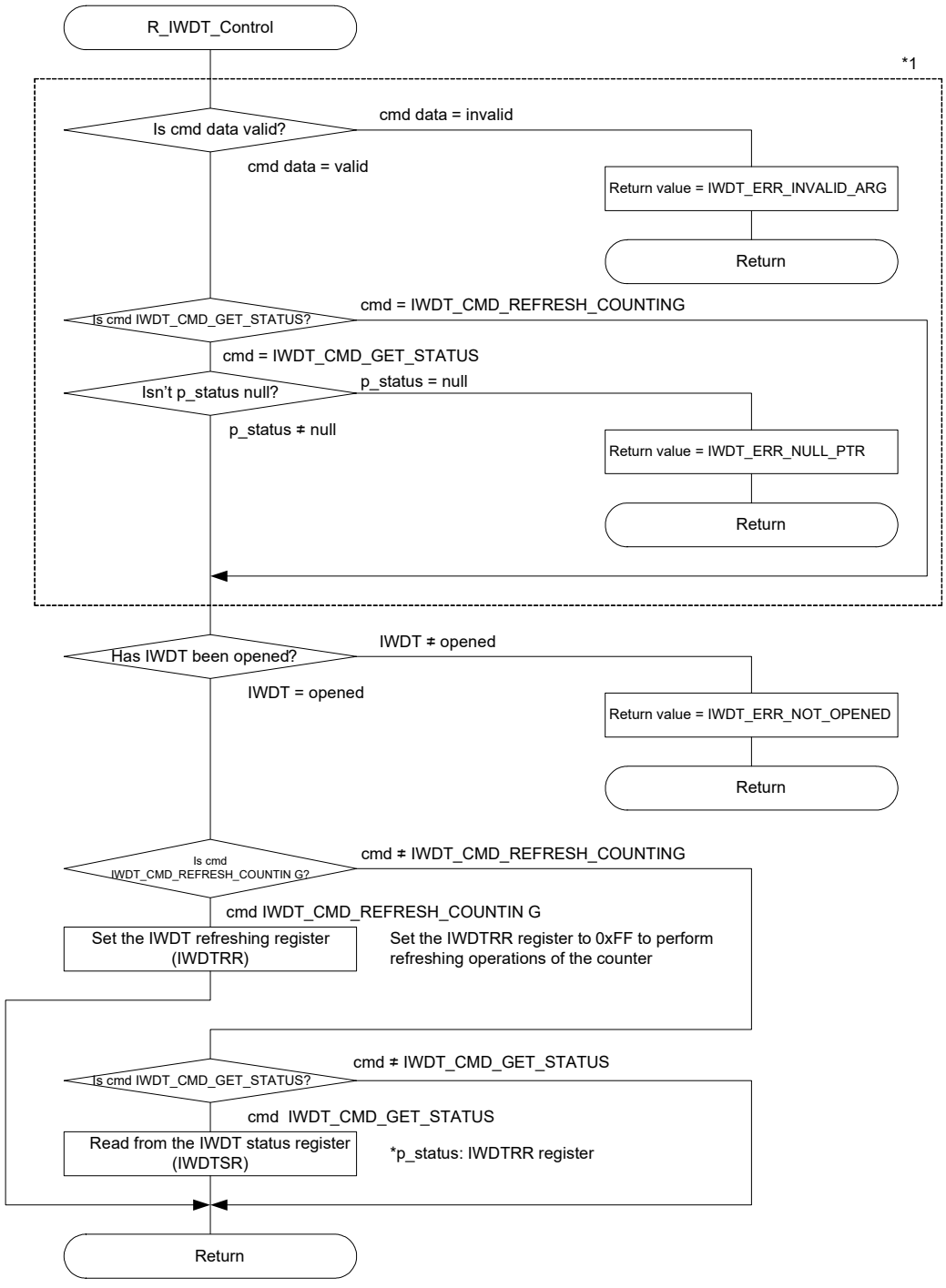


Note 1. The operations enclosed with the dashed line are performed only when IWDT_CFG_PARAM_CHECKING_ENABLE is set to 1 by using r_iwdt_config.h

Figure 6.7 IWDT Open Function

6.9.4 IWDT Control Function

Figure 6.8 shows a flowchart of the IWDT control function.



Note 1. The operations enclosed with the dashed line are performed only when IWDT_CFG_PARAM_CHECKING_ENABLE is set to 1 by using r_iwdt_config.h.

Figure 6.8 IWDT Control Function

6.9.5 IRQ9 Interrupt (IRQ Pin Interrupt 5) Processing

Figure 6.9 shows a flowchart of the IRQ9 interrupt (IRQ pin interrupt 5) processing.

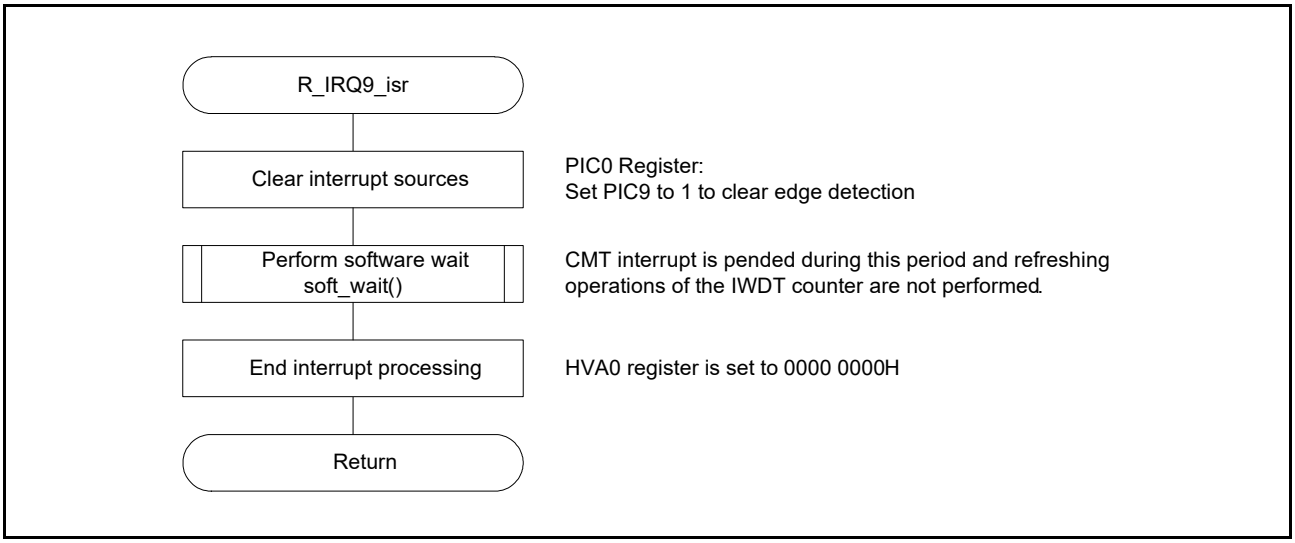


Figure 6.9 IRQ9 Interrupt (IRQ Pin Interrupt 5) Processing

6.9.6 IRQ21 Interrupt (Compare Match Timer Ch0 Interrupt) Processing

Figure 6.10 shows a flowchart of IRQ21 interrupt (compare match timer ch0 interrupt) processing.

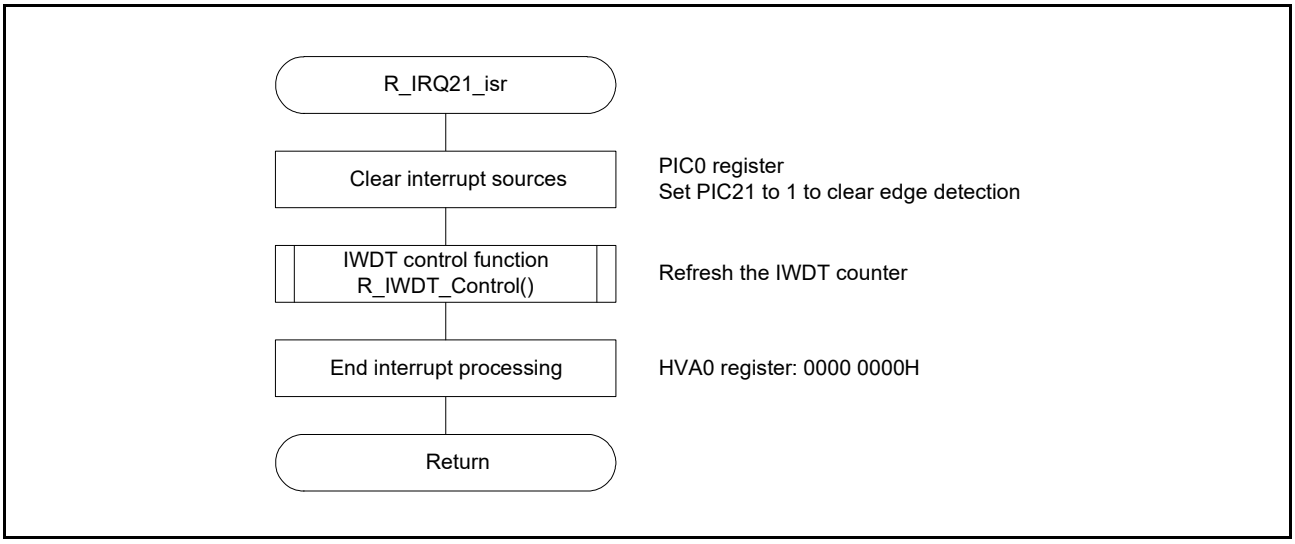


Figure 6.10 IRQ21 Interrupt (Compare Match Timer ch0 Interrupt) Processing

7. Sample Program

The sample program is available on the Renesas Electronics website.

8. Reference Documents

User's manual: hardware:
RZ/T1 Group User's Manual: Hardware
(Download the latest version of the manual from the Renesas Electronics website.)

RZ/T1 Evaluation Board RTK7910022C00000BR User's Manual
(Download the latest version of the manual from the Renesas Electronics website.)

Technical Update / Technical News
(Download the latest version of the update or news from the Renesas Electronics website.)

User's manual: Development Environment
For IAR integrated development environment (IAR Embedded Workbench® for Arm), visit the IAR Systems website.
(Download the latest version from the IAR Systems website.)

Website and Support

Renesas Electronics website

http://www.renesas.com/

Inquiries

http://www.renesas.com/inquiry

Revision History	Application Note: Independent Watchdog Timer (IWDTA)

Rev.	Date	Description	
		Page	Summary
0.20	Mar. 18, 2015	—	First Edition issued
1.00	Apr. 10, 2015	—	Only the revision number was changed to be posted on a website.
1.10	Aug. 18, 2015	2. Operating Environment	
		4	Table 2.1 Operating Environment: Integrated Development Environment, partially amended and added
		6. Software	
		9	6.2.4 Required Memory Size: Description and reference added
		9	Table 6.2: Table title was partially amended
		10	Table 6.3 added
		10	Table 6.4 added
1.20	Dec. 04, 2015	2. Operating Environment	
		4	Table 2.1 Operating Environment: Integrated Development Environment, information partially amended
1.30	Apr. 05, 2017	2. Operating Environment	
		4	Table 2.1 Operating Environment: Integrated Development Environment, modified
		6. Software	
		—	6.2.4 Required Memory Size, deleted
1.40	Jun. 07, 2018	2. Operating Environment	
		4	Table 2.1 Operating Environment: The description on the integrated development environment, modified
		5. Hardware	
		7	Figure 5.1 Hardware configuration example: The name of module, modified
		8. Related Documents	
		22	The name of IAR Embedded Workbench, modified

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

RENESAS

SALES OFFICES

Renesas Electronics Corporation

http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

Colophon 7.0