RX63N Group, RX631 Group

Example of Using the External Bus (Separate Bus)

R01AN2119EJ0100
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Abstract

This document describes an example of connecting the SRAM to the MCU using the separate bus interface in the RX63N and RX631 Groups.

Products

- RX63N Group 177-pin and 176-pin packages with a ROM size between 768 KB and 2 MB
- RX63N Group 145-pin and 144-pin packages with a ROM size between 768 KB and 2 MB
- RX63N Group 100-pin package with a ROM size between 768 KB and 2 MB
- RX631 Group 177-pin and 176-pin packages with a ROM size between 256 KB and 2 MB
- RX631 Group 145-pin and 144-pin packages with a ROM size between 256 KB and 2 MB
- RX631 Group 100-pin package with a ROM size between 256 KB and 2 MB

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

The SRAM is connected to the MCU using the external bus with the separate bus interface to write, read, and verify data in 16-bit bus width.

After a reset, data is written in words to a 4-Mbit SRAM area which is an external address space. When all SRAM areas have been written, the written data are read.

If the read value matches the written value (verification succeeded), LED0 is turned on. If the values do not match (verification error), LED1 is turned on.

If a bus error occurs, LED2 is turned on.

Table 1.1 lists the Peripheral Functions and Their Applications, Table 1.2 lists the Specification of the SRAM, and Figure 1.1 shows the Block Diagram.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
Bus (external bus)	Connection to the SRAM
Interrupt controller	Bus error detection
I/O ports	Turn on LEDs

Table 1.2 Specification of the SRAM

Peripheral Function	Application
Product	R1RW0416DSB-2PI (Renesas Electronics)
Organization	256 Kwords × 16 bits
Memory size	4 Mbits
Access time	12 ns (max.)

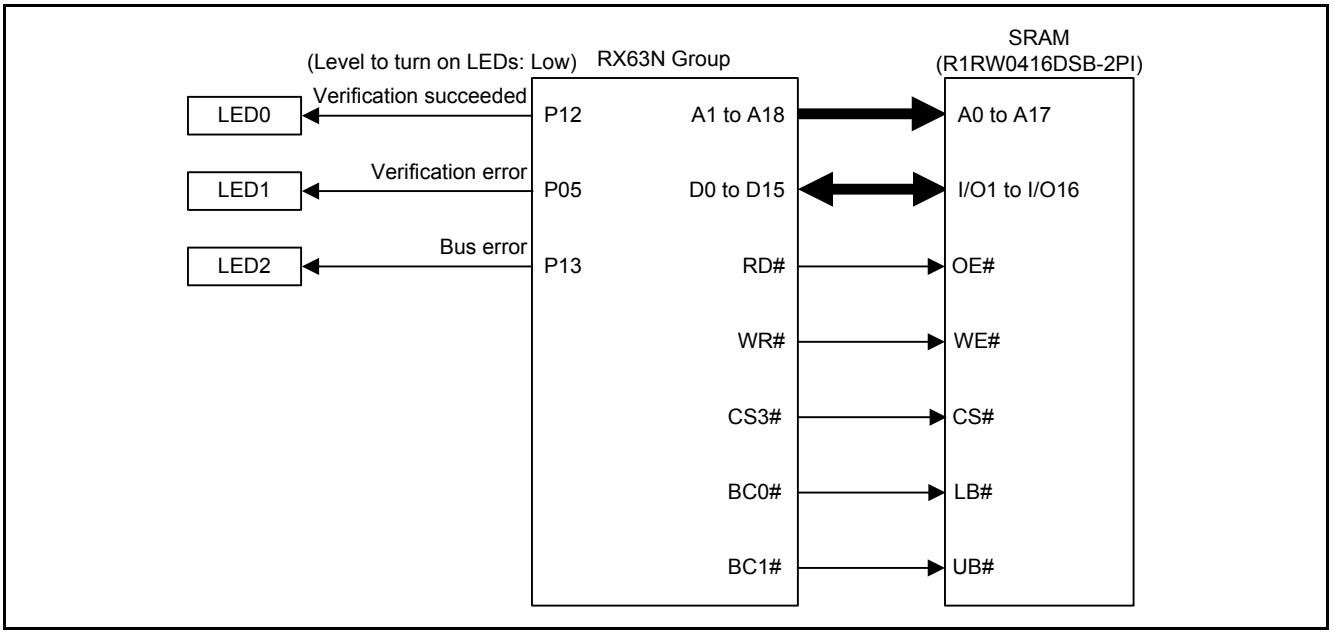

Figure 1.1 Block Diagram

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	R5F563NBDDFC (RX63N Group)
Operating frequencies	- Main clock: 12 MHz - PLL: 192 MHz (main clock divided by 1 and multiplied by 16) - System clock (ICLK): 96 MHz (PLL divided by 2) - Peripheral module clock B (PCLKB): 48 MHz (PLL divided by 4) - External bus clock (BCLK): 96 MHz (PLL divided by 2)
Operating voltage	3.3 V
Integrated development environment	Renesas Electronics Corporation High-performance Embedded Workshop Version 4.09.01
C compiler	Renesas Electronics Corporation C/C++ Compiler Package for RX Family V.1.02 Release 01
	Compile options -cpu=rx600 -output=obj="$(CONFIGDIR)\$(FILELEAF).obj" -debug -nologo (The default setting is used in the integrated development environment.)
iodefine.h version	Version 1.6A
Endian	Little endian
Operating mode	On-chip ROM enabled expansion mode
Processor mode	Supervisor mode
Sample code version	Version 1.00
SRAM	Renesas R1RW0416DSB-2PI (256 Kwords × 16 bits)

3. Reference Application Note

For additional information associated with this document, refer to the following application note.

- RX63N Group, RX631 Group Initial Setting Rev. 1.10 (R01AN1245EJ)

The initial setting functions in the reference application note are used in the sample code in this application note. The revision number of the reference application note is current as of when this application note was made. However the latest version is always recommended. Visit the Renesas Electronics Corporation website to check and download the latest version.

4. Hardware

4.1 Hardware Configuration

In this application note, the SRAM is accessed by connecting with 16-bit data bus using the separate bus interface.

Figure 4.1 shows the Connection Example with 16-Bit Separate Bus.

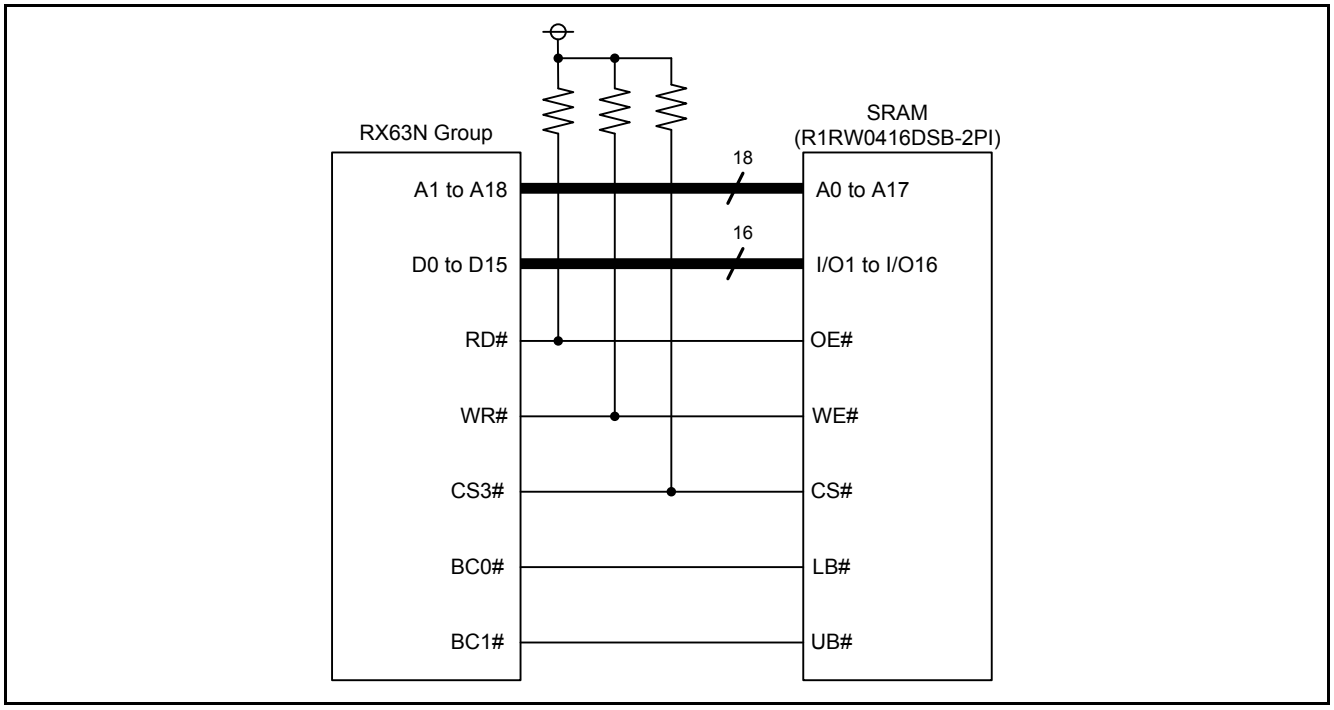

Figure 4.1 Connection Example with 16-Bit Separate Bus

4.2 Pins Used

Table 4.1 lists the Pins Used and Their Functions.

Table 4.1 Pins Used and Their Functions

Pin Name	I/O	Function
P12	Output	LED0 output (verification succeeded)
P05	Output	LED1 output (verification error)
P13	Output	LED2 output (bus error)
PA7 to PA1/A7 to A1	Output	Pins to output addresses
PB7 to PB0/A15 to A8	Output	Pins to output addresses
PC2 to PC0/A18 to A16	Output	Pins to output addresses
PD7 to PD0/D7 to D0	I/O	Data I/O pins
PE7 to PE0/D15 to D8	I/O	Data I/O pins
PA0/A0/BC0#	Output	Pin to output a strobe signal which indicates D7 to D0 are enabled
P51//BC1#	Output	Pin to output a strobe signal which indicates D15 to D8 are enabled
P52/RD#	Output	Pin to output a strobe signal which indicates read operation is in progress
P50/WR0#/WR#	Output	Pin to output a strobe signal which indicates write operation is in progress
PC4/CS3#	Output	Pin to output the chip select signal for area 3 (CS3)

5. Software

After a reset, settings to access the CS3 area of the external bus in 16-bit bus width are configured and on-chip ROM enabled expansion mode is selected.

The data is written to all areas in the SRAM starting from the start address of the CS3 area. The data to be written is incremented every write operation.

The written data is read from the start address of the CS3 area and verified with data for verification. If all data in the SRAM and data for verification match, LED0 is turned on. If the data do not match, LED1 is turned on.

If a bus error occurs, LED2 is turned on in the bus error interrupt handling.

Table 5.1 shows the Wait Control Setting Cycles.

High driving ability output is selected according to the wiring capacity on external bus pins.

Table 5.1 Wait Control Setting Cycles

Wait Control Name	Symbol	Setting Cycles
Wait for CS assertion	CSON	0 cycles
Wait for write data output	WDON	1 cycle
Wait for WR assertion	WRON	1 cycle
Wait for normal write cycle	CSWWAIT	2 cycles
Extension cycle of write data output	WDOFF	1 cycle
Write-access CS extension cycle	CSWOFF	1 cycle
Wait for RD assertion	RDON	0 cycles
Wait for normal read cycle	CSRWAIT	4 cycles
Read-access CS extension cycle	CSROFF	1 cycle

Note: • Cycles for control signals need to be adjusted taking into account influences of the AC characteristic of the SRAM, signal pathways to connect to the MCU, and so on.

5.1 Operation Overview

16-bit data is written to and read from the address in the CS3 area.

Read/write operations are controlled by control signals on external bus pins according to timings specified.

Control timings for external bus signals need to be specified taking in account influences of the external bus clock cycle (approximately 10.41 ns here), the AC characteristic of the SRAM, signal pathways to connect to the SRAM, and so on.

5.1.1 SRAM Control Timing

Figure 5.1 shows the R1RW0416DSB-2PI Control Timing for Read/Write Operations.

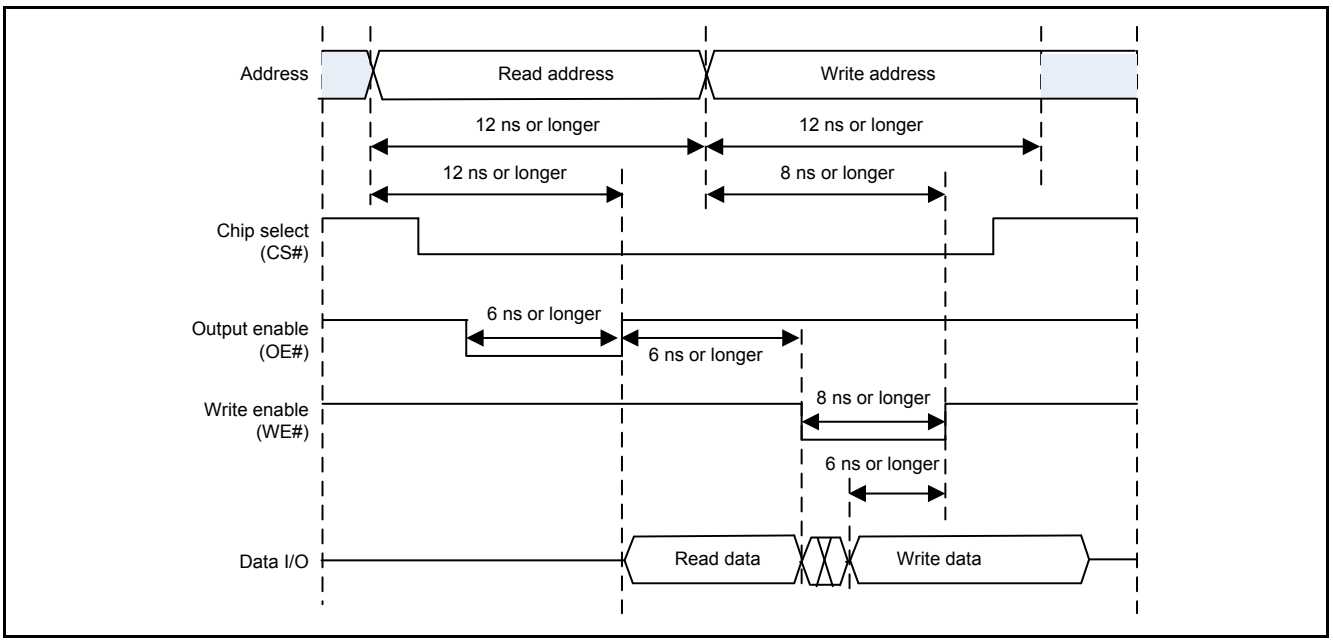

Figure 5.1 R1RW0416DSB-2PI Control Timing for Read/Write Operations

5.1.2 Writing Data to the SRAM

Figure 5.2 shows the Bus Timing for Normal Write in Single Write Strobe Mode.

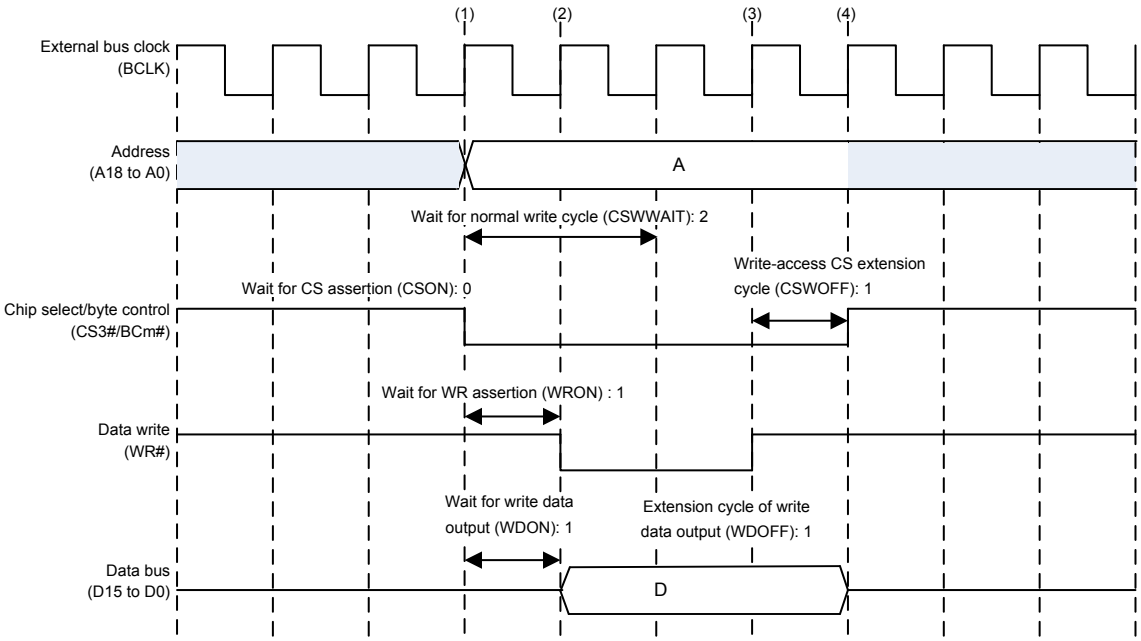

Figure 5.2 Bus Timing for Normal Write in Single Write Strobe Mode (m = 0 and 1)

(1) Address output and CS assertion

The write destination address for the data is output, the CS3# signal is asserted, and normal write access is started.

(2) WR assertion and write data output

The WR# signal is asserted and the write data is output at the same time.

(3) WR negation

The WR# signal is negated at the next cycle of the cycle which the wait period for normal write cycle is completed.

(4) CS negation and completion of write data output extension

The CS# signal is negated and the extension cycle of write data output is completed at the same time, and normal write access is completed.

5.1.3 Reading Data from the SRAM

Figure 5.3 shows the bus timing when reading data from the SRAM (normal read).

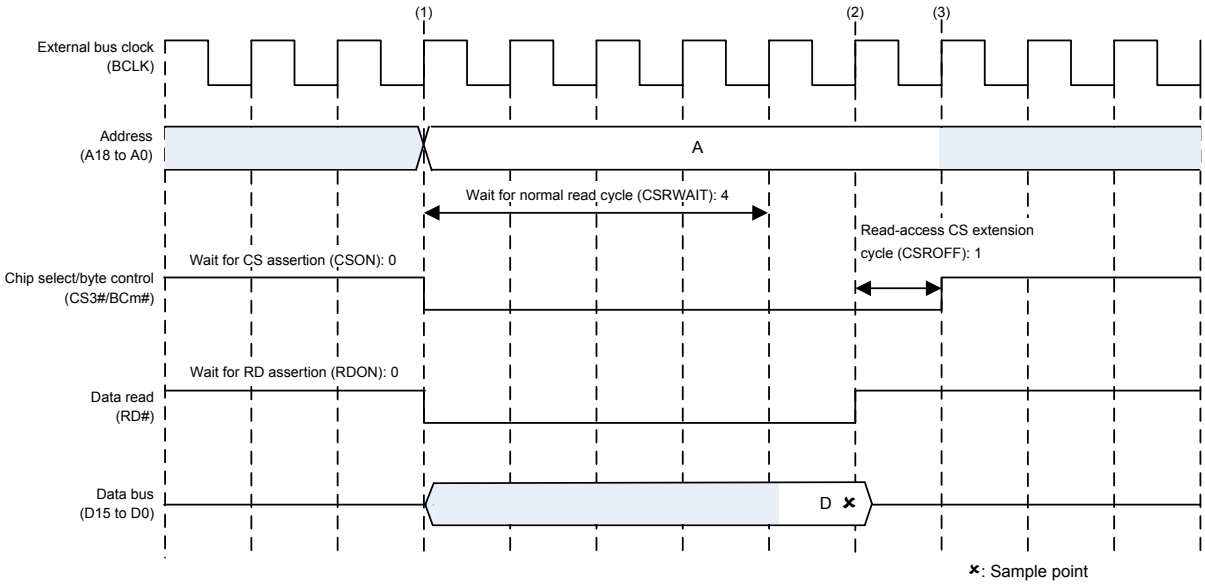

Figure 5.3 Bus Timing for Normal Read (m = 0 and 1)

(1) Address output, CS assertion, and RD assertion

The read source address for the data is output, the CS3# and RD# signals are asserted, and normal read access is started.

(2) Read data sampling

The RD# signal is negated at the next cycle of the cycle which the wait period for normal read cycle is completed, and the read data is sampled.

(3) CS negation

The CS3# signal is negated and normal read access is completed.

5.2 File Composition

Table 5.2 lists the File Used in the Sample Code, Table 5.3 lists the Standard Include Files, and Table 5.4 lists the Functions and Setting Values in the Reference Application Note. Files generated by the integrated development environment are not included in this table.

Table 5.2 File Used in the Sample Code

File Name	Outline
main.c	Main processing

Table 5.3 Standard Include Files

File Name	Outline
stdint.h	Defines macros declaring the integer type with the specified width.
machine.h	Defines types of intrinsic function for the RX Family.

Table 5.4 Functions and Setting Values in the Reference Application Note
(RX63N Group, RX631 Group Initial Setting)

File Name	Function	Description
r_init_stop_module.c	R_INIT_StopModule()	Module-stop state is canceled for DMAC/DTC, EXDMAC, RAM0, and RAM1.
r_init_stop_module.h	—	
r_init_non_existent_port.c	R_INIT_NonExistentPort()	
r_init_non_existent_port.h	—	176-pin package is specified.
r_init_clock.c	R_INIT_Clock()	External bus clock (BCLK) is set to divide-by-2.
r_init_clock.h	—	Sub-clock is not used.

5.3 Option-Setting Memory

Table 5.5 lists the Option-Setting Memory Configured in the Sample Code. When necessary, set a value suited to the user system.

Table 5.5 Option-Setting Memory Configured in the Sample Code

Symbol	Address	Setting Value	Contents
OFS0	FFFF FF8Fh to FFFF FF8Ch	FFFF FFFFh	The IWDT is stopped after a reset. The WDT is stopped after a reset.
OFS1	FFFF FF8Bh to FFFF FF88h	FFFF FFFFh	The voltage monitor 0 reset is disabled after a reset. HOCO oscillation is disabled after a reset.
MDES	FFFF FF83h to FFFF FF80h	FFFF FFFFh	Little endian

5.4 Constants

Table 5.6 lists the Constants Used in the Sample Code (main.c) .

Table 5.6 Constants Used in the Sample Code (main.c)

Constant Name	Setting Value	Contents
SRAM_TOP	(void*)(0x05000000)	Start address of the SRAM area
SRAM_END	(void*)(0x05080000)	End address of the SRAM area + 1
CS3_WRCV	2	Number of cycles for write recovery
CS3_RRCV	2	Number of cycles for read recovery
BSC_CSRECEN	0x0000	Value of the CS recovery cycle insertion enable register
CS3_CSRWAIT	4	Number of cycles for the wait for normal read cycle
CS3_CSWWAIT	2	Number of cycles for the wait for normal write cycle
CS3_CSPRWAIT	7	Number of cycles for the wait for page read cycle
CS3_CSPWWAIT	7	Number of cycles for the wait for page write cycle
CS3_CSON	0	Number of cycles for the wait for CS assertion
CS3_WDON	1	Number of cycles for the wait for write data output
CS3_WRON	1	Number of cycles for the wait for WR assertion
CS3_RDON	0	Number of cycles for the wait for RD assertion
CS3_AWAIT	0	Number of cycles for the wait for address cycle
CS3_WDOFF	0	Number of cycles for extension cycle of write data output
CS3_CSWOFF	1	Number of cycles for write-access CS extension cycle
CS3_CSROFF	1	Number of cycles for read-access CS extension cycle
LED0_REG_PODR	PORT1.PODR.BIT.B2	Output data store bit for LED0
LED0_REG_PDR	PORT1.PDR.BIT.B2	I/O select bit for LED0
LED0_REG_PMR	PORT1.PMR.BIT.B2	Pin mode control bit for LED0
LED1_REG_PODR	PORT0.PODR.BIT.B5	Output data store bit for LED1
LED1_REG_PDR	PORT0.PDR.BIT.B5	I/O select bit for LED1
LED1_REG_PMR	PORT0.PMR.BIT.B5	Pin mode control bit for LED1
LED2_REG_PODR	PORT1.PODR.BIT.B3	Output data store bit for LED2
LED2_REG_PDR	PORT1.PDR.BIT.B3	I/O select bit for LED2
LED2_REG_PMR	PORT1.PMR.BIT.B3	Pin mode control bit for LED2
LED_ON	0	LED output data: Turn on
LED_OFF	1	LED output data: Turn off

5.5 Variables

Table 5.7 lists the static Variables.

Table 5.7 static Variables

Type	Variable Name	Contents	Function Used
uint16_t *	p_sram_adr	SRAM access address	main
uint16_t	sram_data	Write data	main
uint16_t	sram_cmp_data	Data for verification	main

5.6 Functions

Table 5.8 lists the Functions (main.c).

Table 5.8 Functions (main.c)

Function Name	Outline
main	Main processing
port_init	Port initialization
peripheral_init	Peripheral function initialization
R_INIT_StopModule	Stop processing for active peripheral functions after a reset
R_INIT_NonExistentPort	Nonexistent port initialization
R_INIT_Clock	Clock initialization
sram_verify_err	SRAM verification error processing
Excep_BSC_BUSERR	Bus error interrupt handling

5.7 Function Specifications

The following tables list the sample code function specifications.

main	
Outline	Main processing
Header	None
Declaration	void main(void)
Description	After the initial setting has been done, configures the external bus, and writes to and reads from the SRAM.
Arguments	None
Return Value	None

port_init	
Outline	Port initialization
Header	None
Declaration	void port_init(void)
Description	Initializes ports.
Arguments	None
Return Value	None

peripheral_init	
Outline	Peripheral function initialization
Header	None
Declaration	void peripheral_init(void)
Description	Configures the external bus and enters on-chip ROM enabled expansion mode.
Arguments	None
Return Value	None

R_INIT_StopModule	
Outline	Stop processing for active peripheral functions after a reset
Header	r_init_stop_module.h
Declaration	void R_INIT_StopModule(void)
Description	Configures the setting to enter the module-stop state.
Arguments	None
Return Value	None
Remarks	Transition to the module-stop state is not performed in the sample code. Refer to the RX63N Group, RX631 Group Initial Setting Rev. 1.10 application note for details on this function.

R_INIT_NonExistentPort	
Outline	Nonexistent port initialization
Header	r_init_non_existent_port.h
Declaration	void R_INIT_NonExistentPort(void)
Description	Initializes port direction registers for ports that do not exist in products with less than 176 pins.
Arguments	None
Return Value	None
Remarks	The number of pins in the sample code is set for the 176-pin package (PIN_SIZE=176). After this function is called, when writing in byte units to the PDR registers or PODR registers which have nonexistent ports, set the corresponding bits for nonexistent ports as follows: set the I/O select bits in the PDR registers to 1 and set the output data store bits in the PODR registers to 0. Refer to the RX63N Group, RX631 Group Initial Setting Rev. 1.10 application note for details on this function.

R_INIT_Clock	
Outline	Clock initialization
Header	r_init_clock.h
Declaration	void R_INIT_Clock(void)
Description	Initializes the clock.
Arguments	None
Return Value	None
Remarks	The sample code selects processing which uses PLL as the system clock without using the sub-clock. Refer to the RX63N Group, RX631 Group Initial Setting Rev. 1.10 application note for details on this function.

sram_verify_err	
Outline	SRAM verification error processing
Header	None
Declaration	static void sram_verify_err(void)
Description	When an SRAM verification error occurs, turns on LED1 and performs loop processing.
Arguments	None
Return Value	None

Excep_BSC_BUSERR	
Outline	Bus error interrupt handling
Header	None
Declaration	static void Excep_BSC_BUSERR(void)
Description	Performs the bus error interrupt handling. When a bus error occurs, turns on LED2 and performs loop processing.
Arguments	None
Return Value	None

5.8 Flowcharts

5.8.1 Main Processing

Figure 5.4 shows the Main Processing.

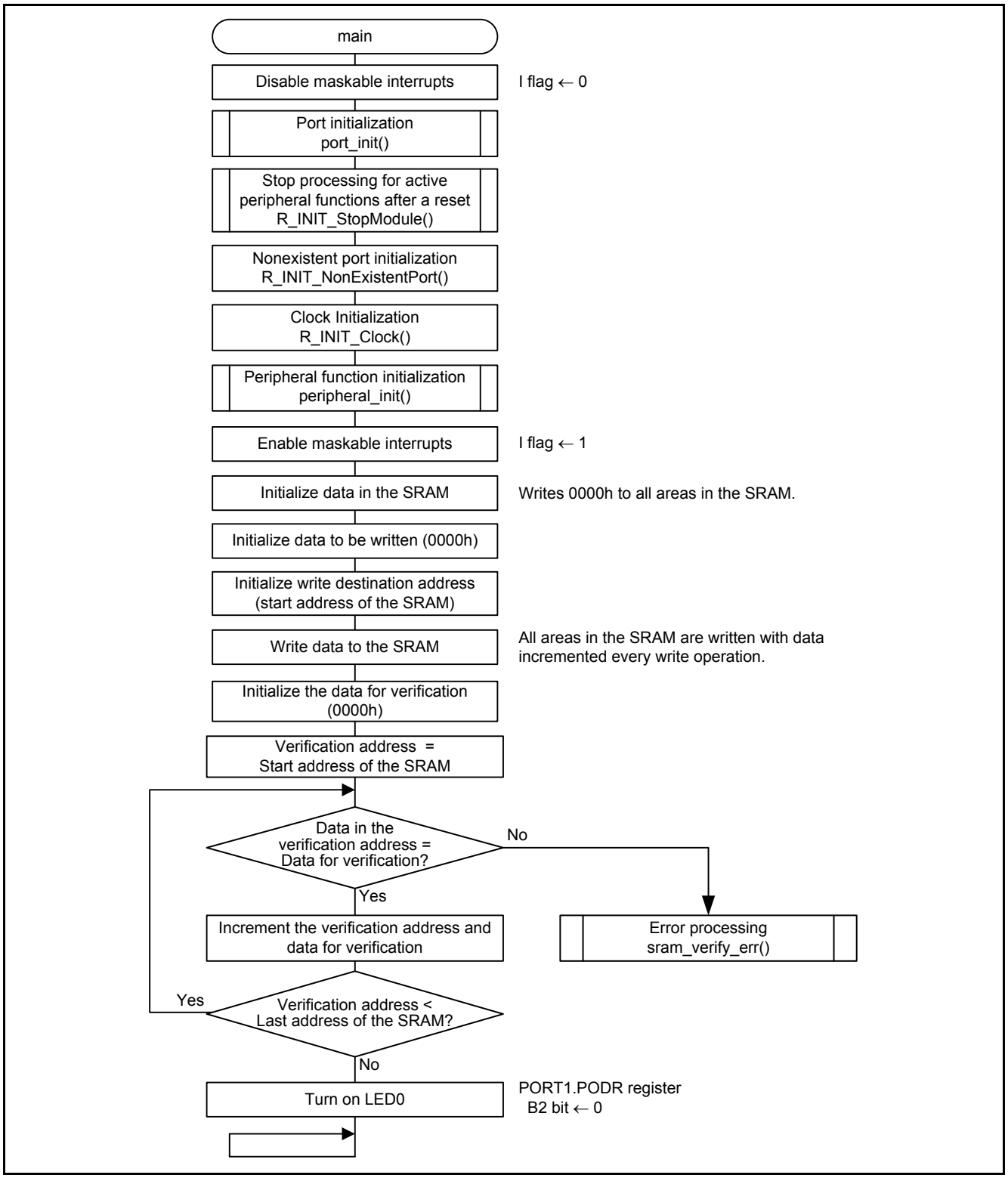

Figure 5.4 Main Processing

5.8.2 Port Initialization

Figure 5.5 shows the Port Initialization.

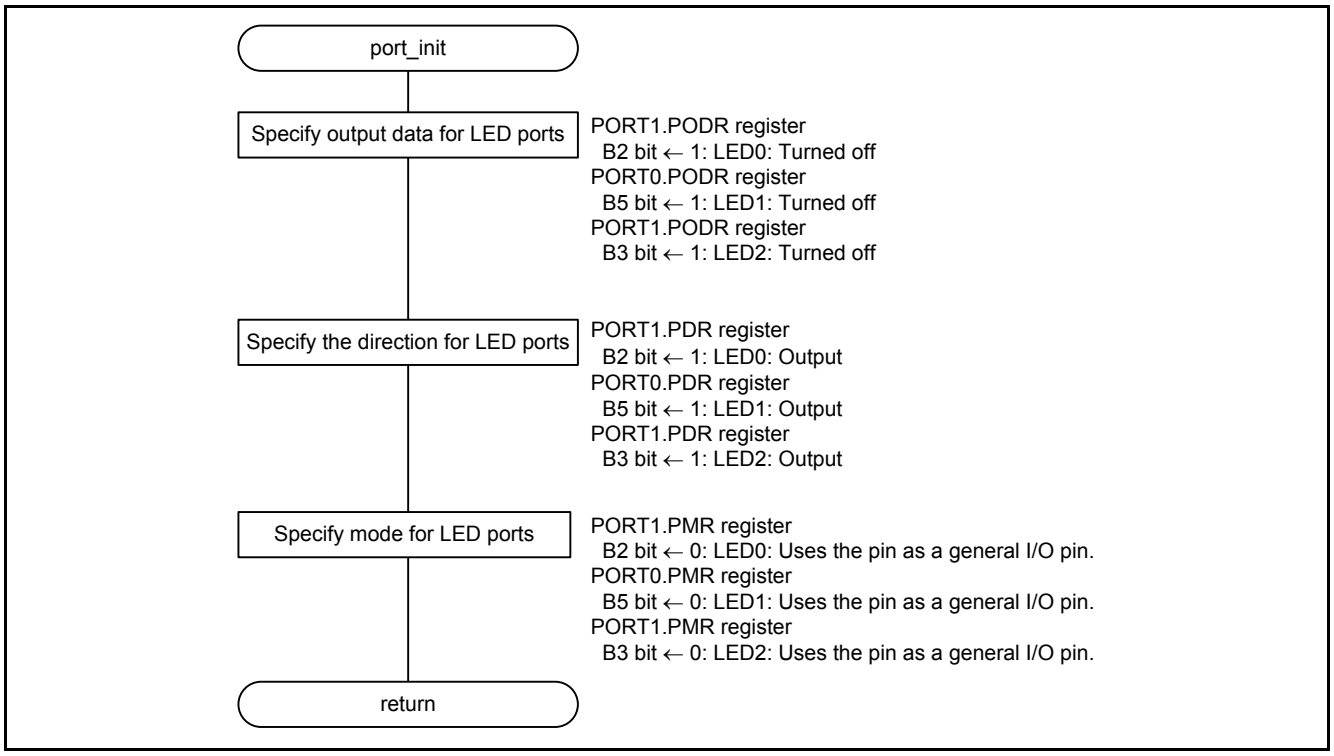

Figure 5.5 Port Initialization

5.8.3 Peripheral Function Initialization

Figure 5.6 to Figure 5.8 show the Peripheral Function Initialization.

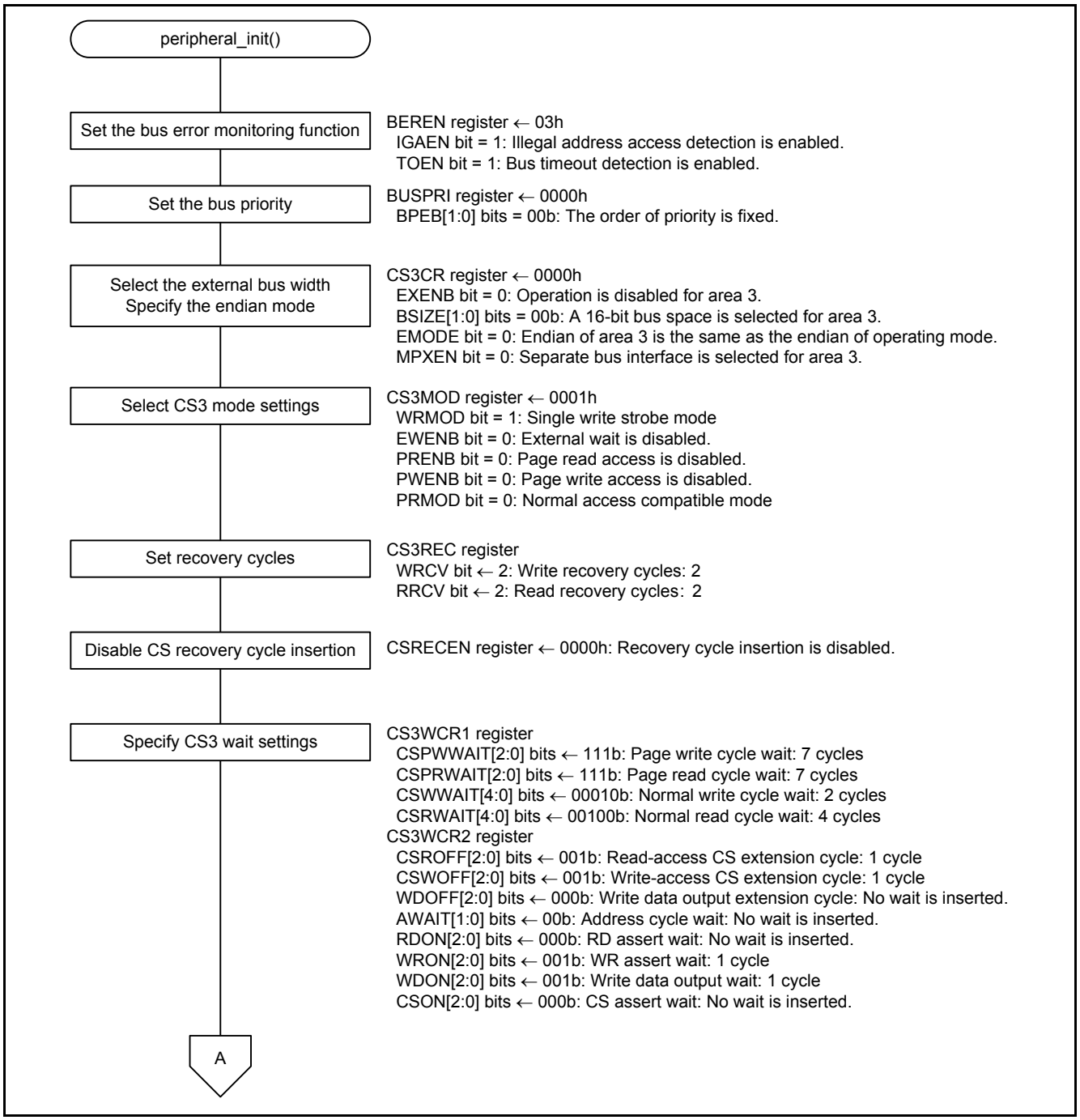

Figure 5.6 Peripheral Function Initialization (1/3)

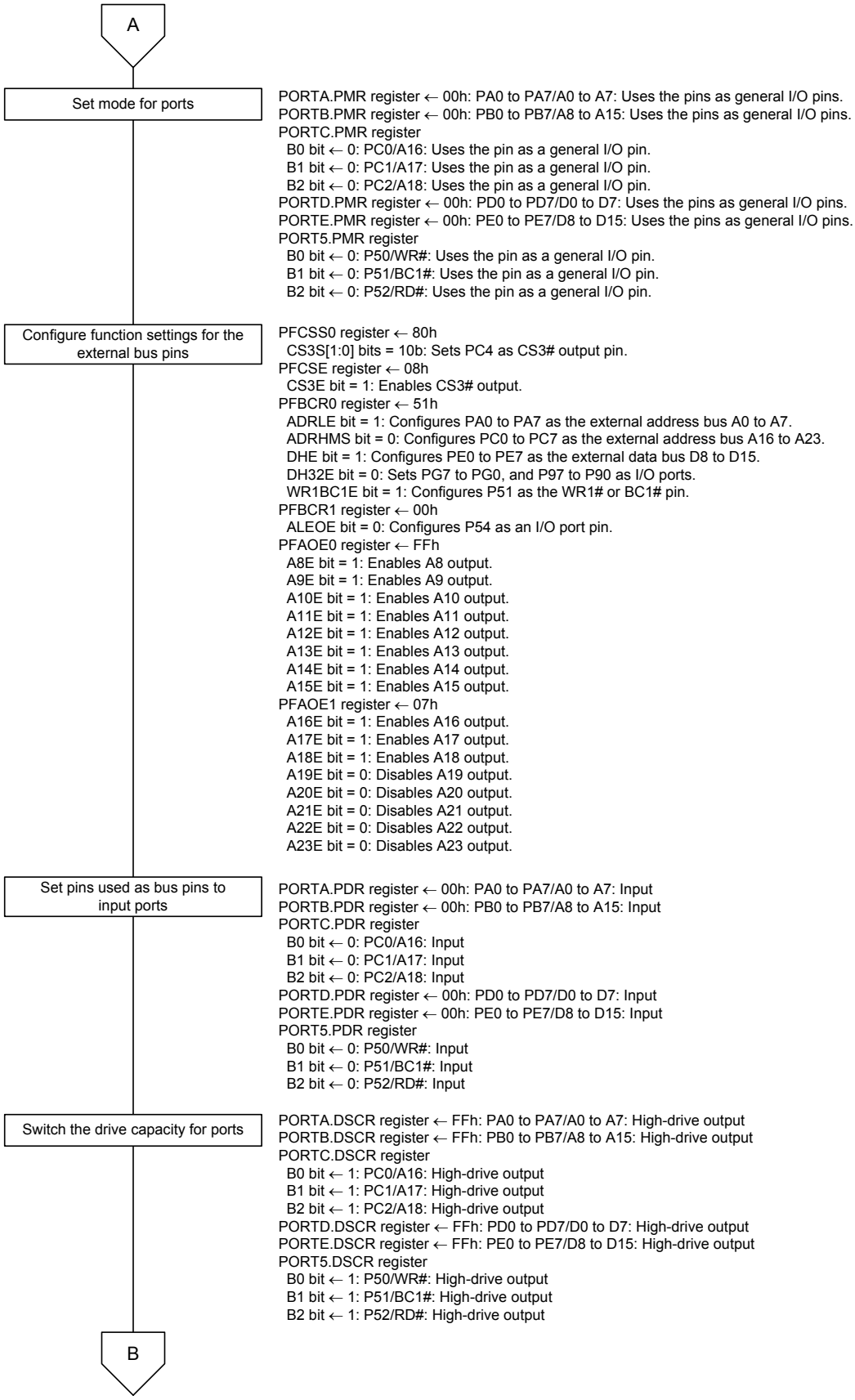

Figure 5.7 Peripheral Function Initialization (2/3)

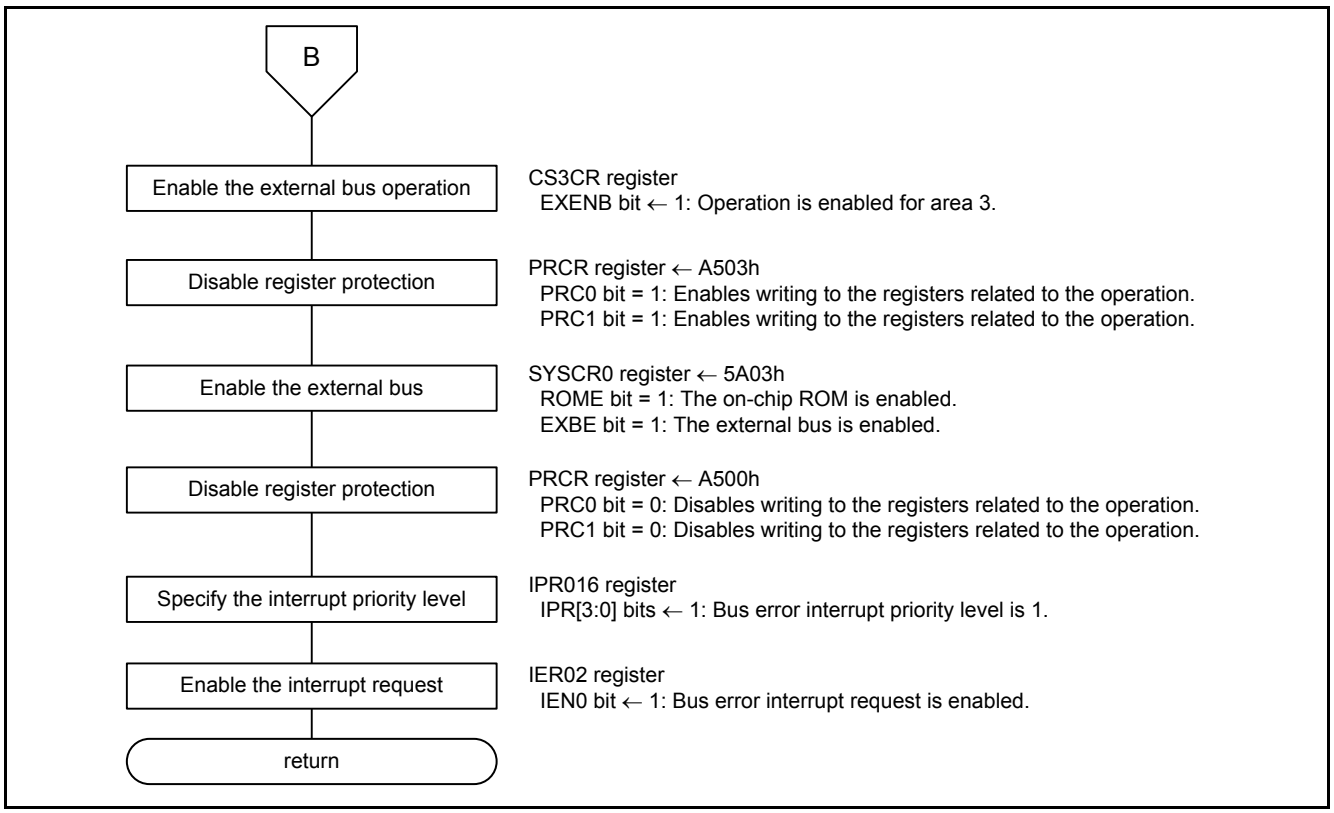

Figure 5.8 Peripheral Function Initialization (3/3)

5.8.4 SRAM Verification Error Processing

Figure 5.9 shows the SRAM Verification Error Processing.

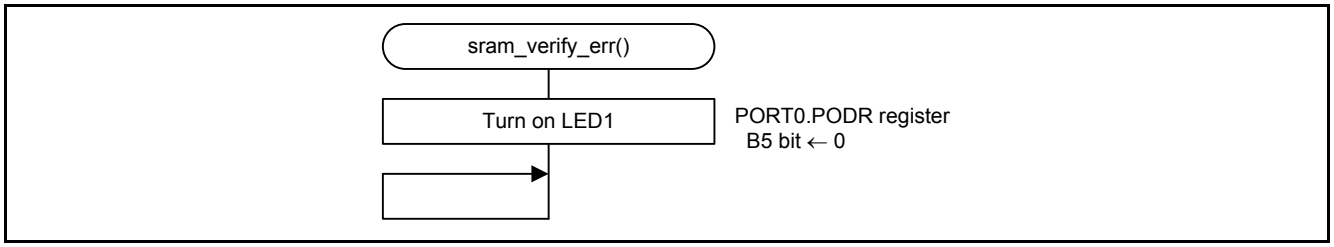

Figure 5.9 SRAM Verification Error Processing

5.8.5 Bus Error Interrupt Handling

Figure 5.10 shows the Bus Error Interrupt Handling.

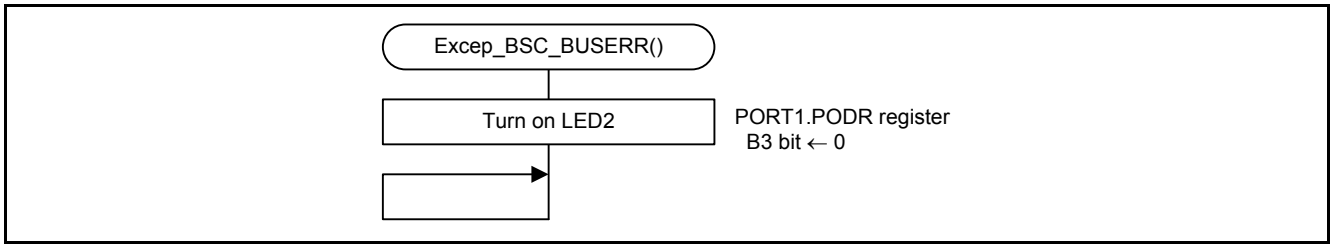

Figure 5.10 Bus Error Interrupt Handling

6. Application Example

6.1 Inserting the Recovery Cycle

The external bus may not be accessed continuously due to the influence of the circuit connected to the SRAM. In this case, inserting the recovery cycle allows the external bus to be accessed continuously.

Cycles to be inserted as the recovery cycle can be specified for each set of read/write operations. Refer to the section “Insertion of Recovery Cycles” of “Buses” in the User’s Manual: Hardware for details.

Figure 6.1 shows the Operation Example of the Recovery Cycle with Separate Bus Interface.

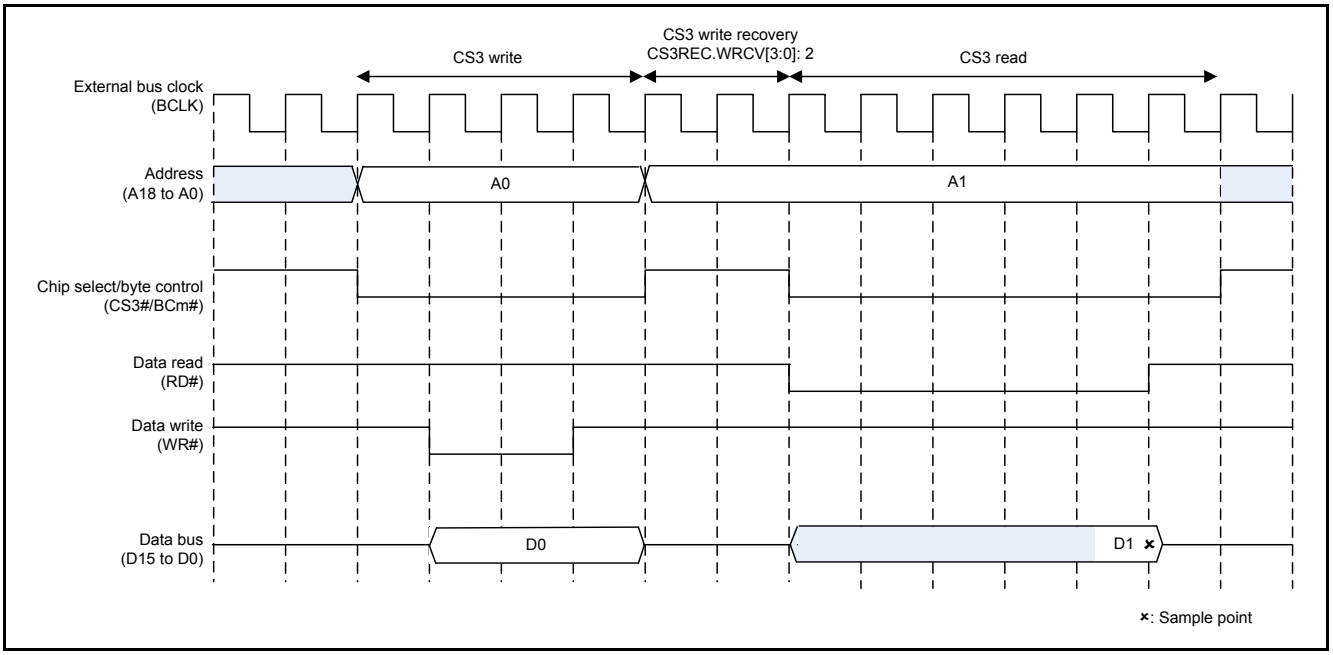

Figure 6.1 Operation Example of the Recovery Cycle with Separate Bus Interface (m = 0 and 1)

6.2 Other Connection Examples

Figure 6.2 shows a Connection Example with 8-Bit Separate Bus and Figure 6.3 shows a Connection Example with 32-Bit Separate Bus for your reference.

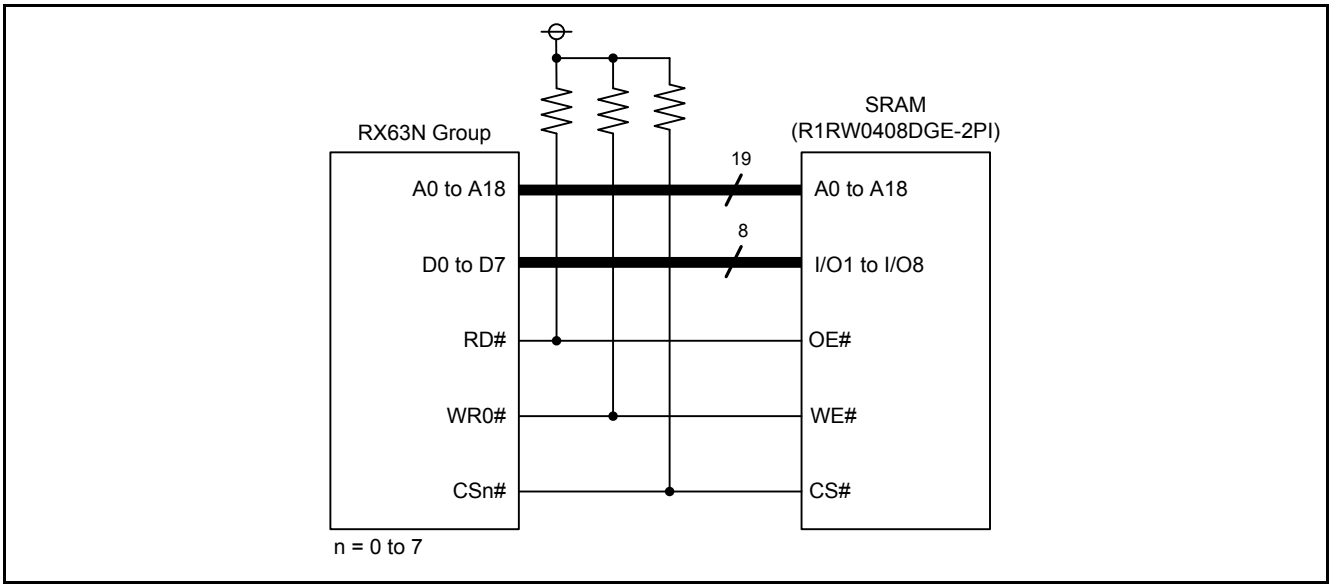

Figure 6.2 Connection Example with 8-Bit Separate Bus

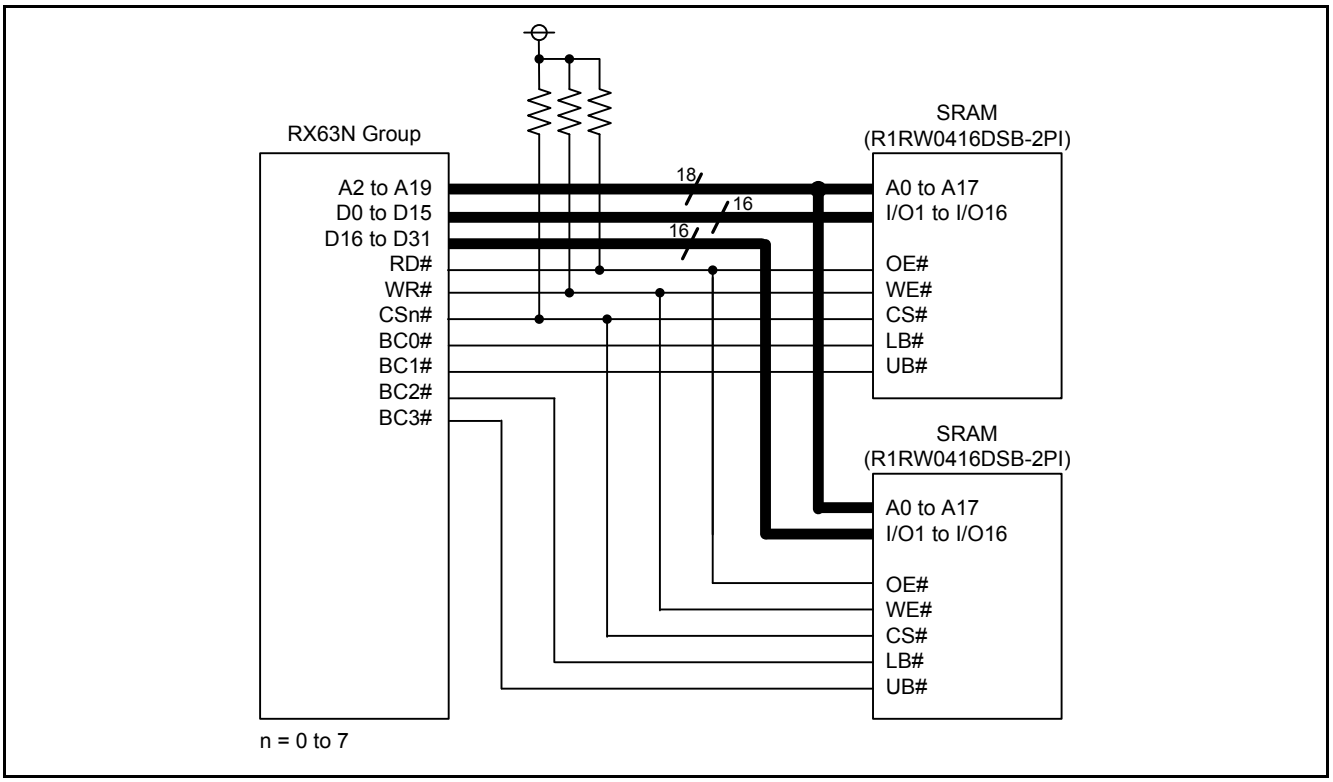

Figure 6.3 Connection Example with 32-Bit Separate Bus

7. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

8. Reference Documents

User's Manual: Hardware

RX63N Group, RX631 Group User's Manual: Hardware Rev.1.70 (R01UH0041EJ)
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

User's Manual: Development Tools

RX Family C/C++ Compiler Package V.1.01 User's Manual Rev.1.00 (R20UT0570EJ)
The latest version can be downloaded from the Renesas Electronics website.

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REVISION HISTORY	RX63N Group, RX631 Group Application Note Example of Using the External Bus (Separate Bus)

Rev.	Date	Description	
		Page	Summary
1.00	July 1, 2014	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Ku, Seoul, 135-920, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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