RX630 Group, RX210 Group

Comparing the RX630 and RX210 Groups (LQFP100)

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Abstract

This application note is a reference document that compares the 100-pin packages for the RX630 and RX210 Groups.

Throughout this document, items in red indicate differences between the two groups.

Products

RX630 Group, RX210 Group

Contents

1. Comparison of Functions

Table 1.1 lists the Comparison of Functions between the RX630 Group and RX210 Group. Refer to 4. Detailed Comparison and 5. Reference Documents for details on individual functions.

Table 1.1 Comparison of Functions

Function	RX630	RX210
Voltage detection circuit (LVDA in the RX630 Group and LVDAa in the RX210 Group)	△	△
Clock generation circuit	✓	✓
Frequency measurement circuit (MCK)	✓	×
Clock frequency accuracy measurement circuit (CAC)	×	✓
Low power consumption	✓	✓
Battery backup function	✓	×
Register write protection function	✓	✓
Interrupt controller (ICUb)	✓	✓
Buses	✓	✓
Memory-protection unit (MPU)	✓	×
DMA controller (DMACA)	✓	✓
Data transfer controller (DTCa)	✓	✓
Event link controller (ELC)	×	✓
Multi-function pin controller (MPC)	✓	✓
Multi-function timer pulse unit 2 (MTU2a)	✓	✓
Port output enable 2 (POE2a)	✓	✓
16-bit timer pulse unit (TPUa)	✓	× (1)
Programmable pulse generator (PPG)	✓	×
8-bit timer (TMR)	✓	✓
Compare match timer (CMT)	✓	✓
Realtime clock (RTCa in the RX630 Group and RTCb in the RX210 Group)	△	△
Watchdog timer (WDTA)	✓	✓
Independent watchdog timer (IWDTa)	✓	✓
USB 2.0 function module (USBa)	✓	×
Serial communications interface (SCIc, SCId)	✓	✓
I2C bus interface (RIIC)	✓	✓
CAN module (CAN)	✓	×
Serial peripheral interface (RSPI)	✓	✓
IEBus controller (IEB)	✓	×
CRC calculator (CRC)	✓	✓
12-bit A/D converter (S12ADa in the RX630 Group and S12ADb in the RX210 Group)	△	△
10-bit A/D converter (ADb)	✓	×
Temperature sensor	△	△
D/A converter (DAa in the RX630 Group and DA in the RX210 Group)	△	△
Comparator A (CMPA)	×	✓
Comparator B (CMPB)	×	✓
Data operation circuit (DOC)	×	✓
On-chip debugging system	✓	✓

✓: Incorporated; ×: Not incorporated; △: Difference in version

Note 1: Incorporated in products with 144-pins or more.

2. Overview Comparison

Table 2.1 to Table 2.4 list the differences in the functions.

Table 2.1 Function Differences (1/4)

Item		RX630	RX210
CPU	Maximum operating frequency	100 MHz	50 MHz
Memory	ROM capacity	384 KB, 512 KB, 768 KB, 1 MB, 1.5 MB, 2 MB	64 KB, 96 KB, 128 KB, 256 KB, 384 KB, 512 KB, 768 KB, 1 MB
	RAM capacity	64KB, 96KB, 128 KB	12 KB, 16 KB, 20 KB, 32 KB, 64 KB, 96 KB
MCU operating modes		• Single-chip mode • On-chip ROM enabled extended mode • On-chip ROM disabled extended mode (software switching)	• Single-chip mode • On-chip ROM enabled expansion mode • On-chip ROM disabled expansion mode (software switching)
Clock generation circuit		• Main clock oscillator • Sub-clock oscillator • Low-speed on-chip oscillator • High-speed on-chip oscillator • IWDT-dedicated on-chip oscillator • PLL frequency synthesizer	• Main clock oscillator • Sub-clock oscillator • Low-speed on-chip oscillator • High-speed on-chip oscillator • IWDT-dedicated on-chip oscillator • PLL frequency synthesizer
System clock (ICLK)		100 MHz (max)	50 MHz (max)
Peripheral module clock B (PCLKB)		50 MHz (max)	32 MHz (max)
Peripheral module clock D (PCLKD)		—	50 MHz (max)
External bus clock (BCLK)		50 MHz (max)	25 MHz (max)
Flash interface clock (FCLK)		50 MHz (max)	32 MHz (max)
Resets		• RES# pin reset • Power-on reset • Voltage-monitoring reset • Watchdog timer reset • Independent watchdog timer reset • Software reset • Deep software standby reset	• RES# pin reset • Power-on reset • Voltage-monitoring reset • Watchdog timer reset • Independent watchdog timer reset • Software reset • Deep software standby reset
Low power consumption		• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode
Operating power control modes		• High-speed operating mode • Low-speed operating mode 1 • Low-speed operating mode 2	• High-speed operating mode • Low-speed operating mode 1 • Low-speed operating mode 2 • Middle-speed operating mode 1A • Middle-speed operating mode 1B • Middle-speed operating mode 2A (1) • Middle-speed operating mode 2B (1)
Interrupt vectors		Peripheral function interrupts: 180 sources	Interrupt vectors: 167

Note 1: These operating modes are only available in the RX210 Group, chip version B.

Table 2.2 Function Differences (2/4)

Item	RX630	RX210
Non-maskable interrupts	• NMI pin interrupt • Oscillation stop detection interrupt • Voltage-monitoring 1 interrupt • Voltage-monitoring 2 interrupt • IWDT underflow/refresh error interrupt • WDT underflow/refresh error interrupt	• NMI pin interrupt • Oscillation stop detection interrupt • Voltage-monitoring 1 interrupt • Voltage-monitoring 2 interrupt • IWDT underflow/refresh error interrupt • WDT underflow/refresh error interrupt
External bus extension	• External address spaces: 8 (CS0 to CS7) • Capacity of each area: 16 MB (CS0 to CS7) • Bus space: 8-/16-bit bus (1) • Each area is selectable as little endian or big endian (only for data) • Bus formats: Separate bus, multiplex bus • Wait control available • Write buffer facility	• External address spaces: 4 (CS0 to CS3) • Capacity of each area: 16 MB (CS0 to CS3) • Bus space: 8-/16-bit bus • Each area is selectable as little endian or big endian (only for data) • Bus formats: Separate bus, multiplex bus • Wait control available • Write buffer facility
General I/O ports	• Open-drain outputs: 78 • 5-V tolerance: 44	• Open-drain outputs: 54 • 5-V tolerance: 4
TPUa	• 6 channels (2) • Maximum of 16 pulse-input/output possible • Input capture/output compare function • PWM mode (up to 15 phases) • Buffered operation, phase-counting mode (two phase encoder input), cascade-connected operation (32 bits × 2 channels) • PPG output trigger can be generated • Capable of generating conversion start triggers for the A/D converters • Clock frequency measuring method	— (3)

Note 1: The bus width differs according to the number of pins.
Note 2: The number of channels differs according to the number of pins.
Note 3: Products with 144 pins or more incorporate the TPU.

Table 2.3 Function Differences (3/4)

Item	RX630	RX210
MTU2a	• 6 channels × 1 unit • Time bases for the six 16-bit timer channels can be provided via up to 16 pulse-input/output lines and three pulse-input lines • Counter-input clock signals: PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD (channel 5 only has four signals available) • Input capture function • 21 output compare/input capture registers • Complementary PWM output mode • Reset synchronous PWM mode • Phase-counting mode • Generation of triggers for A/D converter conversion • PPG output trigger can be generated • Clock frequency measuring function	• 6 channels × 1 unit • Time bases for the six 16-bit timer channels can be provided via up to 16 pulse-input/output lines and three pulse-input lines • Counter-input clock signals: PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD (channel 5 only has four signals available) • Input capture function • 21 output compare/input capture registers • Complementary PWM output mode • Reset synchronous PWM mode • Phase counting mode • Generation of triggers for A/D converter conversion
TMR	• 2 channels × 2 units • Internal clock signals: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192; one external clock signal • Capable of outputting pulse trains with desired duty cycles • Two channels of each unit can be cascaded to create a 16-bit timer • Generation of triggers for A/D converter conversion • Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12	• 2 channels × 2 units • Internal clock signals: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192; one external clock signal • Capable of outputting pulse trains with desired duty cycles • Two channels of each unit can be cascaded to create a 16-bit timer • Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12
WDTA	14 bits × 1 channel	14 bits × 1 channel
RTC	• Clock sources: Main clock, sub-clock • Battery backup operation	• Clock sources: Sub-clock
SCIc, SCId	9 channels (1)	7 channels (1)

Note 1: The number of channels differs according to the number of pins.

Table 2.4 Function Differences (4/4)

Item		RX630	RX210
RIIC		2 channels (1)	1 channel (1)
RSPI		2 channels (1)	1 channel (1)
S12AD	Channels	14 channels (1)	16 channels (1)
	Operating modes	• Single scan mode • Continuous scan mode	• Single scan mode • Continuous scan mode • Group scan mode • Double trigger mode
	Self-diagnosis	—	Incorporated
	Assistance in detecting disconnected analog inputs	—	Incorporated
	A/D conversion start conditions	Software trigger, external trigger, trigger from a timer (MTU, TPU, or TMR)	Software trigger, external trigger, trigger from a timer (MTU, TPU (2)), ELC, TEMPS
	Channel-dedicated sample-and-hold function	—	Incorporated (channels AN000, AN001, and AN002)
TEMPS		Incorporated	Incorporated
DA	Channels	1 channel	2 channels
	Resolution	10 bits	10 bits
	Output voltage	0 V to VREFH	0 V to VREFH
Power supply voltages and operating frequencies		VCC = 2.7 to 3.6 V at 100 MHz	VCC = 1.62 to 1.8 V at 20 MHz VCC = 1.8 to 2.7 V at 32 MHz VCC = 2.7 to 5.5 V at 50 MHz
On-chip debugging system		• E1 emulator (JTAG and FINE interfaces) • E20 emulator (JTAG and FINE interfaces)	• E1 emulator (FINE interface) • E20 emulator (FINE interface)

Note 1: The number of channels differs according to the number of pins.
Note 2: Only incorporated in products with 144 pins or more.

3. Comparison of Pin Functions

Table 3.1 and Table 3.2 list the differences in pin functions.

Table 3.1 Differences in Pin Functions (1/2)

Port	RX630	RX210
P03	—	DA0
P05	IRQ13, DA1	DA1
P07	IRQ15, ADTRG0#	ADTRG0#
P12	TMCI1, RXD2, SMISO2, SSCL2, SCL0[FM+], IRQ2	TMCI1, SCL, IRQ2
P13	MTIOC0B, TIOCA5, TMO3, PO13, TXD2, SMOSI2, SSDA2, SDA0[FM+], IRQ3, ADTRG#	MTIOC0B, TMO3, SDA, IRQ3
P14	MTIOC3A, MTCLKA, TIOCB5, TCLKA, TMRI2, PO15, CTS1#, RTS1#, SS1#, CTX1, USB0_DPUPE, IRQ4	MTIOC3A, MTCLKA, TMRI2, CTS1#, RTS1#, SS1#, IRQ4
P15	MTIOC0B, MTCLKB, TIOCB2, TCLKB, TMCI2, PO13, RXD1, SCK3, SMISO1, SSCL1, CRX1-DS, IRQ5	MTIOC0B, MTCLKB, TMCI2, RXD1, SMISO1, SSCL1, IRQ5
P16	MTIOC3C, MTIOC3D, TIOCB1, TCLKC, TMO2, PO14, RTCOUT, TXD1, RXD3, SMOSI1, SMISO3, SSDA1, SSCL3, MOSIA, SCL2-DS, IERXD, USB0_VBUS, IRQ6, ADTRG0#	MTIOC3C, MTIOC3D, TXD1, SMOSI1, IRQ6, RTCOUT, TMO2, SSDA1, MOSIA, ADTRG0#, SCL-DS
P17	MTIOC3A, MTIOC3B, TIOCB0, TCLKD, TMO1, PO15, POE8#, SCK1, TXD3, SMOSI3, SSDA3, MISOA, SDA2-DS, IETXD, IRQ7, ADTRG#	MTIOC3A, MTIOC3B, TMO1, POE8#, SCK1, MISOA, SDA-DS, IRQ7
P20	MTIOC1A, TIOCB3, TMRI0, PO0, TXD0, SMOSI0, SSDA0, IRQ8	MTIOC1A, TMRI0, TXD0, SMOSI0, SSDA0
P21	MTIOC1B, TIOCA3, TMCI0, PO1, RXD0, SMISO0, SSCL0, IRQ9	MTIOC1B, TMCI0, RXD0, SMISO0, SSCL0
P22	MTIOC3B, MTCLKC, TIOCC3, TMO0, PO2, SCK0	MTIOC3B, MTCLKC, TMO0, SCK0
P23	MTIOC3D, MTCLKD, TIOCD3, PO3, TXD3, CTS0#, RTS0#, SMOSI3, SS0#, SSDA3	MTIOC3D, MTCLKD, CTS0#, RTS0#, SS0#
P24	CS4#, MTIOC4A, MTCLKA, TIOCB4, TMRI1, PO4, SCK3	CS0#, MTIOC4A, MTCLKA, TMRI1
P25	CS5#, MTIOC4C, MTCLKB, TIOCA4, PO5, RXD3, SMISO3, SSCL3, ADTRG0#	CS1#, MTIOC4C, MTCLKB, ADTRG0#
P26	TDO, CS6#, MTIOC2A, TMO1, PO6, TXD1, CTS3#, RTS3#, SMOSI1, SS3#, SSDA1, MOSIB	CS2#, MTIOC2A, TMO1, TXD1, SMOSI1, SSDA1
P27	TCK, FINEC, CS7#, MTIOC2B, TMCI3, PO7, SCK1, RSPCKB	CS3#, MTIOC2B, TMCI3, SCK1, FINEC
P30	TDI, MTIOC4B, TMRI3, PO8, RTCIC0, POE8#, RXD1, SMISO1, SSCL1, MISOB, IRQ0-DS	MTIOC4B, TMRI3, POE8#, RXD1, SMISO1, SSCL1, IRQ0-DS, RTCIC0
P31	TMS, MTIOC4D, TMCI2, PO9, RTCIC1, CTS1#, RTS1#, SS1#, SSLB0, IRQ1-DS	MTIOC4D, TMCI2, CTS1#, RTS1#, SS1#, IRQ1-DS, RTCIC1
P32	MTIOC0C, TIOCC0, TMO3, PO10, RTCOUT, RTCIC2, TXD6, TXD0, SMOSI6, SMOSI0, SSDA6, SSDA0, CTX0, IRQ2-DS	MTIOC0C, TMO3, TXD6, SMOSI6, SSDA6, IRQ2-DS, RTCOUT, RTCIC2
P33	MTIOC0D, TIOCD0, TMRI3, PO11, POE3#, RXD6, RXD0, SMISO6, SMISO0, SSCL6, SSCL0, CRX0, IRQ3-DS	MTIOC0D, TMRI3, POE3#, RXD6, SMISO6, SSCL6, IRQ3-DS
P34	TRST#, MTIOC0A, TMCI3, PO12, POE2#, SCK6, SCK0, IRQ4	MTIOC0A, TMCI3, POE2#, SCK6, IRQ4
P35	NMI	NMI
P36	EXTAL	EXTAL
P37	XTAL	XTAL
P40	IRQ8-DS, AN000	AN000
P41	IRQ9-DS, AN001	AN001
P42	IRQ10-DS, AN002	AN002
P43	IRQ11-DS, AN003	AN003
P44	IRQ12-DS, AN004	AN004
P45	IRQ13-DS, AN005	AN005
P46	IRQ14-DS, AN006	AN006
P47	IRQ15-DS, AN007	AN007
P50	WR0#, WR#, TXD2, SMOSI2, SSDA2, SSLB1	WR0#, WR#
P51	WR1#, BC1#, WAIT#, SCK2, SSLB2	WR1#, BC1#, WAIT#
P52	RD#, RXD2, SMISO2, SSCL2, SSLB3	RD#
P53	BCLK	BCLK
P54	ALE, MTIOC4B, TMCI1, CTS2#, RTS2#, SS2#, CTX1	ALE, MTIOC4B, TMCI1
P55	WAIT#, MTIOC4D, TMO3, CRX1, IRQ10	WAIT#, MTIOC4D, TMO3
PA0	A0, BC0#, MTIOC4A, TIOCA0, PO16, SSLA1	A0, BC0#, MTIOC4A, SSLA1, CACREF
PA1	A1, MTIOC0B, MTCLKC, TIOCB0, PO17, SCK5, SSLA2, IRQ11	A1, MTIOC0B, MTCLKC, SCK5, SSLA2, CVREFA
PA2	A2, PO18, RXD5, SMISO5, SSCL5, SSLA3	A2, RXD5, SMISO5, SSCL5, SSLA3
PA3	A3, MTIOC0D, MTCLKD, TIOCD0, TCLKB, PO19, RXD5, SMISO5, SSCL5, IRQ6-DS	A3, MTIOC0D, MTCLKD, RXD5, SMISO5, SSCL5, IRQ6-DS, CMPB1
PA4	A4, MTIC5U, MTCLKA, TIOCA1, TMRI0, PO20, TXD5, SMOSI5, SSDA5, SSLA0, IRQ5-DS	A4, MTIC5U, MTCLKA, TMRI0, TXD5, SMOSI5, SSDA5, SSLA0, IRQ5-DS, CVREFB1

Table 3.2 Differences in Pin Functions (2/2)

Port	RX630	RX210
PA5	A5, TIOCB1, PO21, RSPCKA	A5, RSPCKA
PA6	A6, MTIC5V, MTCLKB, TIOCA2, TMCI3, PO22, POE2#, CTS5#, RTS5#, SS5#, MOSIA	A6, MTIC5V, MTCLKB, TMCI3, POE2#, CTS5#, RTS5#, SS5#, MOSIA
PA7	A7, TIOCB2, PO23, MISOA	A7, MISOA
PB0	A8, MTIC5W, TIOCA3, PO24, RXD6, SMISO6, SSCL6, RSPCKA, IRQ12	A8, MTIC5W, RXD6, SMISO6, SSCL6, RSPCKA
PB1	A9, MTIOC0C, MTIOC4C, TIOCB3, TMCI0, PO25, TXD6, SMOSI6, SSDA6, IRQ4-DS	A9, MTIOC0C, MTIOC4C, TMCI0, TXD6, SMOSI6, SSDA6, IRQ4-DS
PB2	A10, TIOCC3, TCLKC, PO26, CTS6#, RTS6#, SS6#	A10, CTS6#, RTS6#, SS6#
PB3	A11, MTIOC0A, MTIOC4A, TIOCD3, TCLKD, TMO0, PO27, POE3#, SCK6	A11, MTIOC0A, MTIOC4A, TMO0, POE3#, SCK6
PB4	A12, TIOCA4, PO28, CTS9#, RTS9#, SS9#	A12, CTS9#, RTS9#, SS9#
PB5	A13, MTIOC2A, MTIOC1B, TIOCB4, TMRI1, PO29, POE1#, SCK9	A13, MTIOC2A, MTIOC1B, TMRI1, POE1#, SCK9
PB6	A14, MTIOC3D, TIOCA5, PO30, RXD9, SMISO9, SSCL9	A14, MTIOC3D, RXD9, SMISO9, SSCL9
PB7	A15, MTIOC3B, TIOCB5, PO31, TXD9, SMOSI9, SSDA9	A15, MTIOC3B, TXD9, SMOSI9, SSDA9
PC0	A16, MTIOC3C, TCLKC, PO17, CTS5#, RTS5#, SS5#, SSLA1, IRQ14	A16, MTIOC3C, CTS5#, RTS5#, SS5#, SSLA1
PC1	A17, MTIOC3A, TCLKD, PO18, SCK5, SSLA2, IRQ12	A17, MTIOC3A, SCK5, SSLA2
PC2	A18, MTIOC4B, TCLKA, PO21, RXD5, SMISO5, SSCL5, SSLA3, IERXD	A18, MTIOC4B, RXD5, SMISO5, SSCL5, SSLA3
PC3	A19, MTIOC4D, TCLKB, PO24, TXD5, SMOSI5, SSDA5, IETXD	A19, MTIOC4D, TXD5, SMOSI5, SSDA5
PC4	A20, CS3#, MTIOC3D, MTCLKC, TMCI1, PO25, POE0#, SCK5, CTS8#, RTS8#, SS8#, SSLA0	A20, CS3#, MTIOC3D, MTCLKC, TMCI1, POE0#, SCK5, CTS8#, RTS8#, SS8#, SSLA0
PC5	A21, CS2#, WAIT#, MTIOC3B, MTCLKD, TMRI2, PO29, SCK8, RSPCKA	A21, CS2#, WAIT#, MTIOC3B, MTCLKD, TMRI2, SCK8, RSPCKA
PC6	A22, CS1#, MTIOC3C, MTCLKA, TMCI2, PO30, RXD8, SMISO8, SSCL8, MOSIA, IRQ13	A22, CS1#, MTIOC3C, MTCLKA, TMCI2, RXD8, SMISO8, SSCL8, MOSIA
PC7	A23, CS0#, MTIOC3A, MTCLKB, TMO2, PO31, TXD8, SMOSI8, SSDA8, MISOA, IRQ14	A23, CS0#, MTIOC3A, TMO2, MTCLKB, TXD8, SMOSI8, SSDA8, MISOA, CACREF
PD0	D0[A0/D0], IRQ0, AN008	D0[A0/D0], IRQ0
PD1	D1[A1/D1], MTIOC4B, CTX0 (1), IRQ1, AN009	D1[A1/D1], MTIOC4B, IRQ1
PD2	D2[A2/D2], MTIOC4D, CRX0 (1), IRQ2, AN010	D2[A2/D2], MTIOC4D, IRQ2
PD3	D3[A3/D3], POE8#, IRQ3, AN011	D3[A3/D3], POE8#, IRQ3
PD4	D4[A4/D4], POE3#, IRQ4, AN012	D4[A4/D4], POE3#, IRQ4
PD5	D5[A5/D5], MTIC5W, POE2#, IRQ5, AN013	D5[A5/D5], MTIC5W, POE2#, IRQ5
PD6	D6[A6/D6], MTIC5V, POE1#, IRQ6, AN6	D6[A6/D6], MTIC5V, POE1#, IRQ6
PD7	D7[A7/D7], MTIC5U, POE0#, IRQ7, AN7	D7[A7/D7], MTIC5U, POE0#, IRQ7
PE0	D8[A8/D8], SCK12, SSLB1, ANEX0	D8[A8/D8], SCK12, AN008
PE1	D9[A9/D9], MTIOC4C, PO18, TXD12, SMOSI12, SSDA12, TXDX12, SIOX12, SSLB2, RSPCKB, ANEX1	D9[A9/D9], MTIOC4C, TXD12, TXDX12, AN009, CMPB0, SIOX12, SMOSI12, SSDA12
PE2	D10[A10/D10], MTIOC4A, PO23, RXD12, SMISO12, SSCL12, RXDX12, SSLB3, MOSIB, IRQ7-DS, AN0	D10[A10/D10], MTIOC4A, RXD12, RXDX12, SMISO12, SSCL12, IRQ7-DS, AN010, CVREFB0
PE3	D11[A11/D11], MTIOC4B, PO26, POE8#, CTS12#, RTS12#, SS12#, MISOB, AN1	D11[A11/D11], MTIOC4B, POE8#, CTS12#, RTS12#, SS12#, AN011, CMPA1
PE4	D12[A12/D12], MTIOC4D, MTIOC1A, PO28, SSLB0, AN2	D12[A12/D12], MTIOC4D, MTIOC1A, AN012, CMPA2
PE5	D13[A13/D13], MTIOC4C, MTIOC2B, RSPCKB, IRQ5, AN3	D13[A13/D13], MTIOC4C, MTIOC2B, IRQ5, AN013
PE6	D14[A14/D14], MOSIB, IRQ6, AN4	D14[A14/D14], IRQ6, AN014
PE7	D15[A15/D15], MISOB, IRQ7, AN5	D15[A15/D15], IRQ7, AN015
PH0	—	CACREF
PH1	—	TMO0, IRQ0
PH2	—	TMRI0, IRQ1
PH3	—	TMCI0
PJ1	—	MTIOC3A
PJ3	MTIOC3C, CTS6#, RTS6#, CTS0#, RTS0#, SS6#, SS0#	MTIOC3C, CTS6#, RTS6#, SS6#

Note 1: Enabled only for the ROM capacity of 768 Kbytes or more.

4. Detailed Comparisons

4.1 Difference in the Operating Modes

Table 4.1 lists the Difference in the Operating Modes.

Table 4.1 Difference in the Operating Modes

RX630	RX210
• Single-chip mode • Boot mode • User boot mode • On-chip ROM enabled extended mode • On-chip ROM disabled extended mode • USB boot mode	• Single-chip mode • Boot mode • User boot mode • On-chip ROM enabled expansion mode • On-chip ROM disabled expansion mode

4.2 Difference in the Option-Setting Memory

Table 4.2 lists the Difference in the I/O Register Associated with the Option-Memory Setting.

Table 4.2 Difference in the I/O Register Associated with the Option-Memory Setting

Register Symbol	Bit Symbol	RX630	RX210
OFS1	VDSEL[1:0]	Reserved	Voltage detection 0 level select

4.3 Differences in the LVDA and LVDAa

Table 4.3 lists the Differences in the LVDA and LVDAa.

Table 4.3 Differences in the LVDA and LVDAa

Item		RX630 (LVDA)	RX210 (LVDAa)
Voltage monitoring 0	Detection voltage	One level fixed	Selectable from four levels
Voltage monitoring 1	Detection voltage	One level fixed	Selectable from 16 levels
	Interrupts	Non-maskable	Non-maskable, maskable
Voltage monitoring 2	Detected events	• Voltage rises or drops past Vdet2	• Voltage rises or drops past Vdet2 • Input voltages to pins VCC and the CMPA2 can be switched using the LVCMPCR.EXVCCINP2 bit
	Detection voltage	One level fixed	Selectable from 16 levels
	Interrupts	Non-maskable	Non-maskable, maskable
Event link function		—	Vdet1 or Vdet2 passage detection event output

Table 4.4 lists the Differences in the I/O Registers Associated with LVDA and LVDAa.

Table 4.4 Differences in the I/O Registers Associated with LVDA and LVDAa

Register Symbol	Bit Symbol	RX630	RX210
LVCMPCR	EXVREFINP1	Reserved	Comparator A1 reference voltage external input select
	EXVCCINP1	Reserved	Comparator A1 comparison voltage external input select
	EXVREFINP2	Reserved	Comparator A2 reference voltage external input select
	EXVCCINP2	Reserved	Comparator A2 comparison voltage external input select
LVD1CR1	LVD1IRQSEL	Reserved	Voltage monitoring 1/comparator A1 interrupt type select
LVD2CR1	LVD2IRQSEL	Reserved	Voltage monitoring 2/comparator A2 interrupt type select
LVDLVLR	LVD1LVL[3:0]	Voltage detection 1 level select (standard voltage during drop in voltage) 1010: 2.95 V	Voltage detection 1 level select (standard voltage during drop in voltage) 0000: 4.15 V 0001: 4.00 V 0010: 3.85 V 0011: 3.70 V 0100: 3.55 V 0101: 3.40 V 0110: 3.25 V 0111: 3.10 V 1000: 2.95 V 1001: 2.80 V 1010: 2.65 V 1011: 2.50 V 1100: 2.35 V 1101: 2.20 V 1110: 2.05 V 1111: 1.90 V
	LVD2LVL[3:0]	Voltage detection 2 level select (standard voltage during drop in voltage) 1010: 2.95 V	Voltage detection 2 level select (standard voltage during drop in voltage) (When LVCMPCR.EXVCCINP2 = 0 (VCC select)) 0000: 4.15V 0001: 4.00V 0010: 3.85V 0011: 3.70V 0100: 3.55V 0101: 3.40V 0110: 3.25V 0111: 3.10V 1000: 2.95V 1001: 2.80V 1010: 2.65V 1011: 2.50V 1100: 2.35V 1101: 2.20V 1110: 2.05V 1111: 1.90V When LVCMPCR.EXVCCINP2 = 1 (CMPA2 pin select)) 0001: 1.33 V

4.4 Differences in the Clock Generation Circuit

Table 4.5 lists the Differences in I/O Registers Associated with the Clock Generation Circuit.

Table 4.5 Differences in I/O Registers Associated with the Clock Generation Circuit

Register Symbol	Bit Symbol	RX630	RX210
SCKCR	PCKD[3:0]	Reserved	Peripheral module clock D (PCLKD) select bits
SCKCR2	—	System clock control register 2	—
VRCR	—	—	Voltage regulator control register
PLLCR	PLIDIV[1:0]	PLL input frequency division ratio select bits Set these bits so the frequency of the PLL input signal is within the range of 4 to 16 MHz.	PLL input frequency division ratio select bits Set these bits so the frequency of the PLL input signal is within the range of 4 to 12.5 MHz.
	STC[5:0] (RX630) STC[4:0] (RX210)	Frequency multiplication factor select 000111: ×8 001001: ×10 001011: ×12 001111: ×16 010011: ×20 010111: ×24 011000: ×25 110001: ×50 Set these bits so that the output frequency is within the range of the VCO oscillation frequency for the PLL (104 to 200 MHz)	Frequency multiplication factor select 00111: ×8 01001: ×10 01011: ×12 01111: ×16 10011: ×20 10111: ×24 11000: ×25 Set these bits to the output frequency is within the range of the VCO oscillation frequency for the PLL (50 to 100 MHz)
HOCOCR2	—	—	High-speed on-chip oscillator control register 2
MOFCR	MOFXIN	Main clock oscillator forced oscillation	Reserved
	MODRV[2:0]	Reserved	Main clock oscillator drive capability switch
	MODRV2[1:0]	Reserved	Main clock oscillator drive capability switch 2
	MOSEL	Reserved	Main clock oscillator switch
PLLPCR	—	—	PLL power control register (1)

Note 1: This register is only present in chip version B of the RX210 Group.

Table 4.6 and Table 4.7 list the Differences in the Clock Generation Circuit.

Table 4.6 Differences in the Clock Generation Circuit (1/2)

Item	RX630	RX210
Uses	• Generates the ICLK to be supplied to the CPU, DMAC, DTC, ROM, and RAM. • Generates PCLKB to be supplied to peripheral modules. • Generates FCLK to be supplied to the flash interface. • Generates the BCLK to be supplied to the external bus. • Generates the RTC-dedicated sub clock (RTCSCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the USB clock (UCLK) to be supplied to the USB. • Generates the IEBUS clock (IECLK) to be supplied to the IEBUS. • Generates the RTC-dedicated main clock (RTCMCLK) to be supplied to the RTC. • Generates the JTAG-dedicated clock (JTAGTCK) to be supplied to the JTAG.	• Generates ICLK to be supplied to the CPU, DMAC, DTC, ROM, and RAM. • Generates PCLKB and PCLKD to be supplied to peripheral modules. • Generates FCLK to be supplied to the flash interface. • Generates the BCLK to be supplied to the external bus • Generates the CAC clock (CACCLK) to be supplied to the CAC.
Operating frequencies	• ICLK: 100 MHz (max) • PCLKB: 50 MHz (max) • FCLK: 4 to 50 MHz for programming and erasing the ROM and E2 DataFlash, and 50 MHz (max) for reading the E2 DataFlash • BCLK: 50 MHz (max) • BCLK pin output: 25 MHz (max) • RTCSCLK: 32.768 kHz • IWDTCLK: 125 kHz • UCLK: 48 MHz (max) • CANMCLK: 20 MHz (max) • IECLK: 50 MHz (max) • RTCMCLK: 4 to 16 MHz • JTAGTCK: 10 MHz (max)	• ICLK: 50 MHz (max) • PCLKB: 32 MHz (max) • PCLKD: 50 MHz • FCLK: 4 to 32 MHz for programming and erasing the ROM and E2 DataFlash, and 32 MHz (max) for reading the E2 DataFlash • BCLK: 25 MHz (max) • BCLK pin output: 12.5 MHz (max) • RTCSCLK: 32.768 kHz • IWDTCLK: 125 kHz • CACCLK: Same as frequency of each oscillator

Note 1: Only present in chip version B of the RX210 Group.

Table 4.7 Differences in the Clock Generation Circuit (2/2)

Item	RX630	RX210
Main clock oscillator	• Resonator frequency: 4 to 16 MHz • External clock input frequency: 20 MHz (max) • Connectable resonator or additional circuit: Ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When an oscillation stop is detected with the main clock, the system clock source is switched to LOCO, and MTU output can be forcedly driven to the high-impedance.	• Resonator frequency: 1 to 20 MHz • External clock input frequency: 20 MHz (max) • Connectable resonator or additional circuit: Ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When an oscillation stop is detected with the main clock, the system clock source is switched to LOCO and MTU output can be forcedly driven to the high-impedance.
PLL circuit	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 to 16 MHz • Frequency multiplication ratio: Selectable from 8, 10, 12, 16, 20, 24, 25, and 50 • VCO oscillation frequency: 104 to 200 MHz	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 to 12.5 MHz • Frequency multiplication ratio: Selectable from 8, 10, 12, 16, 20, 24, and 25 • VCO oscillation frequency: 50 to 100 MHz • PLL power control (1)
High-speed on-chip oscillator (HOCO)	• Oscillation frequency: 50 MHz • HOCO power supply control	• Oscillation frequencies: 32, 36.864, 40, and 50 MHz • HOCO power supply control
External clock input (TCK) for JTAG	Input clock frequency: 10 MHz (max)	—

4.5 Differences in Low Power Consumption Functions

Table 4.8 to Table 4.10 list the differences in the low power consumption functions.

Table 4.8 Differences in Low Power Consumption Functions

Item	RX630	RX210
Functions for lower operating power consumption	• High-speed operating mode • Low-speed operating mode 1 • Low-speed operating mode 2	• High-speed operating mode • Low-speed operating mode 1 • Low-speed operating mode 2 • Middle-speed operating mode 2A (1) • Middle-speed operating mode 2B (1) • Middle-speed operating mode 1A • Middle-speed operating mode 1B
Deep software standby mode	RAM0 is stopped (retained/undefined) (2)	ROM0 is stopped (undefined)

Note 1: This mode only exists in chip version B of the RX210 Group.
Note 2: Retained or undefined can be selected by setting the DPSBYCR.DEEPCUT[1:0] bits.

Table 4.9 Differences in the Operating Voltage Range Between 2.7 to 3.6 V When Programming and Erasing the Flash Memory

Operating Power Control Mode	Clock	Operating Frequency Range		
		RX630	RX210 (chip version B)	RX210 (chip version C)
High-speed operating mode	FCLK	4 to 50 MHz	4 to 32 MHz	4 to 32 MHz
Middle-speed operating mode 1A	FCLK	—	4 to 32 MHz	4 to 32 MHz
Middle-speed operating mode 1B	FCLK	—	4 to 32 MHz	4 to 32 MHz
Middle-speed operating mode 2A	FCLK	—	4 to 32 MHz	—
Middle-speed operating mode 2B	FCLK	—	4 to 32 MHz	—
Low-speed operating mode 1	FCLK	—	—	—
Low-speed operating mode 2	FCLK	—	—	—

Table 4.10 Differences in the Operating Voltage Range Between 2.7 to 3.6 V When Reading the Flash Memory

Operating Power Control Mode	Clock	Operating Frequency Range		
		RX630	RX210 (chip version B)	RX210 (chip version C)
High-speed operating mode	ICLK	100 MHz (max)	50 MHz (max)	50 MHz (max)
	FCLK	50 MHz (max)	32 MHz (max)	32 MHz (max)
	PCLKD	—	50 MHz (max)	50 MHz (max)
	PCLKB	50 MHz (max)	32 MHz (max)	32 MHz (max)
	BCLK	50 MHz (max)	25 MHz (max)	25 MHz (max)
Middle-speed operating mode 1A	ICLK	—	32 MHz (max)	32 MHz (max)
	FCLK	—	32 MHz (max)	32 MHz (max)
	PCLKD	—	32 MHz (max)	32 MHz (max)
	PCLKB	—	32 MHz (max)	32 MHz (max)
	BCLK	—	25 MHz (max)	25 MHz (max)
Middle-speed operating mode 1B	ICLK	—	32 MHz (max)	32 MHz (max)
	FCLK	—	32 MHz (max)	32 MHz (max)
	PCLKD	—	32 MHz (max)	32 MHz (max)
	PCLKB	—	32 MHz (max)	32 MHz (max)
	BCLK	—	25 MHz (max)	25 MHz (max)
Middle-speed operating mode 2A	ICLK	—	32 MHz (max)	—
	FCLK	—	32 MHz (max)	—
	PCLKD	—	32 MHz (max)	—
	PCLKB	—	32 MHz (max)	—
	BCLK	—	25 MHz (max)	—
Middle-speed operating mode 2B	ICLK	—	32 MHz (max)	—
	FCLK	—	32 MHz (max)	—
	PCLKD	—	32 MHz (max)	—
	PCLKB	—	32 MHz (max)	—
	BCLK	—	25 MHz (max)	—
Low-speed operating mode 1	ICLK	1 MHz (max)	8 MHz (max)	1 MHz (max)
	FCLK	1 MHz (max)	8 MHz (max)	1 MHz (max)
	PCLKD	—	8 MHz (max)	1 MHz (max)
	PCLKB	1 MHz (max)	8 MHz (max)	1 MHz (max)
	BCLK	1 MHz (max)	8 MHz (max)	1 MHz (max)
Low-speed operating mode 2	ICLK	125 kHz (max)	32.768 kHz (max)	32.768 kHz (max)
	FCLK	125 kHz (max)	32.768 kHz (max)	32.768 kHz (max)
	PCLKD	—	32.768 kHz (max)	32.768 kHz (max)
	PCLKB	125 kHz (max)	32.768 kHz (max)	32.768 kHz (max)
	BCLK	125 kHz (max)	32.768 kHz (max)	32.768 kHz (max)

Table 4.11 to Table 4.13 list the differences in I/O registers associated with the low power consumption functions.

Table 4.11 Differences in I/O Registers Associated with Low Power Consumption Functions (1/3)

Register Symbol	Bit Symbol	RX630	RX210
MSTPCRA	MSTPA10	Programmable pulse generator (unit 1) module stop	Reserved
	MSTPA11	Programmable pulse generator (unit 0) module stop	Reserved
	MSTPA12	16-bit timer pulse unit 1 (unit 1) module stop	Reserved
	MSTPA13	16-bit timer pulse unit 0 (unit 0) module stop	16-bit timer pulse unit module stop (1)
	MSTPA23	10-bit A/D converter module stop	Reserved
MSTPCRB	MSTPB0	CAN module 0 module stop	Reserved
	MSTPB1	CAN module 1 module stop	Reserved
	MSTPB2	CAN module 2 module stop	Reserved
	MSTPB6	Reserved	DOC module stop
	MSTPB9	Reserved	ELC module stop
	MSTPB10	Reserved	Comparator B module stop
	MSTPB16	Serial peripheral interface 1 module stop	Reserved
	MSTPB19	Universal serial bus interface (port 0) module stop	Reserved
	MSTPB20	I^2C bus interface 1 module stop (1)	Reserved
	MSTPB28	Serial communication interface 3 module stop	Serial communication interface 3 module stop (1)
	MSTPB29	Serial communication interface 2 module stop	Serial communication interface 2 module stop (1)
MSTPCRC	MSTPC1	RAM1 module stop	RAM1 module stop
	MSTPC16	I^2C bus interface 3 module stop	Reserved
	MSTPC17	I^2C bus interface 2 module stop	Reserved
	MSTPC18	IEBus module stop	Reserved
	MSTPC19	Frequency measurement circuit module stop	Clock frequency accuracy measurement circuit module stop
	MSTPC22	Serial peripheral interface 2 module stop (1)	Reserved
OPCCR	OPCM[2:0]	Operating power control mode select 000: High-speed operating mode (1) 110: Low-speed operating mode 1 111: Low-speed operating mode 2	Operating power control mode select 000: High-speed operating mode 010: Medium-speed operating mode 1A (2) 011: Medium-speed operating mode 1B 100: Medium-speed operating mode 2A (3) 101: Medium-speed operating mode 2B (3) 110: Low-speed operating mode 1 111: Low-speed operating mode 2

Note 1: This bit cannot be used with packages that have 100 pins or less.
Note 2: Mode after a reset is released.
Note 3: This mode only exists in chip version B of the RX210 Group.

Table 4.12 Differences in I/O Registers Associated with Low Power Consumption Functions (2/3)

Register Symbol	Bit Symbol	RX630	RX210
MOSCWTCR	NSTS[4:0]	Main clock oscillator wait time select 00000: Waiting time = 2 cycles 00001: Waiting time = 4 cycles 00010: Waiting time = 8 cycles 00011: Waiting time = 16 cycles 00100: Waiting time = 32 cycles 00101: Waiting time = 64 cycles 00110: Waiting time = 512 cycles 00111: Waiting time = 1024 cycles 01000: Waiting time = 2048 cycles 01001: Waiting time = 4096 cycles 01010: Waiting time = 16384 cycles 01011: Waiting time = 32768 cycles 01100: Waiting time = 65536 cycles 01101: Waiting time = 131072 cycles 01110: Waiting time = 262144 cycles 01111: Waiting time = 524288 cycles	Main clock oscillator wait time select 00000: Waiting time = 2 cycles 00001: Waiting time = 4 cycles 00010: Waiting time = 8 cycles 00011: Waiting time = 16 cycles 00100: Waiting time = 32 cycles 00101: Waiting time = 256 cycles 00110: Waiting time = 512 cycles 00111: Waiting time = 1024 cycles 01000: Waiting time = 2048 cycles 01001: Waiting time = 4096 cycles 01010: Waiting time = 16384 cycles 01011: Waiting time = 32768 cycles 01100: Waiting time = 65536 cycles 01101: Waiting time = 131072 cycles 01110: Waiting time = 262144 cycles 01111: Waiting time = 524288 cycles
SOSCWTCR	SSTS[4:0]	Sub-clock oscillator wait time select 00000: Waiting time = 2 cycles 00001: Waiting time = 4 cycles 00010: Waiting time = 8 cycles 00011: Waiting time = 16 cycles 00100: Waiting time = 32 cycles 00101: Waiting time = 64 cycles 00110: Waiting time = 512 cycles 00111: Waiting time = 1024 cycles 01000: Waiting time = 2048 cycles 01001: Waiting time = 4096 cycles 01010: Waiting time = 16384 cycles 01011: Waiting time = 32768 cycles 01100: Waiting time = 65536 cycles 01101: Waiting time = 131072 cycles 01110: Waiting time = 262144 cycles 01111: Waiting time = 524288 cycles	Sub-clock oscillator wait time select 00000: Waiting time = 2 s + 2 cycles 00001: Waiting time = 2 s + 4 cycles 00010: Waiting time = 2 s + 8 cycles 00011: Waiting time = 2 s + 16 cycles 00100: Waiting time = 2 s + 32 cycles 00101: Waiting time = 2 s + 64 cycles 00110: Waiting time = 2 s + 512 cycles 00111: Waiting time = 2 s + 1024 cycles 01000: Waiting time = 2 s + 2048 cycles 01001: Waiting time = 2 s + 4096 cycles 01010: Waiting time = 2 s + 16384 cycles 01011: Waiting time = 2 s + 32768 cycles 01100: Waiting time = 2 s + 65536 cycles 01101: Waiting time = 2 s + 131072 cycles 01110: Waiting time = 2 s + 262144 cycles 01111: Waiting time = 2 s + 524288 cycles

Table 4.13 Differences in I/O Registers Associated with Low Power Consumption Functions (3/3)

Register Symbol	Bit Symbol	RX630	RX210
HOCOWTCR2	—	—	HOCO wait control register 2
DPSBYCR	DEEPCUT[1:0] (RX630) DEEPCUT1 (RX210)	Deep cut 00: Power is supplied to the RAM (RAM0) and USB resume detecting unit in deep software standby mode 01: Power is not supplied to the RAM (RAM0) and USB resume detecting unit in deep software standby mode 10: Setting prohibited 11: Power is not supplied to the RAM (RAM0) and USB resume detecting unit in deep software standby mode. In addition, LVD is stopped and the low power consumption function in a power-on reset circuit is enabled.	Deep cut 0: LVD and POR can be operated at deep software standby mode. 1: LVD does not operate at deep software standby mode and POR operates in the low power consumption operation mode at deep software standby mode.
DPSIER1	—	Deep standby interrupt enable register 1	—
DPSIER2	DUSBIE	USB suspend/resume deep standby cancel signal enabled	Reserved
DPSIER3	—	Deep standby interrupt enable register 1	—
DPSIFR1	—	Deep standby interrupt flag register 1	—
DPSIFR2	DUSBIF	USB suspend/resume deep standby cancel flag	Reserved
DPSIFR3	—	Deep standby interrupt flag register 3	—
DPSIEGR1	—	Deep standby interrupt edge register 1	—
DPSIEGR3	—	Deep standby interrupt edge register 1	—
FHSSBYCR	—	—	Flash HOCO software standby control register

4.6 Differences in the Register Write Protection Function

Table 4.14 lists the Differences in the Register Write Protection Function.

Table 4.14 Differences in the Register Write Protection Function

Bit Symbol	RX630	RX210
PRC0	Registers associated with the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR	Registers associated with the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, HOCOCR2
PRC1	• Registers related to the operating modes: SYSCR0, SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR, RSTCKCR, MOSCWTCR, SOSCWTCR, PLLWTCR, DPSBYCR, DPSIER0, DPSIER1, DPSIER2, DPSIER3, DPSIFR0, DPSIFR1, DPSIFR2, DPSIFR3, DPSIEGR0, DPSIEGR1, DPSIEGR2, DPSIEGR3 • Registers related to clock generation circuit: MOFCR, HOCOPCR • Software reset register: SWRR	• Registers related to the operating modes: SYSCR0, SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR, RSTCKCR, MOSCWTCR, SOSCWTCR, PLLWTCR, DPSBYCR, DPSIER0,DPSIER2, DPSIFR0,DPSIFR2, DPSIEGR0, DPSIEGR2, FHSSBYCR, HOCOWTCR2 • Registers related to clock generation circuit: MOFCR, HOCOPCR, PLLPCR • Software reset register: SWRR
PRC2	—	VRCR
PRC3	Registers related to the LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	Registers related to the LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

Table 4.15 lists the Difference in the I/O Register Associated With the Register Write Protection Function.

Table 4.15 Difference in the I/O Register Associated With the Register Write Protection Function

Register Symbol	Bit Symbol	RX630	RX210
PRCR	PRC2	Reserved	Protect bit 2

4.7 Differences in the ICU

Table 4.16 lists the Differences in the ICU.

Table 4.16 Differences in the ICU

Item	RX630	RX210
Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection (edge detection or level detection is fixed for each source of connected peripheral modules) • Interrupt grouping: Multiple interrupt requests can be allocated to a single interrupt vector • Number of groups for edge detection interrupts: 7 (groups 0 to 6) • Number of groups for level detection interrupts: 1 (group 12) • Interrupt unit selection: One of the two interrupt request units can be selected as an interrupt request source. • Number of units: 6	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection (edge detection or level detection is fixed for each source of connected peripheral modules)
External pin interrupts	• Interrupts from pins IRQ0 to IRQ15 • Number of sources: 16 • Interrupt detection: Low level/falling edge/rising edge/rising and falling edges (one of these detection methods can be set for each source) • Digital filter function: Supported	• Interrupts from pins IRQ0 to IRQ7 • Number of sources: 8 • Interrupt detection: Low level/falling edge/rising edge/rising and falling edges (one of these detection methods can be set for each source) • Digital filter function: Supported
Event link interrupts	—	The ELSR18I or ELSR19I interrupt is generated by an ELC event
Return from power-down modes	• Sleep mode: Return is initiated by non-maskable interrupts or any other interrupt source. • All-module clock stop mode: Return is initiated by non-maskable interrupts, IRQ0 to IRQ15 interrupts, TMR interrupts, USB resume interrupts, or RTC alarm/periodic interrupts. • Software standby mode: Return is initiated by non-maskable interrupts, IRQ0 to IRQ15 interrupts, USB resume interrupts, or RTC alarm/periodic interrupts.	• Sleep mode: Return is initiated by non-maskable interrupts or any other interrupt source. • All-module clock stop mode: Return is initiated by non-maskable interrupts, IRQ0 to IRQ7 interrupts, TMR interrupts, or RTC alarm/periodic interrupts. • Software standby mode: Return is initiated by non-maskable interrupts, IRQ0 to IRQ7 interrupts, or RTC alarm/periodic interrupts.

Table 4.17 lists the Differences in the I/O Registers Associated With the ICU.

Table 4.17 Differences in the I/O Registers Associated With the ICU

Register Symbol	Bit Symbol	RX630	RX210
IRQFLTE1	—	IRQ pin digital filter enable register 1	—
IRQFLTC1	—	IRQ pin digital filter setting register 1	—
GRPm (m = group number)	—	Group m interrupt source register	—
GENm (m = group number)	—	Group m interrupt enable register	—
GCRm (m = group number)	—	Group m interrupt clear register	—
SEL	—	Unit selecting register (cannot be used in products with 100 pins or less)	—

4.8 Differences in Buses

Table 4.18 lists the Differences in Buses.

Table 4.18 Differences in Buses

Item	RX630	RX210
Internal peripheral bus 2	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with PCLKB	• Connected to peripheral modules (modules other than those connected to internal peripheral bus 1) • Operates in synchronization with PCLKB and PCLKD
Internal peripheral bus 3	• Connected to the USB module • Operates in synchronization with PCLKB	—
Internal peripheral bus 4	Reserved area	—
Internal peripheral bus 5	Reserved area	—

Table 4.19 lists the Difference in the I/O Register Associated With Buses.

Table 4.19 Difference in the I/O Register Associated With Buses

Register Symbol	Bit Symbol	RX630	RX210
CSnCR (n = 0 to 3)	BSIZE[1:0]	External bus width select 00: A 16-bit bus space is selected 01: A 32-bit bus space is selected (1) 10: An 8-bit bus space is selected 11: Setting prohibited	External bus width select 00: A 16-bit bus space is selected 01: Setting prohibited 10: An 8-bit bus space is selected 11: Setting prohibited
CSnCR (n = 4 to 7)	—	CSn Control Register (CSnCR)	—

Note 1: This setting cannot be used in products with 100 pins or less.

4.9 Difference in the DMAC

Table 4.20 lists the Difference in the DMAC.

Table 4.20 Difference in the DMAC

Item	RX630	RX210
Event link function (output)	—	Event link request is generated after one data transfer (for block, after one block transfer).

4.10 Difference in the DTC Controller

Table 4.21 lists the difference in the DTC controller.

Table 4.21 Difference in the DTC Controller

Item	RX630	RX210
Event link function (output)	—	Event link request is generated after one data transfer (for block, after one block transfer).

4.11 Differences in the I/O Ports

Table 4.22 and Table 4.23 list the differences in the I/O ports.

Table 4.22 Differences in the I/O Ports (1/2)

Item	Port	RX630	RX210
Open drain output	P03	No pin present	Not selectable
	P05, P07	Selectable	Not selectable
	P12 to P17	Selectable	Selectable
	P20 to P27	Selectable	Selectable
	P30 to P34, P36, P37	Selectable	Selectable
	P35	Not selectable	Not selectable
	P40 to P47	Selectable	Not selectable
	P50 to P55	Selectable	Not selectable
	PA0 to PA7	Selectable	Selectable
	PB0 to PB7	Selectable	Selectable
	PC0 to PC7	Selectable	Selectable
	PD0 to PD7	Selectable	Not selectable
	PE0 to PE7	Selectable	Selectable
	PH0 to PH3	No pins present	Not selectable
	PJ1	No pin present	Not selectable
	PJ3	Selectable	Not selectable
Drive ability switching	P03	No pin present	Fixed to normal output
	P05, P07	Fixed to high driving ability output	Fixed to normal output
	P12 to P17	Fixed to high driving ability output	Selectable
	P20 to P26	Fixed to high driving ability output	Selectable
	P27	Selectable	Selectable
	P30 to P34, P37	Fixed to high driving ability output	Selectable
	P35	Not selectable	Not selectable
	P36	Fixed to normal output	Selectable
	P40 to P47	Fixed to normal output	Fixed to normal output
	P50 to P52	Selectable	Selectable
	P53 to P55	Fixed to high driving ability output	Selectable
	PA0 to PA7	Selectable	Selectable
	PB0 to PB7	Selectable	Selectable
	PC0 to PC7	Selectable	Selectable
	PD0 to PD7	Selectable	Selectable
	PE0 to PE7	Selectable	Selectable
	PH0 to PH3	No pins present	Selectable
	PJ1	No pin present	Selectable
	PJ3	Fixed to high driving ability output	Selectable

Table 4.23 Differences in the I/O Ports (2/2)

Item	Port	RX630	RX210
5-V tolerant	P03	No pin present	Not 5-V tolerant
	P05	Not 5-V tolerant	Not 5-V tolerant
	P07	5-V tolerant	Not 5-V tolerant
	P12, P13, P16, P17	5-V tolerant	5-V tolerant
	P14, P15	5-V tolerant	Not 5-V tolerant
	P20 to P25	5-V tolerant	Not 5-V tolerant
	P26, P27	Not 5-V tolerant	Not 5-V tolerant
	P30 to P34	5-V tolerant	Not 5-V tolerant
	P35 to P37	Not 5-V tolerant	Not 5-V tolerant
	P40 to P47	Not 5-V tolerant	Not 5-V tolerant
	P50 to P52	5-V tolerant	Not 5-V tolerant
	P53	Not 5-V tolerant	Not 5-V tolerant
	P54, P55	5-V tolerant	Not 5-V tolerant
	PA0, PA5, PA7	Not 5-V tolerant	Not 5-V tolerant
	PA1 to PA4, PA6	5-V tolerant	Not 5-V tolerant
	PB0 to PB7	5-V tolerant	Not 5-V tolerant
	PC0 to PC7	5-V tolerant	Not 5-V tolerant
	PD0 to PD7	Not 5-V tolerant	Not 5-V tolerant
	PE0 to PE7	Not 5-V tolerant	Not 5-V tolerant
	PH0 to PH3	No pins present	Not 5-V tolerant
	PJ1	No pin present	Not 5-V tolerant
	PJ3	Not 5-V tolerant	Not 5-V tolerant

Table 4.24 lists the Difference in the I/O Register Associated With I/O ports.

Table 4.24 Difference in the I/O Register Associated With I/O ports

Register Symbol	Bit Symbol	RX630	RX210
ODR0	B2, B3	For port PE1 pins 00: CMOS output 01: N-channel open-drain output 10: P-channel open-drain output 11: Setting prohibited	PE1 00: CMOS output 01: N-channel open-drain output 10: P-channel open-drain output 11: Hi-Z

4.12 Differences in the MPC

Table 4.25 to Table 4.33 list the differences in the MPC.

Table 4.25 Differences in the MPC (1/9)

Module/ Function	Channel	Pin Functions	Allocation Port	RX630	RX210
Interrupt		NMI	P35	Selectable	Selectable
Interrupts	IRQ0	IRQ0-DS (input) (1)	P30	Selectable	Selectable
		IRQ0 (input)	PD0	Selectable	Selectable
			PH1	Not selectable	Selectable
	IRQ1	IRQ1-DS (input) (1)	P31	Selectable	Selectable
		IRQ1 (input)	PD1	Selectable	Selectable
			PH2	Not selectable	Selectable
	IRQ2	IRQ2-DS (input) (1)	P32	Selectable	Selectable
		IRQ2 (input)	P12	Selectable	Selectable
			PD2	Selectable	Selectable
	IRQ3	IRQ3-DS (input) (1)	P33	Selectable	Selectable
		IRQ3 (input)	P13	Selectable	Selectable
			PD3	Selectable	Selectable
	IRQ4	IRQ4-DS (input) (1)	PB1	Selectable	Selectable
		IRQ4 (input)	P14	Selectable	Selectable
			P34	Selectable	Selectable
			PD4	Selectable	Selectable
	IRQ5	IRQ5-DS (input) (1)	PA4	Selectable	Selectable
		IRQ5 (input)	P15	Selectable	Selectable
			PD5	Selectable	Selectable
			PE5	Selectable	Selectable
	IRQ6	IRQ6-DS (input) (1)	PA3	Selectable	Selectable
		IRQ6 (input)	P16	Selectable	Selectable
			PD6	Selectable	Selectable
			PE6	Selectable	Selectable
	IRQ7	IRQ7-DS (input) (1)	PE2	Selectable	Selectable
		IRQ7 (input)	P17	Selectable	Selectable
			PD7	Selectable	Selectable
			PE7	Selectable	Selectable
	IRQ8	IRQ8-DS (input) (1)	P40	Selectable	No pin(s) present
		IRQ8 (input)	P20	Selectable	No pin(s) present
	IRQ9	IRQ9-DS (input) (1)	P41	Selectable	No pin(s) present
		IRQ9 (input)	P21	Selectable	No pin(s) present
	IRQ10	IRQ10-DS (input) (1)	P42	Selectable	No pin(s) present
		IRQ10 (input)	P55	Selectable	No pin(s) present
	IRQ11	IRQ11-DS (input) (1)	P43	Selectable	No pin(s) present
		IRQ11 (input)	PA1	Selectable	No pin(s) present
	IRQ12	IRQ12-DS (input) (1)	P44	Selectable	No pin(s) present
		IRQ12 (input)	PB0	Selectable	No pin(s) present
			PC1	Selectable	No pin(s) present
	IRQ13	IRQ13-DS (input) (1)	P45	Selectable	No pin(s) present
		IRQ13 (input)	P05	Selectable	No pin(s) present
			PC6	Selectable	No pin(s) present

Note 1: Pin names to which –DS is appended are for pins that can be used as trigger release from deep software standby mode.

Table 4.26 Differences in the MPC (2/9)

Module/ Function	Channel	Pin Functions	Allocation Port	RX630	RX210
Interrupts	IRQ14	IRQ14-DS (input) (1)	P46	Selectable	No pin(s) present
		IRQ14 (input)	PC0	Selectable	No pin(s) present
			PC7	Selectable	No pin(s) present
	IRQ15	IRQ15-DS (input) (1)	P47	Selectable	No pin(s) present
		IRQ15 (input)	P07	Selectable	No pin(s) present
MTU2a	MTU0	MTIOC0A (I/O)	P34	Selectable	Selectable
			PB3	Selectable	Selectable
		MTIOC0B (I/O)	P13	Selectable	Selectable
			P15	Selectable	Selectable
			PA1	Selectable	Selectable
		MTIOC0C (I/O)	P32	Selectable	Selectable
			PB1	Selectable	Selectable
		MTIOC0D (I/O)	P33	Selectable	Selectable
			PA3	Selectable	Selectable
	MTU1	MTIOC1A (I/O)	P20	Selectable	Selectable
			PE4	Selectable	Selectable
		MTIOC1B (I/O)	P21	Selectable	Selectable
			PB5	Selectable	Selectable
	MTU2	MTIOC2A (I/O)	P26	Selectable	Selectable
			PB5	Selectable	Selectable
		MTIOC2B (I/O)	P27	Selectable	Selectable
			PE5	Selectable	Selectable
	MTU3	MTIOC3A (I/O)	P14	Selectable	Selectable
			P17	Selectable	Selectable
			PC1	Selectable	Selectable
			PC7	Selectable	Selectable
		MTIOC3B (I/O)	P17	Selectable	Selectable
			P22	Selectable	Selectable
			PB7	Selectable	Selectable
			PC5	Selectable	Selectable
		MTIOC3C (I/O)	P16	Selectable	Selectable
			PC0	Selectable	Selectable
			PC6	Selectable	Selectable
			PJ3	Selectable	Selectable
		MTIOC3D (I/O)	P16	Selectable	Selectable
			P23	Selectable	Selectable
			PB6	Selectable	Selectable
			PC4	Selectable	Selectable

Note 1: Pin names to which –DS is appended are for pins that can be used as trigger release from deep software standby mode.

Table 4.27 Differences in the MPC (3/9)

Module/ Function	Channel	Pin Functions	Allocation Port	RX630	RX210
MTU2a	MTU4	MTIOC4A (I/O)	P24	Selectable	Selectable
			PA0	Selectable	Selectable
			PB3	Selectable	Selectable
			PE2	Selectable	Selectable
		MTIOC4B (I/O)	P30	Selectable	Selectable
			P54	Selectable	Selectable
			PC2	Selectable	Selectable
			PD1	Selectable	Selectable
			PE3	Selectable	Selectable
		MTIOC4C (I/O)	P25	Selectable	Selectable
			PB1	Selectable	Selectable
			PE1	Selectable	Selectable
			PE5	Selectable	Selectable
		MTIOC4D (I/O)	P31	Selectable	Selectable
			P55	Selectable	Selectable
			PC3	Selectable	Selectable
			PD2	Selectable	Selectable
			PE4	Selectable	Selectable
	MTU5	MTIC5U (input)	PA4	Selectable	Selectable
			PD7	Selectable	Selectable
		MTIC5V (input)	PA6	Selectable	Selectable
			PD6	Selectable	Selectable
		MTIC5W (input)	PB0	Selectable	Selectable
			PD5	Selectable	Selectable
	MTU	MTCLKA (input)	P14	Selectable	Selectable
			P24	Selectable	Selectable
			PA4	Selectable	Selectable
			PC6	Selectable	Selectable
		MTCLKB (input)	P15	Selectable	Selectable
			P25	Selectable	Selectable
			PA6	Selectable	Selectable
			PC7	Selectable	Selectable
		MTCLKC (input)	P22	Selectable	Selectable
			PA1	Selectable	Selectable
			PC4	Selectable	Selectable
		MTCLKD (input)	P23	Selectable	Selectable
			PA3	Selectable	Selectable
			PC5	Selectable	Selectable

Table 4.28 Differences in the MPC (4/9)

Module/ Function	Channel	Pin Functions	Allocation Port	RX630	RX210
POE2a	POE0	POE0# (input)	PC4	Selectable	Selectable
			PD7	Selectable	Selectable
	POE1	POE1# (input)	PB5	Selectable	Selectable
			PD6	Selectable	Selectable
	POE2	POE2# (input)	P34	Selectable	Selectable
			PA6	Selectable	Selectable
			PD5	Selectable	Selectable
	POE3	POE3# (input)	P33	Selectable	Selectable
			PB3	Selectable	Selectable
			PD4	Selectable	Selectable
	POE8	POE8# (input)	P17	Selectable	Selectable
			P30	Selectable	Selectable
			PD3	Selectable	Selectable
			PE3	Selectable	Selectable
TMR	TMR0	TMO0 (output)	P22	Selectable	Selectable
			PB3	Selectable	Selectable
			PH1	No pin(s) present	Selectable
		TMCI0 (input)	P21	Selectable	Selectable
			PB1	Selectable	Selectable
			PH3	No pin(s) present	Selectable
		TMRI0 (input)	P20	Selectable	Selectable
			PA4	Selectable	Selectable
			PH2	No pin(s) present	Selectable
	TMR1	TMO1 (output)	P17	Selectable	Selectable
			P26	Selectable	Selectable
		TMCI1 (input)	P12	Selectable	Selectable
			P54	Selectable	Selectable
			PC4	Selectable	Selectable
		TMRI1 (input)	P24	Selectable	Selectable
			PB5	Selectable	Selectable
	TMR2	TMO2 (output)	P16	Selectable	Selectable
			PC7	Selectable	Selectable
		TMCI2 (input)	P15	Selectable	Selectable
			P31	Selectable	Selectable
			PC6	Selectable	Selectable
		TMRI2 (input)	P14	Selectable	Selectable
			PC5	Selectable	Selectable
	TMR3	TMO3 (output)	P13	Selectable	Selectable
			P32	Selectable	Selectable
			P55	Selectable	Selectable
		TMCI3 (input)	P27	Selectable	Selectable
			P34	Selectable	Selectable
			PA6	Selectable	Selectable
		TMRI3 (input)	P30	Selectable	Selectable
			P33	Selectable	Selectable

Table 4.29 Differences in the MPC (5/9)

Module/ Function	Channel	Pin Functions	Allocation Port	RX630	RX210
SCIc, SCId	SCI0	RXD0 (input)/SMISO0 (I/O)/SSCL0(I/O)	P21	Selectable	Selectable
			P33	Selectable	Not selectable
		TXD0 (output)/SMOSI0 (I/O)/SSDA0 (I/O)	P20	Selectable	Selectable
			P32	Selectable	Not selectable
		SCK0 (I/O)	P22	Selectable	Selectable
			P34	Selectable	Not selectable
		CTS0# (input)/RTS0# (output)/ SS0# (input)	P23	Selectable	Selectable
			PJ3	Selectable	Not selectable
	SCI1	RXD1 (input)/SMISO1 (I/O)/SSCL1 (I/O)	P15	Selectable	Selectable
			P30	Selectable	Selectable
		TXD1(output)/SMOSI1 (I/O)/SSDA1 (I/O)	P16	Selectable	Selectable
			P26	Selectable	Selectable
		SCK1 (I/O)	P17	Selectable	Selectable
			P27	Selectable	Selectable
		CTS1# (input)/RTS1# (output)/ SS1# (input)	P14	Selectable	Selectable
			P31	Selectable	Selectable
	SCI2	RXD2 (input)/SMISO2 (I/O)/SSCL2 (I/O)	P12	Selectable	Selectable
			P52	Selectable	Selectable
		TXD2 (output)/SMOSI2 (I/O)/SSDA2 (I/O)	P13	Selectable	Selectable
			P50	Selectable	Selectable
		SCK2 (I/O)	P51	Selectable	Selectable
		CTS2# (input)/RTS2# (output)/ SS2# (input)	P54	Selectable	Selectable
	SCI3	RXD3 (input)/SMISO3 (I/O)/SSCL3(I/O)	P16	Selectable	Selectable
			P25	Selectable	Selectable
		TXD3 (output)/SMOSI3 (I/O)/SSDA3 (I/O)	P17	Selectable	Selectable
			P23	Selectable	Selectable
		SCK3 (I/O)	P15	Selectable	Selectable
			P24	Selectable	Selectable
		CTS3# (input)/RTS3# (output)/ SS3# (input)	P26	Selectable	Selectable
	SCI5	RXD5 (input)/SMISO5 (I/O)/SSCL5 (I/O)	PA2	Selectable	Selectable
			PA3	Selectable	Selectable
			PC2	Selectable	Selectable
		TXD5 (output)/SMOSI5 (I/O)/SSDA5 (I/O)	PA4	Selectable	Selectable
			PC3	Selectable	Selectable
		SCK5 (I/O)	PA1	Selectable	Selectable
			PC1	Selectable	Selectable
			PC4	Selectable	Selectable
		CTS5# (input)/RTS5# (output)/ SS5# (input)	PA6	Selectable	Selectable
			PC0	Selectable	Selectable

Table 4.30 Differences in the MPC (6/9)

Module/ Function	Channel	Pin Functions	Allocation Port	RX630	RX210
SCIc, SCId	SCI6	RXD6 (input)/SMISO6 (I/O)/SSCL6 (I/O)	P33	Selectable	Selectable
			PB0	Selectable	Selectable
		TXD6 (output)/SMOSI6 (I/O)/SSDA6 (I/O)	P32	Selectable	Selectable
			PB1	Selectable	Selectable
		SCK6 (I/O)	P34	Selectable	Selectable
			PB3	Selectable	Selectable
		CTS6# (input)/RTS6# (output)/SS6# (input)	PB2	Selectable	Selectable
			PJ3	Selectable	Selectable
	SCI8	RXD8 (input)/SMISO8 (I/O)/SSCL8 (I/O)	PC6	Selectable	Selectable
		TXD8 (output)/SMOSI8 (I/O)/SSDA8 (I/O)	PC7	Selectable	Selectable
		SCK8 (I/O)	PC5	Selectable	Selectable
		CTS8# (input)/RTS8# (output)/SS8# (input)	PC4	Selectable	Selectable
	SCI9	RXD9 (input)/SMISO9 (I/O)/SSCL9 (I/O)	PB6	Selectable	Selectable
		TXD9 (output)/SMOSI9 (I/O)/SSDA9 (I/O)	PB7	Selectable	Selectable
		SCK9 (I/O)	PB5	Selectable	Selectable
		CTS9# (input)/RTS9# (output)/SS9# (input)	PB4	Selectable	Selectable
	SCI12	RXD12 (input)/SMISO12 (I/O)/SSCL12 (I/O)/ RXDX12 (input)	PE2	Selectable	Selectable
		TXD12 (output)/SMOSI12 (I/O)/SSDA12 (I/O)/ TXDX12 (output)/SIOX12(I/O)	PE1	Selectable	Selectable
		SCK12 (I/O)	PE0	Selectable	Selectable
		CTS12# (input)/RTS12# (output)/ SS12# (input)	PE3	Selectable	Selectable
RIIC	RIIC0	SCL-DS (I/O)	P16	Not selectable	Selectable
		SCL0[FM+] (I/O)	P12	Selectable	Selectable
		SDA-DS (I/O)	P17	Not selectable	Selectable
		SDA0[FM+] (I/O)	P13	Selectable	Selectable
	RIIC1	SCL1 (I/O)	P21	Selectable	No pin(s) present
		SDA1 (I/O)	P20	Selectable	No pin(s) present
	RIIC2	SCL2 (I/O)	P16	Selectable	No pin(s) present
		SDA2 (I/O)	P17	Selectable	No pin(s) present
	RIIC3	SCL3 (I/O)	PC0	Selectable	No pin(s) present
		SDA3 (I/O)	PC1	Selectable	No pin(s) present

Table 4.31 Differences in the MPC (7/9)

Module/ Function	Channel	Pin Functions	Allocation Port	RX630	RX210
RSPI	RSPI0	RSPCKA (I/O)	PA5	Selectable	Selectable
			PB0	Selectable	Selectable
			PC5	Selectable	Selectable
		MOSIA (I/O)	P16	Selectable	Selectable
			PA6	Selectable	Selectable
			PC6	Selectable	Selectable
		MISOA (I/O)	P17	Selectable	Selectable
			PA7	Selectable	Selectable
			PC7	Selectable	Selectable
		SSLA0 (I/O)	PA4	Selectable	Selectable
			PC4	Selectable	Selectable
		SSLA1 (output)	PA0	Selectable	Selectable
			PC0	Selectable	Selectable
		SSLA2 (output)	PA1	Selectable	Selectable
			PC1	Selectable	Selectable
		SSLA3 (output)	PA2	Selectable	Selectable
			PC2	Selectable	Selectable
	RSPI1	RSPCKB (I/O)	P27	Selectable	No pin(s) present
			PE1	Selectable	No pin(s) present
			PE5	Selectable	No pin(s) present
		MOSIB (I/O)	P26	Selectable	No pin(s) present
			PE2	Selectable	No pin(s) present
			PE6	Selectable	No pin(s) present
		MISOB (I/O)	P30	Selectable	No pin(s) present
			PE3	Selectable	No pin(s) present
			PE7	Selectable	No pin(s) present
		SSLB0 (I/O)	P31	Selectable	No pin(s) present
			PE4	Selectable	No pin(s) present
		SSLB1 (output)	P50	Selectable	No pin(s) present
			PE0	Selectable	No pin(s) present
		SSLB2 (output)	P51	Selectable	No pin(s) present
			PE1	Selectable	No pin(s) present
		SSLB3 (output)	P52	Selectable	No pin(s) present
			PE2	Selectable	No pin(s) present
RTC		RTCOUT (output)	P16	Selectable	Selectable
			P32	Selectable	Selectable
		RTCIC0 (input)	P30	Selectable	Selectable
		RTCIC1 (input)	P31	Selectable	Selectable
		RTCIC2 (input)	P32	Selectable	Selectable

Table 4.32 Differences in the MPC (8/9)

Module/Function	Pin Functions	Allocation Port	RX630	RX210
S12AD	AN000 (input)	P40	Selectable	Selectable
	AN001 (input)	P41	Selectable	Selectable
	AN002 (input)	P42	Selectable	Selectable
	AN003 (input)	P43	Selectable	Selectable
	AN004 (input)	P44	Selectable	Selectable
	AN005 (input)	P45	Selectable	Selectable
	AN006 (input)	P46	Selectable	Selectable
	AN007 (input)	P47	Selectable	Selectable
	AN008 (input)	PD0	Selectable	Not selectable
		PE0	Not selectable	Selectable
	AN009 (input)	PD1	Selectable	Not selectable
		PE1	Not selectable	Selectable
	AN010 (input)	PD2	Selectable	Not selectable
		PE2	Not selectable	Selectable
	AN011 (input)	PD3	Selectable	Not selectable
		PE3	Not selectable	Selectable
	AN012(input)	PD4	Selectable	Not selectable
		PE4	Not selectable	Selectable
	AN013 (input)	PD5	Selectable	Not selectable
		PE5	Not selectable	Selectable
	AN014 (input)	PD6	Selectable	Not selectable
		PE6	Not selectable	Selectable
	AN015 (input)	PD7	Selectable	Not selectable
		PE7	Not selectable	Selectable
	ADTRG0# (input)	P07	Selectable	Selectable
		P16	Selectable	Selectable
		P25	Selectable	Selectable
DA	DA0 (output)	P03	Selectable	Selectable
	DA1 (output)	P05	Selectable	Selectable

Table 4.33 Differences in the MPC (9/9)

Module/Function	Pin Functions	Allocation Port	RX630	RX210
External bus	CS0# (output)	P24	Not selectable	Selectable
		PC7	Selectable	Selectable
	CS1# (output)	P25	Not selectable	Selectable
		PC6	Selectable	Selectable
	CS2# (output)	P26	Not selectable	Selectable
		PC5	Selectable	Selectable
	CS3# (output)	P27	Not selectable	Selectable
		PC4	Selectable	Selectable
	CS4# (output)	P24	Selectable	No pin(s) present
	CS5# (output)	P25	Selectable	No pin(s) present
	CS6# (output)	P26	Selectable	No pin(s) present
	CS7# (output)	P27	Selectable	No pin(s) present
	A0 to A7 (output)	PA0 to PA7	Selectable	Selectable
	A8 to A15 (output)	PB0 to PB7	Selectable	Selectable
	A16 to A23 (output)	PC0 to PC7	Selectable	Selectable
	D0 to D7 (I/O)	PD0 to PD7	Selectable	Selectable
	D8 to D15 (I/O)	PE0 to PE7	Selectable	Selectable
	BCLK (output)	P53	Selectable	Selectable
	RD# (output)	P52	Selectable	Selectable
	WR# (output)	P50	Selectable	Selectable
	WR0# (output)	P50	Selectable	Selectable
	WR1# (output)	P51	Selectable	Selectable
	BC0# (output)	PA0	Selectable	Selectable
	BC1# (output)	P51	Selectable	Selectable
	WAIT# (input)	P51	Selectable	Selectable
		P55	Selectable	Selectable
		PC5	Selectable	Selectable
	ALE (output)	P54	Selectable	Selectable

Table 4.34 lists the Differences in the I/O Registers Associated With the MPC.

Table 4.34 Differences in the I/O Registers Associated With the MPC

Register Symbol	Bit Symbol	RX630	RX210
P0nPFS (n = 5, 7)	ISEL	Interrupt input function select	Reserved
P2nPFS (n = 0 to 7)	ISEL	Interrupt input function select	Reserved
P4nPFS (n = 0 to 7)	ISEL	Interrupt input function select	Reserved
P55PFS	ISEL	Interrupt input function select	Reserved
PAnPFS (n = 1, 3, 4)	ASEL	Reserved	Analog function select
PCnPFS (n = 0 to 7)	ISEL	Interrupt input function select	Reserved
PDnPFS (n = 0 to 7)	ASEL	Analog function select	Reserved
PFCSE	CS0E	CS0 enable 0: CS0# output disabled 1: CS0# output enabled	CS0 enable of PC7 0: Configures the PC7 as an I/O pin 1: Configures the PC7 as a CS0# output pin
	CS1E	CS1 enable 0: CS1# output disabled 1: CS1# output enabled	CS1 enable of PC6 0: Configures the PC6 as an I/O pin 1: Configures the PC6 as a CS1# output pin
	CS2E	CS2 enable 0: CS2# output disabled 1: CS2# output enabled	CS2 enable of P26 0: Configures the P26 as an I/O pin 1: Configures the P26 as a CS2# output pin
	CS3E	CS3 enable 0: CS3# output disabled 1: CS3# output enabled	CS3 enable of P27 0: Configures the P27 as an I/O pin 1: Configures the P27 as a CS3# output pin
	CS4E	CS4 enable 0: CS4# output disabled 1: CS4# output enabled	CS0 enable of P24 0: Configures the P24 as an I/O pin 1: Configures the P24 as a CS0# output pin
	CS5E	CS5 enable 0: CS5# output disabled 1: CS5# output enabled	CS1 enable of P25 0: Configures the P25 as an I/O pin 1: Configures the P25 as a CS1# output pin
	CS6E	CS6 enable 0: CS6# output disabled 1: CS6# output enabled	CS2 enable of PC5 0: Configures the PC5 as an I/O pin 1: Configures the PC5 as a CS2# output pin
	CS7E	CS7 enable 0: CS7# output disabled 1: CS7# output enabled	CS3 enable of PC4 0: Configures the PC4 as an I/O pin 1: Configures the PC4 as a CS3# output pin
PFCSS0	—	CS output pin select register 0	—
PFCSS1	—	CS output pin select register 1	—
PFBCR0	ADRHNS	A16 to A23 output enabled	Reserved
	DH32E (1)	D16 to D31 output enable	Reserved
	WR32BC32E (1)	WR3#/BC3# Output Enable WR2#/BC2# Output Enable	Reserved
PFBCR1	WAITS[1:0]	WAIT select 00: Configures P57 as the WAIT# input pin. (1) 01: Configures P55 as the WAIT# input pin. 10: Configures PC5 as the WAIT# input pin. 11: Configures P51 as the WAIT# input pin.	WAIT select 00: Configures P55 as the WAIT# input pin. 01: Configures P55 as the WAIT# input pin. 10: Configures PC5 as the WAIT# input pin. 11: Configures P51 as the WAIT# input pin.

Note 1: This pin cannot be used in packages with 100 pins or less.

4.13 Difference in the MTU2a

Table 4.35 lists the Difference in the MTU2a.

Table 4.35 Difference in the MTU2a

Item	RX630	RX210
Trigger generation	Programmable pulse generator (PPG) output trigger can be generated	—

4.14 Difference in the POE2a

Table 4.36 lists the Difference in the POE2a.

Table 4.36 Difference in the POE2a

Item	RX630	RX210
High-impedance is controlled by an event signal	—	Pins for complementary PWM output from the MTU and output pins for MTU0 can be placed in the high-impedance by an event signal from the event link controller (ELC).

4.15 Differences in the TMR

Table 4.37 lists the Differences in the TMR.

Table 4.37 Differences in the TMR

Item	RX630	RX210
A/D converter conversion start trigger	Compare match A of TMR0 and TMR2	—
Event link function (output)	—	Compare match A, compare match B, and overflow (TMR0, TMR2)
Event link function (input)	—	(1) Count start operation (TMR0, TMR2) (2) Event counter operation (TMR0, TMR2) (3) Count restart operation (TMR0, TMR2)

Table 4.38 lists the Difference in the I/O Register Associated With the TMR.

Table 4.38 Difference in the I/O Register Associated With the TMR

Register Symbol	Bit Symbol	RX630	RX210
TCSR	ADTE	A/D trigger enable	Reserved

4.16 Differences in the CMT

Table 4.39 lists the Differences in the CMT.

Table 4.39 Differences in the CMT

Item	RX630	RX210
Event link facilities (output)	—	An event signal is output upon a CMT1 compare match.
Event link facilities (input)	—	Linking to the specified module is possible. Count start, event count, or count restart is possible upon the specified event.

4.17 Differences in the RTC

Table 4.40 lists the Differences in the RTC.

Table 4.40 Differences in the RTC

Item	RX630	RX210
Count source	Sub-clock (XCIN) or main clock (EXTAL)	Sub-clock (XCIN)
Event link function (input)	—	Periodic event output

Table 4.41 lists the Differences in the I/O Registers Associated With the RTC.

Table 4.41 Differences in the I/O Registers Associated With the RTC

Register Symbol	Bit Symbol	RX630	RX210
RCR2	RESET	In writing 0: Writing is invalid. 1: The prescaler and target registers (R64CNT, RSECAR, RMINAR, RHRAR, RWKAR, RDAYAR, RMONAR, RYRAR, RYRAREN, RADJ, RTCCRy, RSECCPy, RMINCPy, RHRCPy, RDAYCPy, RMONCPy, RCR2.ADJ30, RCR2.AADJE, RCR2.RTCOE, RCR3 (1)) are reset by RTC software reset. In reading 0: In normal clock operation, or RTC software reset has completed. 1: During a RTC software reset	In writing 0: Writing is invalid. 1: The prescaler and target registers are reset by RTC software reset. (R64CNT, RSECAR, RMINAR, RHRAR, RWKAR, RDAYAR, RMONAR, RYRAR, RYRAREN, RADJ, RTCCRy, RSECCPy, RMINCPy, RHRCPy, RDAYCPy, RMONCPy, RCR2.ADJ30, RCR2.AADJE, RCR2.RTCOE) In reading 0: In normal time operation, or RTC software reset has completed. 1: During an RTC software reset
RCR3	RTCDV[2:0]	Reserved	Sub-clock oscillator drive ability control
RCR4	—	RTC control register 4	—
RFRH RFRL	—	Frequency register H Frequency register L	—

Note 1: As per Table 1.3 List of Products in the user's manual, in products with footnote *2, the RCR3 register is not initialized by an RTC software reset. For all other products, executing an RTC software reset sets the RCR3 register to 00h.

4.18 Difference in the IWDT

Table 4.42 lists the Difference in the IWDT.

Table 4.42 Difference in the IWDT

Item	RX630	RX210
Event link function (output)	—	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)

4.19 Differences in SCIc and SCId

Table 4.43 lists the Differences in SCIc and SCId.

Table 4.43 Differences in SCIc and SCId

Item	RX630	RX210
Number of channels	9 (1)	7 (1)
Event link function (output)	—	• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output

Note 1: The number of channels differs according to the number of pins on the package.

4.20 Differences in the RIIC

Table 4.44 lists the Differences in the RIIC.

Table 4.44 Differences in the RIIC

Item	RX630	RX210
Number of channels	2 (1)	1
Transfer rate	Up to 1 Mbps	Up to 400 kbps
Event link function (output)	—	• Error in transfer or occurrence of events (detection of AL, NACK, time-out, a start condition including a restart condition, or a stop condition) • Receive-data-full (including matching with a slave address) • Transmit-data-empty (including matching with a slave address) • Transmission complete

Note 1: The number of channels differs according to the number of pins on the package.

Table 4.45 lists the Difference in the I/O Register Associated With the RIIC.

Table 4.45 Difference in the I/O Register Associated With the RIIC

Register Symbol	Bit Symbol	RX630	RX210
ICFER	FNPE (1)	Fast-mode plus enable	Reserved

Note 1: This bit is only supported by RIIC0. In RIIC1 to RIIC3, b7 is reserved.

4.21 Differences in the RSPI

Table 4.46 lists the Differences in the RSPI.

Table 4.46 Differences in the RSPI

Item	RX630	RX210
Number of channels	2 (1)	1
Event link function	—	The following five types of events can be output to the ELC: • Reception-buffer full event output • Transmission-buffer empty event output • Mode fault, overrun, or parity error event output • RSPI idle event output • Transmission-completed event output

Note 1: The number of channels differs according to the number of pins on the package.

4.22 Differences in the S12AD

Table 4.47 and Table 4.48 list the differences in the S12AD.

Table 4.47 Differences in the S12AD (1/2)

Item	RX630	RX210
Number of channels	14 (1)	16
Data registers	• For analog input: 14 (1) • For temperature sensor: 1 • For internal reference voltage: 1 • The A/D conversion result is held in a 12-bit A/D data register. • In A/D-converted value addition mode, A/D conversion results are stored in a 14-bit A/D data register.	• For analog input: 16 • For duplication of A/D conversion data in double trigger mode: 1 • For temperature sensor: 1 • For internal reference voltage: 1 • The A/D conversion result is stored in 12-bit A/D data registers. • In addition mode, A/D conversion results are added and stored in A/D data registers as 14-bit data. • Duplication of A/D conversion data: (1) A/D conversion data of one selected analog input channel is stored into the ADDRy register when conversion is started by the first trigger and into the duplication register when started by the second trigger (y = 0 to 15). (2) Duplication is available only in double trigger mode in single scan mode or group scan mode.
Operating modes	• Single-cycle scan mode: A/D conversion is to be performed for only once on the analog inputs of up to 14 (1) arbitrarily selected channels. A/D conversion is to be performed only once on the temperature sensor output. A/D conversion is to be performed only once on the internal reference voltage. • Continuous scan mode: A/D conversion is to be performed sequentially on the analog inputs of up to 14 (1) arbitrarily selected channels.	• Single scan mode: A/D conversion is performed for only once on the analog inputs of up to 16 arbitrarily selected channels. A/D conversion is performed only once on the temperature sensor output. A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of up to 16 arbitrarily selected channels. • Group scan mode: Up to 16 channels of analog inputs are divided into group A and group B and A/D conversion is performed only once on all the selected channels on a group basis. The scan start conditions of group A and group B can be independently selected, thus allowing A/D conversion of group A and group B to be started independently.
Conditions of A/D conversion start	• Software trigger • Synchronous trigger: Trigger by MTU, TPU, or TMR • Asynchronous trigger: A/D conversion can be started by the ADTRG0# pin.	• Software trigger • Synchronous trigger: Trigger by MTU, TPU (1), ELC, or temperature sensor • Asynchronous trigger: A/D conversion can be triggered from the ADTRG0# pin.

Note 1: The number of channels differs according to the number of pins on the package.

Table 4.48 Differences in the S12AD (2/2)

Item	RX630	RX210
Functions	• Sample-and-hold function • Number of sampling states is adjustable. • A/D-converted value addition mode	• Sample-and-hold function • Variable sampling state count • A/D-converted value addition mode • Self-diagnosis of 12-bit A/D converter • Analog input disconnection detection assist • Double trigger mode (duplication of A/D conversion data) • Channel-dedicated sample-and-hold function
Interrupt sources	• A scan end interrupt (S12ADI0) request can be generated on completion of A/D conversion. • An S12ADI0 interrupt can activate the DMAC or DTC.	• A scan end interrupt (S12ADI0) request can be generated on completion of A/D conversion. • In double trigger mode, an S12ADI0 interrupt request can be generated on completion of double scan. • In group scan mode, an S12ADI0 interrupt request can be generated on completion of group A scan, whereas an A/D scan end interrupt specially for group B (GBADI) request can be generated on completion of group B scan. • In group scan mode with double trigger mode, an S12ADI0 interrupt request can be generated on completion of double scan of group A, whereas a GBADI interrupt request can be generated on completion of group B scan. • An S12ADI0 or GBADI interrupt can activate the DMAC or DTC.
Event link function (output)	—	• An ELC event can be generated on completion of scans except for group B scan in group scan mode.
Event link function (input)	—	• A/D conversion can be started by the trigger from ELC.

Note 1: Excluding double trigger mode and group scan mode, an S12ADI0 interrupt is generated after a scan is completed.

Table 4.49 lists the Differences in the I/O Registers Associated With the S12AD.

Table 4.49 Differences in the I/O Registers Associated With the S12AD

Register Symbol	Bit Symbol	RX630	RX210
ADCSR	DBLANS[4:0]	—	A/D conversion data duplication channel select
	GBADIE	—	Group B scan end interrupt enable
	DBLE	—	Double trigger mode select
	CKS[1:0]	A/D conversion clock select	—
ADANSn (n = 0, 1)	—	A/D channel select register n	—
ADANSn (n = A, B)	—	—	A/D channel select register n
ADADSn (n = 0, 1)	—	A/D-converted value addition mode select register n	—
ADADS	—	—	A/D-converted value addition mode select register
ADCER	DIAGVAL[1:0]	Reserved	Conversion voltage select for self-diagnosis
	DIAGLD	Reserved	Self-diagnosis mode select
	DIAGM	Reserved	Self-diagnosis enable
ADSTRGR	TRSB[3:0]	—	A/D conversion start trigger select for group B
ADEXICR	TSSAD	Temperature sensor output A/D converted value addition mode select	Reserved
ADDRy	—	A/D data register y (y = 0 to 13) (1)	A/D data register y (y = 0 to 15)
ADSSTR01	—	A/D sampling state register 01	—
ADSSTR23	—	A/D sampling state register 23	—
ADSSTRn (n = 0 to 7, L, T, O)	—	—	A/D sampling state register n
ADDBLDR	—	—	A/D data duplication register
ADRD	—	—	A/D self-diagnosis data register
ADSHCR	—	—	A/D sample and hold circuit control register
ADDISCR	—	—	A/D disconnecting detection control register

Note 1: The number of channels differs according to the number of pins on the package.

4.23 Differences in the DA

Table 4.50 lists the Differences in the DA.

Table 4.50 Differences in the DA

Item	RX630	RX210
Countermeasure against mutual interference between analog modules	Measure against interference between D/A and A/D conversion: The D/A converter can perform conversion simultaneously with the 10-bit A/D converter (degradation of A/D conversion accuracy caused by interference is reduced by controlling the D/A converter inrush current generation timing with the enable signal).	—
Event link function	—	D/A0 conversion can be started when an event signal is input.

Table 4.51 lists the Difference in the I/O Register Associated With the DA.

Table 4.51 Difference in the I/O Register Associated With the DA

Register Symbol	Bit Symbol	RX630	RX210
DAADSCR	—	D/A A/D synchronous start control register	—

4.24 Differences in the TEMPS

Table 4.52 lists the Difference in the TEMPS.

Table 4.52 Difference in the TEMPS

Item	RX630	RX210
Temperature sensor voltage output	Temperature sensor outputs a voltage to the 12-bit A/D converter.	Temperature sensor outputs a voltage to the 12-bit A/D converter via a programmable gain amplifier (PGA).

Table 4.53 lists the Differences in the I/O Registers Associated With the TEMPS.

Table 4.53 Differences in the I/O Registers Associated With the TEMPS

Register Symbol	Bit Symbol	RX630	RX210
TSCR	PGAGAIN[1:0]	Reserved	PGA gain select
	PGAEN	Reserved	PGA enable
	TSOE	Temperature sensor output enable	Reserved

4.25 Difference in the RAM

Table 4.54 lists the Difference in the RAM.

Table 4.54 Difference in the RAM

Item	RX630	RX210
RAM capacity	128 KB (max) (RAM0: 64 KB, RAM1: 64 KB)	96 KB (max) (RAM0: 64 KB, RAM1: 32 KB)

4.26 Differences in the ROM and E2 DataFlash

Table 4.55 lists the Differences in the ROM.

Table 4.55 Differences in the ROM

Item	RX630	RX210
Memory space (RX630) Memory capacity (RX210)	User area: 2 MB (max) User boot area: 16 KB	User area: 1 MB (max) User boot area: 16 KB
Units of programming and erasure	• Units of programming for the user area or user boot area: 128 bytes • Units of erasure for the user area: In block units • Units of erasure for the user boot area: 16 Kbytes	• Units of programming for the user area or user boot area: 2, 8, or 128 bytes • Units of erasure for the user area: In block units • Units of erasure for the user boot area: 16 Kbytes
On-board programming	Programming in boot mode • The asynchronous serial interface (SCI1) is used. • The transfer rate is adjusted automatically. • The user boot area can also be programmed. Programming in user boot mode • Able to create original boot programs of the user's making. Programming by a routine for ROM programming within the user program • This allows ROM programming without resetting the system. Programming in USB boot mode • USB0 is used. • Dedicated hardware is not required, so direct connection to a computer is possible.	Reprogramming in boot mode • The clock synchronous serial interface (SCI1) is used. • The bit rate is automatically adjusted. • The user boot area is also programmable. Reprogramming in user boot mode • The user-specific boot program can be programmed. Reprogramming using the ROM reprogramming routine in the user program • ROM is reprogrammable without resetting the system.

Table 4.56 lists the Differences in the E2 DataFlash.

Table 4.56 Differences in the E2 DataFlash

Item	RX630	RX210
Memory space (RX630) Memory capacity (RX210)	Data area: 32 KB	Data area: 8 KB
Read cycle (RX630) Reading via the peripheral bus (RX210)	A read operation takes 6 cycles of FCLK in words or bytes	A read operation takes 4 cycles of FCLK in words or bytes
Units of programming and erasure	• Unit of programming for the data area: 2 bytes • Unit of erasure for the data area: 32 bytes	• Unit of programming for the data area: 2 or 8 bytes • Unit of erasure for the data area: 128 bytes

Table 4.57 lists the Differences in the I/O Registers Associated With the ROM and the E2 DataFlash.

Table 4.57 Differences in the I/O Registers Associated With the ROM and the E2 DataFlash

Register Symbol	Bit Symbol	RX630	RX210
DFLRE0	DBRE00	0000-0063 block read enable	DB00 to DB15 block read enable
	DBRE01	0064-0127 block read enable	DB16 to DB31 block read enable
	DBRE02	0128-0191 block read enable	DB32 to DB47 block read enable
	DBRE03	0192-0255 block read enable	DB48 to DB63 block read enable
	DBRE04	0256-0319 block read enable	Reserved
	DBRE05	0320-0383 block read enable	Reserved
	DBRE06	0384-0447 block read enable	Reserved
	DBRE07	0448-0511 block read enable	Reserved
DFLRE1	—	E2 DataFlash read enable register	—
DFLWE0	DBWE00	0000-0063 block programming/ erasure enable	DB00 to DB15 block programming/ erasure enable
	DBWE01	0064-0127 block programming/ erasure enable	DB16 to DB31 block programming/ erasure enable
	DBWE02	0128-0191 block programming/ erasure enable	DB32 to DB47 block programming/ erasure enable
	DBWE03	0192-0255 block programming/ erasure enable	DB48 to DB63 block programming/ erasure enable
	DBWE04	0256-0319 block programming/ erasure enable	Reserved
	DBWE05	0320-0383 block programming/ erasure enable	Reserved
	DBWE06	0384-0447 block programming/ erasure enable	Reserved
	DBWE07	0448-0511 block programming/ erasure enable	Reserved
DFLWE1	—	E2 DataFlash P/E enable register 1	—
FENTRYR	FENTRY2	ROM P/E mode entry 2	Reserved
	FENTRY3	ROM P/E mode entry 3	Reserved

5. Reference Documents

User's Manual: Hardware

RX630 User's Manual: Hardware Rev.1.50 (R01UH0040EJ)

RX210 User's Manual: Hardware Rev.1.40 (R01UH0037EJ)

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

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REVISION HISTORY	RX630 Group, RX210 Group Application Note Comparing the RX630 and RX210 Groups (LQFP100)

Rev.	Date	Description	
		Page	Summary
1.00	Aug. 1, 2013	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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