RX610 Group

Asynchronous SCI Transmission/Reception Using DMAC

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Abstract

This application note presents an example of asynchronous serial communication using the serial communication interface (SCI) and DMA controller (DMAC) of a Renesas MCU.

Target Device

RX610 Group

Introduction

This application note applies to the following MCUs and conditions.

RX610 Group

The program can be used with other RX Family MCUs that have the same I/O registers (peripheral device control registers) as the RX610 Group. Check the latest version of the manual for any additions and modifications to the functions used by this application note. Careful evaluation is recommended before using this application note.

The program works with an endian specification of big or little and with left or right specified as the bit order.

Contents

1. Specifications

The DMA controller (DMAC) is used to transmit and receive serial data between the serial communication interface (SCI) and the on-chip RAM. Figure 1 presents an overview of asynchronous serial data transmission and reception using the DMAC.

1. Channel 1 of the SCI and channels 1 (transmit) and 0 (receive) of the DMAC are used.
2. The communication format is a bit length of 8 bits, one stop bit, and no parity.
3. In the transmit operation, the DMAC is started by a transmit data empty interrupt request, and the transmit data is transferred from a pre-specified transfer source to the transmit data register (TDR) of the SCI.
4. In the receive operation, the DMAC is started by a receive data full interrupt request, and the receive data is transferred from the receive data register (RDR) of the SCI to a pre-specified transfer destination.
5. After the specified number of transfers complete, preparation is made for retransmission.

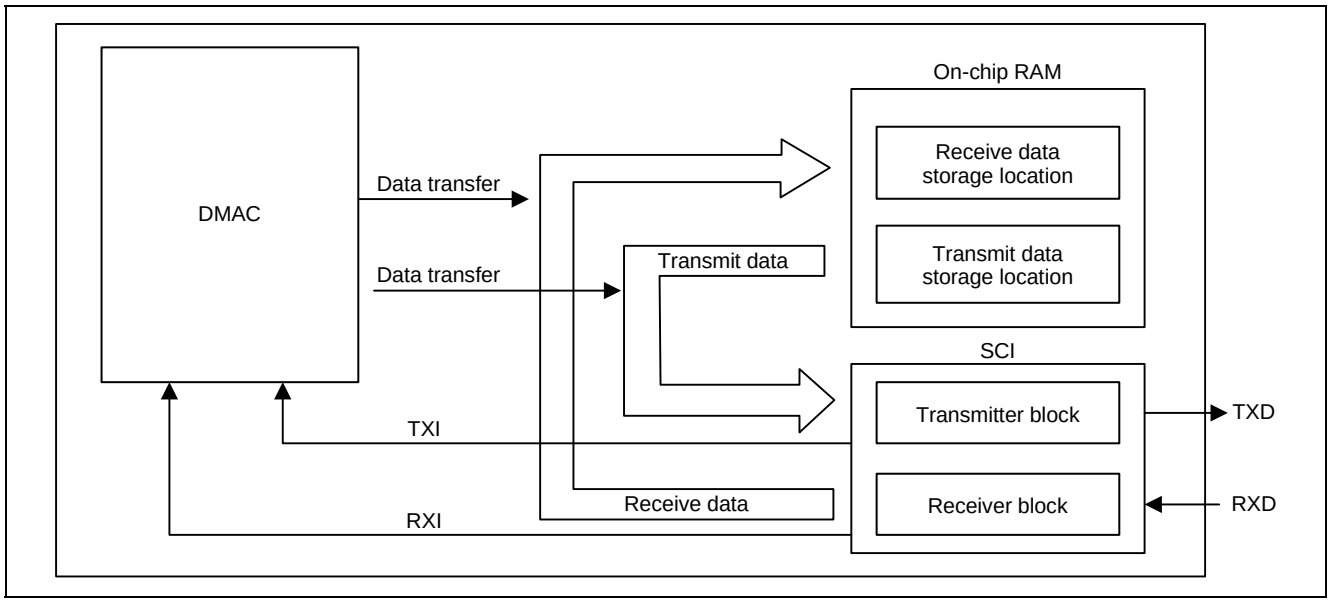

Figure 1 Overview of Asynchronous Serial Data Transmission/Reception Using DMAC

Functions Used

Serial communication interface (SCI)

DMA controller (DMAC)

2. Description of Functions

In the sample program, the transmit data empty interrupt (TXI) and receive data full interrupt (RXI) of the SCI are the sources used to activate the DMAC. Data transfer is performed in the specified transfer mode, resulting in asynchronous serial data transmission and reception.

2.1 Operation of Serial Communication Interface (SCI)

When the SCI operates in asynchronous mode, serial communication is accomplished by transmitting and receiving characters, each of which contains a start bit indicating the start of the transfer, a stop bit or bits indicating the end of the transfer, and data bits. Synchronization is by character unit. The transmitter block and receiver block each have a double-buffered structure, allowing data to be read and written during transmission and reception.

The communication line is normally held in the mark state (high level) during asynchronous serial communication. The SCI monitors the communications line, and when it detects a space state (low level) it treats it as a start bit and starts serial communication.

In serial communication, one character comprises a start bit (low level), data bits (LSB-first: starting from the lowest-order bit), a parity bit (high/low), and a stop bit or bits, in that order.

For details of the SCI, see the section Serial Communication Interface (SCI) in the *RX610 Group Hardware Manual*.

Table 1 provides an overview of asynchronous serial communication and, figure 2 shows the data format used.

Table 1 Overview of Asynchronous Serial Communication

Item	Description
Channels	7 channels (SCI0 to SCI6)
Transfer speed	On-chip baud rate generator allowing setting of any bit rate
Clock sources	Internal clock: PCLK, PCLK/4, PCLK/16, PCLK/64 (PCLK: Peripheral module clock) External clock: Clock input on SCKn pin
Data formats	Transfer data length: 7 bits/8 bits Transmit stop bits: 1 bit/2 bits Parity function: Even parity/odd parity/no parity Transfer order: LSB first/MSB first
Baud rates	Internal clock selected: 100 bps to 1,562,500 bps (PCLK = 50 MHz) External clock selected: Max. 781,250 bps (PCLK = 50 MHz)
Error detection	Parity error, overrun error, framing error
Interrupt requests	Transmit data empty interrupt (TXI) Receive data full interrupt (RXI) Receive error interrupt (ERI) Transmit error interrupt (TEI)
Clock source selection	Selectable between internal clock and external clock

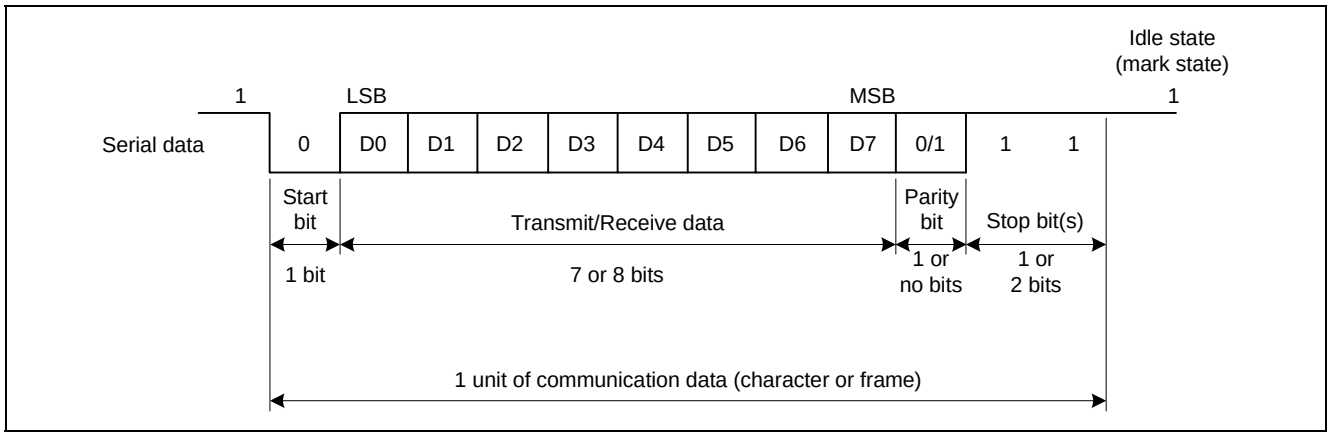

Figure 2 Asynchronous Serial Communication Data Format (8 Data Bits/Parity/2 Stop Bits)

Figure 3 is a block diagram of the SCI (SCI0 to SCI4). The registers are described below.

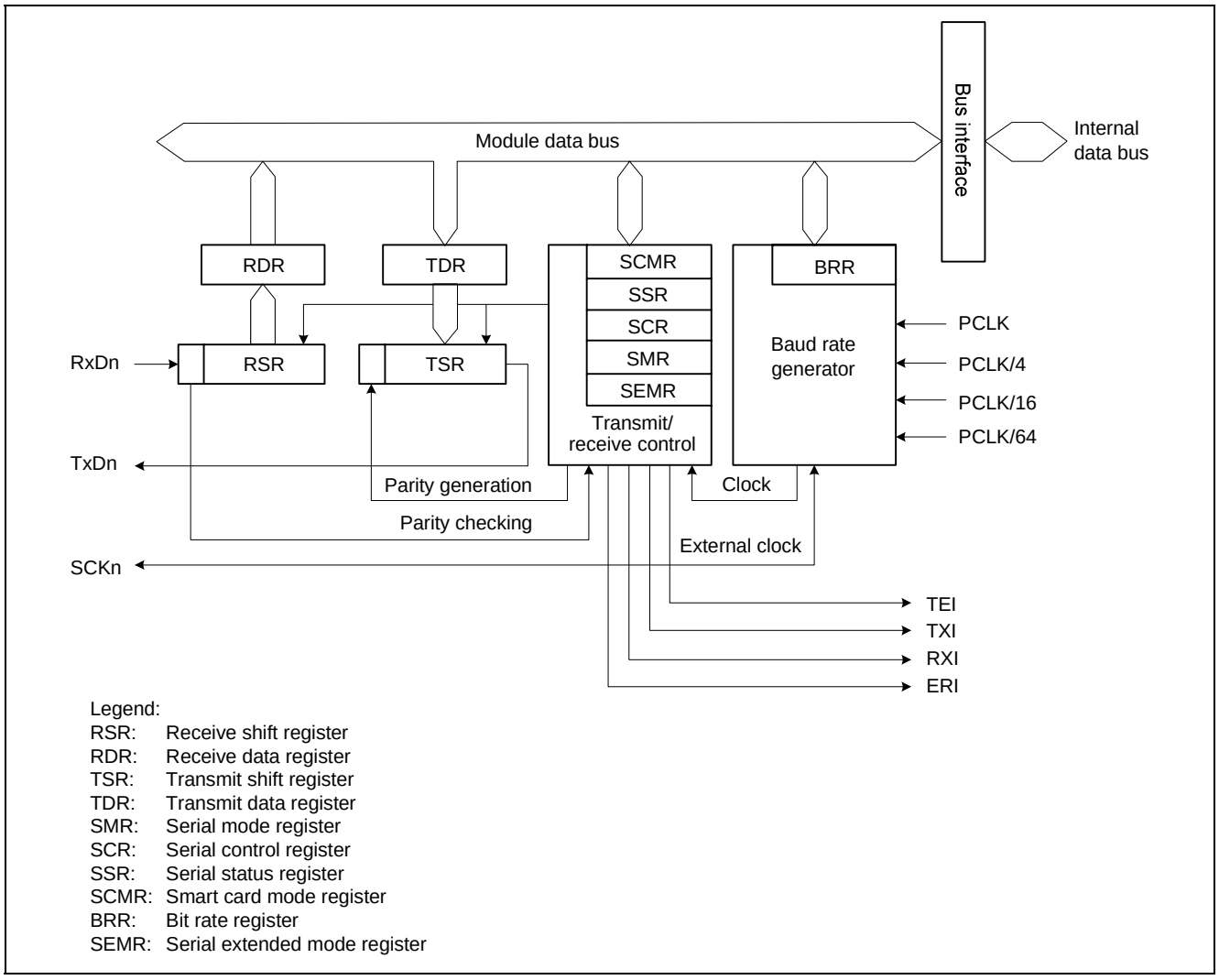

Figure 3 Block diagram of SCI (SCI0 to SCI4)

- Receive shift register (RSR)
  RSR is a shift register that converts to parallel data serial data input to the RxDn pin. When one frame of data has been received, it is transferred to RDR automatically.

- Receive data register (RDR)
  RDR is a register that stores receive data. When the SCI has received one frame of data, it transfers the receive data from RSR to RDR, allowing RSR to receive the next frame of data. RSR and RDR form a double-buffered structure, so continuous receive operations can be performed. Read RDR only once after a receive data full interrupt (RXI) request occurs. Note that an overrun error occurs if the next frame of data is received before the receive data in RDR is read. RDR cannot be written to by the CPU.

- Transmit data register (TDR)
  TDR is an 8-bit register that stores transmit data. When the SCI detects that TSR is empty, it transfers the transmit data written in TDR to TSR and starts transmission. TDR and TSR form a double-buffered structure, so continuous transmit operations can be performed. If after a frame of data is transmitted the next frame of transmit data has already been written to TDR, the SCI transfers it to TSR to continue transmission. The CPU can read from or write to TDR at any time. Only write transmit data to TDR once after each transmit data empty interrupt (TXI) request.

- Transmit shift register (TSR)
  TSR is a shift register for transmitting serial data. To perform serial data transmission, transmit data written to TDR is automatically transferred to TSR and then sent to the TxDn pin. TSR cannot be accessed directly by the CPU.

- Serial mode register (SMR)
  SMR is used to select the communication format and the clock source of the on-chip baud rate generator.

- Serial control register (SCR)
  SCR is used to select settings for transmit/receive control, interrupt control, and transmit/receive clock sources. For information on interrupts, see the Interrupt Control Unit (ICU) section in the *RX610 Group Hardware Manual*.

- Serial status register (SSR)
  SSR contains status flags for the SCI.

- Bit rate register (BRR)
  BRR is a register used to adjust the bit rate. The SCI performs baud rate generator control independently for each channel, different bit rates can be set for each channel.

- Serial extended mode register (SEMR)
  SEMR is a register used to select the clock for a 1-bit period in asynchronous mode.

- Smart card mode register (SCMR)
  SCMR is a register used to select the smart card interface mode and its format.

2.2 Operation of DMA Controller (DMAC)

When a DMA transfer request is issued, the DMAC starts transfer operation according to the specified channel priority, and transfer operation ends when the transmit end condition is satisfied. There are two transfer modes: operand and nonstop. Operand transfer mode supports either single-operand transfer or consecutive-operand transfer. Note that regardless of the transfer mode the set number of bytes of data are transferred in a DMA transfer operation. Each time a unit of data is transferred the number of bytes to be transferred is decremented, and when the set number of bytes reaches 0 the DMA transfer operation ends. For details of the DMAC, see the DMA Controller (DMAC) section in the *RX610 Group Hardware Manual*. Table 2 presents an overview of the DMAC.

Table 2 Overview of DMAC

Item		Description	
Number of channels		4 (DMACn (n = 0 to 3))	
Transfer space		4 GB	
Max. transfer byte count		64 MB	
DMA request sources		• Software trigger • Trigger input to external pin interrupt • Interrupt requests of peripheral functions	
Channel priority		Channel 0 > channel 1 > channel 2 > channel 3 (Channel 0 has top priority.)	
Transfer data	1 data unit	Bit length: 8 bits, 16 bits, 32 bits	
	1 operand	Data count: 1, 2, 4, 8, 16, 32, 64, 128	
Transfer modes	Operand transfer mode	Single	• One operand is transferred by a single DMA request. • Channel arbitration takes place after transfer of one operand ends. • A DMA request is required after each operand transfer ends until the DMA transfer operation finishes.
		Consecutive	• By a single DMA request, single operands are transferred consecutively until the DMA transfer operation finishes. • Channel arbitration takes place after transfer of each operand ends. • Only an initial DMA request is needed.
	Nonstop transfer mode	• By a single DMA request, operation takes place continuously until the DMA transfer operation finishes. • Channel arbitration takes place after transfer of each operand ends. • Only an initial DMA request is needed.	
DMA transmit start conditions		DMA transfer starts when all of the following conditions are met. • DEN bit in DMCR of DMACn set to 1 (DMA transfer enabled) • DMST bit in DMSCNT set to 1 (DMAC start) • DMA request generated for channel n (DMACn) and execution right obtained by channel arbitration	
DMA transmit end condition		Value of DMCBC register of DMACn is 0000000h.	
Interrupt request generation timing		Value of DMCBC register of DMACn is 0000000h.	

Figure 4 is a block diagram of the DMAC.

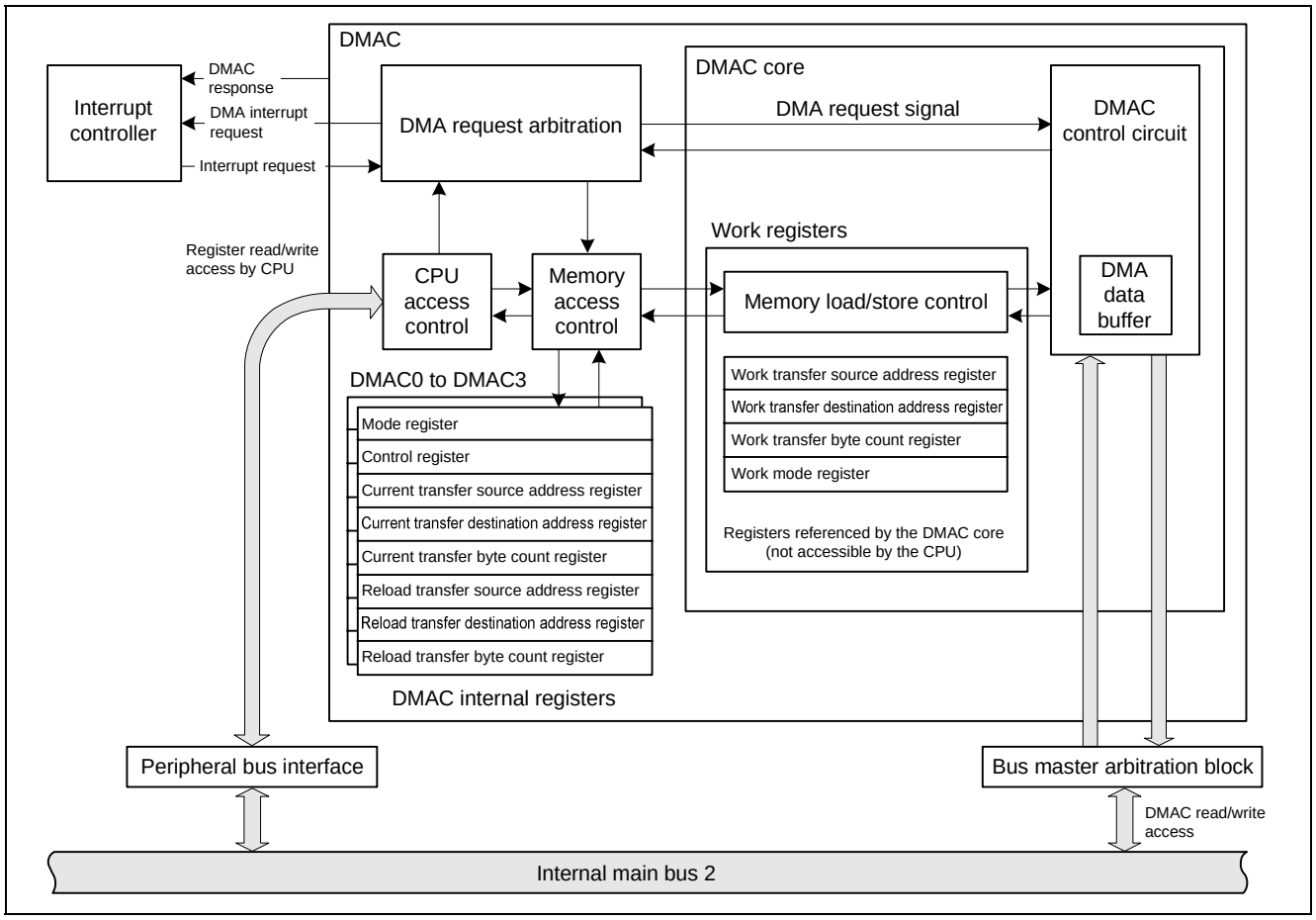

Figure 4 Block Diagram of DMAC

- DMA mode register (DMMOD)
  DMMOD is used to select the direction for calculating the transfer source or transfer destination address and to set the transfer data size.
- DMA control register A (DMCRA)
  DMCRA is used to control the DMAC functions. It is used to specify settings for DMA source request, reload function, and transfer type.
- DMA control register B (DMCRB)
  DMCRB is used to control DMA transfers. It initializes the internal state of the DMAC.
- DMA control register C (DMCRC)
  DMCRC is used to control DMA transfers. It controls the DMA transfer enable bit at the end of a DMA transfer.
- DMA control register D (DMCRD)
  DMCRD is used to control DMA transfers. It indicates the presence or absence of a DMA request.
- DMA control register E (DMCRE)
  DMCRE is used to control DMA transfers. It controls enabling of a DMA transfer.
- DMA current transfer source address register (DMCSA)
  DMCSA is used to set the transfer source start address.
- DMA current transfer destination address register (DMCDA)
  DMCDA is used to set the transfer destination start address.
- DMA current transfer byte count register (DMCBC)
  DMCBC is used to set the number of bytes to be transferred.
- DMA reload transfer source address register (DMRSA)
  DMRSA is used to set the address reloaded in the DMCSA register.
- DMA reload transfer destination address register (DMRDA)
  DMRDA is used to set the address reloaded in the DMCDA register.
- DMA reload transfer byte count register (DMRBC)
  DMRBC is used to set the DMA transfer byte count reloaded in the DMCBC register.
- DMA interrupt control register (DMICNT)
  DMICNT is used to enable DMA interrupt requests for individual channels.
- DMA start register (DMSCNT)
  DMSCNT is used to start the DMAC.
- DMA arbitration status register (DMASTS)
  DMASTS shows the data transfer state of each channel.
- DMA transfer end detect register (DMEDET)
  DMEDET is used to end DMA transfer operation for individual channels.

3. Operation

Table 3 lists the settings conditions for the SCI communication function, and table 4 the DMAC transfer conditions, used by the sample program. Figure 5 shows the operation timing.

Table 3 SCI Settings Conditions

Channel used	SCI1
Communication mode	Asynchronous mode
Interrupts	Transmit data empty interrupt (TXI) Receive data full interrupt (RXI) Receive error interrupt (ERI) Transmit end interrupt (TEI)
Communication speed	38,400 bps (PCLK = 50 MHz)
Data length	8 bits
Stop bits	1 stop bit
Parity	None

Table 4 DMAC Transfer Conditions

Conditions	Transfer conditions of SCI transmission-side DMAC (TXI1)	Transfer conditions of SCI reception-side DMAC (RXI1)
Channel used	Channel 1 (DMAC1)	Channel 0 (DMAC0)
Transfer mode	Operand transfer (single)	Operand transfer (single)
Number of transfers	256 times	256 times
Transfer data	Size: Byte Data contents: 256 bytes consisting of H'00 to H'FF.	Size: Byte Data contents: Any 256 bytes
Transfer source	On-chip RAM	Receive data register (SCI1.RDR)
Transfer destination	Transmit data register (SCI1.TDR)	On-chip RAM
Transfer source address	Transfer source address is incremented after each transfer.	Transfer source is fixed.
Transfer destination address	Transfer destination is fixed.	Transfer destination address is incremented after each transfer.
Activation source	SCI transmit data empty interrupt	SCI receive data full interrupt
Interrupt	Interrupt to CPU enabled after specified data transfer finishes.	Interrupt to CPU enabled after specified data transfer finishes.

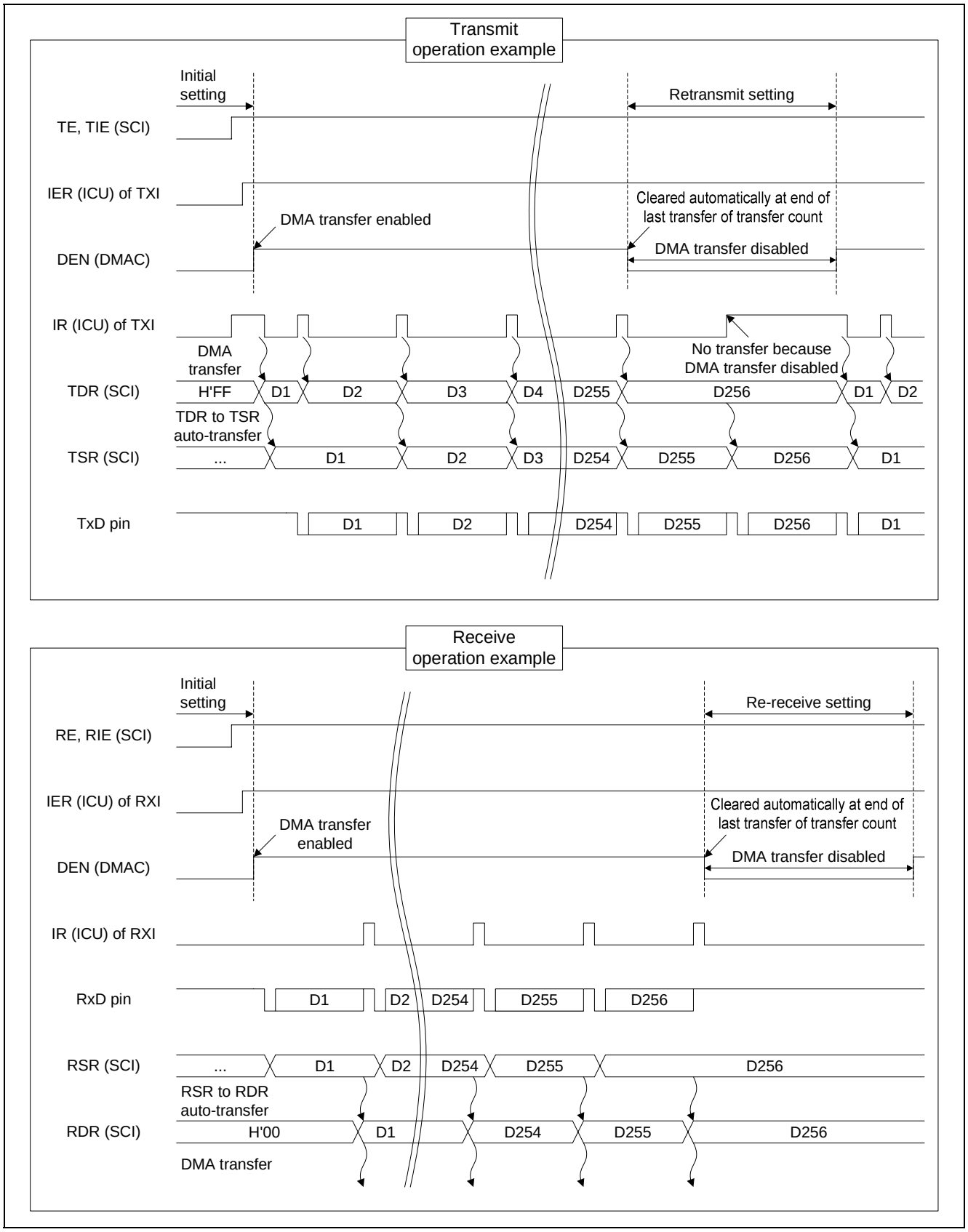

Figure 5 Operation Timing

4. Software

4.1 List of Functions

Table 5 is a list of the functions used by the sample program.

Table 5 List of Functions

Function	Description
HardwareSetup	Initialization processing, clock setting, cancelling of module stop state
main	Main process Initial setting of ICU, interrupt level setting
dmac1_init	Initial setting of DMAC1
dmac0_init	Initial setting of DMAC0
sci1_init	Initial setting of SCI, transfer clock setting
DMAC1_dmtend_int	DMAC1 transfer end interrupt
DMAC0_dmtend_int	DMAC0 transfer end interrupt
int_sci_tei1	Transmit end interrupt
int_sci_eri1	Receive error interrupt

4.2 Variables Used

Table 6 lists the variables used by the sample program.

Table 6 List of Variables

Variable, Label	Description
recvBuf[256]	Array variable for storing serial receive data
trnsBuf[256]	Array variable for storing serial transmit data

4.3 Processing Sequence

Figures 6 to 14 show the processing sequence of the sample program.

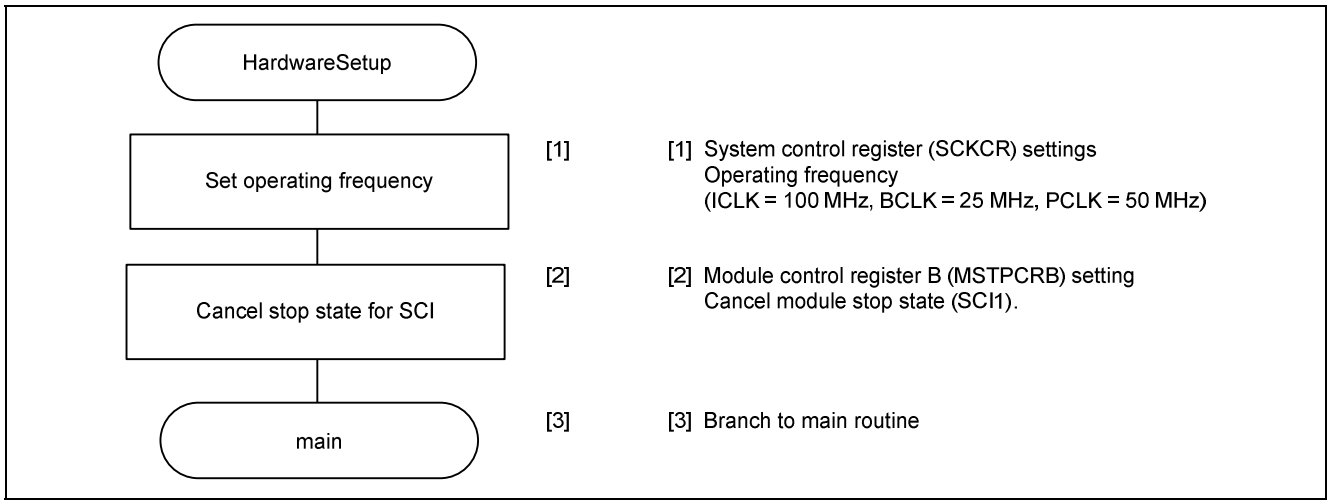

Figure 6 Initialization Processing

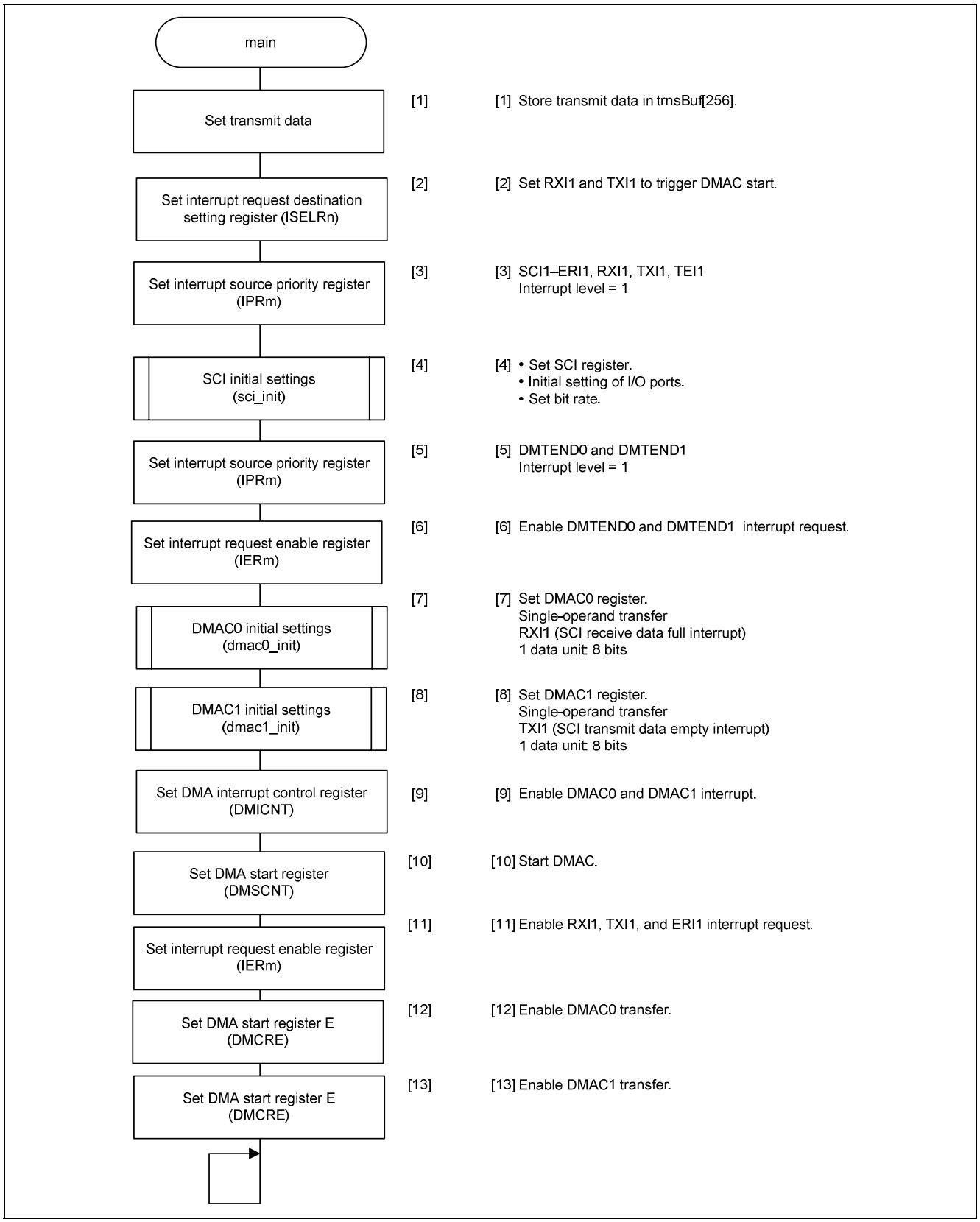

Figure 7 Main Process

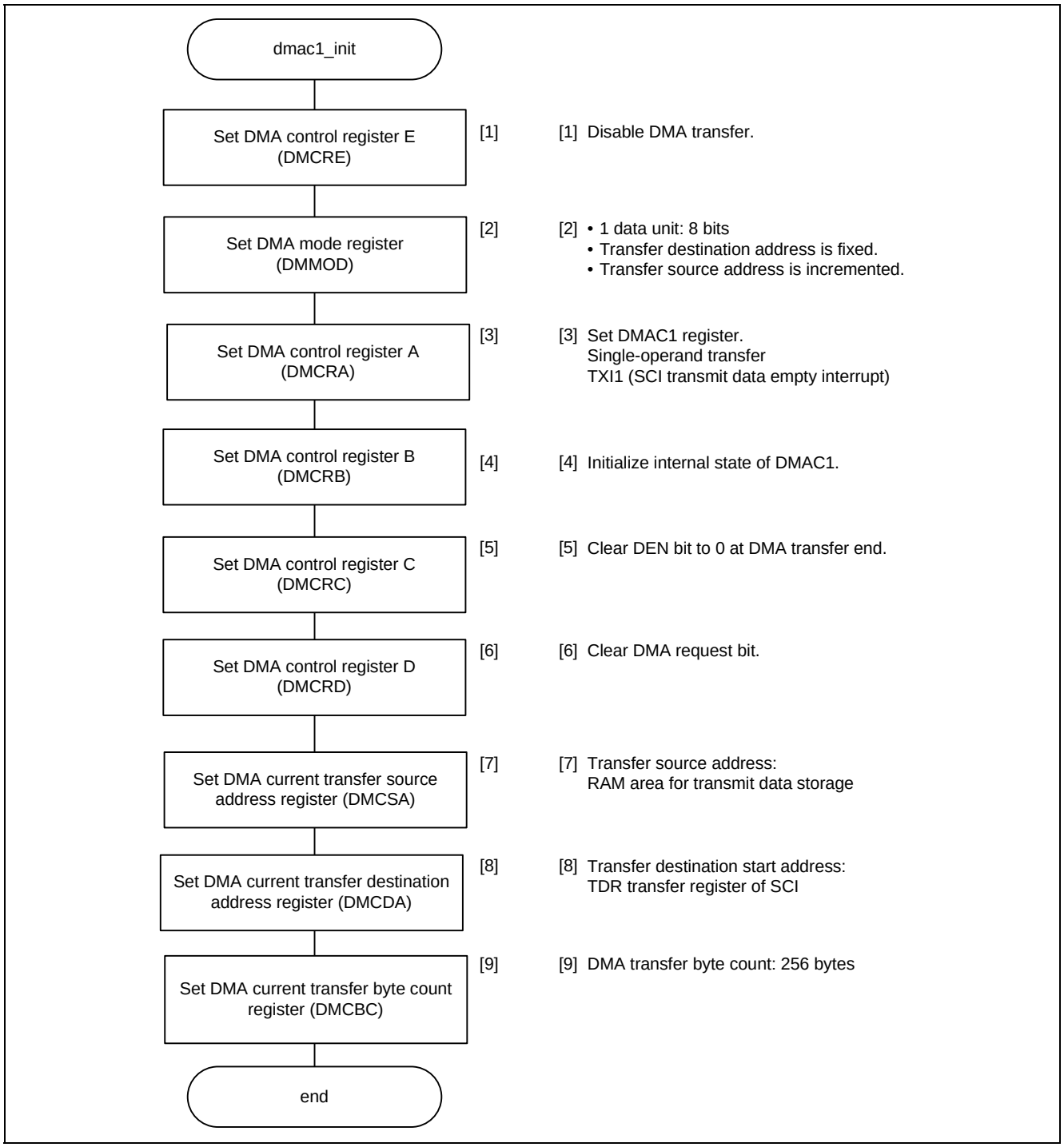

Figure 8 DMAC1 Initial Settings

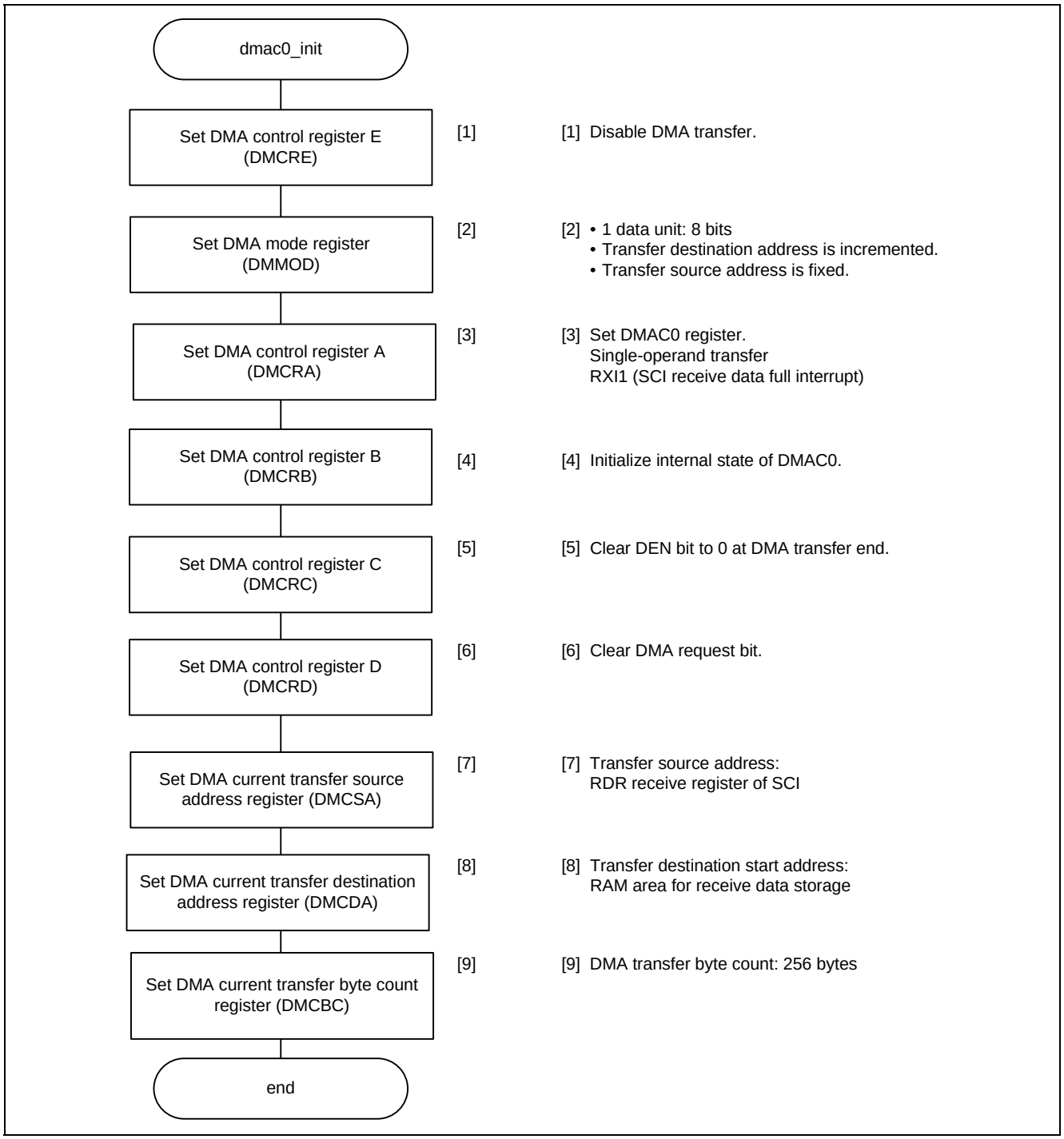

Figure 9 DMAC0 Initial Settings

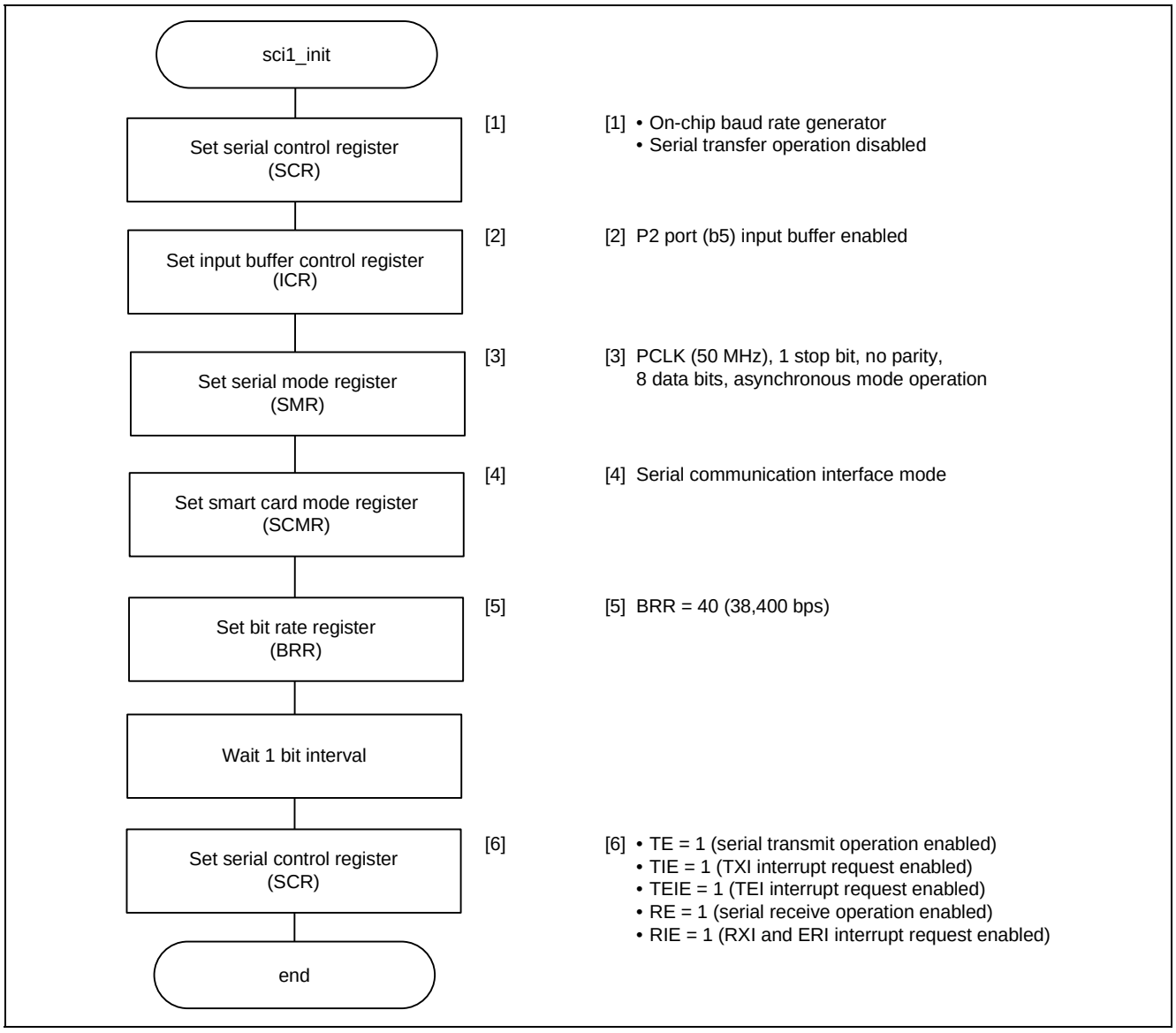

Figure 10 SCI Initial Settings

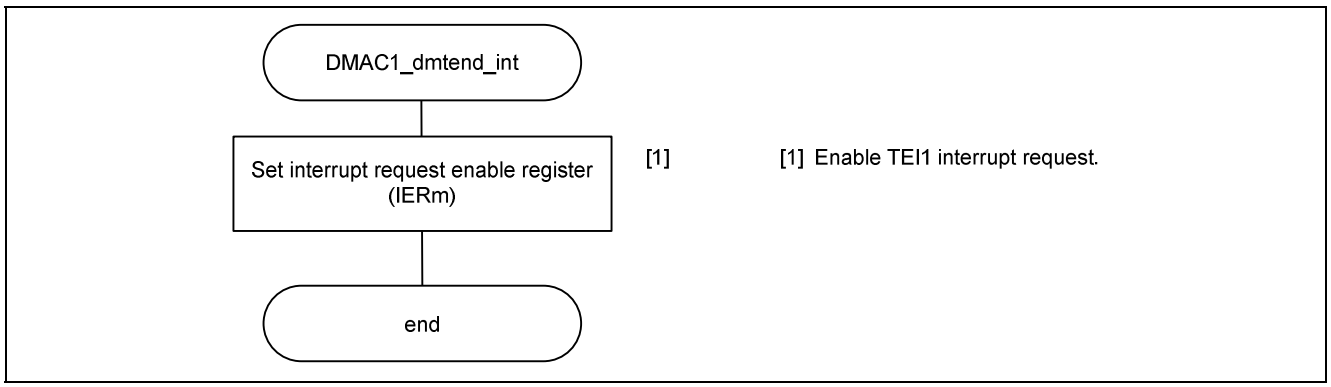

Figure 11 DMAC1 Transfer End Interrupt Handler

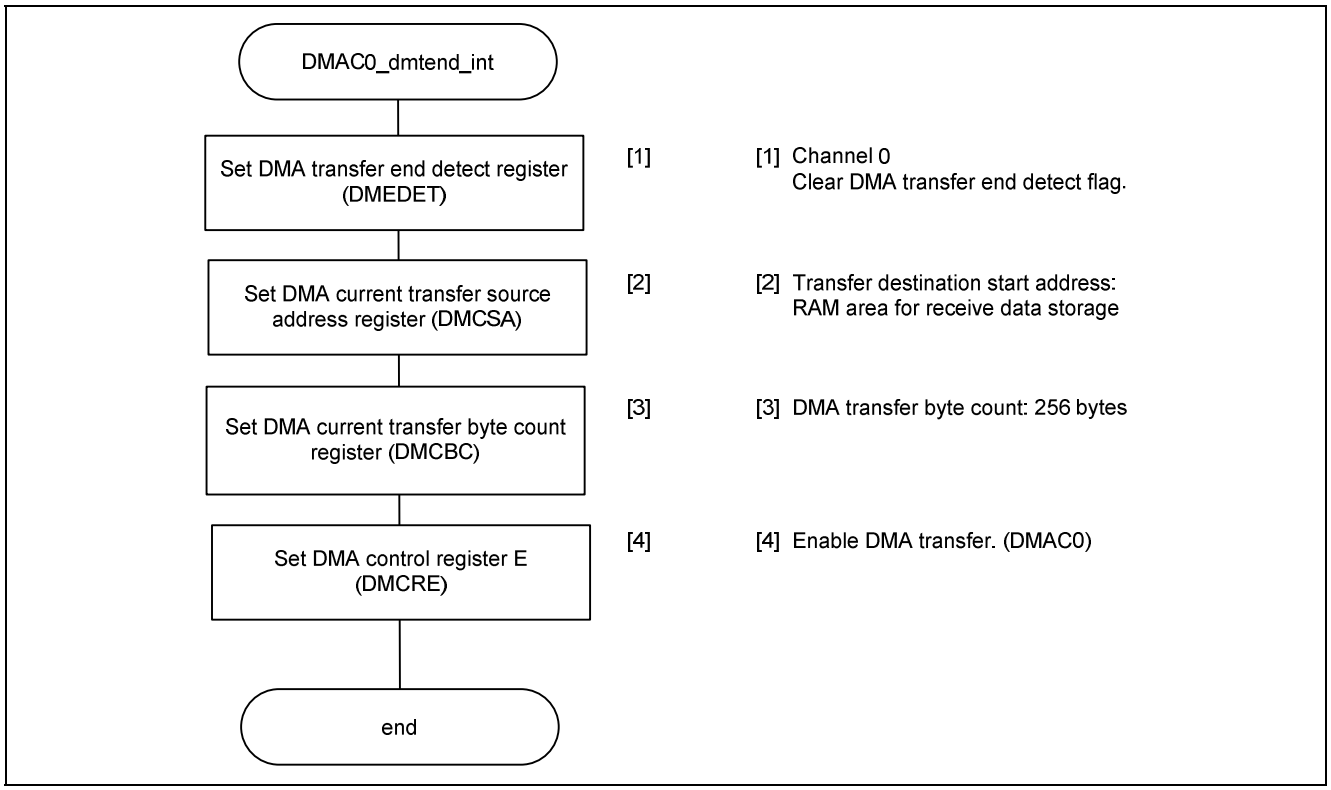

Figure 12 DMAC0 Transfer End Interrupt Handler

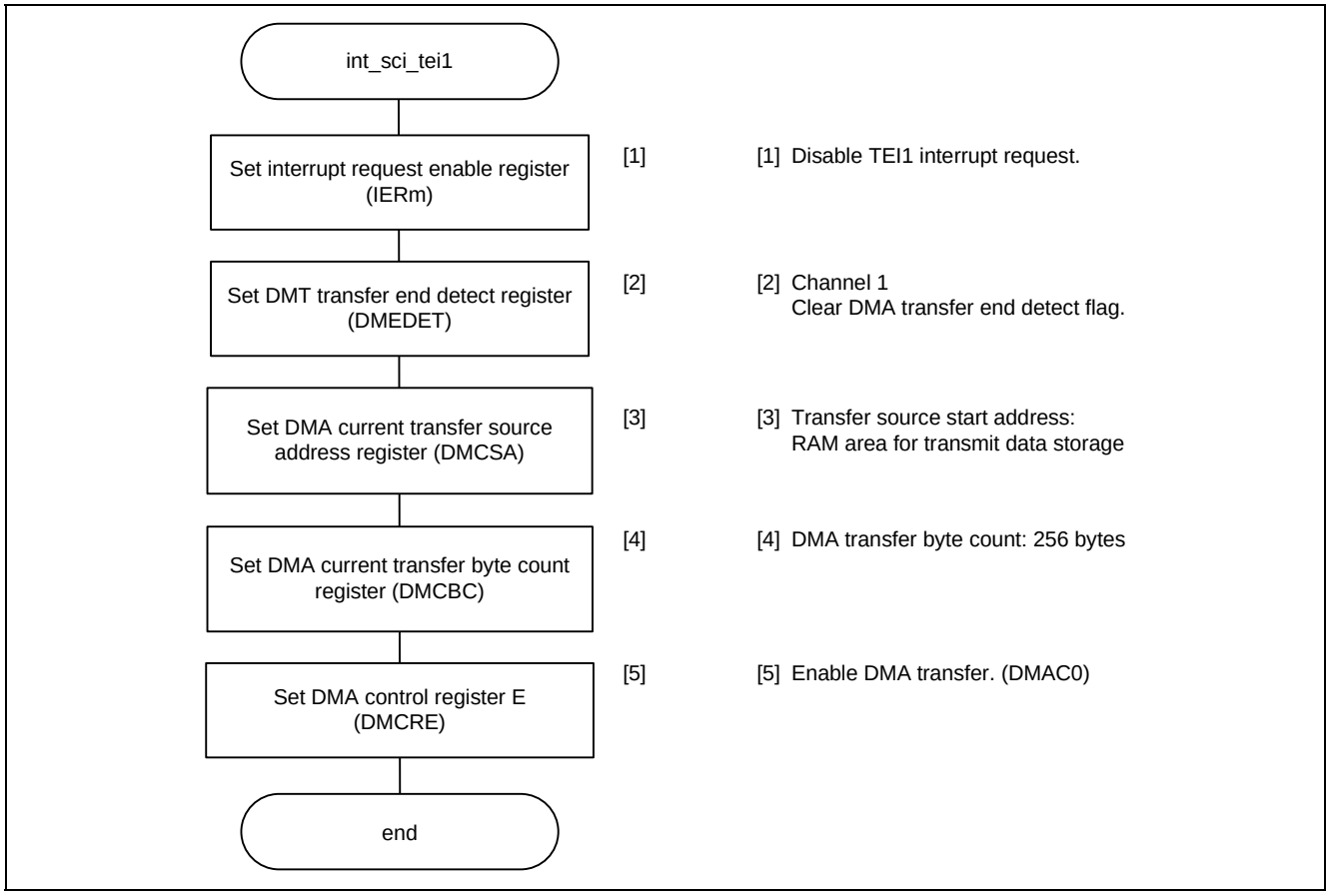

Figure 13 Transmit End Interrupt

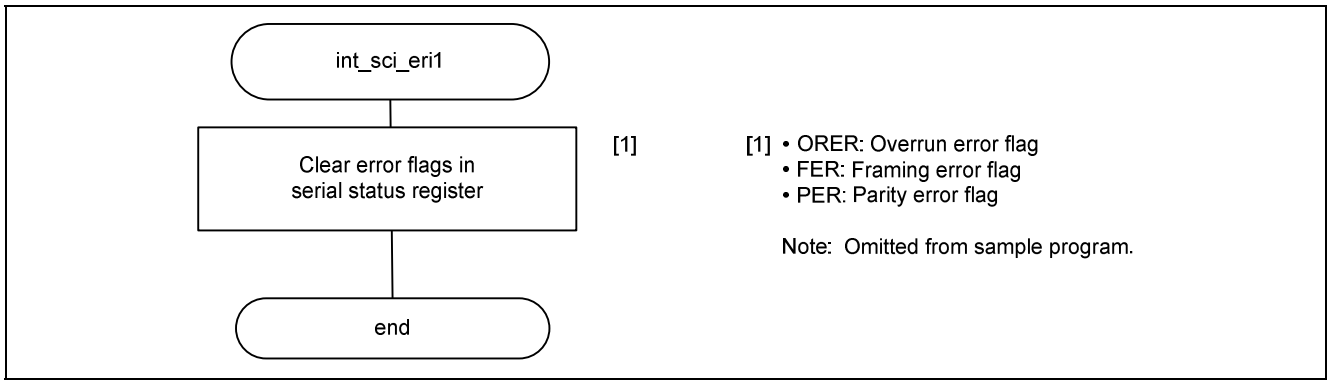

Figure 14 Receive Error Interrupt

5. Verified Operation Environment

Table 7 shows the environment in which operation of the sample program has been verified.

Table 7 Verified Operation Environment

Item	Name
Device	RX610 (R5F56108VNFP)
Board	Evaluation board
Power supply voltage	5.0 V (CPU operating voltage is 3.3 V)
Input clock	12.5 MHz (ICLK = 100 MHz, PCLK = 50 MHz, BCLK = 25 MHz)
Operating temperature	Room temperature
HEW	Version 4.07.00.007
Toolchain	RX Standard Toolchain (V.1.0.0.0) RX Family C/C++ Compile Driver V.1.00.00.001 RX Family C/C++ Compiler V.1.00.00.001 RX Family Assembler V.1.00.00.001 Optimizing Linkage Editor V.10.00.00.001 RX Family C/C++ Standard Library Generator V.1.00.00.001
Debugger	RX E20 SYSTEM V.1.00.00.000

6. Reference Documents

- Hardware Manual
  RX610 Group Hardware Manual
  (The latest version can be downloaded from the Renesas Electronics Web site.)
- Development Environment Manual
  RX Family C/C++ Compiler Package User's Manual
  (The latest version can be downloaded from the Renesas Electronics Web site.)
- Technical Updates
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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Dec.09.10	—	First edition issued

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1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

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