RX210 Group, RX111 Group

Comparison of the RX210 Group and RX111 Group

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Abstract

This document compares the specifications of the following MCUs:

- 64-pin package of the RX210 Group to the 64-pin package of the RX111 Group
- 46-pin package of the RX210 Group to the 48-pin package of the RX111 Group

Products

RX210 Group, RX111 Group

Contents

1. Comparison of Modules and Functions

Table 1.1 lists a Comparison of Modules and Functions in the 64-pin Packages.

Table 1.1 Comparison of Modules and Functions in the 64-pin Packages

No.	Function	RX210 Group	RX111 Group
1	Operating modes	Differing specs	
2	Resets	Differing specs	
3	Option-setting memory	Differing specs	
4	Voltage detection circuit (LVDAa)	Differing specs	
5	Clock generation circuit	Differing specs	
6	Clock frequency accuracy measurement circuit (CAC)	Both	
7	Low power consumption	Differing specs	
8	Register write protection function	Differing specs	
9	Exception handling	Both	
10	Interrupt controller (ICUb)	Differing specs	
11	Buses	Differing specs	
12	DMA controller (DMACA)	Available	N/A
13	Data transfer controller (DTCa)	Both	
14	Event link controller (ELC)	Differing specs	
15	I/O ports	Differing specs	
16	Multi-function pin controller (MPC)	Differing specs	
17	Multi-function timer pulse unit 2 (MTU2a)	Both	
18	Port output enable 2 (POE2a)	Differing specs	
19	8-bit timer (TMR)	Available	N/A
20	Compare match timer (CMT)	Differing specs	
21	Realtime clock (RTCb / RTCA)	Differing specs	
22	Watchdog timer (WDTA)	Available	N/A
23	Independent watchdog timer (IWDTa)	Differing specs	
24	USB 2.0 host/function module (USBc)	N/A	Available
25	Serial communications interface (SCIc, SCId / SCIe, SCIf)	Differing specs	
26	I2C bus interface (RIIC)	Both	
27	Serial peripheral interface (RSPI)	Differing specs	
28	CRC calculator (CRC)	Both	
29	12-bit A/D converter (S12ADb)	Differing specs	
30	D/A converter (DA)	Differing specs	
31	Temperature sensor (TEMPSa)	Differing specs	
32	Comparator A (CMPA)	Available	N/A
33	Comparator B (CMPB)	Available	N/A
34	Data operation circuit (DOC)	Both	
35	RAM	Both	
36	ROM (flash memory for code storage)	Differing specs	
37	E2 DataFlash memory (flash memory for data storage)	Differing specs	

Legend

Both: The module/function is available in both groups.
Available: The module/function is available.
N/A: The module/function is not available.
Differing specs: The module/function is available in both groups, but have differing specifications. Differences in the module/function symbol are written as "Module/Function name (RX210 Group symbol / RX111 Group symbol)".

Table 1.2 lists a Comparison of Modules and Functions in the 48-pin Packages.

Table 1.2 Comparison of Modules and Functions in the 48-pin Packages

No.	Function	RX210 Group	RX111 Group
1	Operating modes	Differing specs	
2	Resets	Differing specs	
3	Option-setting memory	Differing specs	
4	Voltage detection circuit (LVDAa)	Differing specs	
5	Clock generation circuit	Differing specs	
6	Clock frequency accuracy measurement circuit (CAC)	Both	
7	Low power consumption	Differing specs	
8	Register write protection function	Differing specs	
9	Exception handling	Both	
10	Interrupt controller (ICUb)	Differing specs	
11	Buses	Differing specs	
12	DMA controller (DMACA)	Available	N/A
13	Data transfer controller (DTCa)	Both	
14	Event link controller (ELC)	Differing specs	
15	I/O ports	Differing specs	
16	Multi-function pin controller (MPC)	Differing specs	
17	Multi-function timer pulse unit 2 (MTU2a)	Both	
18	Port output enable 2 (POE2a)	Differing specs	
19	8-bit timer (TMR)	Available	N/A
20	Compare match timer (CMT)	Differing specs	
21	Realtime clock (RTCb / RTCA)	N/A	Available
22	Watchdog timer (WDTA)	Available	N/A
23	Independent watchdog timer (IWDTa)	Differing specs	
24	USB 2.0 host/function module (USBc)	N/A	Available
25	Serial communications interface (SCIc, SCId / SCIe, SCIf)	Differing specs	
26	I2C bus interface (RIIC)	Both	
27	Serial peripheral interface (RSPI)	Differing specs	
28	CRC calculator (CRC)	Both	
29	12-bit A/D converter (S12ADb)	Differing specs	
30	D/A converter (DA)	Not available *1	
31	Temperature sensor (TEMPSa)	Differing specs	
32	Comparator A (CMPA)	Available	N/A
33	Comparator B (CMPB)	Available	N/A
34	Data operation circuit (DOC)	Both	
35	RAM	Both	
36	ROM (flash memory for code storage)	Differing specs	
37	E2 DataFlash memory (flash memory for data storage)	Differing specs	

Note 1. Neither of the 48-pin packages comes equipped with a D/A converter.

Legend

Both: The module/function is available in both groups.
Available: The module/function is available.
N/A: The module/function is not available.
Differing specs: The module/function is available in both groups, but have differing specifications. Differences in the module/function symbol are written as "Module/Function name (RX210 Group symbol / RX111 Group symbol)".

2. Comparison of Specifications

Table 2.1 to Table 2.3 list comparisons of specifications. Items in blue indicate that the specification exists in one of the two groups; items in red indicate that the same specification has a difference between the two groups; items in black represent specifications that exist in both groups.

Table 2.1 Comparison of Specifications (1/3)

Item			RX210 Group	RX111 Group
CPU	Maximum operating frequency		50 MHz	32 MHz
Memory	ROM	64-pin	512/384/256/128/96/64 KB	128/96/64/32/16 KB
		48-pin	256/128/96/64 KB	128/96/64/32/16 KB
	RAM	64-pin	64/32/20/16/12 KB	16/10/8 KB
		48-pin	32/20/16/12 KB	16/10/8 KB
	E2 DataFlash		8 KB	8 KB
MCU operating modes			Single-chip mode On-chip ROM enabled extended mode On-chip ROM disabled extended mode (mode switched by software)	Single-chip mode
Clock generation circuits			Main clock oscillator Sub-clock oscillator Low-speed on-chip oscillator High-speed on-chip oscillator PLL frequency synthesizer IWDT-dedicated on-chip oscillator	Main clock oscillator Sub-clock oscillator Low-speed on-chip oscillator High-speed on-chip oscillator PLL frequency synthesizer IWDT-dedicated on-chip oscillator
System clock (ICLK)			50 MHz (max.)	32 MHz (max.)
Peripheral module clock B (PCLKB)			32 MHz (max.)	32 MHz (max.)
Peripheral module clock D (PCLKD)			50 MHz (max.)	32 MHz (max.)
External bus clock (BCLK)			25 MHz (max.)	N/A
Resets			RES# pin reset Power-on reset Voltage monitoring reset Watchdog timer reset Independent watchdog timer reset Deep software standby reset Software reset	RES# pin reset Power-on reset Voltage monitoring reset Independent watchdog timer reset Software reset
Voltage detection			• Voltage detection circuit 0 is capable of selecting the detection voltage from 4 levels • Voltage detection circuit 1 is capable of selecting the detection voltage from 16 levels • Voltage detection circuit 2 is capable of selecting the detection voltage from 16 levels	• Voltage detection circuit 1 is capable of selecting the detection voltage from 10 levels • Voltage detection circuit 2 is capable of selecting the detection voltage from 4 levels

Table 2.2 Comparison of Specifications (2/3)

Item		RX210 Group	RX111 Group
Low power consumption functions		• Module stop function Low power function modes • Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode	• Module stop function Low power function modes • Sleep mode • Deep sleep mode • Software standby mode
Function for lowering operating power consumption		High-speed operating mode Middle-speed operating mode 1A Middle-speed operating mode 1B Middle-speed operating mode 2A *1 Middle-speed operating mode 2B *1 Low-speed operating mode 1 Low-speed operating mode 2	High-speed operating mode Middle-speed operating mode Low-speed operating mode
Interrupt vectors		167	82
Non-maskable interrupts		NMI pin interrupt Oscillation stop detection interrupt Voltage monitoring 1 interrupt Voltage monitoring 2 interrupt WDT interrupt IWDT interrupt	NMI pin interrupt Oscillation stop detection interrupt Voltage monitoring 1 interrupt Voltage monitoring 2 interrupt IWDT interrupt
External pin interrupts	64-pin	7 channels (IRQ0 to IRQ2, IRQ4 to IRQ7)	8 channels (IRQ0 to IRQ7)
	48-pin	6 channels (IRQ0, IRQ1, IRQ4 to IRQ7)	8 channels (IRQ0 to IRQ7)
External bus extension		N/A	N/A
DMACA		Available	N/A
DTCa		Available	Available
General I/O ports	64-pin	I/O: 48 ports Pull-up resistors: 48 ports Open-drain output: 35 ports 5-V tolerance: 2 ports	I/O: 46 ports Pull-up resistors: 38 ports Open-drain output: 34 ports 5-V tolerance: 4 ports
	48-pin	I/O: 34 ports Pull-up resistors: 34 ports Open-drain output: 26 ports 5-V tolerance: 2 ports	I/O: 30 ports Pull-up resistors: 24 ports Open-drain output: 24 ports 5-V tolerance: 4 ports
ELC		• Event signals of 59 types can be directly connected to the module • Capable of event link operation for ports B and E	• Event signals of 36 types can be directly connected to the module • Capable of event link operation for port B
TMR		Available	N/A
CMT		2 channels × 2 units	2 channels × 1 unit
RTCb: RX210 RTCA: RX111	64-pin	Available	Available
	48-pin	N/A	Available
WDTA		Available	N/A
SCIc: RX210 SCIe: RX111	64-pin	6 channels (SCI1, SCI5, SCI6, SCI8, SCI9, SCI12)	3 channels (SCI1, SCI5, SCI12)
	48-pin	5 channels (SCI1, SCI5, SCI6, SCI8, SCI12)	3 channels (SCI1, SCI5, SCI12)
RSPI	64-pin	1 channel	1 channel
	48-pin	1 channel	1 channel (SSLA1 and SSLA3 are not supported)

Note 1. This mode only exists in chip version B. It does not exist in chip version C.

Table 2.3 Comparison of Specifications (3/3)

Item		RX210 Group	RX111 Group
USBc		N/A	Available
S12ADb	64-pin	12 channels (AN000 to AN004, AN006, AN008 to AN013)	14 channels (AN000 to AN004, AN006, AN008 to AN015) 6 high-precision channels
	48-pin	8 channels (AN000 to AN002, AN006, AN009 to AN012)	10 channels (AN000 to AN002, AN006, AN008 to AN012, AN015) 4 high-precision channels
		Sample-and-hold function Channel-dedicated sample-and-hold function Variable sampling state count Self-diagnosis function A/D-converted value addition mode Analog input disconnection detection assist Double trigger mode	Variable sampling state count A/D-converted value addition mode Double trigger mode
TEMPSa		• 1 channel • PGA gain switchable: Four levels according to the voltage range	• 1 channel
DA	64-pin	2 channels	2 channels
	48-pin	N/A	N/A
		Resolution: 10 bits	Resolution: 8 bits
CRC		Available	Available
CMPA		• 2 channels (CMPA1, CMPA2) • Reference input voltage Input voltage to the CVREFA pin • Digital filter supported	• 1 channel (CMPA2) • Reference input voltage Internal reference voltage • Digital filter not supported
CMPB		Available	N/A
Power supply voltage/Operating frequency		VCC = 1.62 to 1.8 V: 20 MHz VCC = 1.8 to 2.7 V: 32 MHz VCC = 2.7 to 5.5 V: 50 MHz	VCC = 1.8 to 2.4 V: 8 MHz VCC = 2.4 to 2.7 V: 16 MHz VCC = 2.7 to 3.6 V: 32 MHz

3. Comparison of Pin Functions

Table 3.1 and Table 3.2 list comparisons of pin functions in the 64-pin packages, and Table 3.3 and Table 3.4 list comparisons of pin functions in the 48-pin packages. Items in blue indicate that the specification exists in one of the two groups.

Table 3.1 Comparison of Pin Functions in the 64-pin Packages (1/2)

I/O Port	RX210 Group	RX111 Group
P03	DA0	DA0
P05	DA1	DA1
P14	IRQ4, MTIOC3A, MTCLKA, TMRI2, CTS1#/RTS1#/SS1#	IRQ4, MTIOC3A, MTCLKA, MTIOC0A, CTS1#/RTS1#/SS1#, TXD12/SMOSI12/SSDA12/TXDX12/SIOX12, SSLA0, USB0_OVRCURA
P15	IRQ5, MTIOC0B, MTCLKB, TMCI2, RXD1/SMISO1/SSCL1	IRQ5, MTIOC0B, MTCLKB, RSPCKA, CLKOUT, RXD1/SMISO1/SSCL1
P16	IRQ6, MTIOC3C, MTIOC3D, TMO2, ADTRG0#, TXD1/SMOSI1/SSDA1, MOSIA, SCL-DS	IRQ6, MTIOC3C, MTIOC3D, RTCOUT, ADTRG0#, TXD1/SMOSI1/SSDA1, MOSIA, SCL0, USB0_VBUSEN, USB0_VBUS, USB0_OVRCURB
P17	IRQ7, MTIOC3A, MTIOC3B, TMO1, POE8#, SCK1, MISOA, SDA-DS	IRQ7, MTIOC3A, MTIOC3B, MTIOC0C, POE8#, SCK1, RXD12/SMISO12/SSCL12/RXDX12, MISOA, SDA0
P26	MTIOC2A, TMO1, TXD1/SMOSI1/SSDA1	MTIOC2A, TXD1/SMOSI1/SSDA1, USB0_VBUSEN
P27	MTIOC2B, TMCI3, SCK1	IRQ3, CMPA2, MTIOC2B, CACREF, ADTRG0#, SCK1, SCK12
P30	IRQ0-DS, MTIOC4B, TMRI3, POE8#, RTCIC0, RXD1/SMISO1/SSCL1	IRQ0, MTIOC4B, POE8#, RXD1/SMISO1/SSCL1
P31	IRQ1-DS, RTCIC1, MTIOC4D, TMCI2, CTS1#/RTS1#/SS1#	IRQ1, MTIOC4D, CTS1#/RTS1#/SS1#
P32	IRQ2-DS, RTCIC2, MTIOC0C, TMO3, RTCOUT, TXD6/SMOSI6/SSDA6	IRQ2, MTIOC0C, RTCOUT
P35	NMI	NMI
P40	AN000	AN000
P41	AN001	AN001
P42	AN002	AN002
P43	AN003	AN003
P44	AN004	AN004
P46	AN006	AN006
P54	MTIOC4B, TMCI1	MTIOC4B
P55	MTIOC4D, TMO3	MTIOC4D
PA0	MTIOC4A, CACREF, SSLA1	MTIOC4A, CACREF, SSLA1
PA1	CVREFA, MTIOC0B, MTCLKC, SCK5, SSLA2	MTIOC0B, MTCLKC, RTCOUT, SCK5, SSLA2
PA3	IRQ6-DS, MTIOC0D, MTCLKD, CMPB1, RXD5/SMISO5/SSCL5	IRQ6, MTIOC0D, MTCLKD, MTIOC1B, POE0#, RXD5/SMISO5/SSCL5, MISOA
PA4	IRQ5-DS, CVREFB1, MTIC5U, MTCLKA, TMRI0, TXD5/SMOSI5/SSDA5, SSLA0	IRQ5, MTIC5U, MTCLKA, MTIOC2B, TXD5/SMOSI5/SSDA5, SSLA0

Table 3.2 Comparison of Pin Functions in the 64-pin Packages (2/2)

I/O Port	RX210 Group	RX111 Group
PA6	MTIC5V, MTCLKB, TMCI3, POE2#, CTS5#/RTS5#/SS5#, MOSIA	IRQ3, MTIC5V, MTCLKB, MTIOC2A, POE2#, CTS5#/RTS5#/SS5#, MOSIA, SDA0
PB0	MTIC5W, RXD6/SMISO6/SSCL6, RSPCKA	IRQ2, MTIC5W, MTIOC0C, RTCOUT, ADTRG0#, RSPCKA, SCL0
PB1	IRQ4-DS, MTIOC0C, MTIOC4C, TMCI0, TXD6/SMOSI6/SSDA6	IRQ4, MTIOC0C, MTIOC4C
PB3	MTIOC0A, MTIOC4A, TMO0, POE3#, SCK6	MTIOC0A, MTIOC4A, MTIOC3B, POE3#, USB0_OVRCURA
PB5	MTIOC2A, MTIOC1B, TMRI1, POE1#, SCK9	MTIOC2A, MTIOC1B, POE1#
PB6	MTIOC3D, RXD9/SMISO9/SSCL9	MTIOC3D
PB7	MTIOC3B, TXD9/SMOSI9/SSDA9	MTIOC3B
PC2	MTIOC4B, RXD5/SMISO5/SSCL5, SSLA3	MTIOC4B, RXD5/SMISO5/SSCL5, SSLA3
PC3	MTIOC4D, TXD5/SMOSI5/SSDA5	MTIOC4D, TXD5/SMOSI5/SSDA5
PC4	MTIOC3D, MTCLKC, TMCI1, POE0#, SCK5, CTS8#/RTS8#/SS8#, SSLA0	IRQ2, MTIOC3D, MTCLKC, POE0#, CLKOUT, SCK5, SSLA0, USB0_VBUSEN, USB0_VBUS
PC5	MTIOC3B, MTCLKD, TMRI2, SCK8, RSPCKA	MTIOC3B, MTCLKD, SCK1, RSPCKA, USB0_ID
PC6	MTIOC3C, MTCLKA, TMCI2, RXD8/SMISO8/SSCL8, MOSIA	MTIOC3C, MTCLKA, RXD1/SMISO1/SSCL1, MOSIA, USB0_EXICEN
PC7	MTIOC3A, MTCLKB, TMO2, CACREF, TXD8/SMOSI8/SSDA8, MISOA	MTIOC3A, MTCLKB, CACREF, TXD1/SMOSI1/SSDA1, MISOA, USB0_OVRCURB
PE0	AN008, SCK12	IRQ0, AN008, MTIOC2A, POE3#, SCK12
PE1	AN009, CMPB0, MTIOC4C, TXD12/SMOSI12/SSDA12/TXDX12/SIOX12	IRQ1, AN009, MTIOC4C, TXD12/SMOSI12/SSDA12/TXDX12/SIOX12
PE2	IRQ7-DS, AN010, CVREFB0, MTIOC4A, RXD12/SMISO12/SSCL12/RXDX12	IRQ7, AN010, MTIOC4A, RXD12/SMISO12/SSCL12/RXDX12
PE3	AN011, CMPA1, MTIOC4B, POE8#, CTS12#/RTS12#/SS12#	IRQ3, AN011, MTIOC4B, MTIOC1B, MTIOC0A, POE8#, CTS12#/RTS12#/SS12#, RSPCKA
PE4	AN012, CMPA2, MTIOC4D, MTIOC1A	IRQ4, AN012, MTIOC4D, MTIOC1A, MTIOC3A, MOSIA
PE5	IRQ5, AN013, MTIOC4C, MTIOC2B	IRQ5, AN013, MTIOC4C, MTIOC2B
PE6	—	IRQ6, AN014
PE7	—	IRQ7, AN015
PH0	CACREF	—
PH1	IRQ0, TMO0	—
PH2	IRQ1, TMRI0	—
PH3	TMCI0	—
PJ6	—	VREFH0/AVCC0
PJ7	—	VREFL0/AVSS0

Table 3.3 Comparison of Pin Functions in the 48-pin Packages (1/2)

I/O Port	RX210 Group	RX111 Group
P14	IRQ4, MTIOC3A, MTCLKA, TMRI2, CTS1#/RTS1#/SS1#	IRQ4, MTIOC3A, MTCLKA, MTIOC0A, CTS1#/RTS1#/SS1#, TXD12/SMOSI12/SSDA12/TXDX12/SIOX12, SSLA0, USB0_OVRCURA
P15	IRQ5, MTIOC0B, MTCLKB, TMCI2, RXD1/SMISO1/SSCL1	IRQ5, MTIOC0B, MTCLKB, RSPCKA, CLKOUT, RXD1/SMISO1/SSCL1
P16	IRQ6, MTIOC3C, MTIOC3D, TMO2, RTCOUT, ADTRG0#, TXD1/SMOSI1/SSDA1, MOSIA, SCL-DS	IRQ6, MTIOC3C, MTIOC3D, RTCOUT, ADTRG0#, TXD1/SMOSI1/SSDA1, MOSIA, SCL0, USB0_VBUSEN, USB0_VBUS, USB0_OVRCURB
P17	IRQ7, MTIOC3A, MTIOC3B, TMO1, POE8#, SCK1, MISOA, SDA-DS	IRQ7, MTIOC3A, MTIOC3B, MTIOC0C, POE8#, SCK1, RXD12/SMISO12/SSCL12/RXDX12, MISOA, SDA0
P26	MTIOC2A, TMO1, TXD1/SMOSI1/SSDA1	MTIOC2A, TXD1/SMOSI1/SSDA1, USB0_VBUSEN
P27	MTIOC2B, TMCI3, SCK1	IRQ3, CMPA2, MTIOC2B, CACREF, ADTRG0#, SCK1, SCK12
P30	IRQ0-DS, MTIOC4B, TMRI3, POE8#, RXD1/SMISO1/SSCL1	—
P31	IRQ1-DS, MTIOC4D, TMCI2, CTS1#/RTS1#/SS1#	—
P35	NMI	NMI
P40	AN000	AN000
P41	AN001	AN001
P42	AN002	AN002
P46	AN006	AN006
PA1	CVREFA, MTIOC0B, MTCLKC, SCK5, SSLA2	MTIOC0B, MTCLKC, RTCOUT, SCK5, SSLA2
PA3	IRQ6-DS, CMPB1, MTIOC0D, MTCLKD, RXD5/SMISO5/SSCL5	IRQ6, MTIOC0D, MTCLKD, MTIOC1B, POE0#, RXD5/SMISO5/SSCL5, MISOA
PA4	IRQ5-DS, CVREFB1, MTIC5U, MTCLKA, TMRI0, TXD5/SMOSI5/SSDA5, SSLA0	IRQ5, MTIC5U, MTCLKA, MTIOC2B, TXD5/SMOSI5/SSDA5, SSLA0
PA6	MTIC5V, MTCLKB, TMCI3, POE2#, CTS5#/RTS5#/SS5#, MOSIA	IRQ3, MTIC5V, MTCLKB, MTIOC2A, POE2#, CTS5#/RTS5#/SS5#, MOSIA, SDA0
PB0	MTIC5W, RXD6/SMISO6/SSCL6, RSPCKA	IRQ2, MTIC5W, MTIOC0C, RTCOUT, ADTRG0#, RSPCKA, SCL0
PB1	IRQ4-DS, MTIOC0C, MTIOC4C, TMCI0, TXD6/SMOSI6/SSDA6	IRQ4, MTIOC0C, MTIOC4C
PB3	MTIOC0A, MTIOC4A, TMO0, POE3#, SCK6	MTIOC0A, MTIOC4A, MTIOC3B, POE3#, USB0_OVRCURA
PB5	MTIOC2A, MTIOC1B, TMRI1, POE1#	MTIOC2A, MTIOC1B, POE1#
PC4	MTIOC3D, MTCLKC, TMCI1, POE0#, SCK5, CTS8#/RTS8#/SS8#, SSLA0	IRQ2, MTIOC3D, MTCLKC, POE0#, CLKOUT, SCK5, SSLA0, USB0_VBUSEN, USB0_VBUS
PC5	MTIOC3B, MTCLKD, TMRI2, SCK8, RSPCKA	MTIOC3B, MTCLKD, SCK1, RSPCKA, USB0_ID
PC6	MTIOC3C, MTCLKA, TMCI2, RXD8/SMISO8/SSCL8, MOSIA	MTIOC3C, MTCLKA, RXD1/SMISO1/SSCL1, MOSIA, USB0_EXICEN

Table 3.4 Comparison of Pin Functions in the 48-pin Packages (2/2)

I/O Port	RX210 Group	RX111 Group
PC7	MTIOC3A, MTCLKB, TMO2, CACREF, TXD8/SMOSI8/SSDA8, MISOA	MTIOC3A, MTCLKB, CACREF, TXD1/SMOSI1/SSDA1, MISOA, USB0_OVRCURB
PE0	—	IRQ0, AN008, MTIOC2A, POE3#, SCK12
PE1	AN009, CMPB0, MTIOC4C, TXD12/SSDA12/TXDX12/SIOX12	IRQ1, AN009, MTIOC4C, TXD12/SSDA12/TXDX12/SIOX12
PE2	IRQ7-DS, AN010, CVREFB0, MTIOC4A, RXD12/SSCL12/RXDX12	IRQ7, AN010, MTIOC4A, RXD12/SSCL12/RXDX12
PE3	AN011, CMPA1, MTIOC4B, POE8#, CTS12#/RTS12#	IRQ3, AN011, MTIOC4B, MTIOC1B, MTIOC0A, POE8#, CTS12#/RTS12#/, RSPCKA
PE4	AN012, CMPA2, MTIOC4D, MTIOC1A	IRQ4, AN012, MTIOC4D, MTIOC1A, MTIOC3A, MOSIA
PH0	CACREF	—
PE7	—	IRQ7, AN015
PH1	IRQ0, TMO0	—
PH2	IRQ1, TMRI0	—
PH3	TMCI0	—
PJ6	—	VREFH0/AVCC0
PJ7	—	VREFL0/AVSS0

4. Comparison of Specification Details

The tables in this chapter list detailed comparisons of specifications. In this chapter, items in blue indicate that the specification exists in one of the two groups; items in red indicate that the same specification has a difference between the two groups. Specifications with no differences between groups are not listed.

4.1 Comparison of Operating Modes

Table 4.1 lists a Comparison of Operating Modes. Table 4.2 lists a Comparison of I/O Registers Associated With the Operating Modes.

Table 4.1 Comparison of Operating Modes

Item	RX210 Group	RX111 Group
Operating modes	• Single-chip mode • Boot mode Uses the SCI • User boot mode • On-chip ROM enabled extended mode • On-chip ROM disabled extended mode	• Single-chip mode • Boot mode SCI USB interface
Mode setting pins	MD, PC7	MD, UB#

Table 4.2 Comparison of I/O Registers Associated With the Operating Modes

Register Symbol	Bit Symbol	RX210 Group	RX111 Group
MDSR	—	Mode status register	No register
SYSCR0	—	System control register 0	No register

4.2 Comparison of Resets

Table 4.3 lists a Comparison of Resets. Table 4.4 lists a Comparison of I/O Registers Associated With the Resets.

Table 4.3 Comparison of Resets

Item	RX210 Group	RX111 Group
Resets	RES# pin reset Power-on reset Voltage monitoring 0 reset Voltage monitoring 1 reset Voltage monitoring 2 reset Deep software standby reset Independent watchdog timer reset Watchdog timer reset Software reset	RES# pin reset Power-on reset Voltage monitoring 1 reset Voltage monitoring 2 reset Independent watchdog timer reset Software reset

Table 4.4 Comparison of I/O Registers Associated With the Resets

Register Symbol	Bit Symbol	RX210 Group	RX111 Group
RSTSR0	LVD0RF	Voltage monitoring 0 reset detect flag	Reserved
	DPSRSTF	Deep software standby reset detect flag	Reserved
RSTSR2	WDTRF	Watchdog timer reset detect flag	Reserved

4.3 Comparison of the Option-Setting Memory

Table 4.5 lists a Comparison of the Option-Setting Memory.

Table 4.5 Comparison of the Option-Setting Memory

Item	RX210 Group	RX111 Group
User boot mode associated	UB code A, UB code B	N/A

4.4 Comparison of LVDA

Table 4.6 lists a Comparison of LVDA. Table 4.7 and Table 4.8 list comparisons of I/O registers associated with LVDA.

Table 4.6 Comparison of LVDA

Item		RX210 Group	RX111 Group
Voltage monitoring 0		Selectable from 4 levels	N/A
Voltage monitoring 1	Monitored voltage	Selectable from 16 levels	Selectable from 10 levels
Voltage monitoring 2	Monitored voltage	Selectable from 16 levels (Varies according to whether VCC or the CMPA2 pin is selected)	Selectable from 4 levels
Digital filter		Voltage monitoring 1, voltage monitoring 2	N/A
CMPA		• 2 channels (CMPA1, CMPA2) • Reference input voltage Input voltage to the CVREFA pin • Digital filter function switching available	• 1 channel (CMPA2) • Reference input voltage Internal reference voltage
Event link function (output)		Vdet1 and Vdet2 passage detection event output	Vdet1 passage detection event output

Table 4.7 Comparison of I/O Registers Associated With LVDA (1/2)

Register Symbol	Bit Symbol	RX210 Group	RX111 Group
LVCMPCR	EXVREFINP1	Comparator A1 reference voltage external input select	Reserved
	EXVCCINP1	Comparator A1 comparison voltage external input select	Reserved
	EXVREFINP2	Comparator A2 comparison voltage external input select	Reserved
LVDLVLR	LVD1LVL[3:0]	Voltage detection 1 level select (standard voltage during drop in voltage) 0000: 4.15 V 0001: 4.00 V 0010: 3.85 V 0011: 3.70 V 0100: 3.55 V 0101: 3.40 V 0110: 3.25 V 0111: 3.10 V 1000: 2.95 V 1001: 2.80 V 1010: 2.65 V 1011: 2.50 V 1100: 2.35 V 1101: 2.20 V 1110: 2.05 V 1111: 1.90 V	Voltage detection 1 level select (standard voltage during drop in voltage) 0101: 3.00 V 0110: 2.90 V 0111: 2.79 V 1000: 2.68 V 1001: 2.58 V 1010: 2.48 V 1011: 2.06 V 1100: 1.96 V 1101: 1.86 V

Table 4.8 Comparison of I/O Registers Associated With LVDA (2/2)

Register Symbol	Bit Symbol	RX210 Group	RX111 Group
LVDLVLR	LVD2LVL[3:0] (RX210) LVD2LVL[1:0] (RX111)	Voltage detection 2 level select (standard voltage during drop in voltage) (When LVCMPCR.EXVCCINP2 = 0 (VCC select)) 0000: 4.15 V 0001: 4.00 V 0010: 3.85 V 0011: 3.70 V 0100: 3.55 V 0101: 3.40 V 0110: 3.25 V 0111: 3.10 V 1000: 2.95 V 1001: 2.80 V 1010: 2.65 V 1011: 2.50 V 1100: 2.35 V 1101: 2.20 V 1110: 2.05 V 1111: 1.90 V (When LVCMPCR.EXVCCINP2 = 1 (CMPA2 pin select)) 0001: 1.33 V	Voltage detection 2 level select (standard voltage during drop in voltage) 00: 2.90 V 01: 2.60 V 10: 2.00 V 11: 1.80 V
LVD1CR0	LVD1DFDIS	Voltage monitoring 1/comparator A1 digital filter disable mode select	Reserved
	LVD1FSAMP[1:0]	Sampling clock select	Reserved
LVD2CR0	LVD2DFDIS	Voltage monitoring 2/comparator A2 digital filter disable mode select	Reserved
	LVD2FSAMP[1:0]	Sampling clock select	Reserved

4.5 Comparison of the Clock Generation Circuits

Table 4.9 lists a Comparison of Clock Generation Circuits, and Table 4.10 lists a Comparison of I/O Registers Associated With Clock Generation Circuits.

Table 4.9 Comparison of Clock Generation Circuits

Item	RX210 Group	RX111 Group
Uses	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, ROM, and RAM. • Generates the external bus clock (BCLK) to be supplied to the external bus.	• Generates the system clock (ICLK) to be supplied to the CPU, DTC, ROM, and RAM. • Generates the USB clock (UCLK) to be supplied to the USB.
Operating frequencies	ICLK: 50 MHz (max.) PCLKB: 32 MHz (max.) PCLKD: 50 MHz (max.) FCLK: 4 to 32 MHz (max.) BCLK: 25 MHz (max.) BCLK pin output: 12.5 MHz (max.) IWDTCLK: 125 kHz	ICLK: 32 MHz (max.) PCLKB: 32 MHz (max.) PCLKD: 32 MHz (max.) FCLK: 1 to 32 MHz (max.) UCLK: 48 MHz IWDTCLK: 15 kHz
Main clock oscillator	1 to 20 MHz	1 to 20 MHz (VCC ≥ 2.4 V), 1 to 8 MHz (VCC < 2.4 V)
PLL circuit	• Input frequency: 4 to 12.5 MHz • Frequency multiplication ratio: Selectable from 8, 10, 12, 16, 20, 24, and 25 • VCO oscillation frequency: 50 to 100 MHz	• Input frequency: 4 to 8 MHz • Frequency multiplication ratio: Selectable from 6 and 8 • VCO oscillation frequency: 32 to 48 MHz (VCC ≥ 2.4 V)
High-speed on-chip oscillator (HOCO)	• Oscillation frequencies: 32, 36.864, 40, or 50 MHz • HOCO power supply control	• Oscillation frequency: 32 MHz
Low-speed on-chip oscillator (LOCO)	125 kHz	4 MHz
IWDT-dedicated on-chip oscillator	125 kHz	15 kHz
Control of output on the BCLK pin	• BCLK output or high-level output is selectable • BCLK or BCLK/2 is selectable	N/A
HOCO oscillation stabilization wait time setting	Set in the HOCOWTCR2 register	Set in the HOCOWTCR register

Table 4.10 Comparison of I/O Registers Associated With Clock Generation Circuits

Register Symbol	Bit Symbol	RX210 Group	RX111 Group
SCKCR	BCK[3:0]	External bus clock (BCLK) select	Reserved
	PSTOP1	BCLK pin output control	Reserved
VRCR	—	Voltage regulator control register	No register
PLLCR	STC[4:0] (RX210) STC[5:0] (RX111)	Frequency multiplication factor select 00111: ×8 01001: ×10 01011: ×12 01111: ×16 10011: ×20 10111: ×24 11000: ×25	Frequency multiplication factor select 001011: ×6 001111: ×8
BCKCR	—	External bus clock control register	No register
HOCOCR2	—	High-speed on-chip oscillator control register 2	No register
MOFCR	MODRV[2:0]	Main clock oscillator drive capability switch	Reserved
	MODRV2[1:0] (RX210) MODRV21 (RX111)	Main clock oscillator drive capability switch 2 01: 1 MHz to 8 MHz 10: 8.1 MHz to 15.9 MHz 11: 16 MHz to 20 MHz	Main clock oscillator drive capability switch VCC ≥ 2.4 V 0: 1 MHz to 10 MHz 1: 10 MHz to 20 MHz VCC < 2.4 V 0: 1 MHz to 8 MHz 1: Setting prohibited
HOCOPCR	—	High-speed on-chip oscillator power supply control register	No register
PLLPCR	—	PLL power control register	No register
OSCOVFSR	—	No register	Oscillation stabilization flag register
CKOCR	—	No register	CLKOUT output control register
HOCOWTCR	—	No register	High-speed on-chip oscillator wait control register

4.6 Comparison of the Low Power Consumption Functions

Table 4.11 lists a Comparison of the Low Power Consumption Functions. Table 4.12 to Table 4.14 list comparisons of I/O registers associated with the low power consumption functions.

Table 4.11 Comparison of the Low Power Consumption Functions

Item	RX210 Group	RX111 Group
Reducing power consumption by switching clock signals	The frequency division ratio is settable independently for the system clock (ICLK), peripheral module clock (PCLKB), S12AD clock (PCLKD), external bus clock (BCLK), and flash interface clock (FCLK).	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKB), S12AD clock (PCLKD), and flash interface clock (FCLK).
BCLK output control function	BCLK output or high-level output can be selected.	N/A
Low power consumption modes	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode	• Sleep mode • Deep sleep mode • Software standby mode
Main clock oscillator	Seven operating power control modes are available High-speed operating mode Middle-speed operating mode 1A Middle-speed operating mode 1B Middle-speed operating mode 2A *1 Middle-speed operating mode 2B *1 Low-speed operating mode 1 Low-speed operating mode 2	Three operating power control modes are available High-speed operating mode Middle-speed operating mode Low-speed operating mode

Note 1. These modes are only available in chip version B. They are not available in chip version C.

Table 4.12 Comparison of I/O Registers Associated With the Low Power Consumption Functions (1/3)

Register Symbol	Bit Symbol	RX210 Group	RX111 Group
SBYCR	OPE	Output port enable	Reserved
	SSBY	Software standby 0: Shifts to sleep mode or all-module clock stop mode after the WAIT instruction is executed 1: Shifts to software standby mode after the WAIT instruction is executed	Software standby 0: Set entry to sleep mode or deep sleep mode after the WAIT instruction is executed 1: Set entry to software standby mode after the WAIT instruction is executed
MSTPCRA	MSTPA4	8-bit timer 3/2 (unit 1) module stop	Reserved
	MSTPA5	8-bit timer 1/0 (unit 0) module stop	Reserved
	MSTPA13	16-bit timer pulse unit module stop	Reserved
	MSTPA14	Compare match timer (unit 1) module stop	Reserved
	MSTPA24	Module stop A24	Reserved
	MSTPA27	Module stop A27	Reserved
	MSTPA28	Target module: DMAC/DTC	Target module: DTC
	MSTPA29	Module stop A29	Reserved
	ACSE	All-module clock stop mode enable	Reserved

Table 4.13 Comparison of I/O Registers Associated With the Low Power Consumption Functions (2/3)

Register Symbol	Bit Symbol	RX210 Group	RX111 Group
MSTPCRB	MSTPB8	Temperature sensor module stop	Reserved
	MSTPB10	Comparator B module stop	Reserved
	MSTPB19	Reserved	USB0 module stop
	MSTPB24	Serial communication interface 7 module stop	Reserved
	MSTPB25	Serial communication interface 6 module stop	Reserved
	MSTPB27	Serial communication interface 4 module stop	Reserved
	MSTPB28	Serial communication interface 3 module stop	Reserved
	MSTPB29	Serial communication interface 2 module stop	Reserved
	MSTPB31	Serial communication interface 0 module stop	Reserved
MSTPCRC	MSTPC1	RAM1 module stop	Reserved
	MSTPC24	Serial communication interface 11 module stop	Reserved
	MSTPC25	Serial communication interface 10 module stop	Reserved
	MSTPC26	Serial communication interface 9 module stop	Reserved
	MSTPC27	Serial communication interface 8 module stop	Reserved
	DSLPE	Reserved	Deep sleep mode enable
OPCCR	OPCM[2:0]	Operating power control mode select 000: High-speed operating mode 010: Middle-speed operating mode 1A 011: Middle-speed operating mode 1B 100: Middle-speed operating mode 2A 101: Middle-speed operating mode 2B 110: Low-speed operating mode 1 111: Low-speed operating mode 2	Operating power control mode select 000: High-speed operating mode 010: Middle-speed operating mode
SOPCCR	—	No register	Sub operating power control register
RSTCKCR	RSTCKSEL[2:0]	Sleep mode return clock source select 001: HOCO is selected 010: Main clock oscillator is selected	Sleep mode return clock source select 000: LOCO is selected 001: HOCO is selected 010: Main clock oscillator is selected

Table 4.14 Comparison of I/O Registers Associated With the Low Power Consumption Functions (3/3)

Register Symbol	Bit Symbol	RX210 Group	RX111 Group
MOSCWTCR	MSTS[4:0]	Main clock oscillator wait time select 00000: Wait time = 2 cycles 00001: Wait time = 4 cycles 00010: Wait time = 8 cycles 00011: Wait time = 16 cycles 00100: Wait time = 32 cycles 00101: Wait time = 256 cycles 00110: Wait time = 512 cycles 00111: Wait time = 1024 cycles 01000: Wait time = 2048 cycles 01001: Wait time = 4096 cycles 01010: Wait time = 16384 cycles 01011: Wait time = 32768 cycles 01100: Wait time = 65536 cycles 01101: Wait time = 131072 cycles 01110: Wait time = 262144 cycles 01111: Wait time = 524288 cycles	Main clock oscillator wait time 00000: Wait time = 2 cycles 00001: Wait time = 1024 cycles 00010: Wait time = 2048 cycles 00011: Wait time = 4096 cycles 00100: Wait time = 8192 cycles 00101: Wait time = 16384 cycles 00110: Wait time = 32768 cycles 00111: Wait time = 65536 cycles
SOSCWTCR	—	Sub-clock oscillator wait control register	No register
PLLWTCR	—	PLL wait control register	No register
HOCOWTCR2	—	HOCO wait control register 2	No register
DPSBYCR	—	Deep standby control register	No register
DPSIER0	—	Deep standby interrupt enable register 0	No register
DPSIER2	—	Deep standby interrupt enable register 2	No register
DPSIFR0	—	Deep standby interrupt flag register 0	No register
DPSIFR2	—	Deep standby interrupt flag register 2	No register
DPSIEGR0	—	Deep standby interrupt edge register 0	No register
DPSIEGR2	—	Deep standby interrupt edge register 2	No register
FHSSBYCR	—	Flash HOCO software standby control register	No register
DPSBKRy (y = 0 to 31)	—	Deep standby backup register	No register

4.7 Comparison of the Register Write Protection Functions

Table 4.15 lists a Comparison of the Register Write Protection Function.

Table 4.15 Comparison of the Register Write Protection Functions

Item	RX210 Group	RX111 Group
PRC0 bit	• Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, HOCOCR2	• Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, CKOCR
PRC1 bit	• Registers related to the operating modes: SYSCR0, SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR, RSTCKCR, MOSCWTCR, SOSCWTCR, PLLWTCR, DPSBYCR, DPSIER0, DPSIER2, DPSIFR0, DPSIFR2, DPSIEGR0, DPSIEGR2, FHSSBYCR, HOCOWTCR2 • Registers related to clock generation circuit: MOFCR, HOCOPCR, PLLPCR (chip version B)	• Register related to the operating modes: SYSCR1 • Registers related to low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR, RSTCKCR, SOPCCR • Registers related to the clock generation circuit: MOFCR, MOSCWTCR
PRC2 bit	VRCR	• Register related to the clock generation circuit: HOCOWTCR

4.8 Comparison of the Interrupt Controllers

Table 4.16 lists a Comparison of the Interrupt Controllers. Table 4.17 lists a Comparison of I/O Registers Associated With the Interrupt Controllers.

Table 4.16 Comparison of the Interrupt Controllers

Item		RX210 Group	RX111 Group
External pin interrupts	64-pin	IRQ0 to IRQ2, IRQ4 to IRQ7	IRQ0 to IRQ7
	48-pin	IRQ0, IRQ1, IRQ4 to IRQ7	IRQ0 to IRQ7
Event link interrupt		The ELSR18I or ELSR19I interrupt is generated by an ELC event.	The ELSR18I interrupt is generated by an ELC event.
DTC/DMAC control		The DTC and DMAC can be activated by interrupt sources.	The DTC can be activated by interrupt sources.
Return from power-down modes		• Sleep mode: Return is initiated by non-maskable interrupts or any other interrupt source. • All-module clock stop mode: Return is initiated by non-maskable interrupts, IRQ0 to IRQ7 interrupts, TMR interrupts, or RTC alarm/periodic interrupts. • Software standby mode: Return is initiated by non-maskable interrupts, IRQ0 to IRQ7 interrupts, or RTC alarm/periodic interrupts.	• Sleep mode, deep sleep mode: Return is initiated by non-maskable interrupts or any other interrupt source. • Software standby mode: Return is initiated by non-maskable interrupts, IRQ0 to IRQ7 interrupts, or RTC alarm/periodic interrupts.

Table 4.17 Comparison of I/O Registers Associated With the Interrupt Controllers

Register Symbol	Bit Symbol	RX210 Group	RX111 Group
DMRSRm	—	DMAC activation request select register m	No register
NMISR	WDTST	WDT underflow/refresh error status flag	Reserved
NMIER	WDTEN	WDT underflow/refresh error enable	Reserved
NMICLR	WDTCLR	WDT clear	Reserved

4.9 Comparison of Buses

Table 4.18 lists a Comparison of the Buses. Table 4.19 lists a Comparison of I/O Registers Associated With the Buses.

Table 4.18 Comparison of the Buses

Item	RX210 Group	RX111 Group
External bus expansion	N/A	N/A
Internal main bus 2	Connected to the DMAC, DTC	Connected to the DTC
Internal peripheral bus 1	Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section)	Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section)
Internal peripheral bus 3	N/A	• Connected to peripheral modules (USB) • Operates in synchronization with the peripheral module clock (PCLKB)
Internal peripheral bus 6	• Connected to ROM (P/E) and E2 DataFlash memory • Operates in synchronization with the flash interface clock (FCLK)	• Connected to ROM (P/E) • Operates in synchronization with the flash interface clock (FCLK)
External bus	• Connected to the external devices • Operates in synchronization with the external-bus clock (BCLK)	N/A

Table 4.19 Comparison of I/O Registers Associated With the Buses

Register Symbol	Bit Symbol	RX210 Group	RX111 Group
BUSPRI	BPEB	External bus priority control	Reserved
CS0MOD	—	CS0 mode register	No register
CS0WCR1	—	CS0 wait control register 1	No register
CS0WCR2	—	CS0 wait control register 2	No register
CS1MOD	—	CS1 mode register	No register
CS1WCR1	—	CS1 wait control register 1	No register
CS1WCR2	—	CS1 wait control register 2	No register
CS2MOD	—	CS2 mode register	No register
CS2WCR1	—	CS2 wait control register 1	No register
CS2WCR2	—	CS2 wait control register 2	No register
CS3MOD	—	CS3 mode register	No register
CS3WCR1	—	CS3 wait control register 1	No register
CS3WCR2	—	CS3 wait control register 2	No register
CS0CR	—	CS0 control register	No register
CS0REC	—	CS0 recovery cycle register	No register
CS1CR	—	CS1 control register	No register
CS1REC	—	CS1 recovery cycle register	No register
CS2CR	—	CS2 control register	No register
CS2REC	—	CS2 recovery cycle register	No register
CS3CR	—	CS3 control register	No register
CS3REC	—	CS3 recovery cycle register	No register
CSRECEN	—	CS recovery cycle insertion enable register	No register

4.10 Comparison of the ELC

Table 4.20 lists a Comparison of the ELC, Table 4.21 lists a Comparison of the ELSRn Register, Table 4.22 and Table 4.23 list comparisons of values that can be set to the ELSRn register, and Table 4.24 lists a Comparison of I/O Registers Associated With the Interrupt Controllers.

Table 4.20 Comparison of the ELC

Item	RX210 Group	RX111 Group
Event link function	• 59 types of event signals can be directly connected to modules. • The operation of timer modules can be selected when an event is input to the timer module. • Event link operation is possible for ports B and E.	• 36 types of event signals can be directly connected to modules. • The operation of timer modules can be selected when an event is input to the timer module. • Event link operation is possible for port B.

Table 4.21 Comparison of the ELSRn Register

Register Symbol	RX210 Group	RX111 Group	Peripheral Function (Module)
ELSR1	Available	Available	MTU1
ELSR2	Available	Available	MTU2
ELSR3	Available	Available	MTU3
ELSR4	Available	Available	MTU4
ELSR7	Available	Available	CMT1
ELSR10	Available	No register	TMR0
ELSR12	Available	No register	TMR2
ELSR15	Available	Available	S12ADb
ELSR16	Available	Available	DA0
ELSR18	Available	Available	Interrupt 1
ELSR19	Available	No register	Interrupt 2
ELSR20	Available	Available	Output port group 1
ELSR21	Available	No register	Output port group 2
ELSR22	Available	Available	Input port group 1
ELSR23	Available	No register	Input port group 2
ELSR24	Available	Available	Single-port 0
ELSR25	Available	Available	Single-port 1
ELSR26	Available	No register	Single-port 2
ELSR27	Available	No register	Single-port 3
ELSR28	Available	No register	Clock source switching to LOCO
ELSR29	Available	No register	POE

Table 4.22 Comparison of Values That Can Be Set to the ELSRn Register (1/2)

Setting Value	RX210 Group	RX111 Group	Name of Event Signal
08h	Can be set	Can be set	MTU1 compare match 1A signal
09h	Can be set	Can be set	MTU1 compare match 1B signal
0Ah	Can be set	Can be set	MTU1 overflow signal
0Bh	Can be set	Can be set	MTU1 underflow signal
0Ch	Can be set	Can be set	MTU2 compare match 2A signal
0Dh	Can be set	Can be set	MTU2 compare match 2B signal
0Eh	Can be set	Can be set	MTU2 overflow signal
0Fh	Can be set	Can be set	MTU2 underflow signal
10h	Can be set	Can be set	MTU3 compare match 3A signal
11h	Can be set	Can be set	MTU3 compare match 3B signal
12h	Can be set	Can be set	MTU3 compare match 3C signal
13h	Can be set	Can be set	MTU3 compare match 3D signal
14h	Can be set	Can be set	MTU3 overflow signal
15h	Can be set	Can be set	MTU4 compare match 4A signal
16h	Can be set	Can be set	MTU4 compare match 4B signal
17h	Can be set	Can be set	MTU4 compare match 4C signal
18h	Can be set	Can be set	MTU4 compare match 4D signal
19h	Can be set	Can be set	MTU4 overflow signal
1Ah	Can be set	Can be set	MTU4 underflow signal
1Fh	Can be set	Can be set	CMT1 compare match 1 signal
22h	Can be set	Cannot be set	TMR0 compare match A0 signal
23h	Can be set	Cannot be set	TMR0 compare match B0 signal
24h	Can be set	Cannot be set	TMR0 overflow signal
28h	Can be set	Cannot be set	TMR2 compare match A2 signal
29h	Can be set	Cannot be set	TMR2 compare match B2 signal
2Ah	Can be set	Cannot be set	TMR2 overflow signal
2Eh	Can be set	Cannot be set	RTC periodic signal
31h	Can be set	Cannot be set	IWDT underflow or refresh error signal
3Ah	Can be set	Can be set	SCI5 error (receive error or error signal detection) signal
3Bh	Can be set	Can be set	SCI5 receive data full signal
3Ch	Can be set	Can be set	SCI5 transmit data empty signal
3Dh	Can be set	Can be set	SCI5 transmit end signal
4Eh	Can be set	Can be set	RIIC0 communication error or event generation signal
4Fh	Can be set	Can be set	RIIC0 receive data full signal
50h	Can be set	Can be set	RIIC0 transmit data empty signal
51h	Can be set	Can be set	RIIC0 transmit end signal

Table 4.23 Comparison of Values That Can Be Set to the ELSRn Register (2/2)

Setting Value	RX210 Group	RX111 Group	Name of Event Signal
52h	Can be set	Cannot be set	RSPI0 error (mode fault, overrun, or parity error) signal
53h	Can be set	Cannot be set	RSPI0 idle signal
54h	Can be set	Cannot be set	RSPI0 receive data full signal
55h	Can be set	Cannot be set	RSPI0 transmit data empty signal
56h	Can be set	Cannot be set	RSPI0 transmit end signal (except during clock synchronous operation in slave mode)
58h	Can be set	Can be set	A/D conversion end signal of 12-bit A/D converter
59h	Can be set	Cannot be set	Comparator B0 comparison result change signal
5Ah	Can be set	Cannot be set	Comparator B0, B1 common comparison result change signal
5Bh	Can be set	Can be set	LVD1 voltage detection signal
5Ch	Can be set	Cannot be set	LVD2 voltage detection signal
5Dh	Can be set	Cannot be set	DMAC0 transfer end signal
5Eh	Can be set	Cannot be set	DMAC1 transfer end signal
5Fh	Can be set	Cannot be set	DMAC2 transfer end signal
60h	Can be set	Cannot be set	DMAC3 transfer end signal
61h	Can be set	Can be set	DTC transfer end signal
62h	Can be set	Cannot be set	Oscillation stop detection signal of clock generation circuit
63h	Can be set	Can be set	Input edge detection signal of input port group 1
64h	Can be set	Cannot be set	Input edge detection signal of input port group 2
65h	Can be set	Can be set	Input edge detection signal of single input port 0
66h	Can be set	Can be set	Input edge detection signal of single input port 1
67h	Can be set	Cannot be set	Input edge detection signal of single input port 2
68h	Can be set	Cannot be set	Input edge detection signal of single input port 3
69h	Can be set	Can be set	Software event signal
6Ah	Cannot be set	Can be set	DOC data operation condition met signal

Table 4.24 Comparison of I/O Registers Associated With the ELC

Register Symbol	Bit Symbol	RX210 Group	RX111 Group
ELOPD	—	Event link option setting register	No register
PGR2	—	Port group setting register 2	No register
PGC2	—	Port group control register 2	No register
PDBF2	—	Port buffer register 2	No register
PEL0	PSP[1:0]	00: Setting is invalid. 01: Port B (corresponding to PGR1) 10: Port E (corresponding to PGR2) 11: Do not set this value.	00: Setting is invalid. 01: Port B (corresponding to PGR1) 10: Setting prohibited 11: Setting prohibited
PEL2	—	Event link port setting register 2	No register
PEL3	—	Event link port setting register 3	No register

4.11 Comparison of I/O Ports

Table 4.25 lists a Comparison of General I/O Functions, Table 4.26 lists a Comparison of the Input Pull-up, Table 4.27 lists a Comparison of 5-V Tolerance, and Table 4.28 lists a Comparison of Registers Associated With the I/O Ports.

Table 4.25 Comparison of General I/O Functions

Item	Port		RX210 Group	RX111 Group
General I/O port	PORT3	64-pin	P30, P31, P32, P35, P36, P37	P30, P31, P32, P35
		48-pin	P30, P31, P35, P36, P37	P35
	PORTH		PH0, PH1, PH2, PH3	PH7
	PORTE	64-pin	PE0, PE1, PE2, PE3, PE4, PE5	PE0, PE1, PE2, PE3, PE4, PE5, PE6, PE7
		48-pin	PE1, PE2, PE3, PE4	PE0, PE1, PE2, PE3, PE4, PE7
	PORTJ		No I/O port	PJ6, PJ7
Switching I/O ports used	PORTB PORTC	64-pin	N/A	The following I/O ports can be switched by the value set to the PRSA register • PB6 or PC0 • PB7 or PC1
		48-pin	N/A	The following I/O ports can be switched by the value set to the PRSB register • PB0 or PC0 • PB1 or PC1 • PB3 or PC2 • PB5 or PC3

Table 4.26 Comparison of the Input Pull-up

Item	Port		RX210 Group	RX111 Group
Input pull-up	PORT4	64-pin	P40, P41, P42, P43, P44, P46	No input pull-up
		48-pin	P40, P41, P42, P46	No input pull-up

Table 4.27 Comparison of 5-V Tolerance

Item	Port	RX210 Group	RX111 Group
5-V tolerance	PORTA	Not 5-V tolerant	PA6
	PORTB	Not 5-V tolerant	PB0

Table 4.28 Comparison of Registers Associated With the I/O Ports

Register Symbol	Bit Symbol	RX210 Group		RX111 Group	
ODR0	B3, B2	• PE1 00: CMOS output 01: N-channel open-drain 10: P-channel open-drain 11: Hi-Z		• PE1 00: CMOS output 01: N-channel open-drain output 10: P-channel open-drain output 11: Setting prohibited.	
ODR1	B1	Reserved		• P14 00: CMOS output 01: N-channel open-drain output 10: P-channel open-drain output 11: Setting prohibited.	
	B0	Pm4 output type select			
DSCR	—	Drive capacity control register		No register	
PSRA	—	64-pin	No register	64-pin	Port switching register A
		48-pin	No register	48-pin	No register
PSRB	—	64-pin	No register	64-pin	No register
		48-pin	No register	48-pin	Port switching register B

4.12 Comparison of the MPC

Table 4.29 to Table 4.35 list comparisons of allocation to multiple pins, and Table 4.36 lists a Comparison of Registers Associated With MPC. "Assigned" means the pin function is allocated to the corresponding I/O port, "N/A" means the pin function is not allocated to the I/O port, and "No I/O port" means the I/O port does not exist.

Table 4.29 Comparison of Allocation to Multiple Pins (1/7)

Module/ Function	Channel	Pin Function	I/O Port	64-pin Package		48-pin Package	
				RX210	RX111	RX210	RX111
Interrupt		NMI (input)	P35	Assigned	Assigned	Assigned	Assigned
Interrupts	IRQ0	IRQ0-DS (input)	P30	Assigned	N/A	Assigned	N/A
		IRQ0 (input)	P30	N/A	Assigned	N/A	N/A
			PE0	N/A	Assigned	No I/O port	Assigned
			PH1	Assigned	No I/O port	Assigned	No I/O port
	IRQ1	IRQ1-DS (input)	P31	Assigned	N/A	Assigned	N/A
		IRQ1 (input)	P31	N/A	Assigned	N/A	Assigned
			PE1	N/A	Assigned	N/A	Assigned
			PH2	Assigned	No I/O port	Assigned	No I/O port
	IRQ2	IRQ2-DS (input)	P32	Assigned	N/A	N/A	N/A
		IRQ2 (input)	P32	N/A	Assigned	No I/O port	N/A
			PB0	N/A	Assigned	N/A	Assigned
			PC4	N/A	Assigned	N/A	Assigned
	IRQ3	IRQ3 (input)	P27	N/A	Assigned	N/A	Assigned
			PA6	N/A	Assigned	N/A	Assigned
			PE3	N/A	Assigned	N/A	Assigned
	IRQ4	IRQ4-DS (input)	PB1	Assigned	N/A	Assigned	N/A
		IRQ4 (input)	P14	Assigned	Assigned	Assigned	Assigned
			PB1	N/A	Assigned	N/A	Assigned
			PE4	N/A	Assigned	N/A	Assigned
	IRQ5	IRQ5-DS (input)	PA4	Assigned	N/A	Assigned	N/A
		IRQ5 (input)	P15	Assigned	Assigned	Assigned	Assigned
			PA4	N/A	Assigned	N/A	Assigned
			PE5	Assigned	Assigned	N/A	N/A
	IRQ6	IRQ6-DS (input)	PA3	Assigned	N/A	Assigned	N/A
		IRQ6 (input)	P16	Assigned	Assigned	Assigned	Assigned
			PA3	N/A	Assigned	N/A	Assigned
			PE6	No I/O port	Assigned	No I/O port	N/A
	IRQ7	IRQ7-DS (input)	PE2	Assigned	N/A	Assigned	N/A
		IRQ7 (input)	P17	Assigned	Assigned	Assigned	Assigned
			PE2	N/A	Assigned	N/A	Assigned
			PE7	No I/O port	Assigned	No I/O port	Assigned

Table 4.30 Comparison of Allocation to Multiple Pins (2/7)

Module/ Function	Channel	Pin Function	I/O Port	64-pin Package		48-pin Package	
				RX210	RX111	RX210	RX111
MTU2a	MTU0	MTIOC0A (I/O)	P14	N/A	Assigned	N/A	Assigned
			PB3	Assigned	Assigned	Assigned	Assigned
			PE3	N/A	Assigned	N/A	Assigned
		MTIOC0B (I/O)	P15	Assigned	Assigned	Assigned	Assigned
			PA1	Assigned	Assigned	Assigned	Assigned
		MTIOC0C (I/O)	P17	N/A	Assigned	N/A	Assigned
			P32	Assigned	Assigned	N/A	N/A
			PB0	N/A	Assigned	N/A	Assigned
			PB1	Assigned	Assigned	Assigned	Assigned
		MTIOC0D (I/O)	PA3	Assigned	Assigned	Assigned	Assigned
	MTU1	MTIOC1A (I/O)	PE4	Assigned	Assigned	Assigned	Assigned
		MTIOC1B (I/O)	PA3	N/A	Assigned	N/A	Assigned
			PB5	Assigned	Assigned	Assigned	Assigned
			PE3	N/A	Assigned	N/A	Assigned
	MTU2	MTIOC2A (I/O)	P26	Assigned	Assigned	Assigned	Assigned
			PA6	N/A	Assigned	N/A	Assigned
			PB5	Assigned	Assigned	Assigned	Assigned
			PE0	N/A	Assigned	No I/O port	Assigned
		MTIOC2B (I/O)	P27	Assigned	Assigned	Assigned	Assigned
			PA4	N/A	Assigned	N/A	Assigned
			PE5	Assigned	Assigned	N/A	N/A
	MTU3	MTIOC3A (I/O)	P14	Assigned	Assigned	Assigned	Assigned
			P17	Assigned	Assigned	Assigned	Assigned
			PC7	Assigned	Assigned	Assigned	Assigned
			PE4	N/A	Assigned	N/A	Assigned
		MTIOC3B (I/O)	P17	Assigned	Assigned	Assigned	Assigned
			PB3	N/A	Assigned	N/A	Assigned
			PB7	Assigned	Assigned	N/A	N/A
			PC5	Assigned	Assigned	Assigned	Assigned
		MTIOC3C (I/O)	P16	Assigned	Assigned	Assigned	Assigned
			PC6	Assigned	Assigned	Assigned	Assigned
		MTIOC3D (I/O)	P16	Assigned	Assigned	Assigned	Assigned
			PB6	Assigned	Assigned	N/A	N/A
			PC4	Assigned	Assigned	Assigned	Assigned

Table 4.31 Comparison of Allocation to Multiple Pins (3/7)

Module/ Function	Channel	Pin Function	I/O Port	64-pin Package		48-pin Package	
				RX210	RX111	RX210	RX111
MTU2a	MTU4	MTIOC4A (I/O)	PA0	Assigned	Assigned	N/A	N/A
			PB3	Assigned	Assigned	Assigned	Assigned
			PE2	Assigned	Assigned	Assigned	Assigned
		MTIOC4B (I/O)	P30	Assigned	Assigned	Assigned	N/A
			P54	Assigned	Assigned	N/A	N/A
			PC2	Assigned	Assigned	N/A	N/A
			PE3	Assigned	Assigned	Assigned	Assigned
		MTIOC4C (I/O)	PB1	Assigned	Assigned	Assigned	Assigned
			PE1	Assigned	Assigned	Assigned	Assigned
			PE5	Assigned	Assigned	N/A	N/A
		MTIOC4D (I/O)	P31	Assigned	Assigned	Assigned	N/A
			P55	Assigned	Assigned	N/A	N/A
			PC3	Assigned	Assigned	N/A	N/A
			PE4	Assigned	Assigned	Assigned	Assigned
	MTU5	MTIC5U (input)	PA4	Assigned	Assigned	Assigned	Assigned
		MTIC5V (input)	PA6	Assigned	Assigned	Assigned	Assigned
		MTIC5W (input)	PB0	Assigned	Assigned	Assigned	Assigned
	MTU	MTCLKA (input)	P14	Assigned	Assigned	Assigned	Assigned
			PA4	Assigned	Assigned	Assigned	Assigned
			PC6	Assigned	Assigned	Assigned	Assigned
		MTCLKB (input)	P15	Assigned	Assigned	Assigned	Assigned
			PA6	Assigned	Assigned	Assigned	Assigned
			PC7	Assigned	Assigned	Assigned	Assigned
		MTCLKC (input)	PA1	Assigned	Assigned	Assigned	Assigned
			PC4	Assigned	Assigned	Assigned	Assigned
		MTCLKD (input)	PA3	Assigned	Assigned	Assigned	Assigned
			PC5	Assigned	Assigned	Assigned	Assigned
POE2a	POE0	POE0# (input)	PA3	N/A	Assigned	N/A	Assigned
			PC4	Assigned	Assigned	Assigned	Assigned
	POE1	POE1# (input)	PB5	Assigned	Assigned	Assigned	Assigned
	POE2	POE2# (input)	PA6	Assigned	Assigned	Assigned	Assigned
	POE3	POE3# (input)	PB3	Assigned	Assigned	Assigned	Assigned
			PE0	N/A	Assigned	No I/O port	Assigned
	POE8	POE8# (input)	P17	Assigned	Assigned	Assigned	Assigned
			P30	Assigned	Assigned	Assigned	N/A
			PE3	Assigned	Assigned	Assigned	Assigned

Table 4.32 Comparison of Allocation to Multiple Pins (4/7)

Module/ Function	Channel	Pin Function	I/O Port	64-pin Package		48-pin Package	
				RX210	RX111	RX210	RX111
TMR	TMR0	TMO0 (output)	PB3	Assigned	N/A	Assigned	N/A
			PH1	Assigned	No I/O port	Assigned	No I/O port
		TMCI0 (input)	PB1	Assigned	N/A	Assigned	N/A
			PH3	Assigned	No I/O port	Assigned	No I/O port
		TMRI0 (input)	PA4	Assigned	N/A	Assigned	N/A
			PH2	Assigned	No I/O port	Assigned	No I/O port
	TMR1	TMO1 (output)	P17	Assigned	N/A	Assigned	N/A
			P26	Assigned	N/A	Assigned	N/A
		TMCI1 (input)	P54	Assigned	N/A	N/A	N/A
			PC4	Assigned	N/A	Assigned	N/A
		TMRI1 (input)	PB5	Assigned	N/A	Assigned	N/A
	TNR2	TMO2 (output)	P16	Assigned	N/A	Assigned	N/A
			PC7	Assigned	N/A	Assigned	N/A
		TMCI2 (input)	P15	Assigned	N/A	Assigned	N/A
			P31	Assigned	N/A	Assigned	N/A
			PC6	Assigned	N/A	Assigned	N/A
		TMRI2 (input)	P14	Assigned	N/A	Assigned	N/A
			PC5	Assigned	N/A	Assigned	N/A
	TR3	TMO3 (output)	P32	Assigned	N/A	N/A	N/A
			P55	Assigned	N/A	N/A	N/A
		TMCI3 (input)	P27	Assigned	N/A	Assigned	N/A
			PA6	Assigned	N/A	Assigned	N/A
			P30	Assigned	N/A	Assigned	N/A
Serial communications interface	SCI1	RXD1 (input)/ SMISO1 (I/O)/ SSCL1 (I/O)	P15	Assigned	Assigned	Assigned	Assigned
			P30	Assigned	Assigned	Assigned	N/A
			PC6	N/A	Assigned	N/A	Assigned
		TXD1 (input)/ SMOSI1 (I/O)/ SSDA1 (I/O)	P16	Assigned	Assigned	Assigned	Assigned
			P26	Assigned	Assigned	Assigned	Assigned
			PC7	N/A	Assigned	N/A	Assigned
		SCK1 (I/O)	P17	Assigned	Assigned	Assigned	Assigned
			P27	Assigned	Assigned	Assigned	Assigned
			PC5	N/A	Assigned	N/A	Assigned
		CTS1# (input)/ RTS1# (output)/ SS1# (input)	P14	Assigned	Assigned	Assigned	Assigned
			P31	Assigned	Assigned	Assigned	N/A

Table 4.33 Comparison of Allocation to Multiple Pins (5/7)

Module/ Function	Channel	Pin Function	I/O Port	64-pin Package		48-pin Package	
				RX210	RX111	RX210	RX111
Serial communications interface	SCI5	RXD5 (input)/ SMISO5 (I/O)/ SSCL5 (I/O)	PA3	Assigned	Assigned	Assigned	Assigned
			PC2	Assigned	Assigned	N/A	N/A
		TXD5 (output)/ SMOSI5 (I/O)/ SSDA5 (I/O)	PA4	Assigned	Assigned	Assigned	Assigned
			PC3	Assigned	Assigned	N/A	N/A
		SCK5 (I/O)	PA1	Assigned	Assigned	Assigned	Assigned
			PC4	Assigned	Assigned	Assigned	Assigned
		CTS5# (input)/ RTS5# (output)/ SS5# (input)	PA6	Assigned	Assigned	Assigned	Assigned
	SCI6	RXD6 (input)/ SMISO6 (I/O)/ SSCL6 (I/O)	PB0	Assigned	N/A	Assigned	N/A
			P32	Assigned	N/A	N/A	N/A
			PB1	Assigned	N/A	Assigned	N/A
		SCK6 (I/O)	PB3	Assigned	N/A	Assigned	N/A
	SCI8	RXD8 (input)/ SMISO8 (I/O)/ SSCL8 (I/O)	PC6	Assigned	N/A	Assigned	N/A
		TXD8 (output)/ SMOSI8 (I/O)/ SSDA8 (I/O)	PC7	Assigned	N/A	Assigned	N/A
		SCK8 (I/O)	PC5	Assigned	N/A	Assigned	N/A
		CTS8# (input)/ RTS8# (output)/ SS8# (input)	PC4	Assigned	N/A	Assigned	N/A
	SCI9	RXD9 (input)/ SMISO9 (I/O)/ SSCL9 (I/O)	PB6	Assigned	N/A	N/A	N/A
		TXD9 (output)/ SMOSI9 (I/O)/ SSDA9 (I/O)	PB7	Assigned	N/A	N/A	N/A
		SCK9 (I/O)	PB5	Assigned	N/A	N/A	N/A
	SCI12	RXD12 (input)/ SMISO12 (I/O)/ SSCL12 (I/O)/ RXDX12 (input)	P17	N/A	Assigned	N/A	Assigned
			PE2	Assigned	Assigned	Assigned *1	Assigned
		TXD12 (output)/ SMOSI12 (I/O)/ SSDA12 (I/O)/ TXDX12 (output)/ SIOX12 (I/O)	P14	N/A	Assigned	N/A	Assigned
		CTS12# (input)/ RTS12# (output)/ SS12# (input)	PE3	Assigned	Assigned	Assigned*2	Assigned
		SCK12 (I/O)	P27	N/A	Assigned	N/A	Assigned
			PE0	Assigned	Assigned	No I/O port	Assigned

Note 1. SMISO12 function is not allocated.
Note 2. SS12# function is not allocated.

Table 4.34 Comparison of Allocation to Multiple Pins (6/7)

Module/ Function	Channel	Pin Function	I/O Port	64-pin Package		48-pin Package	
				RX210	RX111	RX210	RX111
RIIC	RIIC0	SCL-DS (I/O)	P16	Assigned	N/A	Assigned	N/A
		SCL0 (I/O)	P16	N/A	Assigned	N/A	Assigned
			PB0	N/A	Assigned	N/A	Assigned
		SDA-DS (I/O)	P17	Assigned	N/A	Assigned	N/A
		SDA0 (I/O)	P17	N/A	Assigned	N/A	Assigned
			PA6	N/A	Assigned	N/A	Assigned
RSPI	RSPI0	RSPCKA (I/O)	P15	N/A	Assigned	N/A	Assigned
			PB0	Assigned	Assigned	Assigned	Assigned
			PC5	Assigned	Assigned	Assigned	Assigned
			PE3	N/A	Assigned	N/A	Assigned
		MOSIA (I/O)	P16	Assigned	Assigned	Assigned	Assigned
			PA6	Assigned	Assigned	Assigned	Assigned
			PC6	Assigned	Assigned	Assigned	Assigned
			PE4	N/A	Assigned	N/A	Assigned
		MISOA (I/O)	P17	Assigned	Assigned	Assigned	Assigned
			PA3	N/A	Assigned	N/A	Assigned
			PC7	Assigned	Assigned	Assigned	Assigned
		SSLA0 (output)	P14	N/A	Assigned	N/A	Assigned
			PA4	Assigned	Assigned	Assigned	Assigned
			PC4	Assigned	Assigned	Assigned	Assigned
		SSLA1 (output)	PA0	Assigned	Assigned	N/A	N/A
		SSLA2 (output)	PA1	Assigned	Assigned	Assigned	Assigned
		SSLA3 (output)	PC2	Assigned	Assigned	N/A	N/A
USBc	USB0	USB0_EXICEN (output)	PC6	N/A	Assigned	N/A	Assigned
		USB0_VBUSEN (output)	P16	N/A	Assigned	N/A	Assigned
			P26	N/A	Assigned	N/A	Assigned
			PC4	N/A	Assigned	N/A	Assigned
		USB0_OVRCURA (input)	P14	N/A	Assigned	N/A	Assigned
			PB3	N/A	Assigned	N/A	Assigned
		USB0_OCRCURB (input)	P16	N/A	Assigned	N/A	Assigned
			PC7	N/A	Assigned	N/A	Assigned
		USB0_VBUS (input)	P16	N/A	Assigned	N/A	Assigned
			PC4	N/A	Assigned	N/A	Assigned
		USB0_ID (input)	PC5	N/A	Assigned	N/A	Assigned

Table 4.35 Comparison of Allocation to Multiple Pins (7/7)

Module/ Function	Channel	Pin Function	I/O Port	64-pin Package		48-pin Package	
				RX210	RX111	RX210	RX111
RTC		RTCOUT (output)	P16	Assigned	Assigned	N/A	Assigned
			P32	Assigned	Assigned	N/A	N/A
			PA1	N/A	Assigned	N/A	Assigned
			PB0	N/A	Assigned	N/A	Assigned
		RTCIC0 (input)	P30	Assigned	N/A	N/A	N/A
		RTCIC1 (input)	P31	Assigned	N/A	N/A	N/A
		RTCIC2 (input)	P32	Assigned	N/A	N/A	N/A
S12ADb		AN000 (input)	P40	Assigned	Assigned	Assigned	Assigned
		AN001 (input)	P41	Assigned	Assigned	Assigned	Assigned
		AN002 (input)	P42	Assigned	Assigned	Assigned	Assigned
		AN003 (input)	P43	Assigned	Assigned	N/A	N/A
		AN004 (input)	P44	Assigned	Assigned	N/A	N/A
		AN006 (input)	P46	Assigned	Assigned	Assigned	Assigned
		AN008 (input)	PE0	Assigned	Assigned	No I/O port	Assigned
		AN009 (input)	PE1	Assigned	Assigned	Assigned	Assigned
		AN010 (input)	PE2	Assigned	Assigned	Assigned	Assigned
		AN011 (input)	PE3	Assigned	Assigned	Assigned	Assigned
		AN012 (input)	PE4	Assigned	Assigned	Assigned	Assigned
		AN013 (input)	PE5	Assigned	Assigned	N/A	N/A
		AN014 (input)	PE6	No I/O port	Assigned	No I/O port	N/A
		AN015 (input)	PE7	No I/O port	Assigned	No I/O port	Assigned
		VREFH0 (input)	PJ6	No I/O port	Assigned	No I/O port	Assigned
		VREFL0 (input)	PJ7	No I/O port	Assigned	No I/O port	Assigned
		ADTRG0# (input)	P16	Assigned	Assigned	Assigned	Assigned
			P27	N/A	Assigned	N/A	Assigned
			PB0	N/A	Assigned	N/A	Assigned
DA		DA0 (output)	P03	Assigned	Assigned	N/A	N/A
		DA1 (output)	P05	Assigned	Assigned	N/A	N/A
Clocks		CLKOUT (output)	P15	N/A	Assigned	N/A	Assigned
			PC4	N/A	Assigned	N/A	Assigned
CRC		CACREF (input)	P27	N/A	Assigned	N/A	Assigned
			PA0	Assigned	Assigned	N/A	N/A
			PC7	Assigned	Assigned	Assigned	Assigned
			PH0	Assigned	No I/O port	Assigned	No I/O port
CMPA		CMPA1 (input)	PE3	Assigned	N/A	Assigned	N/A
		CMPA2 (input)	P27	N/A	Assigned	N/A	Assigned
			PE4	Assigned	N/A	Assigned	N/A
		CVREFA (input)	PA1	Assigned	N/A	Assigned	N/A
CMPB		CMPB0 (input)	PE1	Assigned	N/A	Assigned	N/A
		CVREFB0 (input)	PE2	Assigned	N/A	Assigned	N/A
		CMPB1 (input)	PA3	Assigned	N/A	Assigned	N/A
		CVREFB1 (input)	PA4	Assigned	N/A	Assigned	N/A

Table 4.36 Comparison of Registers Associated With MPC

Register Symbol	Bit Symbol	RX210 Group	RX111 Group
P2nPFS	ISEL	Reserved	Interrupt input function select
PCnPFS	ISEL	Reserved	Interrupt input function select
PHnPFS	—	PHn pin function control registers	No register
PJnPFS	—	No register	PJn pin function control registers
PFCSE	—	CS output enable register	No register
PFAOE0	—	Address output enable register 0	No register
PFAOE1	—	Address output enable register 1	No register
PFBCR0	—	External bus control register 0	No register
PFBCR1	—	External bus control register 1	No register

4.13 Comparison of POE2

Table 4.37 lists a Comparison of POE2.

Table 4.37 Comparison of POE2

Item	RX210 Group	RX111 Group
High-impedance is controlled by an event signal	Pins for complementary PWM output from the MTU and output pins for MTU0 can be placed in the high-impedance by an event signal from the ELC.	N/A

4.14 Comparison of the CMT

Table 4.38 lists a Comparison of the CMT, and Table 4.39 lists a Comparison of I/O Registers Associated With the CMT.

Table 4.38 Comparison of the CMT

Item	RX210 Group	RX111 Group
Units	2 channels × 2 units	2 channels × 1 unit

Table 4.39 Comparison of I/O Registers Associated With the CMT

Register Symbol	Bit Symbol	RX210 Group	RX111 Group
CMSTR1	—	Compare match timer start register 1	No register
CMT2.CMCR	—	Compare match timer control register	No register
CMT3.CMCR	—	Compare match timer control register	No register
CMT2.CMCNT	—	Compare match counter	No register
CMT3.CMCNT	—	Compare match counter	No register
CMT2.CMCOR	—	Compare match constant register	No register
CMT3.CMCOR	—	Compare match constant register	No register

4.15 Comparison of the RTC

Table 4.40 lists a Comparison of the RTC, and Table 4.41 lists a Comparison of I/O Registers Associated With the RTC. Note that the RTC is not available in the 48-pin package of the RX210 Group.

Table 4.40 Comparison of the RTC

Item	RX210 Group	RX111 Group
Count mode	Calendar count mode	Calendar count mode Binary count mode
Clock output	1-Hz clock output	1-/64-Hz clock output
Interrupts	Recovery from software standby mode or deep software standby mode can be performed by an alarm interrupt or periodic interrupt	Recovery from software standby mode can be performed by an alarm interrupt or periodic interrupt
Time-capture function	Times when any three event signals are input can be captured – the month, date, hour, minute, and second are captured for each event.	N/A

Table 4.41 Comparison of I/O Registers Associated With the RTC

Register Symbol	Bit Symbol	RX210 Group	RX111 Group
RCR1	RTCOS	Reserved	RTCOUT output select
RCR2	CNTMD	Reserved	Count mode select
RCR3	RTCDV[2:0]	Sub-clock oscillator drive ability control 000: Setting prohibited 001: Drive ability for low CL 010: Setting prohibited 011: Setting prohibited 100: Setting prohibited 101: Setting prohibited 110: Drive ability for standard CL 111: Setting prohibited	Sub-clock oscillator drive capacity control 000: Medium drive capacity (4.4 pF type) 001: High drive capacity (6.0 pF type) 010: Low drive capacity (3.7 pF type) Settings other than above are prohibited.
RTCCR0	—	Time capture control register 0	No register
RTCCR1	—	Time capture control register 1	No register
RTCCR2	—	Time capture control register 2	No register
RSECCP0	—	Second capture register 0	No register
RMINCP0	—	Minute capture register 0	No register
RHRCP0	—	Hour capture register 0	No register
RDAYCP0	—	Data capture register 0	No register
RMONCP0	—	Month capture register 0	No register
RSECCP1	—	Second capture register 1	No register
RMINCP1	—	Minute capture register 1	No register
RHRCP1	—	Hour capture register 1	No register
RDAYCP1	—	Data capture register 1	No register
RMONCP1	—	Month capture register 1	No register
RSECCP2	—	Second capture register 2	No register
RMINCP2	—	Minutes capture register 2	No register
RHRCP2	—	Hour capture register 2	No register
RDAYCP2	—	Date capture register 2	No register
RMONCP2	—	Month capture register 2	No register
BCNT0	—	No register	Binary counter 0
BCNT1	—	No register	Binary counter 1
BCNT2	—	No register	Binary counter 2
BCNT3	—	No register	Binary counter 3
BCNT0AR	—	No register	Binary counter 0 alarm register
BCNT1AR	—	No register	Binary counter 1 alarm register
BCNT2AR	—	No register	Binary counter 2 alarm register
BCNT3AR	—	No register	Binary counter 3 alarm register
BCNT0AER	—	No register	Binary counter 0 alarm enable register
BCNT1AER	—	No register	Binary counter 1 alarm enable register
BCNT2AER	—	No register	Binary counter 2 alarm enable register
BCNT3AER	—	No register	Binary counter 3 alarm enable register

4.16 Comparison of the IWDT

Table 4.42 lists a Comparison of the IWDT, and Table 4.43 lists a Comparison of I/O Registers Associated With the IWDT.

Table 4.42 Comparison of the IWDT

Item	RX210 Group	RX111 Group
Auto-start mode	Decrementing is stopped when transitioning to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode.	Decrementing is stopped when transitioning to sleep mode, software standby mode, or deep sleep mode.
Register start mode	Decrementing is stopped when transitioning to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode.	Decrementing is stopped when transitioning to sleep mode, software standby mode, or deep sleep mode.
Event link function	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	N/A

Table 4.43 Comparison of I/O Registers Associated With the IWDT

Register Symbol	Bit Symbol	RX210 Group	RX111 Group
IWDTCR	TOPS[1:0]	00: 1,024 cycles (03FFh) 01: 4,096 cycles (0FFFh) 10: 8,192 cycles (1FFFh) 11: 16,384 cycles (3FFFh)	00: 128 cycles (007Fh) 01: 512 cycles (01FFh) 10: 1,024 cycles (03FFh) 11: 2,048 cycles (07FFh)
IWDTCSTPR	SCLSTP	0: Count stop is disabled 1: Count is stopped at a transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode	0: Count stop is disabled. 1: Count is stopped at a transition to sleep mode, software standby mode, or deep sleep mode.

4.17 Comparison of the SCI

Table 4.44 lists a Comparison of the SCI, and Table 4.45 lists a Comparison of I/O Registers Associated With the SCI.

Table 4.44 Comparison of the SCI

Item		RX210 Group	RX111 Group
Channels	64-pin	6 channels (SCI1, SCI5, SCI6, SCI8, SCI9, SCI12)	3 channels (SCI1, SCI5, SCI12)
	48-pin	5 channels (SCI1, SCI5, SCI6, SCI8, SCI12)	3 channels (SCI1, SCI5, SCI12)
Detecting the start bit in asynchronous mode		Low level only	Selectable from low or falling edge
Clock source for the start bit in asynchronous mode		Transfer rate clock can be input from TMR timers (SCI5, SCI6, and SCI12)	Transfer rate clock can be input from MTU2 timers (SCI1, SCI5, and SCI12)

Table 4.45 Comparison of I/O Registers Associated With the SCI

Register Symbol	Bit Symbol	RX210 Group	RX111 Group
SEMR	RXDESEL	Reserved	Asynchronous start bit edge detection select

4.18 Comparison of the RSPI

Table 4.46 lists a Comparison of the RSPI.

Table 4.46 Comparison of the RSPI

Item		RX210 Group	RX111 Group
Channels	64-pin	1 channel	1 channel
	48-pin	1 channel	1 channel (SSLA1 and SSLA3 are not supported)
Event linking		The following five types of events can be output to the event link controller. • Reception-buffer full event output • Transmission-buffer empty event output • Mode fault, overrun, or parity error event output • RSPI idle event output • Transmission-completed event output	N/A
Maximum bit rate		8.00 Mbps (PCLK = 32 MHz)	16.00 Mbps (PCLK = 32 MHz)

4.19 Comparison of the S12AD

Table 4.47 lists a Comparison of the S12AD, and Table 4.48 lists a Comparison of I/O Registers Associated With the S12AD.

Table 4.47 Comparison of the S12AD

Item		RX210 Group	RX111 Group
Input channels	64-pin	12 channels (AN000 to AN004, AN006, AN008 to AN013)	14 channels (AN000 to AN004, AN006, AN008 to AN015) 6 high-precision channels
	48-pin	8 channels (AN000 to AN002, AN006, AN009 to AN012)	10 channels (AN000 to AN002, AN006, AN008 to AN012, AN015) 4 high-precision channels
Data registers		• For analog input: 16 data registers • For duplication of A/D conversion data in double trigger mode: One data register • For temperature sensor: One data register • For internal reference voltage: One data register	• For analog input: 14 data registers • For duplication of A/D conversion data in double trigger mode: One data register • For temperature sensor: One data register • For internal reference voltage: One data register
A/D conversion start conditions		• Software trigger • Synchronous trigger: Trigger by MTU, ELC, or temperature sensor • Asynchronous trigger: A/D conversion can be triggered from the ADTRG0# pin.	• Software trigger • Synchronous trigger: Trigger by MTU or ELC • Asynchronous trigger: A/D conversion can be triggered from the ADTRG0# pin.
Functions		• Sample-and-hold function • Channel-dedicated sample-and-hold function (0.25 V ≤ analog voltage input ≤ AVCC0 - 0.25 V) • Variable sampling state count • Self-diagnosis of 12-bit A/D converter • A/D-converted value addition mode • Analog input disconnection detection assist • Double trigger mode (duplication of A/D conversion data)	• Variable sampling state count • A/D-converted value addition mode • Double trigger mode (duplication of A/D conversion data)

Table 4.48 Comparison of I/O Registers Associated With the S12AD

Register Symbol	Bit Symbol	RX210 Group		RX111 Group
ADDRy	—	64-pin	y = 0 to 4, 6, 8 to 13	y = 0 to 4, 6, 8 to 12, 15
		48-pin	y = 0 to 2, 6, 9 to 12	y = 0 to 2, 6, 8 to 12, 15
ADCSR	ADHSC	Reserved		A/D conversion mode select
	EXTRG	0: A/D conversion is started by the synchronous trigger (MTU, ELC, or temperature sensor). 1: A/D conversion is started by the asynchronous trigger (ADTRG0#).		0: A/D conversion is started by the synchronous trigger (MTU or ELC). 1: A/D conversion is started by the asynchronous trigger (ADTRG0#).
ADANSA	b5, b7	A/D conversion channels select		Reserved
ADANSB	b5, b7	A/D conversion channels select		Reserved
ADADS	b5, b7	A/D-converted value addition channel select		Reserved
ADCER	DIAGVAL[1:0]	Conversion voltage select for self-diagnosis		Reserved
	DIAGLD	Self-diagnosis mode select		Reserved
	DIAGM	Self-diagnosis enable		Reserved
ADEXICR	TSSAD	Reserved		Temperature sensor output A/D-converted value addition function select
ADSHCR	—	A/D sample and hold circuit control register		No register
ADDISCR	—	A/D disconnecting detection control register		No register

4.20 Comparison of the DA

Table 4.49 lists a Comparison of the DA, and Table 4.50 lists a Comparison of I/O Registers Associated With the DA.

Table 4.49 Comparison of the DA

Item	RX210 Group	RX111 Group
Resolution	10 bits	8 bits

Table 4.50 Comparison of I/O Registers Associated With the DA

Register Symbol	Bit Symbol	RX210 Group	RX111 Group
DACR	DAE	D/A enable	Reserved

4.21 Comparison of the TEMPS

Table 4.51 lists a Comparison of the TEMPS, and Table 4.52 lists a Comparison of I/O Registers Associated With the TEMPS.

Table 4.51 Comparison of the TEMPS

Item	RX210 Group	RX111 Group
Power consumption reduction function	Module stop state can be set.	N/A

Table 4.52 Comparison of I/O Registers Associated With the TEMPS

Register Symbol	Bit Symbol	RX210 Group	RX111 Group
TSCR	—	Temperature sensor control register	No register

4.22 Comparison of the Flash Memory

Table 4.53 lists a Comparison of the Flash Memory. For details on the flash memory in the RX210 Group and RX111 Group, refer to corresponding User's Manual: Hardware listed in chapter 5.

Table 4.53 Comparison of the Flash Memory

Item		RX210 Group	RX111 Group
Memory capacity	64-pin	User area: 512 KB (max.)	User area: 128 KB (max.)
	48-pin	User area: 256 KB (max.)	User area: 128 KB (max.)
		Data area: 8 KB User boot area: 16 KB	Data area: 8 KB
Units of programming and erasure		Units of programming • User area: 2, 8, or 128 bytes • Data area: 2 or 8 bytes • User boot area: 2, 8, or 128 bytes Units of erasure • User area: Block units • Data area: 128 bytes • User boot area: 16 KB	Units of programming • User area: 4 bytes • Data area: 1 byte Units of erasure • User area: Block units • Data area: Block units
On-board programming		• Boot mode Programmable using SCI0 • User boot mode • Single-chip mode	• Boot mode Programmable using SCI0 or USB0 • Single-chip mode
Interrupts		FIFERR and FRDYI interrupts	N/A
Security		• ID code protect (boot mode) • ID code protection on connection of the on-chip debugger • ROM code protection	• Boot mode ID code protection • On-chip debugging emulator ID code protection
Protection		• Protection through I/O registers associated with the flash memory • Protection through the lock bit (user area only)	• Protection through I/O registers associated with the flash memory • Area protection
Start-up program protection		N/A	Available

5. Reference Documents

User's Manual: Hardware

RX210 Group User's Manual: Hardware Rev.1.50 (R01UH0037EJ)

RX111 Group User's Manual: Hardware Rev.1.10 (R01UH0365EJ)

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

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REVISION HISTORY	RX210 Group, RX111 Group Application Note Comparison of the RX210 Group and RX111 Group

Rev.	Date	Description	
		Page	Summary
1.00	Sep. 16, 2014	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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