

RX200 Series

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Using the ELC to link the LVD and LOCO

Introduction

The Event Link Controller (ELC) is a new module to the RX family and was first introduced on the RX210 group. The ELC was designed to allow interlinking of different events from the on-chip peripherals. This would allow for higher performance at lower current consumption by allowing the CPU core to stay in low power mode while at the same time being flexible enough to allow for a wide range of peripheral responses. The included sample project shows how to link the Low Voltage Detection (LVD) module with the Low Speed On-Chip Oscillator (LOCO) and the Compare Match Timer (CMT) to detect Vcc levels and switch clock sources between the LOCO and PLL almost entirely using hardware only when certain configurable voltage thresholds are breached.

Target Device

The following is a list of devices that are currently supported by this API:

- **RX210 Group**

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1. Overview

The Event Link Controller is a module that essentially allows linkage of different peripheral “events” to “action “on other peripherals without any CPU intervention. An example of “events” would be a compare-match event or an overflow event in case of any of the timers or a level shift on an input port. Similarly the list of possible “actions” include things like timer count start, timer count stop, A/D conversion start, interrupt generation etc. Thus the ELC is an agglomeration and an improvement of linking mechanisms provided on earlier microcontrollers whereby modules like the A/D which could be triggered on a timer count or DTC activation by the A/D conversion completion signal.



Figure 1.1: ELC Signal/Action linking

This particular sample workspace links the Low Voltage Detection (LVD) module, and the Low Speed On-Chip Oscillator (LOCO) via the ELC. The Compare Match Timer (CMT1) is also linked to the LVD via the ELC. The LVD is configured to generate a voltage-detect event when Vcc crosses 3.1 volts. When Vcc drops below 3.1 volts, the clock source is switched automatically to the LOCO. When Vcc rises back up above 3.1 volts, it automatically triggers the CMT timer which counts up for a delay after which the PLL is selected as the main clock source. Except for the final part when the PLL is selected as the clock source, there is no CPU intervention required for operation.

1.1 Configuring the Event Link Controller

The Event Link Controller allows the user to link defined events from any peripheral and uses it as a trigger for another defined set of “target” peripherals.

The following table lists all the signals from the different peripherals that can be routed to the ELC and the list of target peripherals.

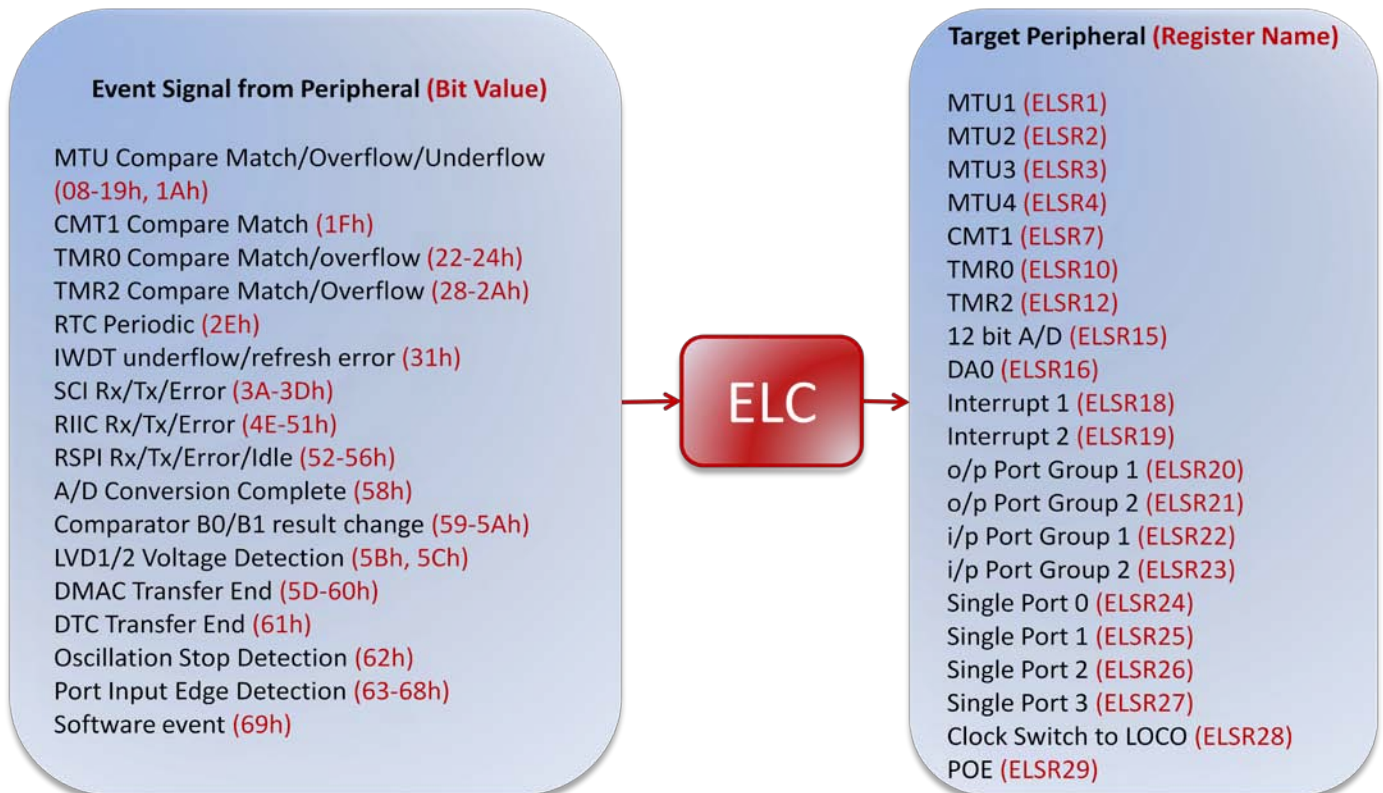


Figure 1.2: Event Signal Bit Value and Target Peripheral Registers

The column on the left hand side lists all the different event signals from the different peripherals that can be routed to the ELC. The expanded list is available in Table 18.3 in the Hardware Manual. Note that each event has a bit value associated with it. For example, the CMT1 Compare Match Event has a bit value of 0x1F. The column on the right hand side lists the available target peripherals. Each peripheral has a register associated with it. For example the 12 bit A/D has the ELSR15 register associated with it.

Thus in order to link the compare match event from CMT1 to the 12 bit A/D, simply set the register value in ELSR15 to 0x1F.

While the Event Signals can be routed to the Target peripherals, configuring the actual behavior of the target peripherals is limited in some cases. For example, The Clock Switch to LOCO (ELSR28) has no other configuration options available and so if an event was linked to this register, then the event would simply switch the clock source to the LOCO. Similarly, in case of the 12 bit A/D (ELSR15), an event would simply cause it to start conversion.

When linking to the timer modules however, there are additional ELC registers available that configure the actual behavior of the timer. Using the ELOPA, ELOPB, ELOPC and ELOPD registers, the user can determine if the target timer starts, restarts, stops or switches to Event Counter mode.

1.2 Linking IO ports

Linking to the I/O ports also allows the user flexibility in determining the behavior. Using the PGR, PGC, PDBF and PEL register the user can determine the state and response of the IO pins.

Only Port B and Port E can be linked by the ELC. These ports can be linked as single ports; for example Port B.1, or they can be linked as port groups.

There are 4 single port options available as shown below

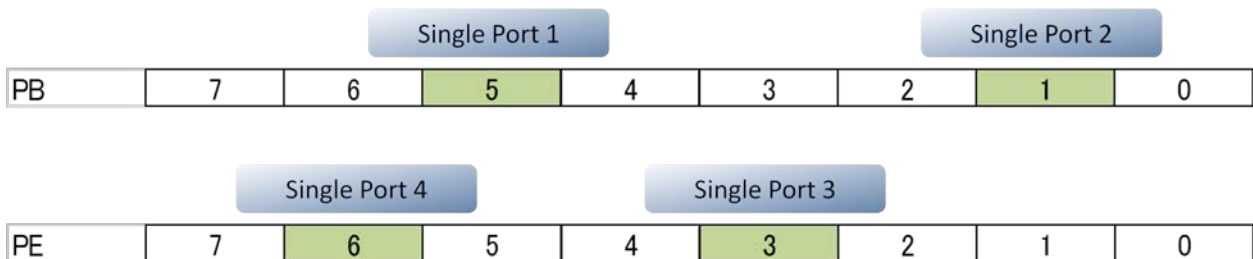


Figure 1.3: Single Port Mode

In group mode, there are two groups to which any four ports can be assigned. Below is an example port configuration.

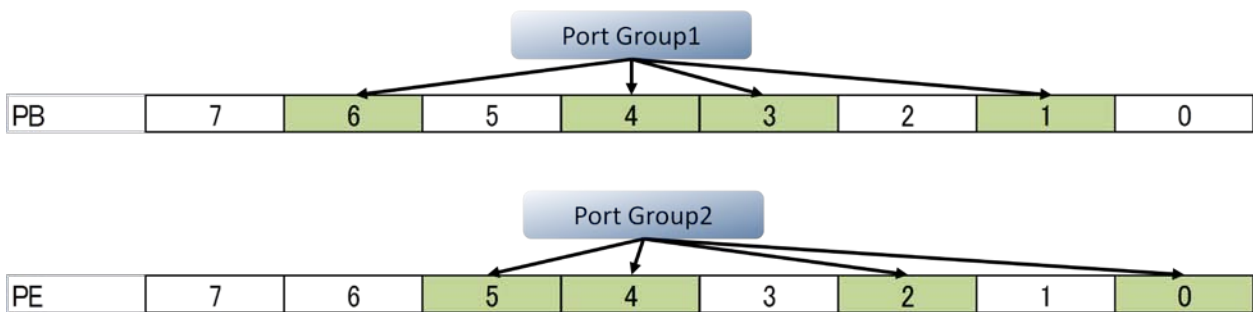


Figure 1.4: Port Group Mode

When the ports are used to generate the Event Signal to the ELC, if they are configured as single ports, then an event (configurable as edge or level detection) on that port will generate the signal to the ELC. If the ports are configured as a group, then an event on any one port in the group will generate an event to the ELC,

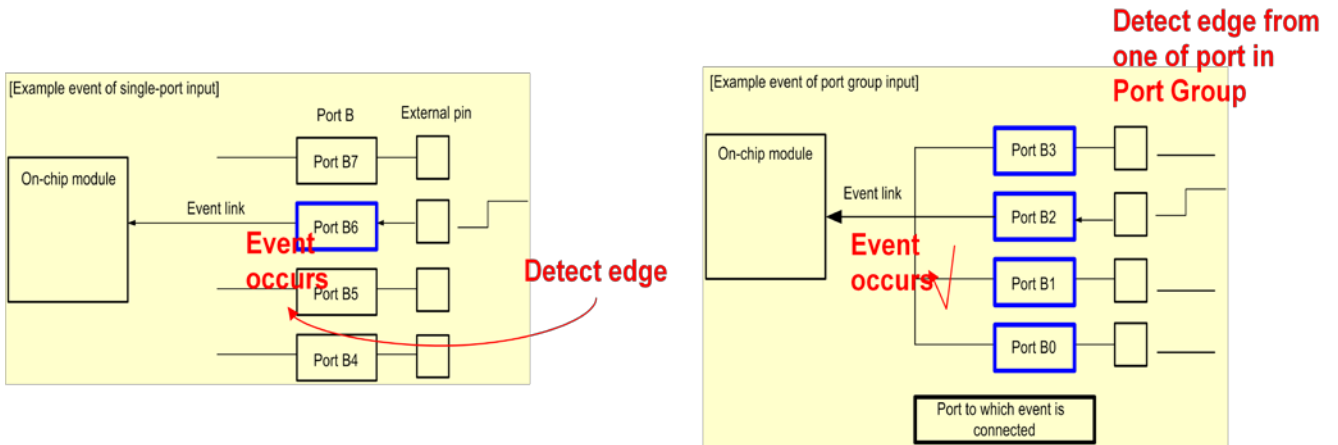
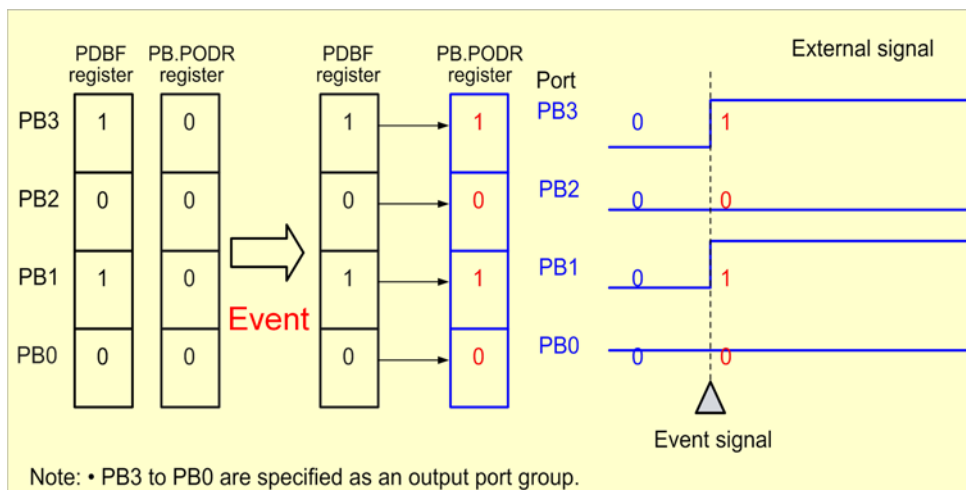


Figure 1.5: Using ports as input to the ELC

Similarly, when the ports are used as “target” for ELC activation, then it is possible to configure either the single ports or port groups to go high, go low or toggle states on receiving an ELC trigger.

It is also possible to configure the ports for buffer operation. The buffer operation is valid with single ports and port groups and can be used in input and output mode. When used in output mode, an ELC trigger will move the data in the buffer register to the port data registers thus changing the pin states.



Note: • PB3 to PB0 are specified as an output port group.

Figure 1.6: Output mode with buffer

Similarly, the ports can also be used with the buffers in input mode

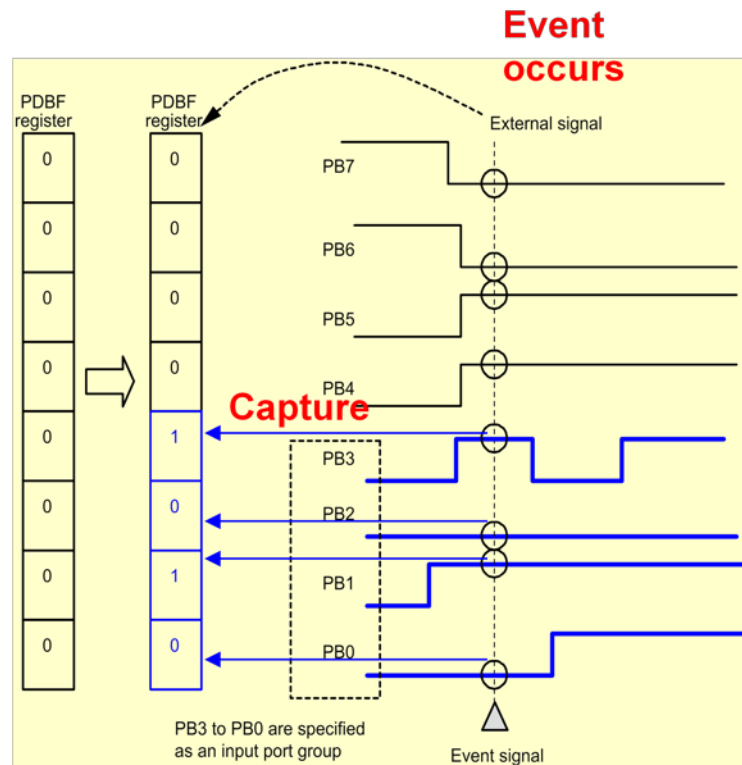


Figure 1.7: Input mode with buffer

Specific configuration of the target peripheral can be done initially and the ELC event would simply act as a trigger to start off the peripheral. In case of timers, the user would have to pre-configure the clock source, count value etc and the ELC would simply start the count.

Since the ELC linkage takes place entirely in hardware, it allows for quicker response times for a variety of conditions and more flexibility. It also allows lower power consumption by precluding or minimizing the need for CPU operation in low power modes while performing tasks like periodic A/D sampling using timers or moving data around using the DTC.

One key point to remember is that since the Event Signals from the peripherals are also routed as interrupts to the CPU, there will be parallel paths of activity. Thus if CMT1 generated a compare match signal it would be routed both to the ELC and to the Interrupt Controller Unit (ICU) potentially creating parallel paths of execution. This is explained in more detail in the following section

For more information on the ELC, refer to the Renesas Interactive Module on ELC and the RX210 hardware manual.

1.3 Running the Program.

This workspace was written for and tested on the RX210 RSK. C

1. Connect a variable power supply (2-5V) to the RSK and set it to 5 volts.
2. Connect the E1 debugger to the PC and the RSK.
3. Compile and download the code to the RSK.
4. The program configures the MCU to output BCLK on the PSTOP1 pin which is located on J2-16 on the RSK. BCLK is configured as main clock source/4.
5. Connect an oscilloscope probe to J2-16 so that BCLK can be viewed.
6. Run the program. The oscilloscope should show BCLK at 25 MHz.
7. Reduce the voltage to below 3.1 volts. The BCLK will now be at 31.2 Khz.
8. Turn the voltage back up above 3.1 volts and BCLK will revert to 25 MHz.

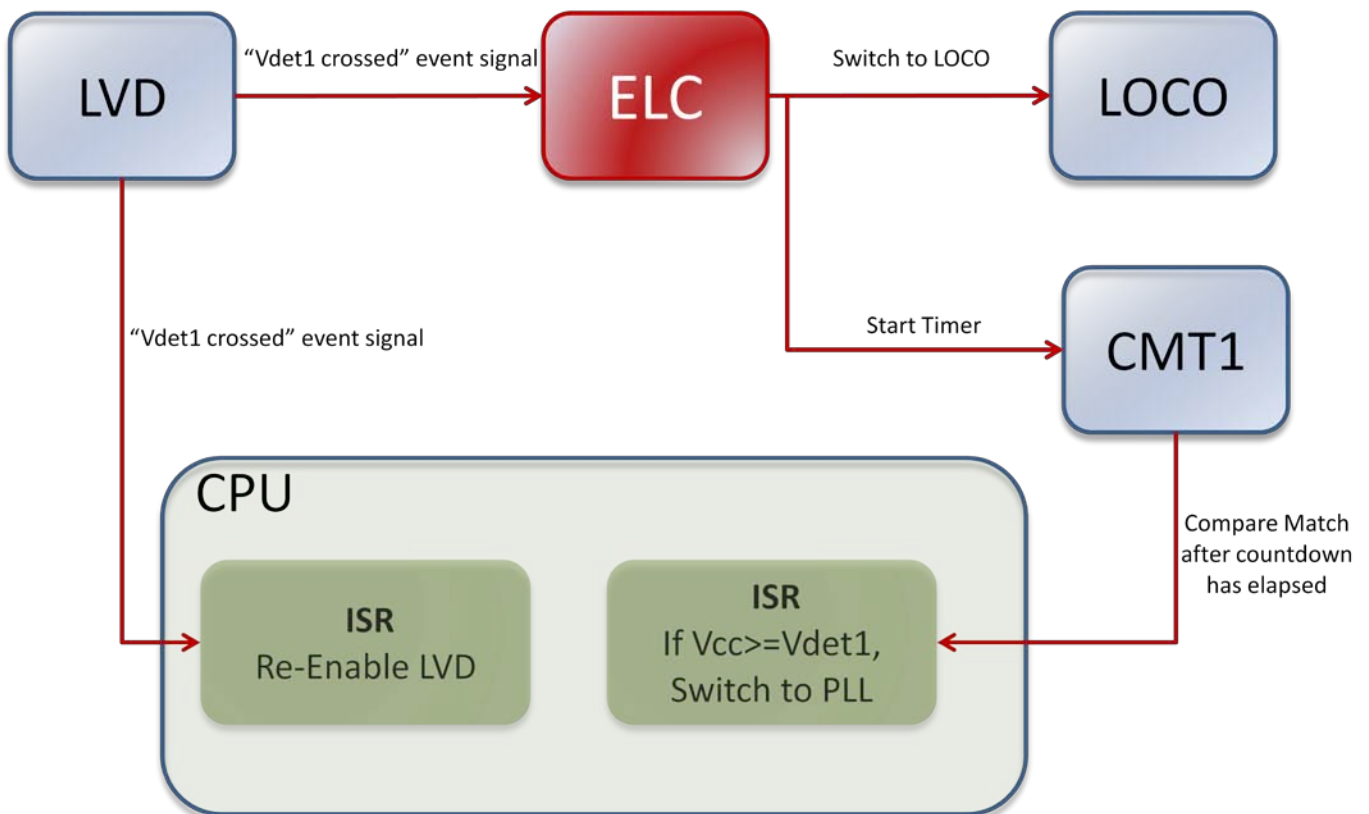
2. Project Files

File Name	Functions	Description
Main.c	main()	The main() function calls the initialization routines and then enters a while loop
ELC.c	config_elc()	The config_elc() function configures the ELC to link the LVD events to the LOCO and the CMT1 timer
CMT.c	config_cmt1() Excep_CMTU0_CMT1()	The config_cmt1() function configures the timer for compare match operation. The interrupt handler reconfigures the PLL.
LVD.c	config_lvd() Excep_LVD1()	The config_lvd() module configures the LVD to detect a voltage level and generates events on level crossing. The ISR re-enables the LVD module.
Hwsetup.c	config_clock()	Configures the clock sources for the MCU.

3. Project Description

3.1 Operation

The following is a flow diagram showing how events are routed in the project. The idea is to detect the value of Vcc and when it steps below a certain threshold, switch clock source to the LOCO and when Vcc crosses above a certain voltage threshold, switch to the PLL as the main clock source. The majority of this activity can be accomplished without using the CPU by directly linking the peripherals using the ELC. The areas shaded in green require CPU processing.



The LVD1 is configured to detect a voltage level of 3.1 volts on the Vcc input and generate an interrupt when Vcc goes across the 3.1 volt level. Thus an event/interrupt will be generated when Vcc goes above or below 3.1 volts.

The timer CMT1 is configured to run in 8 bit mode (ELC linking does not support 16 bit mode for CMT) and uses PCLK/8 as its count source. Since PCLK is configured as PLL/4, which would mean that the CMT1 counting clock frequency is PLL/32 or 3.125 MHz. When the LOCO is the main clock source, the frequency would be 125KHz/32 or 3.9 KHz. Thus the maximum time delay possible by using a compare match value of 0xFF is 800 useconds with the PLL and 250 milliseconds with the LOCO.

However, since the CMT will only ever be triggered while the LOCO is the clock source, the timer will take approximately 250 ms to countdown and jump to the ISR.

The ELC is configured to activate both the “Switch to LOCO” and “Start CMT1” when it receives a signal from the LVD. The “Switch to LOCO” action happens immediately in receiving the ELC trigger and will happen irrespective of whether Vcc is above or below 3.1 volts since the LVD will generate and even for both these conditions. The CMT1 timer will jump into the ISR after the compare-match countdown has elapsed and in the ISR determine the value of Vcc by reading the LVD1MON bit. If the Vcc value is above 3.1 volts, then the clock source will be switched to the PLL. The delay was instituted here to prevent a potential conflict since there is a parallel path of execution here where the MCU would be trying to switch to LOCO and the PLL at the same time if the 250ms delay was not implemented by the compare match timer.

4. Notes

1. Any pre-configurable modules like the Timer, A/D etc have to be pre-configured before enabling the ELC. Similarly when changing the configuration for these modules, disable the ELC before doing so.
2. Make sure that parallel paths of execution do not result in race conditions.

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Revision Record

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		Page	Summary
1.00	June.07.12	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

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1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

- The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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