RL78/G1E Group

Example of Measurement Using a Force Sensor

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Introduction

This application note describes how to measure a physical quantity (force) based on the resistance of a piezoresistive sensor, by using the configurable amplifier, A/D converter, and D/A converter incorporated in the RL78/G1E (R5F10FMx).

In this application note, the PTF (polymer thick film) force sensor FSR 402 (made by Interlink Electronics Inc.) is used as the piezoresistive sensor.

Operation Verified Devices

RL78/G1E (R5F10FMx (x = C, D, or E))

When this application note is applied to other microcontrollers, make the necessary changes according to the specifications of the microcontroller and verify them thoroughly.

Contents

1. Specifications

This application note describes how a piezoresistive sensor is used by providing an example of a system in which the RL78/G1E (R5F10FMx) is used to measure the force based on the amount the resistance of a PTF force sensor (FSR 402) changes.

In this application note, a case is presented in which the resistance of a force sensor is converted to a voltage and then amplified by using the configurable amplifier (used as a transimpedance amplifier) incorporated in the RL78/G1E (R5F10FMx).

The RL78/G1E subtracts the voltage output from the on-chip D/A converter from the voltage output from the configurable amplifier (used as a differential amplifier) incorporated in the RL78/G1E (R5F10FMx) to obtain the offset of the output voltage, uses the offset to cancel the bias voltage, and then amplifies the resulting signal.

The converted and amplified voltage (single-ended voltage) is further converted to a digital value by using the A/D converter incorporated in the RL78/G1E (R5F10FMx).

The force is calculated from the obtained digital value, and the result is displayed on the LCD module (ACM0802C) connected to the RL78/G1E (R5F10FMx).

Figure 1.1 shows a block diagram, and **Table 1.1** shows the elements included in the block diagram.

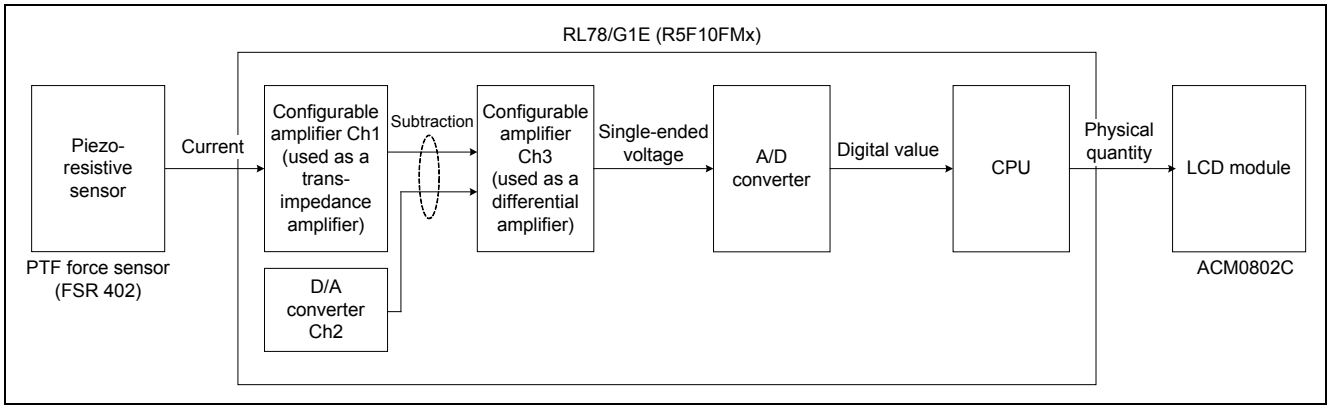


Figure 1.1 Block Diagram

Table 1.1 Description of the Elements in the Block

Element	Function	Description
PTF force sensor FSR 402	Piezoresistive sensor	Sensor whose resistance changes in accordance with an applied force.
RL78/G1E (R5F10FMx)	Configurable amplifier Ch1 (used as a transimpedance amplifier)	Converts the resistance of the PTF force sensor to a voltage and amplifies it.
	Configurable amplifier Ch3 (used as a differential amplifier)	Cancels and amplifies the offset of the voltage output from the configurable amplifier (used as a transimpedance amplifier).
	D/A converter Ch2	Generates the voltage input to the configurable amplifier (used as a differential amplifier). This voltage is used to cancel the bias voltage generated in the configurable amplifier Ch1 (used as a transimpedance amplifier).
	A/D converter	Converts the voltage output from the configurable amplifier Ch3 (used as a differential amplifier) to a digital value.
	CPU	Calculates the physical quantity (force) from the digital value converted by the A/D converter.
ACM0802C	LCD module	Displays the physical quantity (force) calculated by the CPU.

2. Conditions for Verifying Operation

The operation of the sample code shown in this application note has been verified under the conditions shown below.

Table 2.1 Conditions for Verifying Operation

Item	Description
Microcontroller used	RL78/G1E (R5F10FME)
Operating frequency	• High-speed on-chip oscillator (high-speed OCO) clock: 32 MHz • CPU/peripheral hardware clock: 32 MHz
Operating voltage	V_{DD}, DV_{DD}, AV_{DD1}, AV_{DD2}, AV_{DD3}, and LCD module power supply: 5.0 V AV_{DD}: 3.3 V LVD detection voltage (V_{LVIH}): 4.06 V when rising, 3.98 V when falling
External devices used	• PTF force sensor (FSR 402) • LCD module (ACM0802C-NLW-BBH)
Integrated development environment	CubeSuite+ V1.01.01 [31 Jan 2012] made by Renesas Electronics
C compiler (build tool)	CA78K0R V1.30 made by Renesas Electronics

3. Related Application Notes

Related application notes are shown below. Also refer to these documents when using this application note.

- RL78/G13 Initialization (R01AN0451E) Application Note
- RL78/G13 Timer Array Unit (Interval Timer) (R01AN0456E) Application Note
- RL78/G13 Serial Array Unit for 3-Wire Serial I/O (Master Transmission/Reception) (R01AN0460E) Application Note

4. Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of the hardware configuration described in this application note.

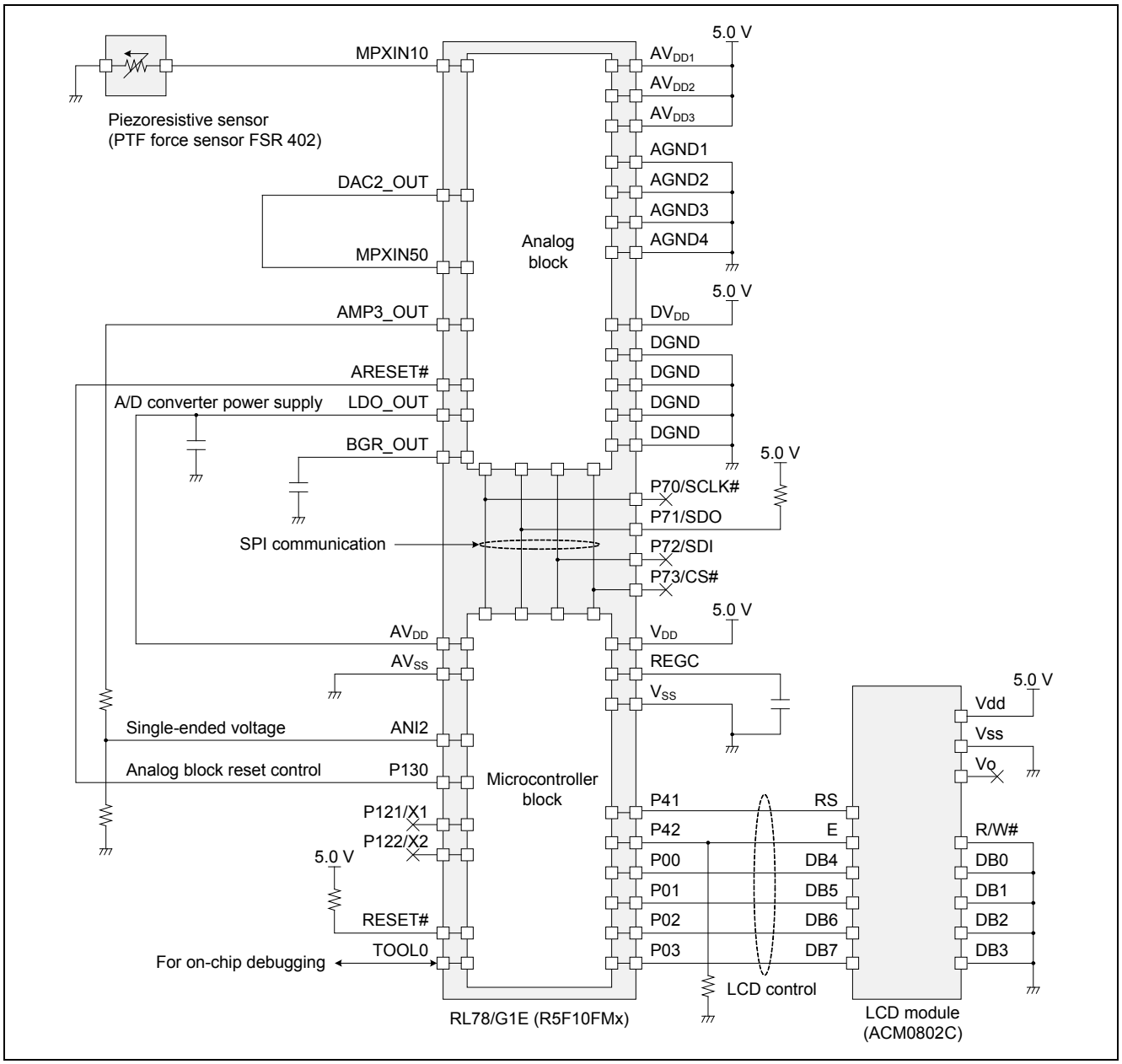


Figure 4.1 Hardware Configuration

Caution This circuit diagram is simplified to show an overview of the circuit connection. When designing an actual circuit, connect pins appropriately so as to satisfy the electrical specifications. (Connect unused input-only ports individually to VDD or VSS via a resistor.)

4.2 Functions Used

Table 4.1 shows the RL78/G1E (R5F10FMx) peripheral functions used in this application note and their applications.

Table 4.1 RL78/G1E (R5F10FMx) Peripheral Functions and Their Applications

RL78/G1E (R5F10FMx) Peripheral Function		Application
Analog block	Configurable amplifier Ch1	Used as a transimpedance amplifier that converts the resistance of the PTF force sensor to a voltage and amplifies it.
	Configurable amplifier Ch3	Used as a differential amplifier that subtracts the D/A converter Ch2 output voltage from the configurable amplifier Ch1 (used as a transimpedance amplifier) output voltage, uses the obtained offset voltage to cancel the bias voltage, and amplifies the result.
	D/A converter	Generates the bias voltage generated in configurable amplifier channels Ch1 and Ch3 (used as a transimpedance amplifier and a differential amplifier, respectively) and the voltage input to configurable amplifier Ch3 (used as a differential amplifier) that is used to cancel the bias voltage generated in configurable amplifier Ch1 (used as a transimpedance amplifier).
	Variable output voltage regulator	Generates the power supply voltage for the A/D converter.
	SPI	Controls SPI communication with the microcontroller block of the RL78/G1E (R5F10FMx).
Microcontroller block	A/D converter	Converts the voltage output from configurable amplifier Ch1 (used as a differential amplifier) to a digital value.
	Serial array unit 1 (channel 1: CSI21)	Controls SPI communication with the analog block by using the 3-wire serial I/O function.
	I/O ports	Controls the analog block and external LCD module.
	Timer array unit 0 (channel 1)	Generates a hardware trigger signal for the A/D converter.
	Timer array unit 0 (channel 3)	Generates the wait time used by software.
	High-speed on-chip oscillator (high-speed OCO)	Generates the 32 MHz clock used as the main system clock.

4.3 Pins Used

Table 4.2 shows the RL78/G1E (R5F10FMx) pins used in this application note and their features.

Table 4.2 RL78/G1E (R5F10FMx) Pins Used and Their Features

Pin Name	I/O	Description
MPXIN10	Input	This is an inverted input pin of the configurable amplifier Ch1 (used as a transimpedance amplifier) in the analog block. This pin is connected to the PTF force sensor.
DAC2_OUT	Output	This is an output pin of the D/A converter Ch2. This pin is connected to MPXIN50 which is the inverted input pin of the configurable amplifier Ch3 (used as a differential amplifier) in the analog block. This pin is used to cancel the bias voltage genetated in the configurable amplifier Ch1 (used as a transimpedance amplifier).
MPXIN50	Input	This is an inverted input pin of the configurable amplifier Ch3 (used as a differential amplifier) in the analog block. This pin is connected to DAC2_OUT which is the output pin of the D/A converter Ch2.
AMP3_OUT	Output	This is an output pin of the configurable amplifier Ch3 (used as a differential amplifier) in the analog block. This pin is connected to ANI2 which is the analog input pin of the A/D converter in the microcontroller block via a resistor divider.
ANI2	Input	This is an analog input pin of the A/D converter in the microcontroller block. This pin is connected to the AMP3_OUT pin in the analog block via a resistor divider which steps down the output voltage from the AMP3_OUT pin. The output voltage stepped down is to be A/D converted.
P130	Output	P130 is an output-only pin in the microcontroller block. This pin is connected to the ARESET# pin in the analog block and is used to control the analog reset feature of the analog block.
P41	Output	P41 is an output pin in the microcontroller block. This pin is connected to the RS pin in the LCD module and is used to control the LCD module display.
P42	Output	P42 is an output pin in the microcontroller block. This pin is connected to the E pin in the LCD module and is used to control the LCD module display.
P00	Output	P00 is an output pin in the microcontroller block. This pin is connected to the DB4 pin in the LCD module. This pin is used to control the LCD module display.
P01	Output	P01 is an output pin in the microcontroller block. This pin is connected to the DB5 pin in the LCD module and is used to control the LCD module display.
P02	Output	P02 is an output pin in the microcontroller block. This pin is connected to the DB6 pin in the LCD module and is used to control the LCD module display.
P03	Output	P03 is an output pin in the microcontroller block. This pin is connected to the DB7 pin in the LCD module and is used to control the LCD module display.

5. Description of Features

5.1 Resistive Sensor

This section provides an overview of typical resistive sensors and the characteristics and operation of the PTF force sensor FSR 402 (made by Interlink Electronics Inc.).

5.1.1 Overview of resistive sensors

The folllowing sensors typically output a resistance value:

- Thermistor

  A thermistor is a resistor whose resistance changes significantly with temperature and is used as a temperature sensor.

- Magnetoresistive element (MR) sensor

  A magnetoresistive element is an element that uses the magnetoresistance effect in which the electrical resistance changes according to the magnetic flux density. The change depends on the material. For semiconductor magnetororesistive elements, the resistance is proportional to the magnetic flux density. For ferromagnetic resistive elements, the resistance is inversely proportional to the magnetic flux density.

- Polymer thick film (PTF)

  The resistance changes when a force is applied to the sensing area. The larger the force is, the smaller the resistance becomes.

5.1.2 Overview of PTF force sensor (FSR 402)

An overview of the PTF force sensor FSR 402 is shown below.

The following shows the electrical characteristics extracted from the datasheet of the PTF force sensor FSR 402 that were referenced when studying the product in this application note. Before using the product, be sure to download the latest datasheet from the Interlink Electronics website.

The extracted specifications of the PTF force sensor FSR 402 are shown in **Table 5.1**.

Table 5.1 PTF Force Sensor FSR 402 Extracted Specifications

PARAMETER	VALUE	NOTES
Force Sensitivity Range	10 g to 10 kg (0.1N to 100N)	Dependent on mechanics
Break Force (Actuation Force)	10 g (0.1N)	Dependent on mechanics and FSR build
Part-to-Part Force Repeatability	±6% of established nominal	With a repeatable actuation system
Single Part Force Repeatability	±2% of initial reading	With a repeatable actuation system
Hysteresis	±10% Average	$(R_{F+} - R_{F-}) / R_{F+}$
Long Term Drift	< 5% per $\log_{10}$ (time)	Tested to 35 days, 1 kg load
Stand-Off Resistance	> 10 MΩ	Unloaded, unbent
Maximum Current	1 mA/cm^2 of applied force	–

The characteristics of the PTF force sensor FSR402 vary depending on factors such as the material and shape of the object that applies the force to the sensing area. In this application note, a pressurizing device (a φ1.3 cm round plastic sheet with a flat pressurizing surface that contacts the sensing area) is used to evaluate the characteristics (with a force of 100 g to 500 g). The approximate line obtained from the evaluation result is shown below.

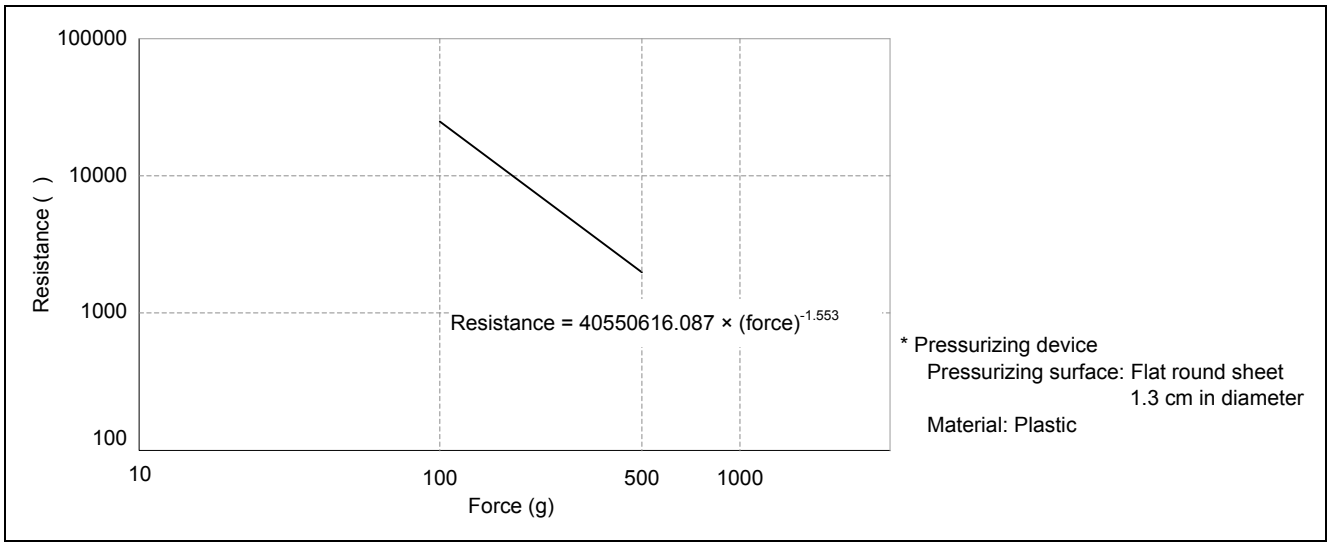


Figure 5.1 Force vs. Resistance in PTF Force Sensor FSR 402

An approximation formula is shown in *Formula 1* below, where RFSR (Ω) is the resistance and F (g) is the force when using the PTF force sensor FSR 402:

$$RFSR = 40550616.087 \times F^{-1.553} \quad \text{...} \quad \textbf{Formula 1}$$

5.2 Configurable Amplifier (Used As a Differential Amplifier)

This section shows how a signal output from the piezoresistive sensor is amplified by using two different methods: a general amplifier and signal converter, and an amplifier and signal converter that are configured by using the configurable amplifier of the RL78/G1E (R5F10FMx).

5.2.1 Example of general amplifier and signal converter

In this application note, the changes in resistance are converted to changes in voltage by using the configurable amplifiers as a transimpedance amplifier and a differential amplifier.

A general transimpedance amplifier and a differential amplifier are shown in **Figure 5.2**.

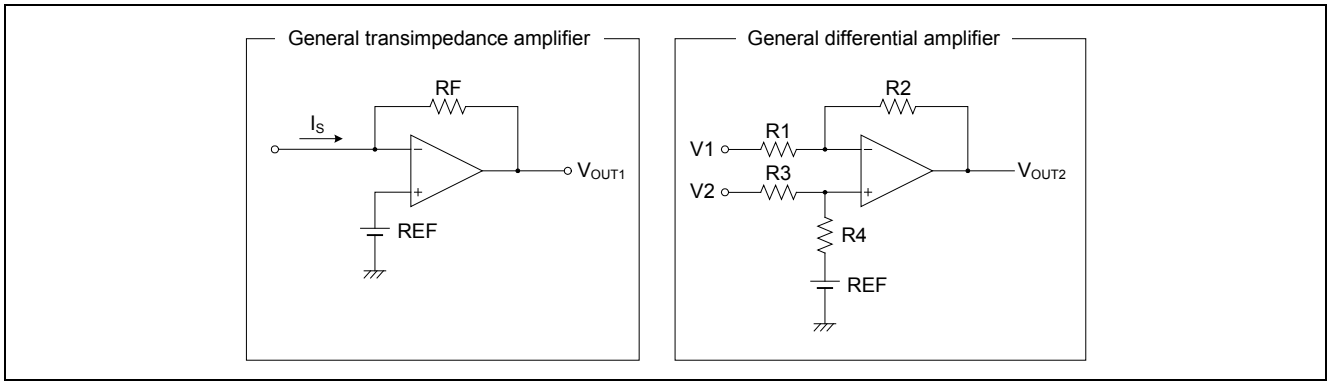


Figure 5.2 General Transimpedance Amplifierand and Differential Amplifier

The voltage output from a general transimpedance amplifier (V_{OUT1}) is obtained by using the following formula:

$$V_{OUT} = -RF \times I_S + REF \quad \text{... Formula 2}$$

A differential amplifier amplifies the difference between two input voltages and converts the result to a single-ended voltage to be output. In general differential amplifiers, the output voltage (V_{OUT2}) is expressed by using the following formula, where R1 = R3 and R2 = R4:

$$V_{OUT2} = (V2 - V1) \times \frac{R2}{R1} + REF \quad \text{... Formula 3}$$

In this application note, the configurable amplifier in the configuration of a transimpedance amplifier is connected to a piezoresistive sensor. **Figure 5.3** shows the connection between the transimpedance amplifier and the piezoresistive sensor.

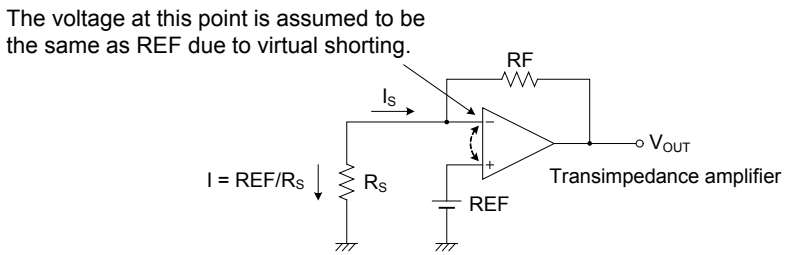


Figure 5.3 Connection Between Transimpedance Amplifier and and Piezoresistive Sensor

In the transimpedance amplifier shown in **Figure 5.3**, the voltage at the non-inverting input pin and the inverting input pin is assumed to be the same due to virtual shorting. Therefore, the current I (A) is expressed by using the following formula, where Rs (Ω) is the resistance of the piezoresistive sensor:

$$I = \frac{REF}{R_S} \quad \cdots \quad \textbf{Formula 4}$$

The voltage output from the transimpedance amplifier (V_{OUT}) is expressed by using the following formula, based on *Formula 2*.

$$V_{OUT} = RF \times \frac{REF}{R_S} + REF = \left(\frac{RF}{R_S} + 1 \right) \times REF \quad \cdots \quad \textbf{Formula 5}$$

5.2.2 Example of amplifier and signal converter configured by using a configurable amplifier

Figure 5.4 shows an example of an amplifier and signal converter that are configured by using the configurable amplifier incorporated in the RL78/G1E (R5F10FMx) and amplifies and converts the resistance to a voltage.

In this application note, configurable amplifier Ch1 is used as a transimpedance amplifier and configurable amplifier Ch3 is used as a differential amplifier.

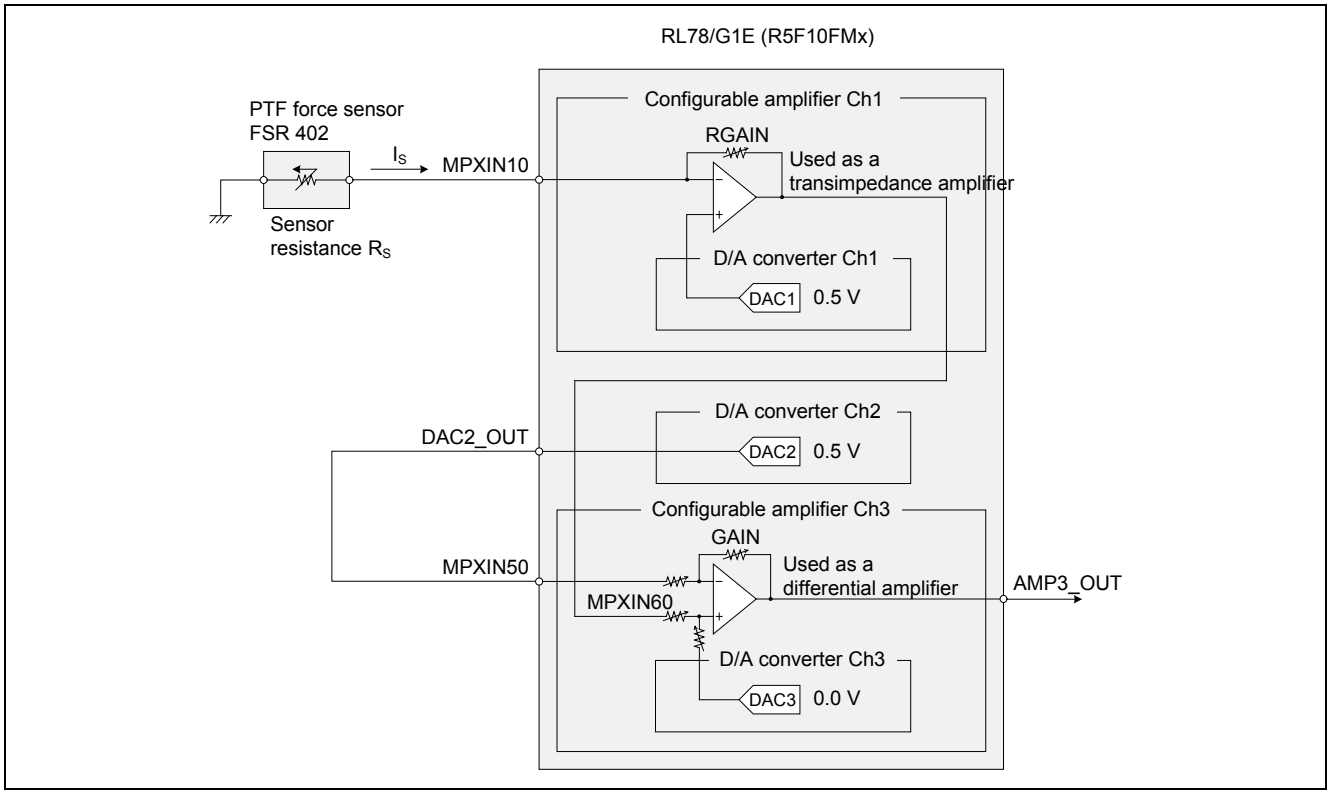


Figure 5.4 Amplifier and Signal Converter Configured by Using a Piezoresistive Sensor

AMP1_OUT (V), the voltage output from configurable amplifier Ch1 (used as a transimpedance amplifier), is expressed as shown in *Formula 5*, where DAC1 is the D/A converter Ch1 output voltage (V) and RGAIN (Ω) is the feedback resistance of the transimpedance amplifier.

$$AMP1\_OUT = \left(\frac{RGAIN}{R_S} + 1 \right) \times DAC1 \quad \text{...} \quad \textbf{Formula 6}$$

If RGAIN (feedback resistance) of configurable amplifier Ch1 (used as a transimpedance amplifier) is 20 kΩ and DAC1 (D/A converter Ch1 output voltage) is 0.5 V, AMP1_OUT in *Formula 6* is expressed as follows:

$$AMP1\_OUT = \left(\frac{20k}{R_S} + 1 \right) \times 0.5 = \frac{10k}{R_S} + 0.5 \quad \text{...} \quad \textbf{Formula 7}$$

AMP3_OUT (V), the voltage output from configurable amplifier Ch3 (used as a differential amplifier), is expressed by using the following formula, where MPXIN50 (V) is the voltage of the inverting input source and MPXIN60 (V) is the voltage of the non-inverting input source for configurable amplifier Ch3 (used as a differential amplifier), GAIN is the gain, and DAC3 (V) is the D/A converter Ch3 output voltage, from *Formula 3*:

$$AMP3\_OUT = (MPXIN60 - MPXIN50) \times GAIN + DAC3 \quad \text{...} \quad \textbf{Formula 8}$$

Connect the inverting input source (MPXIN50) of configurable amplifier Ch3 (used as a differential amplifier) to the D/A converter Ch2 output pin (DAC2_OUT), and the non-inverting input source to the output pin (AMP1_OUT) of configurable amplifier Ch1 (used as a transimpedance amplifier). 0.5 V is output to the D/A converter Ch2 output pin (DAC2_OUT) to cancel the bias voltage generated in configurable amplifier Ch1 (used as a transimpedance amplifier).

If GAIN in configurable amplifier Ch3 (used as a differential amplifier) is two times and the D/A converter Ch3 output voltage (DAC3) is 0 V, AMP3_OUT (V), the voltage output from configurable amplifier Ch3 (used as a differential amplifier), is expressed by using the following formula, based on *Formula 7* and *Formula 8*.

$$AMP3\_OUT = (AMP1\_OUT - 0.5) \times 2 + 0 = \frac{20k}{R_S} \quad \text{...} \quad \textbf{Formula 9}$$

Figure 5.5 shows the relationship between the resistance (Rs) of the PTF force sensor FSR 402 and the voltage output from configurable amplifier Ch3 (used as a differential amplifier).

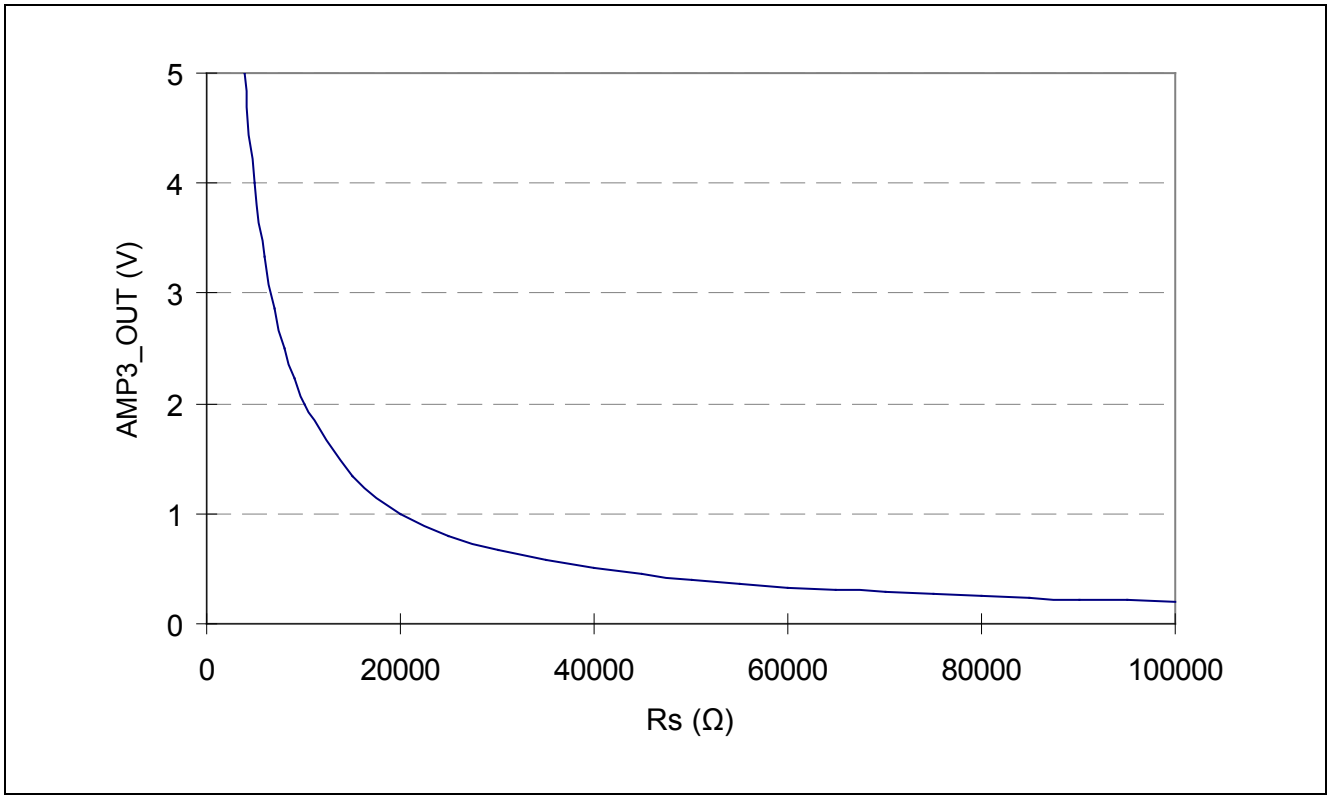


Figure 5.5 Resistance of PTF Force Sensor (Rs) vs. Voltage Output from Configurable Amplifier Ch3 (AMP3_OUT)

5.3 A/D Converter

This section describes the A/D converter incorporated in the RL78/G1E (R5F10FMx), which is used to convert the resistance signal amplified and converted by configurable amplifier Ch1 (used as a transimpedance amplifier) and configurable amplifier Ch3 (used as a differential amplifier) to a digital value.

5.3.1 Overview of A/D converter incorporated in RL78/G1E (R5F10FMx)

The A/D converter incorporated in the RL78/G1E (R5F10FMx) is used to convert an analog input to a digital value. Seventeen analog input channels are available for analog input. 12-bit resolution or 8-bit resolution can be selected.

The settings specified for the A/D converter incorporated in the RL78/G1E (R5F10FMx) are shown below.

- Trigger mode: Hardware trigger no-wait mode
- Channel selection mode: Select mode
- Conversion mode: One-shot conversion mode
- Analog input pin: ANI2
- Conversion resolution: 12 bits
- Reference voltage: AV_{DD} = 3.3 V, AV_{SS} = 0 V

5.3.2 Connecting configurable amplifier Ch3 (used as a differential amplifier) to the A/D converter

The maximum power supply voltage of the A/D converter incorporated in the RL78/G1E (R5F10FMx) is 3.6 V. The power supply voltage used in this application note is 5.0 V, so a stepped down voltage must be supplied to the A/D converter. To achieve this, the output voltage from the variable output voltage regulator in the analog block is set to be 3.3 V (Typ.), which is supplied to the AV_{DD} pin.

Connect the output pin (AMP3_OUT) of the configurable amplifier Ch3 (used as a differential amplifier) in the analog block to the ANI2 analog input pin of the A/D converter. Note that the analog voltage output from AMP3_OUT is 0 to 5 V. To make the output voltage from AMP3_OUT lower than AV_{DD}, therefore, step down it to 0 to 3 V by using a resistor divider and input it to the ANI2 analog input pin of the A/D converter.

Figure 5.6 shows the connection between the configurable amplifier Ch3 (used as a differential amplifier) and the A/D converter incorporated in the RL78/G1E (R5F10FMx).

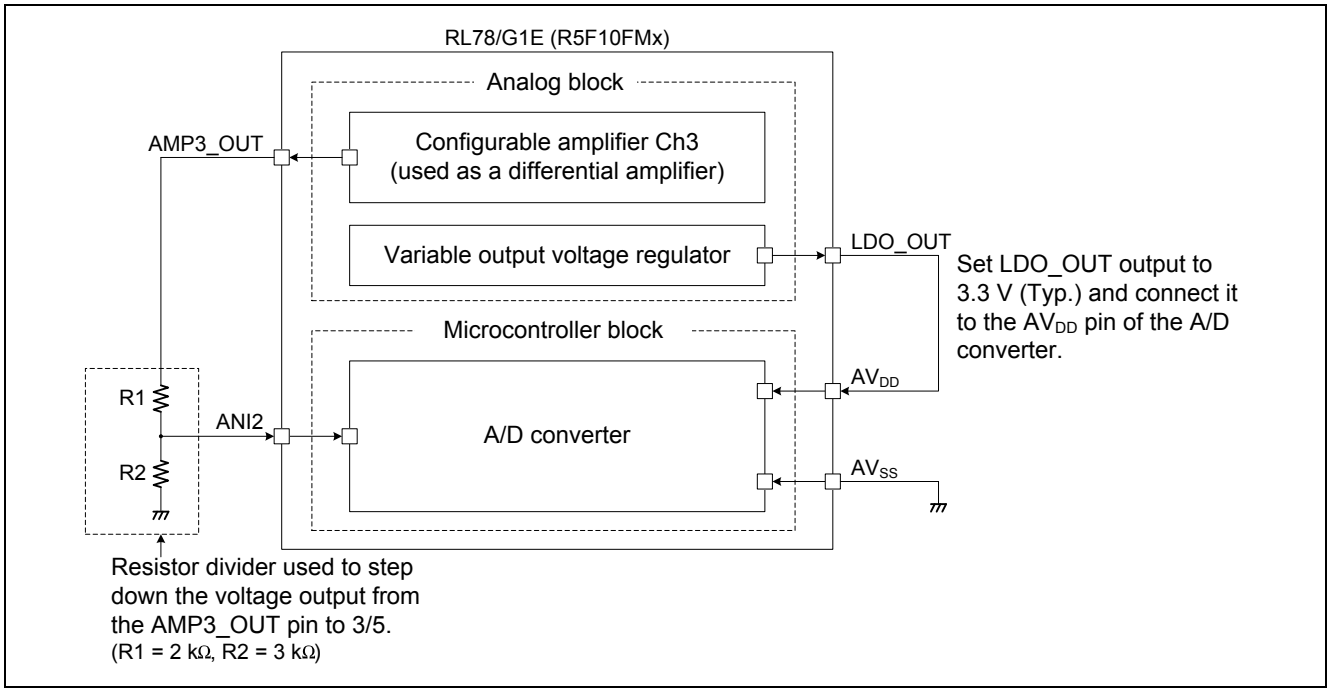


Figure 5.6 Connection Between Configurable Amplifier Ch3 (Used As a Differential Amplifier) and A/D Converter

5.4 CPU (Arithmetic Operation)

This section describes how the CPU calculates the physical quantity (force) based on the A/D conversion result.

The analog voltage input to the ANI2 pin, which is calculated from the A/D conversion result (stored in the 12-bit A/D conversion result register (ADCR)) is expressed as shown in the formula below:

$$ANI2 = \frac{AD\_conversion\_value}{2^{12}-1} \times AV_{DD} \quad \text{... Formula 10}$$

AVDD: Power supply voltage input to the A/D converter (V)
ANI2: Voltage input to analog input pin 2 of the A/D converter (V)

Because the analog voltage output from the AMP3_OUT pin is divided by using the resistor divider and then input to the ANI2 pin, the AMP3_OUT pin voltage (V) is expressed as shown in the formula below (see ***Figure 5.6***):

$$AMP3\_OUT = ANI2 \times \frac{R1+R2}{R2} \quad \text{... Formula 11}$$

The voltage output from the AMP3_OUT pin is expressed as shown in *Formula 9*, so based on *Formula 9* and *Formula 10*, *Formula 11* is expressed as shown below:

$$\frac{20k}{R_S} = \frac{AD\_conversion\_value}{2^{12}-1} \times AV_{DD} \times \frac{R1+R2}{R2} \quad \text{... Formula 12}$$

RS: Resistance of PTF force sensor (Ω)

From *Formula 12*, the resistance (RS) (Ω) of the PTF force sensor FSR 402 is expressed by using the following formula:

$$R_S = 20k \times \frac{2^{12}-1}{AD\_conversion\_value} \times \frac{1}{AV_{DD}} \times \frac{R2}{R1+R2} \quad \text{... Formula 13}$$

Here, based on *Formula 1*, the force (g) (physical quantity) is expressed by using the following formula:

$$Force = \left(\frac{R_S}{40550616.087} \right)^{-\frac{1}{1.553}} \quad \text{... Formula 14}$$

Based on *Formula 13* and *Formula 14*, if AVDD = 3.3 V, R1 = 2 kΩ, and R2 = 3 kΩ, the formula to obtain the force (g) (physical quantity) from the A/D conversion result is expressed by using the following formula:

$$Force = \left(\frac{1}{40550616.087} \times \frac{2^{12}-1}{AD\_conversion\_value} \times \frac{12k}{3.3} \right)^{-\frac{1}{1.553}} \quad \text{... Formula 15}$$

Note The setting values of Formula 15 are the reference values. When using the Fomula 15, set the appropriate values based on the user's evaluation.

5.5 LCD Module

This section describes the contents displayed in the LCD module (ACM0802C).

(1) Specifications of the LCD module

- Model name: ACM0802C-NLW-BBH
- Manufacturer: AZ Displays, Inc.
- Number of displayed characters: 8 characters × 2 lines
- Power supply voltage: 5 V

(2) Displaying the calculation result (physical quantity)

Figure 5.7 shows how the calculation result (force) is displayed on the LCD module. The calculation result is displayed on the upper line. The number is displayed to the first decimal place, justified to the left. The unit is displayed as g. The averaged A/D conversion value is displayed in three-digit hexadecimal on the bottom line.

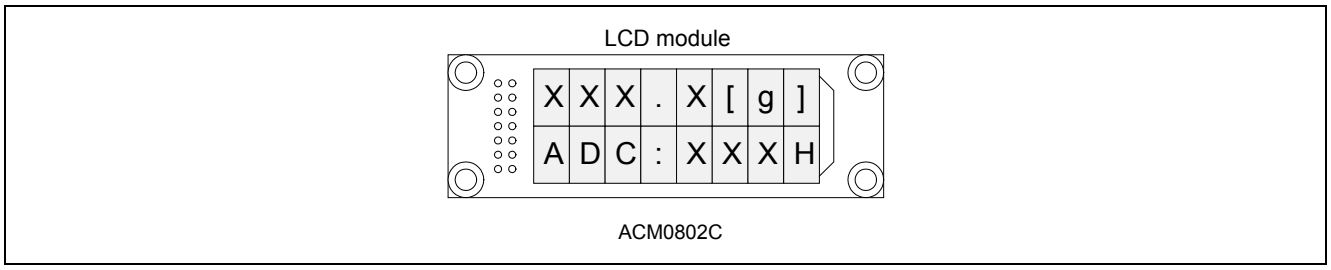


Figure 5.7 LCD Module Display Format

6. Analog Block of RL78/G1E (R5F10FMx)

This section describes the functions used in the analog block of the RL78/G1E (R5F10FMx).

6.1 Overview of Analog Block of RL78/G1E (R5F10FMx)

The analog block of the RL78/G1E (R5F10FMx) has on-chip circuits such as configurable amplifiers, a gain adjustment amplifier, a filter circuit, D/A converters, and a temperature sensor, allowing the R5F10FMx to be used as an analog front-end circuit for processing very small sensor signals.

The block diagram of the analog block of the RL78/G1E (R5F10FMx) is shown below. The blocks described in the following sections are shaded.

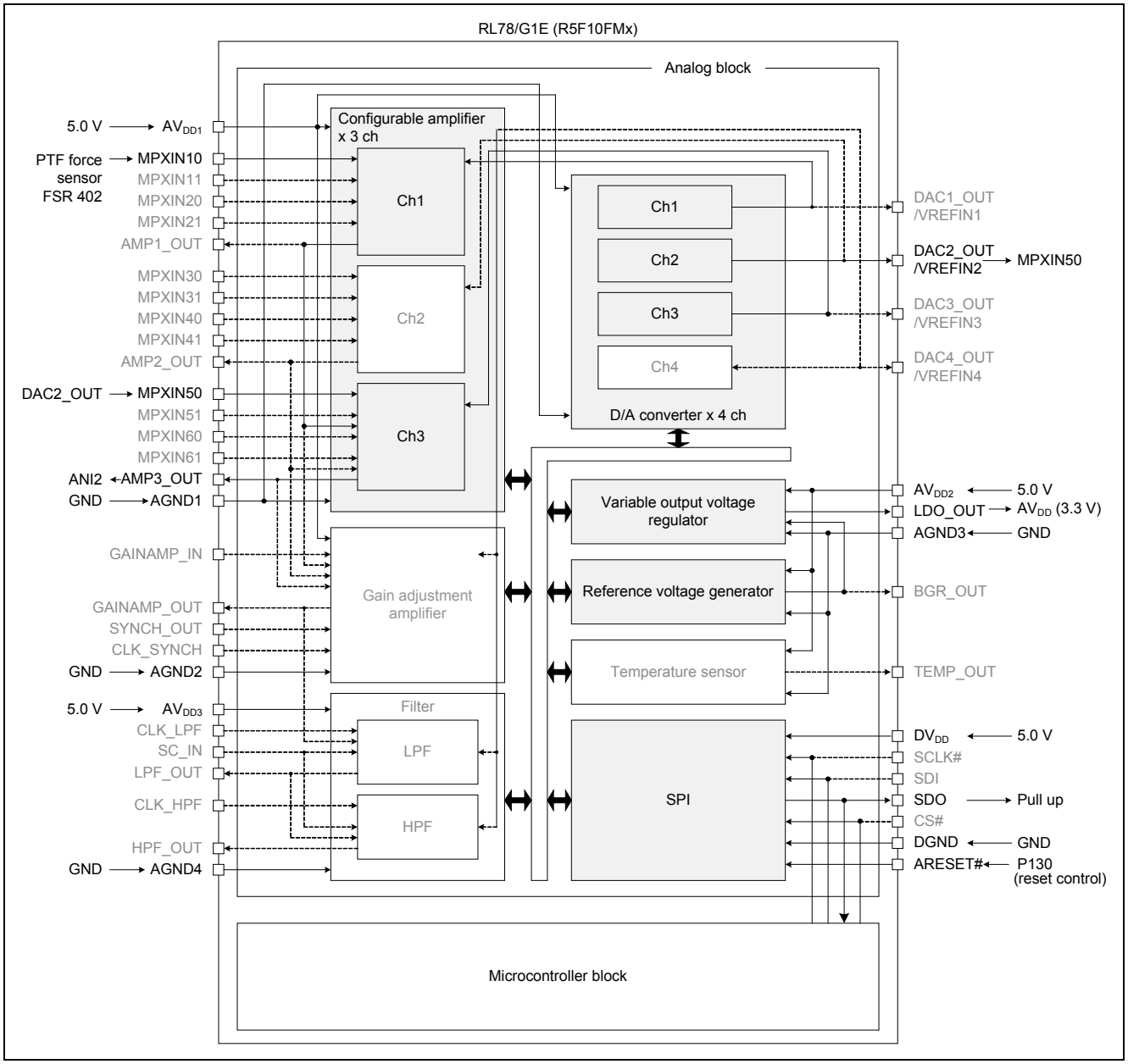


Figure 6.1 Block Diagram of Analog Block of RL78/G1E (R5F10FMx)

6.2 Functions of Analog Block of RL78/G1E (R5F10FMx)

This section describes the analog block of the RL78/G1E (R5F10FMx) used in this application note in detail.

6.2.1 Configurable amplifier

In this application note, configurable amplifier Ch1 is used as a transimpedance amplifier and configurable amplifier Ch3 is used as a differential amplifier.

(1) Overview of configurable amplifier features

The RL78/G1E (R5F10FMx) has three on-chip configurable amplifier channels.

By specifying settings in the SPI control registers, the configurable amplifiers can be used to realize the following features:

Table 6.1 Overview of Configurable Amplifier

Description	Overview
Non-inverting amplifier	• The gain can be specified between 10 dB and 40 dB in 18 steps. • Four operating modes are available. • Includes a power-off feature. * Single-channel operation
Inverting amplifier	• The gain can be specified between 6 dB and 40 dB in 18 steps of 2 dB each. • Four operating modes are available. • Includes a power-off feature. * Single-channel operation
Differential amplifier	• The gain can be specified between 6 dB and 40 dB in 18 steps of 2 dB each. • Four operating modes are available. • Includes a power-off feature. * Single-channel operation
Transimpedance amplifier	• The feedback resistance can be specified between 20 kΩ and 640 kΩ in 6 steps. • Four operating modes are available. • Includes a low-current mode. * Single-channel operation
Instrumentation amplifier	• The gain can be specified between 20 dB and 54 dB in 18 steps of 2 dB each. • Four operating modes are available. • Includes a power-off feature. * On-chip configurable amplifier × 3 ch

(2) Settings specified when using configurable amplifier Ch1 as a transimpedance amplifier

The settings specified when using configurable amplifier Ch1 as a transimpedance amplifier are as follows.

- Connect the PTF force sensor (FSR 402) to the inverted input source (MPXIN10) of configurable amplifier Ch1.
- Specify the settings as shown below when using configurable amplifier Ch1 as a transimpedance amplifier (feedback resistance: 20 kΩ).
  - <1> Set SW11 to 1, SW12 to 1, and SW13 to 1 in configuration register 1 (CONFIG1).
  - <2> Set MPX11 to 0 and MPX10 to 0 in MPX setting register 1 (MPX1) to specify the MPXIN10 pin as the source of inverted input to configurable amplifier Ch1.
  - <3> Set MPX21 to 1 and MPX20 to 0 in MPX setting register 1 (MPX1) to specify the D/A converter Ch1 output signal or the VREFIN1 pin as the source of non-inverted input to configurable amplifier Ch1.
  - <4> Set CC1 to 0 and CC0 to 0 in the AMP operation mode control register (AOMC) to specify high-speed mode as the operating mode of configurable amplifier channels Ch1 to Ch3.
  - <5> Set gain control register 1 (GC1) to 00H to specify 20 kΩ as the feedback resistance (Typ.) of configurable amplifier Ch1 (used as a transimpedance amplifier).
  - <6> Set SW01 to 0 in configuration register 2 (CONFIG2).
  - <7> Set AMP1OF to 1 in power control register 1 (PC1) to start operation of configurable amplifier Ch1 (used as a transimpedance amplifier).

Figure 6.2 shows a block diagram of configurable amplifier Ch1 when used as a transimpedance amplifier.

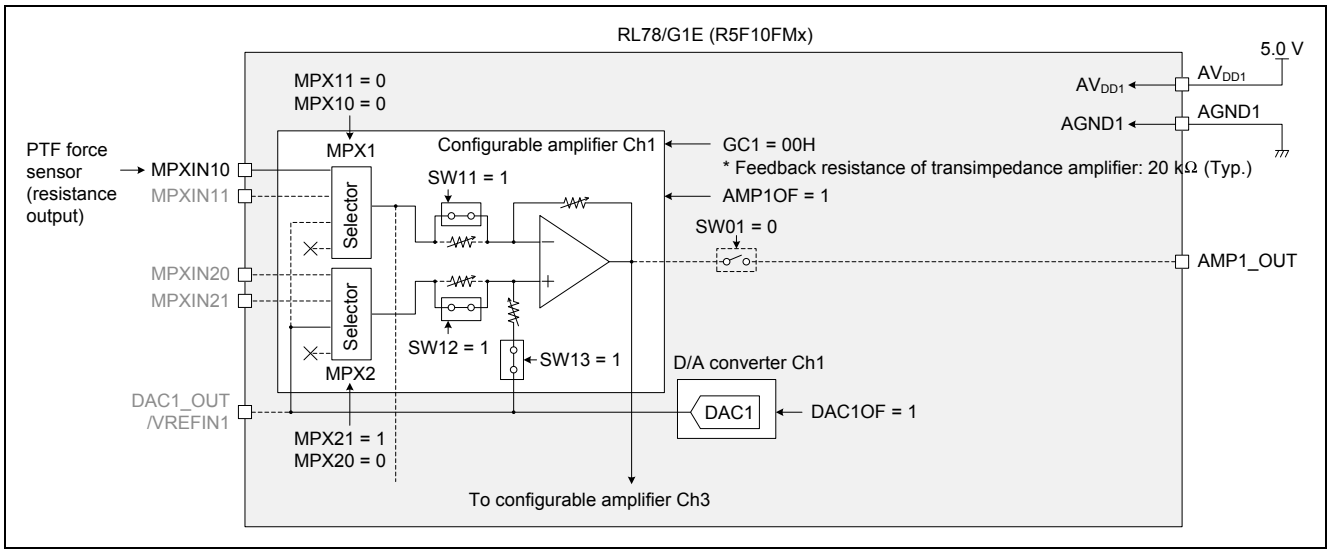


Figure 6.2 Block Diagram of Configurable Amplifier Ch1 (Used As a Transimpedance Amplifier)

(3) Settings specified when using configurable amplifier Ch3 as a differential amplifier

The settings specified when using configurable amplifier Ch3 as a differential amplifier are as follows.

- Specify the settings as shown below when using configurable amplifier Ch3 as a differential amplifier (gain: 6 dB).
  - <1> Set SW31 to 0, SW32 to 0, and SW33 to 1 in configuration register 2 (CONFIG2).
  - <2> Set MPX52 to 0, MPX51 to 0, and MPX50 to 0 in MPX setting register 2 (MPX2) to specify the MPXIN10 pin as the source of inverted input to configurable amplifier Ch3.
  - <3> Set MPX62 to 0, MPX61 to 1, and MPX60 to 0 in MPX setting register 2 (MPX2) to specify the signal output from configurable amplifier Ch1 as the source of non-inverted input to configurable amplifier Ch3.
  - <4> Set CC1 to 0 and CC0 to 0 in the AMP operation mode control register (AOMC) to specify high-speed mode as the operating mode of configurable amplifier channels Ch1 to Ch3.
  - <5> Set gain control register 3 (GC3) to 00H to specify 6 dB as the gain (Typ.) of configurable amplifier Ch3 (used as a differential amplifier).
  - <6> Set AMP3OF to 1 in power control register 1 (PC1) to start operation of configurable amplifier Ch3 (used as a differential amplifier).

Figure 6.3 shows a block diagram of configurable amplifier Ch3 when used as a differential amplifier.

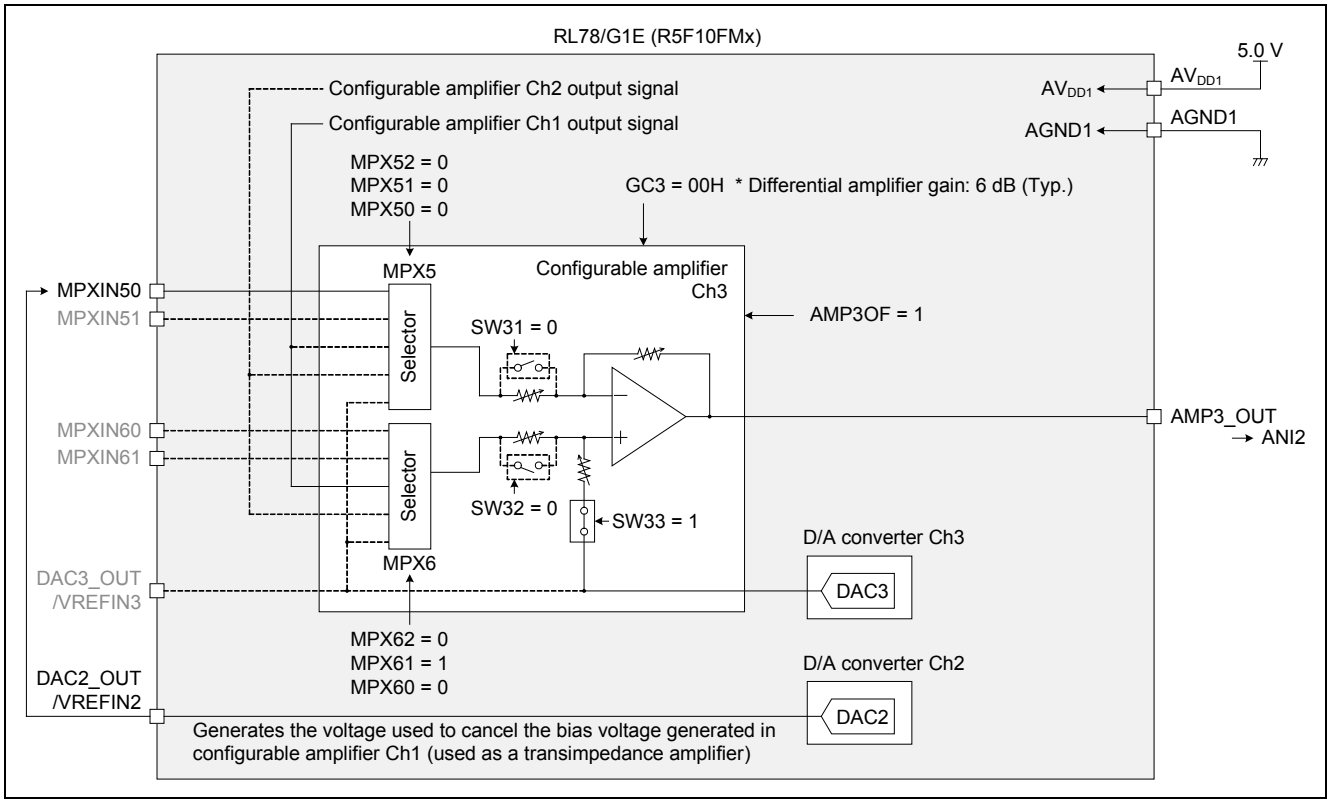


Figure 6.3 Block Diagram of Configurable Amplifier Ch3 (Used As a Differential Amplifier)

6.2.2 Reference voltage generator and variable output voltage regulator

The RL78/G1E (R5F10FMx) has an on-chip reference voltage generator channel and variable output voltage regulator channel. The variable output voltage regulator is a series regulator that generates 3.3 V (default) from a supplied voltage of 5 V. In this application note, the voltage output from the variable output voltage regulator (LDO_OUT) is connected to the AV_{DD} pin in the RL78/G1E (R5F10FMx) and used as a voltage of 3.3 V supplied to the A/D converter.

(1) Overview of variable output voltage regulator features

- Output voltage range: 2.0 to 3.3 V (Typ.)
- Output current: 15 mA (Max.)
- Includes a power-off feature.

(2) Overview of reference voltage generator features

- Output reference voltage: 1.21 V (Typ.)
- Includes a power-off feature.

(3) Settings specified for reference voltage generator and variable output voltage regulator

Specify the settings for the reference voltage generator and variable output voltage regulator as shown below.

<1> Set the LDO control register (LDOC) to 0DH to specify 3.3 V as the voltage output from the variable output voltage regulator.

<2> Set LDOOF to 1 in power control register 2 (PC2) to start operation of the reference voltage generator and variable output voltage regulator.

Figure 6.4 shows a block diagram of the reference voltage generator and variable output voltage regulator.

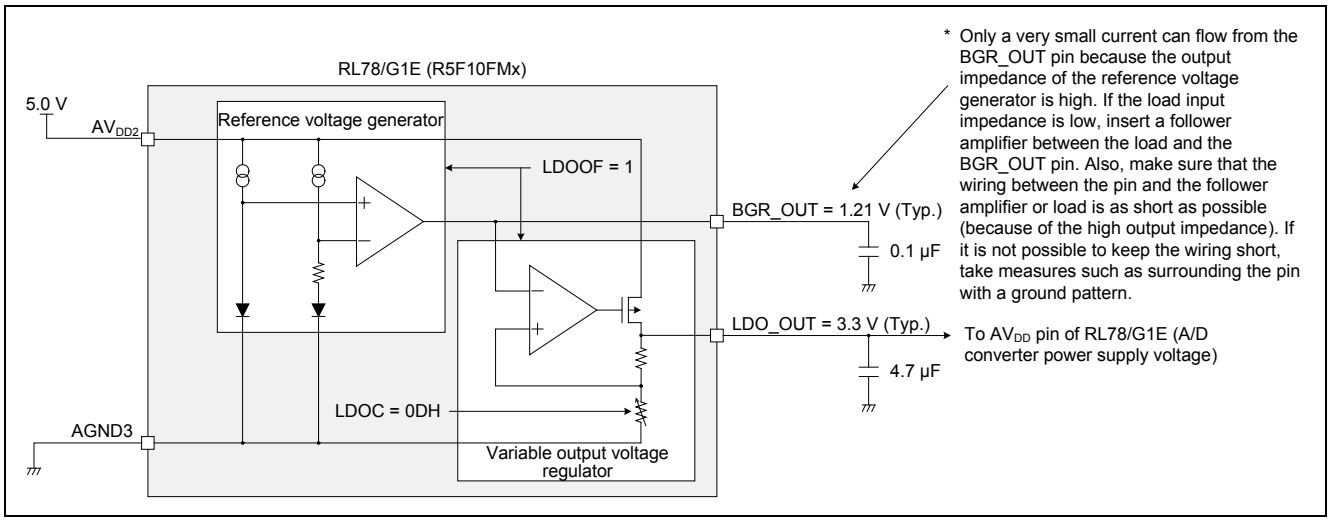


Figure 6.4 Block Diagram of Reference Voltage Generator and Variable Output Voltage Regulator

(4) Notes on using reference voltage generator

Observe the following points when using the reference voltage generator:

- Only a very small current can flow from the BGR_OUT pin because the output impedance of the reference voltage generator is high. If the load input impedance is low, insert a follower amplifier between the load and the BGR_OUT pin. Also, make sure that the wiring between the pin and the follower amplifier or load is as short as possible. If it is not possible to keep the wiring short, take measures such as surrounding the pin with a ground pattern.

6.2.3 D/A converter

The RL78/G1E (R5F10FMx) has four on-chip 8-bit D/A converter channels. In this application note, D/A converter Ch1 is used to generate a bias voltage for configurable amplifier Ch1 (used as a transimpedance amplifier), D/A converter Ch3 is used to generate a bias voltage for configurable amplifier Ch3 (used as a differential amplifier), and D/A converter Ch2 is used to generate the voltage used to cancel the bias voltage for configurable amplifier Ch1 (used as a transimpedance amplifier), which is input to the MPXIN50 pin from which the inverted signal is input to configurable amplifier Ch3 (used as a differential amplifier).

(1) Overview of D/A converter features

- 8-bit resolution × 4 ch
- R-2R ladder method
- Analog output voltage: (reference voltage upper limit – reference voltage lower limit) × 2 × m/255 + 2 × reference voltage lower limit
  (m: Value set to DACnC register)
- Controls the reference voltage for the configurable amplifiers, gain adjustment amplifier, high-pass filter, and low-pass filter
- Includes a power-off feature.
- Conversion speed (settling time): 100 μs (Max.)
- Voltage resolution: 19.608 mV
  * Reference voltage upper limit = AV_{DD1} × 5/10
  * Reference voltage lower limit = AGND1
  * AV_{DD1} = 5.0 V

(2) Settings specified for D/A converter

- In this application note, the reference voltage upper limit for the D/A converter (VRT) is set to AV_{DD1} × 5/10, and the reference voltage lower limit for the D/A converter (VRB) is set to AGND1. The voltage output from D/A converter channels Ch1 to Ch4 therefore ranges from AGND1 to AV_{DD1} (0 to 5 V).
- Specify the settings for the D/A converter as shown below.

<1> Set VRT1 to 0 and VRT0 to 0 in the DAC reference voltage control register (DACRC) to specify "AV_{DD1} × 5/10" as the reference voltage upper limit (VRT) for D/A converter channels Ch1 to Ch4.
<2> Set VRB1 to 0 and VRB0 to 0 in the DAC reference voltage control register (DACRC) to specify AGND1 as the reference voltage lower limit (VRB) for D/A converter channels Ch1 to Ch4.
<3> Specify the output analog voltage value by using DAC control registers 1 to 4 (DAC1C to DAC4C) corresponding to the D/A converter used.

* In this application note, D/A converter Ch1 is used to generate a bias voltage for configurable amplifier Ch1 (used as a transimpedance amplifier). Set the DAC1C register to 19H to specify 0.49 V as the voltage output from the DAC1_OUT pin. (Note that the value set to the DAC1C register is a reference value. The user needs to evaluate the system to determine the actual values.)

* In this application note, D/A converter Ch2 is used to generate the voltage used to cancel the bias voltage for configurable amplifier Ch1 (used as a transimpedance amplifier), which is input to the MPXIN50 pin from which the inverted signal is input to configurable amplifier Ch3 (used as a differential amplifier). Set the DAC2C register to 19H to specify 0.49 V as the voltage output from the DAC2_OUT pin. (Note that the value set to the DAC2C register is a reference value. The user needs to evaluate the system to determine the actual values.)

* In this application note, D/A converter Ch3 is used to generate a bias voltage for configurable amplifier Ch3 (used as a differential amplifier). Set the DAC3C register to 00H to specify 0 V as the voltage output from the DAC3_OUT pin. (Note that the value set to the DAC3C register is a reference value. The user needs to evaluate the system to determine the actual values.)

<4> Set DAC1OF to DAC3OF to 1 in power control register 1 (PC1) to start operation of this channel. Set DAC4OF to 0. (DAC4OF = 0, DAC3OF = 1, DAC2OF = 1, and DAC1OF = 1.)

Figure 6.5 shows a block diagram of D/A converter channels Ch1, Ch2, and Ch3.

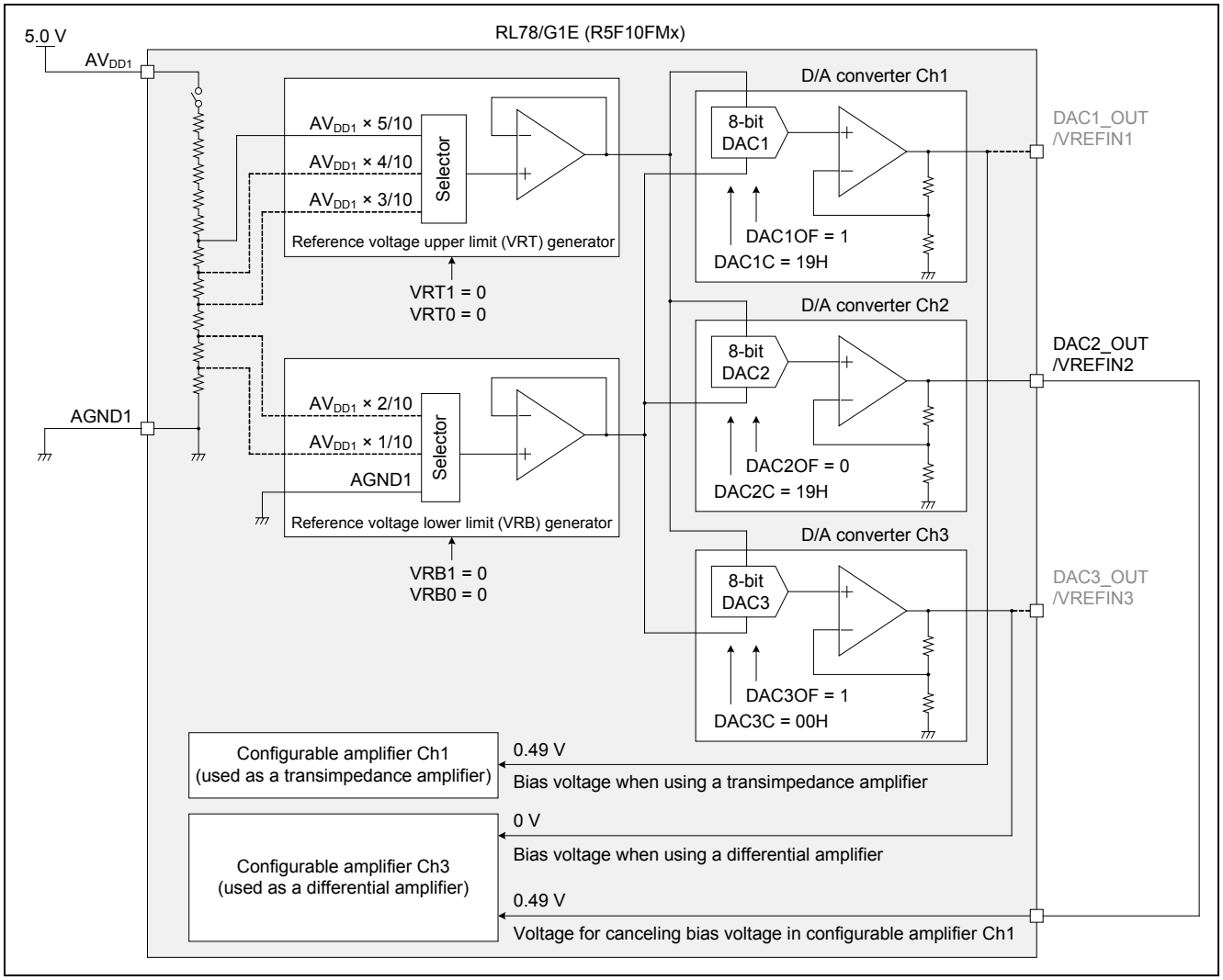


Figure 6.5 Block Diagram of D/A Converter

(3) Notes on using the D/A converter

Observe the following points when using the D/A converter:

- Only a very small current can flow from the DACn_OUT pin because the output impedance of the D/A converter is high. If the load input impedance is low, insert a follower amplifier between the load and the DACn_OUT pin. Also, make sure that the wiring between the pin and the follower amplifier or load is as short as possible. If it is not possible to keep the wiring short, take measures such as surrounding the pin with a ground pattern.
- If inputting an external reference power supply to the VREFINn pin, be sure to set the DACnOF bit to 0.

Remark: n = 1 to 4

6.2.4 SPI

The SPI is used to allow control from external devices by using clocked communication via four lines: a serial clock line (SCLK#), two serial data lines (SDI and SDO), and a slave selection input line (CS#).

(1) Overview of SPI features

- Data transmission/reception:
  - 16-bit data unit
  - MSB first

- The SPI pins SCLK#, SDI, and SDO, which are located in the analog block of the RL78/G1E (R5F10FMx), are connected to the corresponding pins in the 3-wire serial I/O function block (CSI21) of channel 1 of serial array unit 1 in the microcontroller block inside the package. The CS# pin is connected to the P73 pin in the microcontroller block inside the package.

- The RL78/G1E (R5F10FMx) has an on-chip analog reset feature. A reset can be generated in the following two ways:
  - By inputting an external reset signal to the ARESET# pin
  - By generating an internal reset by writing 1 to the RESET bit of the reset control register (RC)

- In this application note, the ARESET# pin in the RL78/G1E (R5F10FMx) is connected to the P130 pin in the microcontroller block to control the analog reset feature.

Figure 6.6 shows the pin connections of the SPI in the RL78/G1E (R5F10FMx).

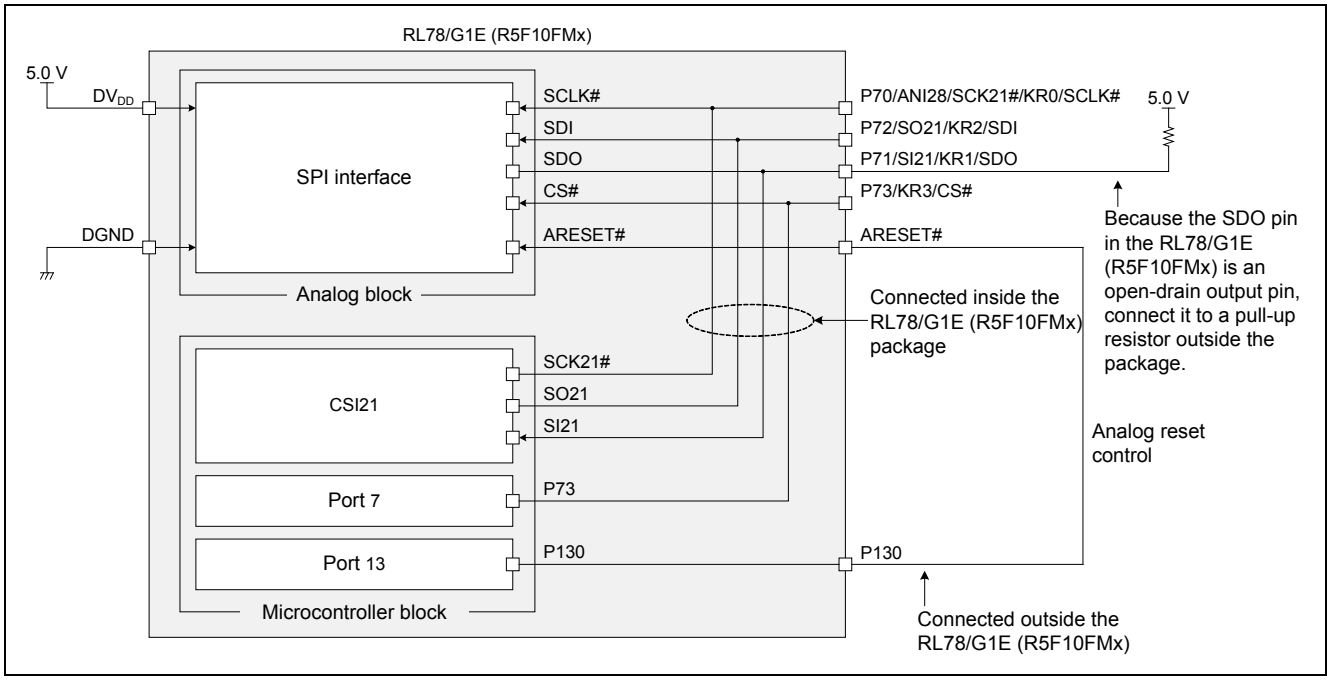


Figure 6.6 SPI Configuration Example

(2) SPI communication

The SPI transmits and receives data in 16-bit units. Data can be transmitted and received when CS# is low. Data is transmitted one bit at a time in synchronization with the falling edge of the serial clock, and is received one bit at a time in synchronization with the rising edge of the serial clock. When the R/W bit is 1, data is written to the SPI control register in accordance with the address/data setting when the rising edge of the 16th SCLK# signal is detected after the fall of CS#. When the R/W bit is 0, the data is output from the register in accordance with the address/data setting, in synchronization with the 9th and later falling edges of SCLK# following the fall of CS#.

In this application note, the SPI in the analog block of the RL78/G1E (R5F10FMx) and CSI21 in the microcontroller block, to which the SPI is connected inside the RL78/G1E (R5F10FMx) chip, are used to perform SPI communication. A 32 MHz clock generated by the high-speed on-chip oscillator is used as the main system clock for the RL78/G1E (R5F10FMx), and 1 MHz is selected as the operating clock for SPI communication. The slave select input (CS#) pin for the SPI is controlled by using the P73 pin in the RL78/G1E (R5F10FMx).

Figure 6.7 shows the SPI communication timing.

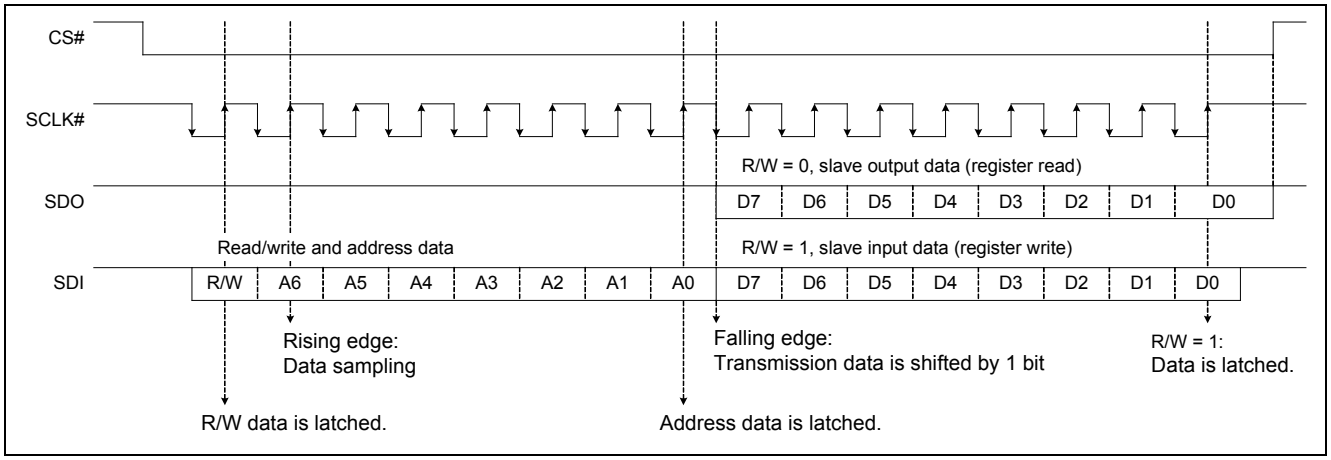


Figure 6.7 SPI Communication Timing

(3) SPI control registers

Table 6.2 shows the SPI control registers.

Table 6.2 SPI Control Registers

Address	SPI Control Register		R/W	After Reset
00H	CONFIG1	Configuration register 1	R/W	00H
01H	CONFIG2	Configuration register 2	R/W	00H
03H	MPX1	MPX setting register 1	R/W	00H
04H	MPX2	MPX setting register 2	R/W	00H
05H	MPX3	MPX setting register 3	R/W	00H
06H	GC1	Gain control register 1	R/W	00H
07H	GC2	Gain control register 2	R/W	00H
08H	GC3	Gain control register 3	R/W	00H
09H	AOMC	AMP operation mode control register	R/W	00H
0AH	GC4	Gain control register 4	R/W	00H
0BH	LDOC	LDO control register	R/W	0DH
0CH	DACRC	DAC reference voltage control register	R/W	00H
0DH	DAC1C	DAC control register 1	R/W	80H
0EH	DAC2C	DAC control register 2	R/W	80H
0FH	DAC3C	DAC control register 3	R/W	80H
10H	DAC4C	DAC control register 4	R/W	80H
11H	PC1	Power control register 1	R/W	00H
12H	PC2	Power control register 2	R/W	00H
13H	RC	Reset control register	R/W	00H[Note]

Note When generating an internal reset by writing 1 to the RESET bit of the reset control register, the reset control register is not initialized.

(4) Analog reset feature

The RL78/G1E (R5F10FMx) has an on-chip analog reset feature. A reset can be generated in the following two ways:

- By inputting an external reset signal to the ARESET# pin
- By generating an internal reset by writing 1 to the RESET bit of the reset control register (RC)

There are no functional differences between an external and an internal reset: both types serve to initialize[Note] the SPI control registers.

If a low-level signal is input to the ARESET# pin or if 1 is written to the RESET bit of the reset control register (RC), the analog circuits enter the statuses shown in **Table 6.3**. The statuses of the SPI control registers after a reset has been acknowledged are shown in **Table 6.4**.

A reset is generated by inputting a low-level signal to the ARESET# pin. The reset is subsequently canceled by inputting a high-level signal to this pin.

When generating an internal reset by writing 1 to the RESET bit of the reset control register, the reset occurs[Note] after 1 is written to the RESET bit, and is subsequently canceled by writing 0 to the same bit.

In this application note, the ARESET# pin in the RL78/G1E (R5F10FMx) is connected to the P130 pin in the microcontroller block to control the analog reset feature.

Note When generating an internal reset by writing 1 to the RESET bit of the reset control register, the reset control register is not initialized.

Caution When generating an external reset, input a low-level signal to the ARESET# pin for at least 10 μs.

Table 6.3 Statuses During an Analog Reset Period

Function Block	By Inputting an External Reset Signal to the ARESET# Pin	By Generating an Internal Reset by Writing 1 to the RESET Bit of the Reset Control Register (RC)
Configurable amplifier	Operation stops.	
Gain adjustment amplifier	Operation stops.	
D/A converter	Operation stops.	
Low-pass filter	Operation stops.	
High-pass filter	Operation stops.	
Temperature sensor	Operation stops.	
Variable output voltage regulator	Operation stops.	
Reference voltage generator	Operation stops.	
SPI	Operation stops.	Operation enabled

Table 6.4 Statuses of SPI Control Registers After an Analog Reset Is Acknowledged

Address	SPI Control Register		Status After an Analog Reset Is Acknowledged
00H	CONFIG1	Configuration register 1	00H
01H	CONFIG2	Configuration register 2	00H
03H	MPX1	MPX setting register 1	00H
04H	MPX2	MPX setting register 2	00H
05H	MPX3	MPX setting register 3	00H
06H	GC1	Gain control register 1	00H
07H	GC2	Gain control register 2	00H
08H	GC3	Gain control register 3	00H
09H	AOMC	AMP operation mode control register	00H
0AH	GC4	Gain control register 4	00H
0BH	LDOC	LDO control register	0DH
0CH	DACRC	DAC reference voltage control register	00H
0DH	DAC1C	DAC control register 1	80H
0EH	DAC2C	DAC control register 2	80H
0FH	DAC3C	DAC control register 3	80H
10H	DAC4C	DAC control register 4	80H
11H	PC1	Power control register 1	00H
12H	PC2	Power control register 2	00H
13H	RC	Reset control register	00H[Note]

Note When generating an internal reset by writing 1 to the RESET bit of the reset control register, the reset control register is not initialized.

6.3 Settings of SPI Control Registers of RL78/G1E (R5F10FMx)

This section describes the settings of the SPI control registers used in this application note. This section omits descriptions of the SPI control registers not used in this application note. (They are used with their default values.) For details, see the *RL78/G1E Hardware User's Manual*.

Caution For how to specify the register settings, see the *RL78/G1E Hardware User's Manual*.

(1) Configuration register 1 (CONFIG1)

This register is used to turn on or off the switches of configurable amplifier Ch1.

Address: 00H After reset: 00H R/W Set value: 70H

Symbol	7	6	5	4	3	2	1	0
CONFIG1	0	SW11	SW12	SW13	0	SW21	SW22	SW23
Set value	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**

SW11	Control of SW11
0	Turn off SW11.
1	**Turn on SW11.**

SW12	Control of SW12
0	Turn off SW12.
1	**Turn on SW12.**

SW13	Control of SW13
0	Turn off SW13.
1	**Turn on SW13.**

(2) Configuration register 2 (CONFIG2)

This register is used to turn on or off the switches of configurable amplifier channels Ch1 and Ch3.

Address: 01H After reset: 00H R/W Set value: 10H

Symbol	7	6	5	4	3	2	1	0
CONFIG2	0	SW31	SW32	SW33	0	SW02	SW01	SW00
Set value	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**

SW31	Control of SW31
0	**Turn off SW31.**
1	Turn on SW31.

SW32	Control of SW32
0	**Turn off SW32.**
1	Turn on SW32.

SW33	Control of SW33
0	Turn off SW33.
1	**Turn on SW33.**

SW01	Control of SW01
0	**Turn off SW01.**
1	Turn on SW01.

(3) MPX setting register 1 (MPX1)

This register is used to control MPX1, MPX2, MPX3, and MPX4.

This register is used to select the signal input to configurable amplifier Ch1.

Address: 03H After reset: 00H R/W Set value: 20H

Symbol	7	6	5	4	3	2	1	0
MPX1	MPX11	MPX10	MPX21	MPX20	MPX31	MPX30	MPX41	MPX40
Set value	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**

MPX11	MPX10	Source of configurable amplifier Ch1 inverted input
0	**0**	**MPXIN10 pin**
0	1	MPXIN11 pin
1	0	D/A converter Ch1 output signal or VREFIN1 pin
1	1	Leave open

MPX21	MPX20	Source of configurable amplifier Ch1 non-inverted input
0	0	MPXIN20 pin
0	1	MPXIN21 pin
1	**0**	**D/A converter Ch1 output signal or VREFIN1 pin**
1	1	Leave open

(4) MPX setting register 2 (MPX2)

This register is used to control MPX5 and MPX6.

This register is used to select the signal input to configurable amplifier Ch3.

Address: 04H After reset: 00H R/W Set value: 02H

Symbol	7	6	5	4	3	2	1	0
MPX2	0	MPX52	MPX51	MPX50	0	MPX62	MPX61	MPX60
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**

MPX52	MPX51	MPX50	Source of configurable amplifier Ch3 inverted input
0	**0**	**0**	**MPXIN50 pin**
0	0	1	MPXIN51 pin
0	1	0	Configurable amplifier Ch1 output signal
0	1	1	Configurable amplifier Ch2 output signal
1	0	0	D/A converter Ch3 output signal or VREFIN3 pin
Other than above			Setting prohibited

MPX62	MPX61	MPX60	Source of configurable amplifier Ch3 non-inverted input
0	0	0	MPXIN60 pin
0	0	1	MPXIN61 pin
0	**1**	**0**	**Configurable amplifier Ch1 output signal**
0	1	1	Configurable amplifier Ch2 output signal
1	0	0	D/A converter Ch3 output signal or VREFIN3 pin
Other than above			Setting prohibited

(5) Gain control register 1 (GC1)

This register is used to specify the gain and feedback resistance of configurable amplifier Ch1.

The value to specify depends on the configuration of configurable amplifier Ch1. In this application note, the configurable amplifier is used as a transimpedance amplifier.

Address: 06H After reset: 00H R/W Set value: 00H

Symbol	7	6	5	4	3	2	1	0
GC1	0	0	0	AMPG14	AMPG13	AMPG12	AMPG11	AMPG10
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

AMPG14	AMPG13	AMPG12	AMPG11	AMPG10	Feedback resistance of configurable amplifier Ch1 used as transimpedance amplifier (Typ.)
0	**0**	**0**	**0**	**0**	**20 kΩ**
0	0	0	0	1	
0	0	0	1	0	
0	0	0	1	1	40 kΩ
0	0	1	0	0	
0	0	1	0	1	
0	0	1	1	0	80 kΩ
0	0	1	1	1	
0	1	0	0	0	
0	1	0	0	1	160 kΩ
0	1	0	1	0	
0	1	0	1	1	
0	1	1	0	0	320 kΩ
0	1	1	0	1	
0	1	1	1	0	
0	1	1	1	1	640 kΩ
1	0	0	0	0	
1	0	0	0	1	
Other than above					Setting prohibited

(6) Gain control register 3 (GC3)

This register is used to specify the gain and feedback resistance of configurable amplifier Ch3.

The value to specify depends on the configuration of configurable amplifier Ch3. In this application note, configurable amplifier Ch3 is used as a differential amplifier.

Address: 08H After reset: 00H R/W Set value: 00H

Symbol	7	6	5	4	3	2	1	0
GC3	0	0	0	AMPG34	AMPG33	AMPG32	AMPG31	AMPG30
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

AMPG34	AMPG33	AMPG32	AMPG31	AMPG30	Gain of configurable amplifier Ch3 used as differential amplifier (Typ.)
0	**0**	**0**	**0**	**0**	**6 dB**
0	0	0	0	1	8 dB
0	0	0	1	0	10 dB
0	0	0	1	1	12 dB
0	0	1	0	0	14 dB
0	0	1	0	1	16 dB
0	0	1	1	0	18 dB
0	0	1	1	1	20 dB
0	1	0	0	0	22 dB
0	1	0	0	1	24 dB
0	1	0	1	0	26 dB
0	1	0	1	1	28 dB
0	1	1	0	0	30 dB
0	1	1	0	1	32 dB
0	1	1	1	0	34 dB
0	1	1	1	1	36 dB
1	0	0	0	0	38 dB
1	0	0	0	1	40 dB
Other than above					Setting prohibited

(7) AMP operation mode control register (AOMC)

This register is used to specify the operating mode of configurable amplifier channels Ch1 to Ch3.

Address: 09H After reset: 00H R/W Set value: 00H

Symbol	7	6	5	4	3	2	1	0
AOMC	0	0	0	0	0	0	CC1	CC0
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

CC1	CC0	Operating mode of configurable amplifier channels Ch1 to Ch3
0	**0**	**High-speed mode**
0	1	Mid-speed mode 2
1	0	Mid-speed mode 1
1	1	Low-speed mode

(8) LDO control register (LDOC)

This register is used to specify the output voltage of the variable output voltage regulator.

Address: 0BH After reset: 0DH R/W Set value: 0DH

Symbol	7	6	5	4	3	2	1	0
LDOC	0	0	0	0	LDO3	LDO2	LDO1	LDO0
Set value	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**1**

LDO3	LDO2	LDO1	LDO0	Output voltage of variable output voltage regulator (Typ.)
0	0	0	0	2.0 V
0	0	0	1	2.1 V
0	0	1	0	2.2 V
0	0	1	1	2.3 V
0	1	0	0	2.4 V
0	1	0	1	2.5 V
0	1	1	0	2.6 V
0	1	1	1	2.7 V
1	0	0	0	2.8 V
1	0	0	1	2.9 V
1	0	1	0	3.0 V
1	0	1	1	3.1 V
1	1	0	0	3.2 V
1	**1**	**0**	**1**	**3.3 V**
Other than above				Setting prohibited

(9) DAC reference voltage control register (DACRC)

This register is used to specify the upper (VRT) and lower (VRB) limits of the reference voltage for D/A converter channels Ch1 to Ch4.

When selecting the upper limit of the reference voltage, use bits 3 and 2. When selecting the lower limit of the reference voltage, use bits 1 and 0.

Address: 0CH After reset: 00H R/W Set value: 00H

Symbol	7	6	5	4	3	2	1	0
DACRC	0	0	0	0	VRT1	VRT0	VRB1	VRB0
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

VRT1	VRT0	Upper limit of reference voltage (Typ.)
0	**0**	**AV_{DD1} × 5/10**
0	1	AV_{DD1} × 4/10
1	0	AV_{DD1} × 3/10
1	1	AV_{DD1} × 5/10

VRB1	VRB0	Upper limit of reference voltage (Typ.)
0	**0**	**AGND1**
0	1	AV_{DD1} × 1/10
1	0	AV_{DD1} × 2/10
1	1	AGND1

(10) DAC control register 1 (DAC1C)

This register is used to specify the analog voltage to be output to the DAC1_OUT pin.

The DAC1_OUT output signal is used to generate a bias voltage for configurable amplifier Ch1 (used as a transimpedance amplifier).

Address: 0DH After reset: 80H R/W Set value: 19H

Symbol	7	6	5	4	3	2	1	0
DAC1C	DAC17	DAC16	DAC15	DAC14	DAC13	DAC12	DAC11	DAC10
Set value	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**1**

- DAC1_OUT output voltage
  = ((reference voltage upper limit – reference voltage lower limit) × 2 × m/255) + 2 × reference voltage lower limit
  = ((AV_{DD1} × 5/10 – AGND1) × 2 × 25/255) + 2 × AGND1
  = ((2.5 V – 0 V) × 2 × 25/255) + 2 × 0 V
  = 0.49 V
  * AV_{DD1} = 5.0 V
  * AGND1 = 0 V
  * m (DAC1C register value) = 25 (19H)

- The value set to the DAC1C register is a reference value. The user needs to evaluate the system to determine the actual values.

(11) DAC control register 2 (DAC2C)

This register is used to specify the analog voltage to be output to the DAC2_OUT pin.

The DAC2_OUT output signal is used to generate the voltage used to cancel the bias voltage for configurable amplifier Ch1 (used as a transimpedance amplifier) and is connected to the inverted input source (MPXIN50 pin) of configurable amplifier Ch3 (used as a differential amplifier).

Address: 0EH After reset: 80H R/W Set value: 19H

Symbol	7	6	5	4	3	2	1	0
DAC2C	DAC27	DAC26	DAC25	DAC24	DAC23	DAC22	DAC21	DAC20
Set value	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**1**

- DAC2_OUT output voltage
  = ((reference voltage upper limit – reference voltage lower limit) × 2 × m/255) + 2 × reference voltage lower limit
  = ((AV_{DD1} × 5/10 – AGND1) × 2 × 25/255) + 2 × AGND1
  = ((2.5 V – 0 V) × 2 × 25/255) + 2 × 0 V
  = 0.49 V
  * AV_{DD1} = 5.0 V
  * AGND1 = 0 V
  * m (DAC2C register value) = 25 (19H)

- The value set to the DAC2C register is a reference value. The user needs to evaluate the system to determine the actual values.

(12) DAC control register 3 (DAC3C)

This register is used to specify the analog voltage to be output to the DAC3_OUT pin.

The DAC3_OUT output signal is used to generate a bias voltage for configurable amplifier Ch3 (used as a differential amplifier).

Address: 0FH After reset: 80H R/W Set value: 00H

Symbol	7	6	5	4	3	2	1	0
DAC3C	DAC37	DAC36	DAC35	DAC34	DAC33	DAC32	DAC31	DAC30
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

- DAC3_OUT output voltage
  = ((reference voltage upper limit – reference voltage lower limit) × 2 × m/255) + 2 × reference voltage lower limit
  = ((AV_{DD1} × 5/10 – AGND1) × 2 × 0/255) + 2 × AGND1
  = ((2.5 V – 0 V) × 2 × 0/255) + 2 × 0 V
  = 0 V
  * AV_{DD1} = 5.0 V
  * AGND1 = 0 V
  * m (DAC3C register value) = 0 (00H)

- The value set to the DAC3C register is a reference value. The user needs to evaluate the system to determine the actual values.

(13) Power control register 1 (PC1)

This register is used to enable or disable operation of the configurable amplifier and D/A converter. Use this register to stop unused functions to reduce power consumption and noise.

When using one of D/A converter channels Ch1 to Ch4, be sure to set the control bit that corresponds to the channel (bits 7 to 4) to 1.

When using one of configurable amplifier channels Ch1 to Ch3, be sure to set the control bit that corresponds to the channel (bits 2 to 0) to 1.

Address: 11H After reset: 00H R/W Set value: 75H

Symbol	7	6	5	4	3	2	1	0
PC1	DAC4OF	DAC3OF	DAC2OF	DAC1OF	0	AMP3OF	AMP2OF	AMP1OF
Set value	**0**	**1**	**1**	**1**	**0**	**1**	**0**	**1**

DAC4OF	Operation of D/A converter Ch4
0	**Stop operation of D/A converter Ch4.**
1	Enable operation of D/A converter Ch4.

DAC3OF	Operation of D/A converter Ch3
0	Stop operation of D/A converter Ch3.
1	**Enable operation of D/A converter Ch3.**

DAC2OF	Operation of D/A converter Ch2
0	Stop operation of D/A converter Ch2.
1	**Enable operation of D/A converter Ch2.**

DAC1OF	Operation of D/A converter Ch1
0	Stop operation of D/A converter Ch1.
1	**Enable operation of D/A converter Ch1.**

AMP3OF	Operation of configurable amplifier Ch3
0	Stop operation of configurable amplifier Ch3.
1	**Enable operation of configurable amplifier Ch3.**

AMP2OF	Operation of configurable amplifier Ch2
0	**Stop operation of configurable amplifier Ch2.**
1	Enable operation of configurable amplifier Ch2.

AMP1OF	Operation of configurable amplifier Ch1
0	Stop operation of configurable amplifier Ch1.
1	**Enable operation of configurable amplifier Ch1.**

(14) Power control register 2 (PC2)

This register is used to enable or disable operation of the gain adjustment amplifier, the low-pass filter, the high-pass filter, the variable output voltage regulator, the reference voltage generator, and the temperature sensor. Use this register to stop unused functions to reduce power consumption and noise.

When using the gain adjustment amplifier, be sure to set bit 4 to 1.

When using the low-pass filter, be sure to set bit 3 to 1.

When using the high-pass filter, be sure to set bit 2 to 1.

When using the variable output voltage regulator and reference voltage generator, be sure to set bit 1 to 1.

When selecting the signal to be input to the temperature sensor, be sure to set bit 0 to 1.

Address: 12H After reset: 00H R/W Set value: 02H

Symbol	7	6	5	4	3	2	1	0
PC2	0	0	0	GAINOF	LPFOF	HPFOF	LDOOF	TEMPOF
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**

GAINOF	Operation of gain adjustment amplifier
0	**Stop operation of the gain adjustment amplifier.**
1	Enable operation of the gain adjustment amplifier.

LPFOF	Operation of low-pass filter
0	**Stop operation of the low-pass filter.**
1	Enable operation of the low-pass filter.

HPFOF	Operation of high-pass filter
0	**Stop operation of the high-pass filter.**
1	Enable operation of the high-pass filter.

LDOOF	Operation of variable output voltage regulator and reference voltage generator
0	Stop operation of the variable output voltage regulator and reference voltage generator.
1	**Enable operation of the variable output voltage regulator and reference voltage generator.**

TEMPOF	Operation of temperature sensor
0	**Stop operation of the temperature sensor.**
1	Enable operation of the temperature sensor.

7. Microcontroller Block of RL78/G1E (R5F10FMx)

This section describes the functions and software used by the microcontroller block of the RL78/G1E (R5F10FMx).

7.1 Functions Assigned to the Microcontroller Block of the RL78/G1E (R5F10FMx)

Figure 7.1 shows the function blocks in the microcontroller block of the RL78/G1E (R5F10FMx), and **Table 7.1** shows the assigned roles.

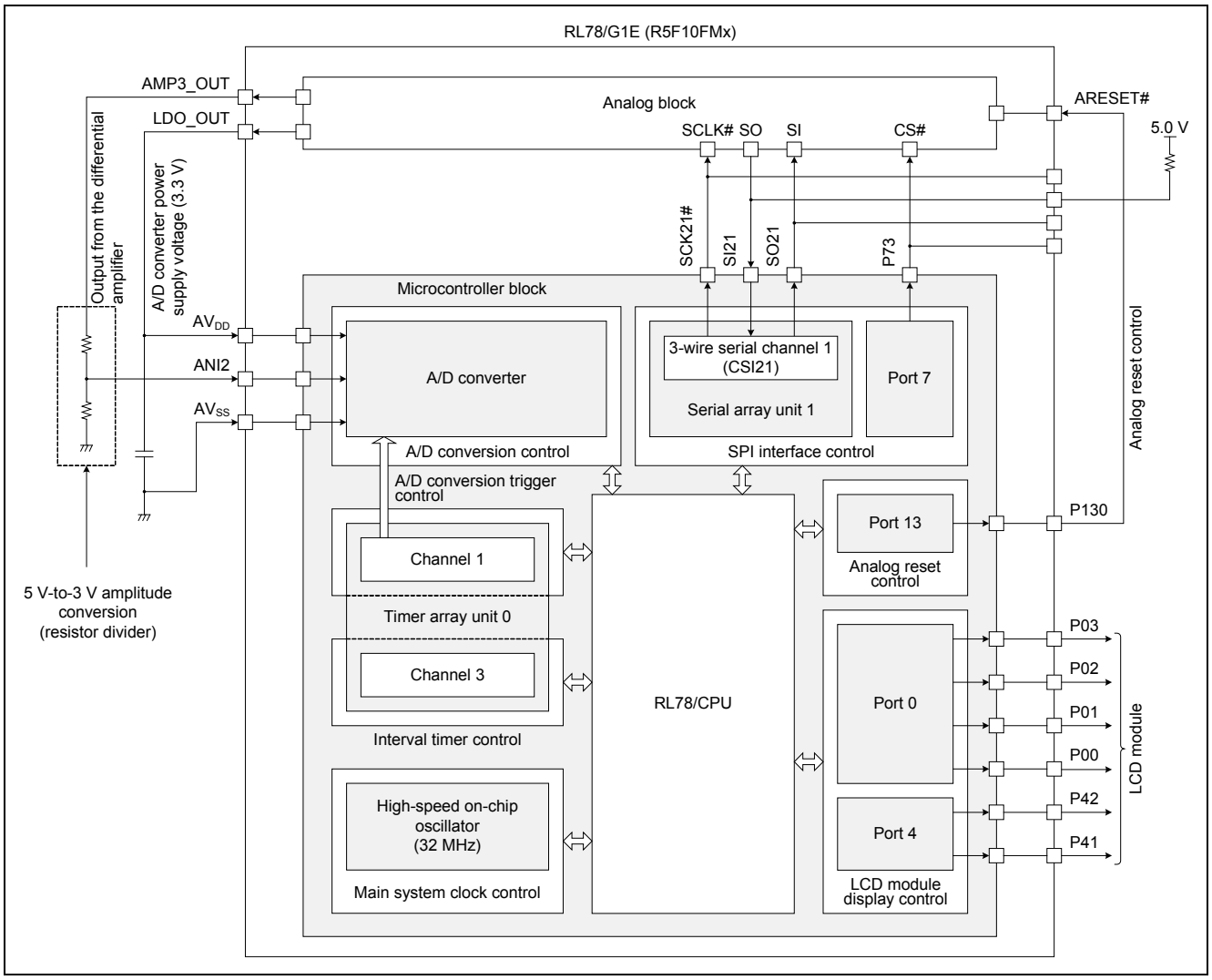


Figure 7.1 Function Blocks in the Microcontroller Block of the RL78/G1E (R5F10FMx)

Table 7.1 Functions Assigned to the Microcontroller Block of the RL78/G1E (R5F10FMx)

Functions Block	Assigned Role
CSI21	Control the communication with the SPI in the analog block of the RL78/G1E (R5F10FMx).
Port 7 (P73)	
A/D converter	Controls A/D conversion of the voltage (AMP3_OUT) output from configurable amplifier Ch3 (used as a differential amplifier), stepped down by using a resistor divider, and input to the ANI2 pin.
Port 13 (P130)	Controls the analog reset feature.
Timer array unit 0 (channel 1)	Controls the hardware trigger signal for the A/D converter.
Timer array unit 0 (channel 3)	Controls the interval timer for generating the wait time used by software.
Port 0 (P00 to P03)	Control the LCD module display.
Port 4 (P41, P42)	
High-speed on-chip oscillator	Generates the 32 MHz clock selected as the main system clock.

7.2 Functions of the Microcontroller Block of the RL78/G1E (R5F10FMx)

7.2.1 High-speed on-chip oscillator (clock generator)

In this application note, a 32 MHz clock generated by the high-speed on-chip oscillator (high-speed OCO) is used as the main system clock. The clock generator features are described below.

- Select 32 MHz as the high-speed on-chip oscillator frequency by using FRQSEL[3:0] of the user option byte (000C2H).
- By setting the user option byte (000C2H), after a reset period ends, the CPU starts operating on the high-speed on-chip oscillator clock (f_{IH} = 32 MHz (Typ.)). Oscillation can be stopped by executing the STOP instruction or by setting the HIOSTOP bit of the clock operation status control register (CSC).
- Select the high-speed on-chip oscillator clock (f_{IH} = 32 MHz (Typ.)) as the main system clock (f_{MAIN}) by using the MCM0 bit of the system clock control register (CKC).
- Enable clock input to timer array unit 0, serial array unit 1, and the A/D converter by using peripheral enable register 0 (PER0). In this application note, clock input to unused peripheral functions is stopped to reduce power consumption and noise.
- The high-speed on-chip oscillator frequency specified by the user option byte (000C2H) can be changed by using the high-speed on-chip oscillator frequency select register (HOCODIV). In this application note, the high-speed on-chip oscillator frequency is not changed.
- The accuracy of the high-speed on-chip oscillator can be adjusted by using the high-speed on-chip oscillator trimming register (HIOTRM). In this application note, the accuracy of the high-speed on-chip oscillator is not changed.

Figure 7.2 shows a block diagram of the clock generator incorporated in the RL78/G1E (R5F10FMx) that is used in this application note.

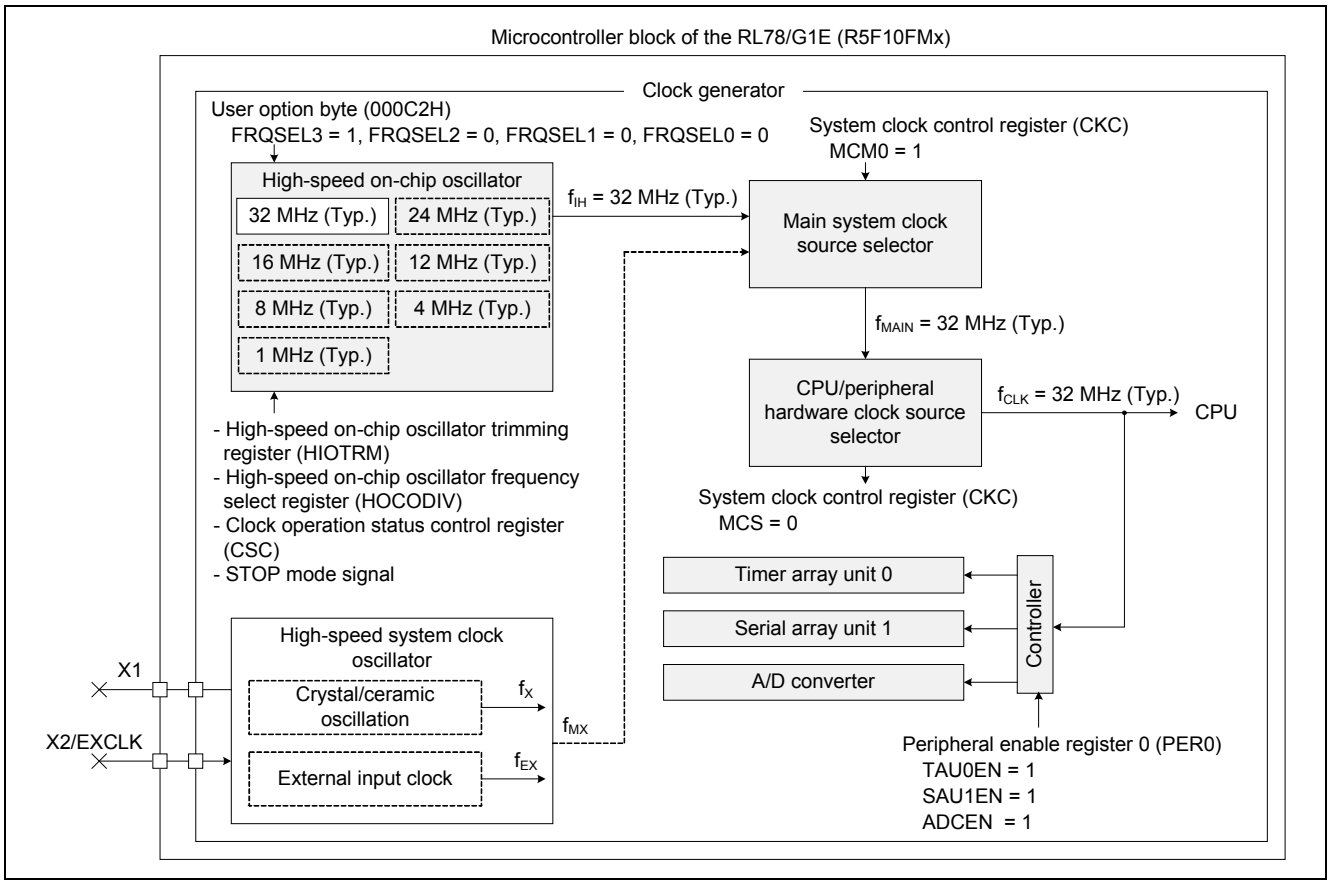


Figure 7.2 Block Diagram of the Clock Generator in the RL78/G1E (R5F10FMx)

7.2.2 SPI control

Communication with the SPI in the analog block of the RL78/G1E (R5F10FMx) is executed by using the 3-wire serial I/O (CSI21) of channel 1 of serial array unit 1 and the P73 pin of port 7 together.

(1) Connection with the SPI in the analog block of the RL78/G1E (R5F10FMx)

The SPI in the analog block of the RL78/G1E (R5F10FMx), CSI21 in the microcontroller block, and the P73 pin are connected in the RL78/G1E (R5F10FMx) package. Because the serial data transmission pin (SDO) in the SPI in the analog block of the RL78/G1E (R5F10FMx) is an open-drain output pin, a pull-up resistor is externally connected to the P71/SI21/KR1/SDO pin of the RL78/G1E (R5F10FMx).

Figure 7.3 shows the pin connections of the SPI of the RL78/G1E (R5F10FMx).

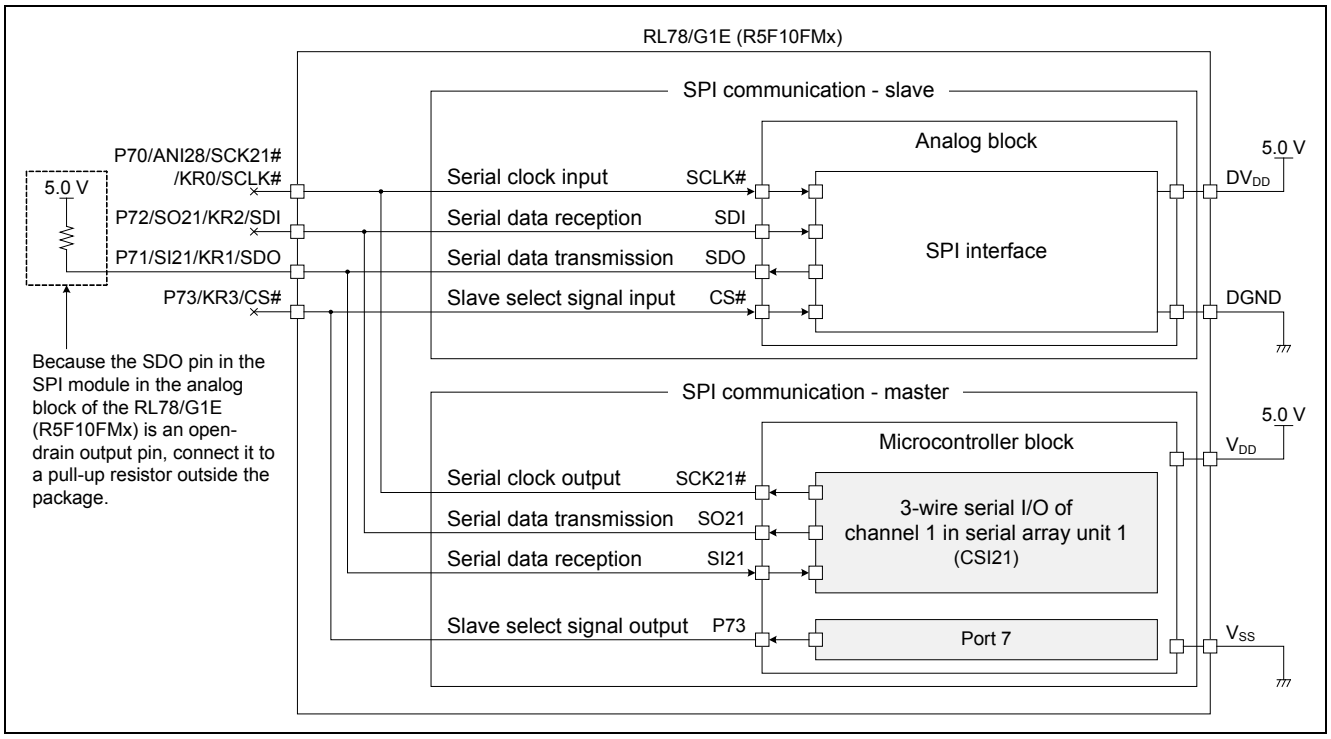


Figure 7.3 Connection with the SPI in the Analog Block of the RL78/G1E (R5F10FMx)

(2) 3-wire serial I/O (CSI21) of channel 1 of serial array unit 1 incorporated in the RL78/G1E (R5F10FMx)

In this application note, channel 1 of serial array unit 1 incorporated in the RL78/G1E (R5F10FMx) is used for 3-wire serial I/O (CSI21).

The 3-wire serial I/O function transmits and receives data in synchronization with the serial clock (SCK#) output from the master. This is a clocked communication interface that uses three communication lines: one for the serial clock (SCK#) and two for the transmission and reception of serial data (SO and SI).

In this application note, to perform SPI communication with the analog block of the RL78/G1E (R5F10FMx), CSI21 and the P73 output pin are used together as a master.

(3) Specifications of SPI communication

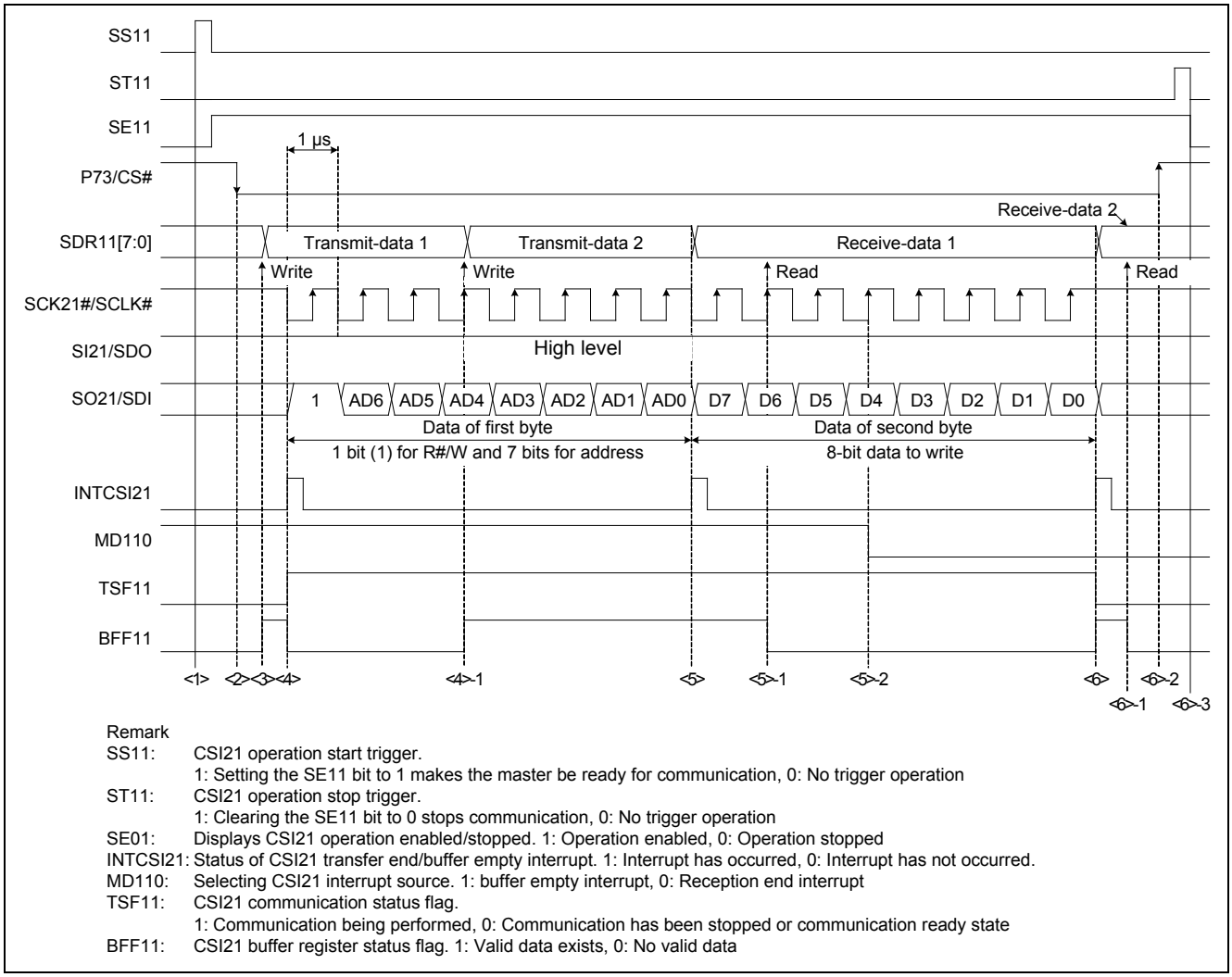
Channel 1 of serial array unit 1 is used for 3-wire serial I/O (CSI21) together with the output of the P73 pin to realize SPI communication with the analog block of the RL78/G1E (R5F10FMx).

Specify the CSI21 settings in accordance with SPI communication timing shown in **Figure 6.7** and the electrical specifications prescribed for the SPI in the analog block of the RL78/G1E (R5F10FMx).

Specify the settings for CSI21 as shown below.

- Supply of input clock to serial array unit 1: Enable
  - Set SAU1EN to 1 in peripheral enable register 0 (PER0) to enable supplying the input clock to channel 1 of serial array unit 1. (Enable reading from and writing to SFRs used by serial array unit 1.)
- Operating mode of channel 1 in serial array unit 1: CSI mode
  - Set MD112 to 0 and MD111 to 0 in serial mode register 11 (SMR11) to set channel 1 of serial array unit 1 to CSI mode.
- Serial data length: 8 bits
  - Set DLS110 to 1 in serial communication operation setting register 11 (SCR11) to specify 8 bits as the data length transferred in CSI mode.
- Data transfer order: MSB first
  - Set the DIR11 bit to 0 in serial communication operation setting register 11 (SCR11) so that data transfer in CSI mode starts from the MSB.
- Phase of data and clock signals: Type 1 (See the SPI communication timing shown in **Figure 6.7**.)
  - Set DAP11 to 0 and CKP11 to 0 in serial communication operation setting register 11 (SCR11) to specify type 1 as the phase of the data and clock signals in CSI mode.
- CSI21 operating mode (communication direction): Transmission and reception (full-duplex communication)
  - Set TXE11 to 1 and RXE11 to 1 in serial communication operation setting register 11 (SCR11) to specify transmission and reception as the CSI21 operating mode.
- CSI21 transfer clock: CSI21 outputs the transfer clock (master operation)
  - Set CCS11 to 0 in serial mode register 11 (SMR11) to specify the clock obtained by dividing the operating clock (f_{MCK}) specified by using the CKS11 bit of the SMR11 register as the CSI21 transfer clock (f_{TCLK}).
- Transfer rate: 1 Mbps
  - Select the 32 MHz clock generated by the high-speed on-chip oscillator (high-speed OCO) as the main system clock. (See *7.2.1 High-speed on-chip oscillator (clock generator)*.)
  - Set PRS103 to 0, PRS102 to 0, PRS101 to 0, and PRS100 to 0 in serial clock select register 1 (SPS1) to specify 32 MHz (when f_{CLK} = 32 MHz) as the frequency of the operating clock (CK10).
  - Set CCS11 to 0 in serial mode register 11 (SMR11) to specify the operating clock (CK10; when f_{CLK} = 32 MHz) specified by using the SPS1 register as the CSI21 operating clock (f_{MCK}).
  - Set the higher 7 bits (SDR11[15:9]) to 0001111B in serial data register 11 (SDR11) to specify f_{MCK}/32 (32 MHz/32 = 1 MHz) as the CSI21 transfer clock.

(4) SPI communication timing chart for write operations (master transmission)



Remark
SS11: CSI21 operation start trigger.
1: Setting the SE11 bit to 1 makes the master be ready for communication, 0: No trigger operation
ST11: CSI21 operation stop trigger.
1: Clearing the SE11 bit to 0 stops communication, 0: No trigger operation
SE01: Displays CSI21 operation enabled/stopped. 1: Operation enabled, 0: Operation stopped
INTCSI21: Status of CSI21 transfer end/buffer empty interrupt. 1: Interrupt has occurred, 0: Interrupt has not occurred.
MD110: Selecting CSI21 interrupt source. 1: buffer empty interrupt, 0: Reception end interrupt
TSF11: CSI21 communication status flag.
1: Communication being performed, 0: Communication has been stopped or communication ready state
BFF11: CSI21 buffer register status flag. 1: Valid data exists, 0: No valid data

Figure 7.4 SPI Communication Timing Chart for Write Operations (Master Transmission)

<1> SS11 is set to 1 and the master enters the communication ready state. MD110 is set to 1 to specify the buffer empty interrupt as the interrupt source.
<2> 0 is output from the P73 pin (CS# = 0) to specify the SPI module in the analog block as the slave.
<3> Transmit-data 1(consisting of 1 bit (1) for R#/W and 7 bits for the address) is set to SDR11[7:0].
<4> The first interrupt occurs. (INTCSI21 = 1 (buffer empty interrupt) and the number of bytes to be transmitted > 0)
<4>-1 Transmit-data 2 (8-bit data) is written to SDR11[7:0] during the interrupt routine.
<5> The second interrupt occurs. (INTCSI21 = 1 (buffer empty interrupt) and the number of bytes to be transmitted ≤ 0)
<5>-1 Receive-data 1 (8-bit dummy data) is read from SDR11[7:0] during the interrupt routine.
<5>-2 MD110 is set to 0 to select the transfer end interrupt as the interrupt source during the interrupt routine.
<6> The third interrupt occurs. (INTCS21 = 1 (transfer end interrupt) and MD110 = 0)
<6>-1 Receive-data 2 (8-bit dummy data) is read from SDR11[7:0] during the interrupt routine.
<6>-2 1 is output from the P73 pin (CS# = 1) to release the SPI module in the analog block as the slave.
<6>-3 ST11 is set to 1 and the master exits the communication ready state.

(5) SPI communication timing chart for read operations (master reception)

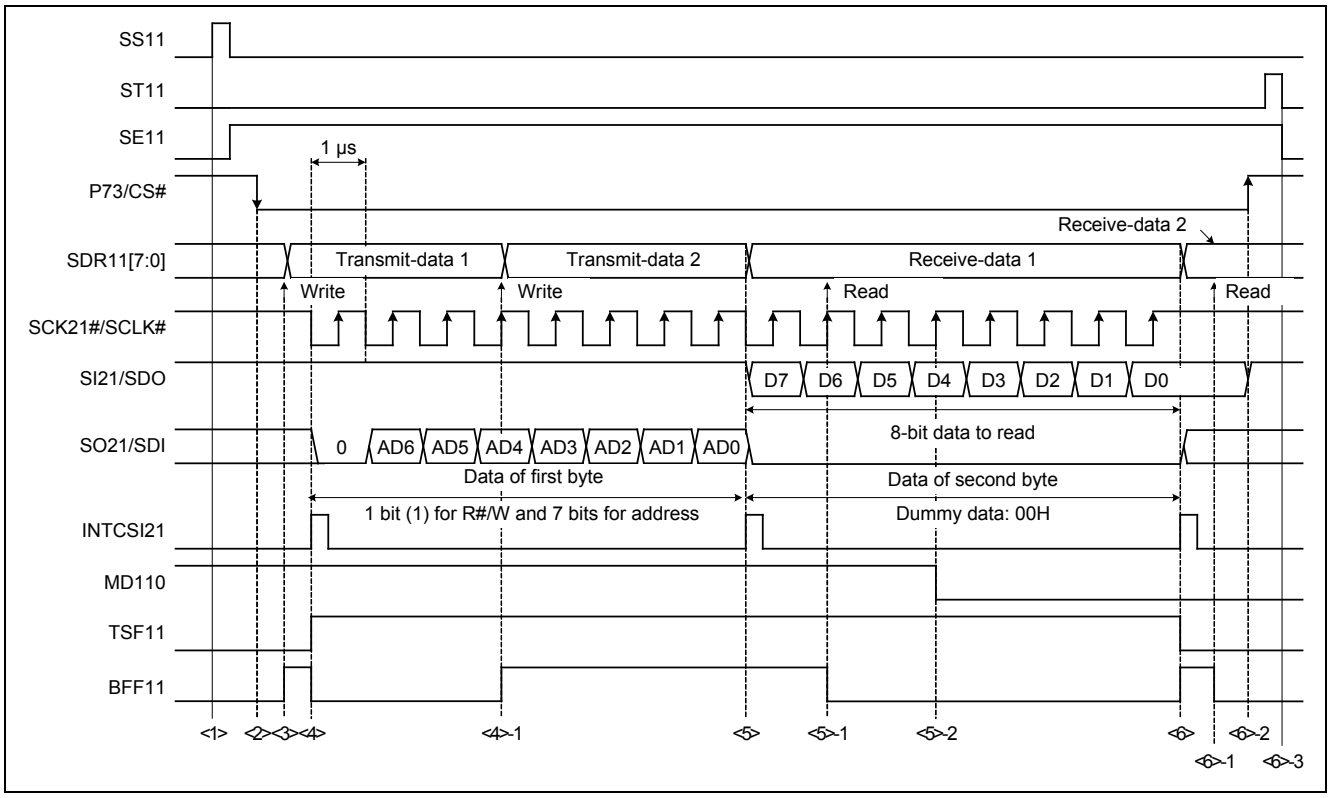


Figure 7.5 SPI Communication Timing Chart for Read Operations (Master Reception)

<1> SS11 is set to 1 and the master enters the communication ready state. MD110 is set to 1 to specify the buffer empty interrupt as the interrupt source.
<2> 0 is output from the P73 pin (CS# = 0) to select the SPI module in the analog block is as the slave.
<3> Transmit-data 1 (consisting of 1 bit (0) for R#/W and 7 bits for the address) is set to SDR11[7:0].
<4> The first interrupt occurs. (INTCSI21 = 1 (buffer empty interrupt) and the number of bytes to be transmitted > 0)
<4>-1 Transmit-data 2 (8-bit dummy data 00H) is written to SDR11[7:0] during the interrupt routine.
<5> The second interrupt occurs. (INTCSI21 = 1 (buffer empty interrupt) and the number of bytes to be transmitted ≤ 0)
<5>-1 Receive-data 1 (8-bit dummy data) is read from SDR11[7:0] during the interrupt routine.
<5>-2 MD110 is set to 0 to select the transfer end interrupt as the interrupt source during the interrupt routine.
<6> The third interrupt occurs. (INTCS21 = 1 (transfer end interrupt) and MD110 = 0)
<6>-1 Receive-data 2 (8-bit data) is read from SDR11[7:0] during the interrupt routine.
<6>-2 1 is output from the P73 pin (CS# = 1) to release the SPI module in the analog block as the slave.
<6>-3 ST11 is set to 1 and the master exits the communication ready state.

Note To continuously perform write/read operations, make sure that the high-level width of the P73/CS# pin in the RL78/G1E (R5F10FMx) satisfies the CS# high-level width (t_{SHA}) prescribed in the SPI section in the electrical specifications in the *RL78/G1E Hardware User's Manual*.

(6) Analog reset control by RL78/G1E (R5F10FMx)

ARESET#, an external reset signal input pin for analog functions in the RL78/G1E (R5F10FMx), is controlled by using the P130 pin output.

The P130 pin in the RL78/G1E (R5F10FMx) is an output-only port pin and outputs a low level during a reset period. That is, a low level is input to the ARESET# pin in the analog block while the microcontroller block of the RL78/G1E (R5F10FMx) is being reset, making the analog block of the RL78/G1E (R5F10FMx) enter the reset state.

The reset state of the analog block of the RL78/G1E (R5F10FMx) ends when the output from the P130 pin is set to high level by using software after the reset period of the microcontroller block of the RL78/G1E (R5F10FMx) ends.

Figure 7.6 shows the pin connections of the analog reset control function in the RL78/G1E (R5F10FMx).

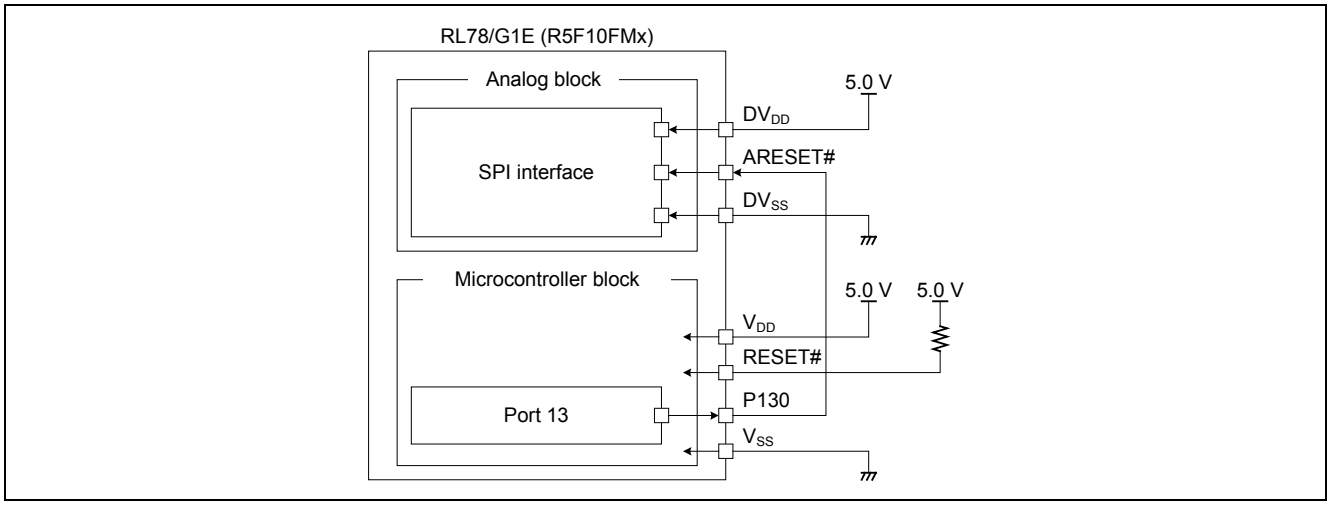
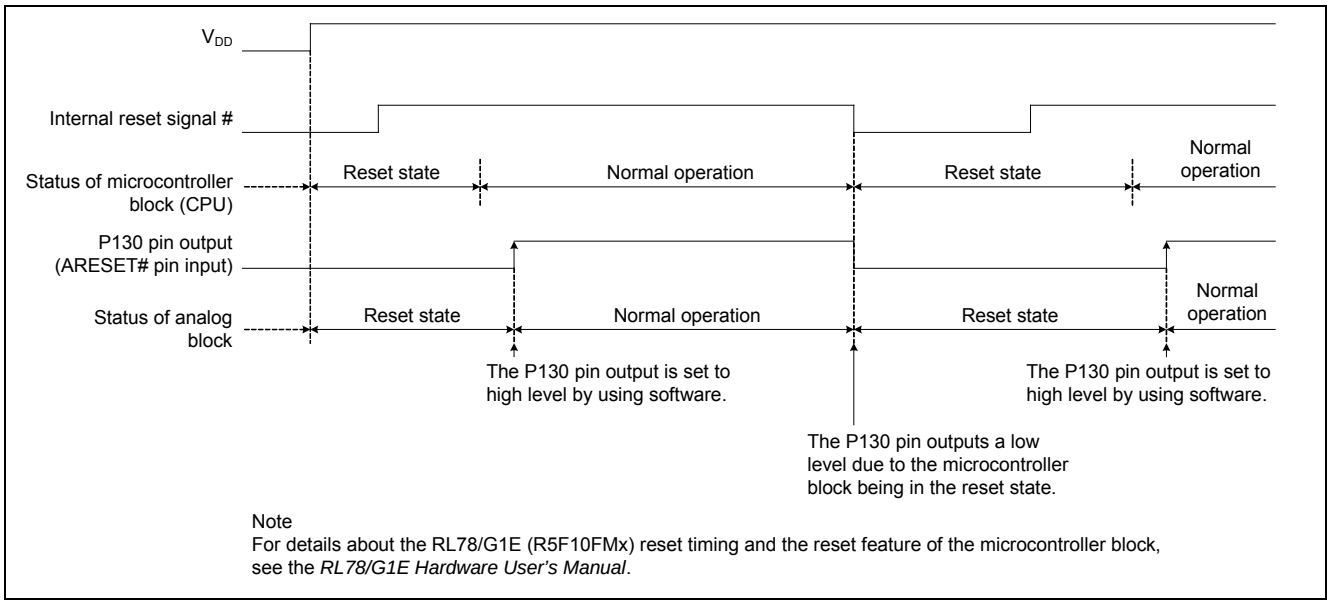


Figure 7.6 Connection of Analog Reset Control Pins in RL78/G1E (R5F10FMx)

Figure 7.7 shows the timing of the analog reset function associated with the microcontroller block of the RL78/G1E.



Note
For details about the RL78/G1E (R5F10FMx) reset timing and the reset feature of the microcontroller block, see the *RL78/G1E Hardware User's Manual*.

Figure 7.7 Analog Reset Function Associated with the Microcontroller Block of the RL78/G1E

7.2.3 A/D converter

The A/D converter incorporated in the RL78/G1E (R5F10FMx) converts the value of the analog voltage output from configurable amplifier Ch3 (used as a differential amplifier) in the analog block and stepped down by using a resistor divider to a digital value. The A/D converter incorporated in the RL78/G1E (R5F10FMx) is described below.

(1) A/D converter incorporated in RL78/G1E (R5F10FMx)

In this application note, the signal of the voltage output from configurable amplifier Ch3 (used as a differential amplifier) in the RL78/G1E (R5F10FMx) and stepped down by using a resistor divider is connected to the ANI2 pin in the A/D converter to enable A/D conversion of signals input to the ANI2 pin.

Specify the settings for the A/D converter as shown below.

- A/D conversion sampling rate: 1 kHz
  - If the LCD module display is updated every 100 ms, for example, 100 results sampled from 100 A/D conversions are averaged and the result is used for calculation. The result is then displayed on the LCD module.
  - To perform an A/D conversion every 1 ms, use the A/D converter with hardware trigger no-wait mode specified as the trigger mode, select mode specified as the channel selection mode, and one-shot conversion mode specified as the conversion operation mode.
  - Use channel 1 of timer array unit 0 as the hardware trigger source.

- Supply of input clock to A/D converter: Enable
  - Set ADCEN to 1 in peripheral enable register 0 (PER0) to enable supplying the input clock to the A/D converter. (Enable reading from and writing to SFRs used by the A/D converter.)

- Reference voltage source: AV_{DD}/AV_{SS}
  - Set ADREFP1 to 0 and ADREFP0 to 0 in A/D converter mode register 2 (ADM2) to specify AV_{DD} as the reference voltage source for the + side of the A/D converter.
  - Set ADREFM to 0 in A/D converter mode register 2 (ADM2) to specify AV_{SS} as the reference voltage source for the - side of the A/D converter.

- A/D conversion time: 54 μs
  - To minimize the effect of signal source impedance, specify $f_{CLK}/32$ (f_{CLK} = 32 MHz) as the conversion clock (f_{AD}) so as to ensure the longest A/D conversion time. * When 12-bit A/D conversion, no stabilization wait time, and hardware trigger no-wait mode are specified

- Resolution: 12 bits
  - Set ADTYP to 0 in A/D converter mode register 2 (ADM2) to specify 12-bit resolution as the A/D conversion resolution.

- Trigger mode: Hardware trigger no-wait mode
  - Set ADTMD1 to 1 and ADTMD0 to 0 in A/D converter mode register 1 (ADM1) to specify hardware trigger no-wait mode as A/D conversion trigger mode.

- Hardware trigger signal: Timer array unit 0 channel 1 interrupt signal (INTTM01)
  - Set ADTRS1 to 0 and ADTRS0 to 0 in A/D converter mode register 1 (ADM1) to specify the "end of count or capture by channel 1 in timer array unit 0" interrupt signal (INTTM01) as the hardware trigger signal.

- Channel selection mode: Select mode
  - Set ADMD to 0 in A/D converter mode register 0 (ADM0) to specify select mode as the A/D conversion channel selection mode.

- Conversion operation mode: One-shot conversion mode
  - Set ADSCM to 1 in A/D converter mode register 1 (ADM1) to specify one-shot conversion mode as the A/D conversion operation mode.

- Analog input channel: ANI2
  - Set ADISS to 0, ADS4 to 0, ADS3 to 0, ADS2 to 0, ADS1 to 1, and ADS0 to 0 in the analog input channel specification register (ADS) to specify ANI2 as the channel to which to input the analog voltage subject to A/D conversion.

(2) A/D conversion timing chart

Figure 7.8 shows the A/D conversion timing chart when hardware trigger no-wait mode is specified as the trigger mode, select mode is specified as the channel selection mode, and one-shot conversion mode is specified as the conversion operation mode.

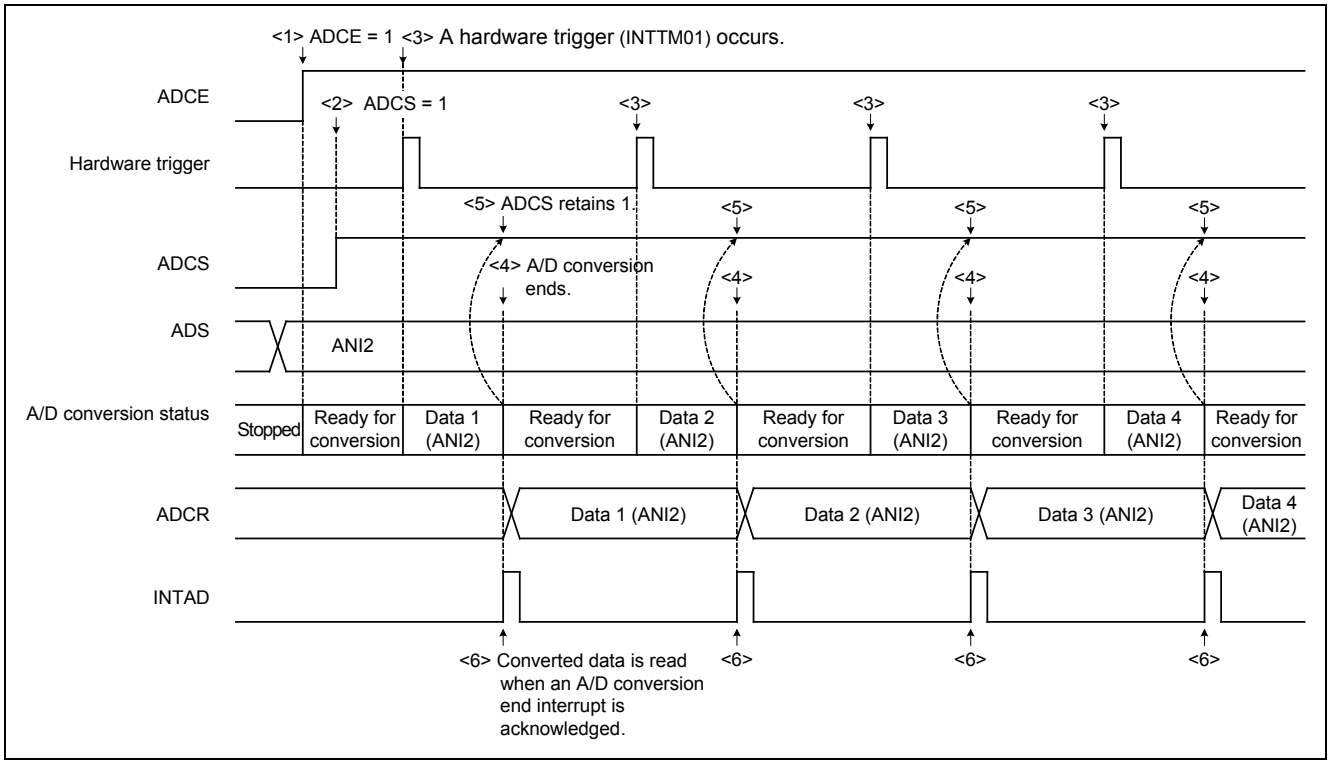


Figure 7.8 A/D Conversion Timing Chart

<1> ADCE is set to 1 in A/D converter mode register 0 (ADM0) and the A/D converter, which was stopped, enters the A/D conversion ready state. The initial settings are applied to the A/D converter.
<2> ADCS is set to 1 in the ADM0 register and the A/D converter waits for a hardware trigger to be input. (A/D conversion does not start in this state.) A/D conversion does not start even if ADCS is set to 1 while the A/D converter is waiting for a hardware trigger to be input.
<3> When the specified hardware trigger (interrupt signal of channel 1 in timer array unit 0 (INTTM01)) is input while ADCS is 1, A/D conversion starts on the analog input channel (ANI2) specified by the analog input channel specification register (ADS).
<4> When A/D conversion ends, the conversion result is stored in the A/D conversion result register (ADCR), and then the A/D conversion end interrupt request signal (INTAD) is generated.
<5> When A/D conversion ends, the ADCS bit remains 1 and the A/D converter enters the A/D conversion ready state.
<6> The A/D conversion result is read from the ADCR register during A/D conversion end interrupt processing.

7.2.4 Timer array unit 0

In this application note, channel 1 of timer array unit 0 is used to generate a hardware trigger signal for the A/D converter, and channel 3 of timer array unit 0 is used to generate the time during which the software is kept waiting (software wait time).

The settings specified for channels 1 and 3 of timer array unit 0 are as follows.

(1) Settings for channel 1 of timer array unit 0

Channel 1 of timer array unit 0 is used to generate a hardware trigger signal for the A/D converter. Using the interval timer in independent channel operation mode, timer array unit 0 generates an A/D converter hardware trigger signal at 1 ms intervals.

Specify the settings for channel 1 of timer array unit 0 as shown below.

- Supply of input clock to timer array unit 0: Enable
  - Set TAU0EN to 1 in peripheral enable register 0 (PER0) to enable supplying the input clock to channel 1 of timer array unit 0. (Enable reading from and writing to SFRs used by timer array unit 0.)

- Mode: Interval timer mode
  - Set MD013 to 0, MD012 to 0, MD011 to 0, and MD010 to 0 in timer mode register 01 (TMR01) to specify interval timer mode as the operating mode of channel 1 of timer array unit 0, and specify that the timer interrupt is not generated when counting starts.

- Interrupt interval: 1 ms
  - Set PRS003 to 0, PRS002 to 0, PRS001 to 0, and PRS000 to 0 in timer clock select register 0 (TPS1) to specify 32 MHz (when f_{CLK} = 32 MHz) as the frequency of the operating clock (CK00).
  - Set CKS011 to 0 and CKS010 to 0 in the TMR01 register to specify the operating clock specified by using the TPS0 register (CK00; 32 MHz) as the operating clock of channel 1 of timer array unit 0 (f_{MCK}).
  - Set CCS01 to 0 in the TMR01 register to specify the operating clock specified by using the CKS011 and CKS010 bits (CK00) as the count clock of channel 1 of timer array unit 0 (f_{TCLK}).
  - Set MASTER01 to 0 in the TMR01 register to specify the independent channel operation mode for channel 1 of timer array unit 0.
  - Set SPLIT01 to 0 in the TMR01 register to specify 16-bit operation for channel 1 of timer array unit 0.
  - Set STS012 to 0, STS011 to 0, and STS010 to 0 in the TMR01 register to specify "only software trigger start is valid (other trigger sources are unselected)" as the start trigger for channel 1 of timer array unit 0.
  - Set timer data register 01 (TDR01) to 7CFFH (31999) to specify 1 ms as the interval of the interrupt generated by channel 1 of timer array unit 0. (31999 + 1) * 1/32000000 = 1 ms

(2) Settings for channel 3 of timer array unit 0

Channel 3 of timer array unit 0 is used to generate the software wait time. Using the interval timer in independent channel operation mode, timer array unit 0 generates a software wait time of 1 ms or 1 μs.

Specify the settings for channel 3 of timer array unit 0 as shown below.

- Supply of input clock to timer array unit 0: Enable
  - Set TAU0EN to 1 in peripheral enable register 0 (PER0) to enable supplying the input clock to channel 1 of timer array unit 0. (Enable reading from and writing to SFRs used by timer array unit 0.)

- Mode: Interval timer mode
  - Set MD033 to 0, MD032 to 0, MD031 to 0, and MD030 to 0 in timer mode register 03 (TMR03) to specify interval timer mode as the operating mode of channel 3 of timer array unit 0, and specify that the timer interrupt is not generated when counting starts.

- Interrupt interval: 1 ms or 1 μs
  - Set PRS003 to 0, PRS002 to 0, PRS001 to 0, and PRS000 to 0 in timer clock select register 0 (TPS1) to specify 32 MHz (when f_{CLK} = 32 MHz) as the frequency of the operating clock (CK00).
  - Set CKS031 to 0 and CKS030 to 0 in the TMR03 register to specify the operating clock specified by using the TPS0 register (CK00; 32 MHz) as the operating clock of channel 3 of timer array unit 0 (f_{MCK}).
  - Set CCS03 to 0 in the TMR03 register to specify the operating clock specified by using the CKS031 and CKS030 bits (CK00) as the count clock of channel 3 of timer array unit 0 (f_{TCLK}).
  - Set MASTER03 to 0 in the TMR03 register to specify the independent channel operation mode for channel 3 of timer array unit 0.
  - Set SPLIT03 to 0 in the TMR03 register to specify 16-bit operation for channel 3 of timer array unit 0.
  - Set STS032 to 0, STS031 to 0, and STS030 to 0 in the TMR03 register to specify "only software trigger start is valid (other trigger sources are unselected)" as the start trigger for channel 3 of timer array unit 0.
  - To set the interrupt interval to 1 ms:
    Set timer data register 03 (TDR03) to 7CFFH (31999) to specify 1 ms as the interval of the interrupt generated by channel 3 of timer array unit 0. (31999 + 1) * 1/32000000 = 1 ms
  - To set the interrupt interval to 1 μs: Set timer data register 03 (TDR03) to 1FH (31) to specify 1 μs as the interval of the interrupt generated by channel 3 of timer array unit 0. (31 + 1) * 1/32000000 = 1 μs

7.2.5 LCD module control

In this application note, the LCD module (ACM0802C) is used to display the physical quantity and results of A/D conversion. The LCD module is controlled by using the output pins of port 4 (P41 and P42) and port 0 (P00 to P03) in the RL78/G1E (R5F10FMx).

Four signal lines are used to interface with the LCD module (4-bit interface). The LCD module can only be written because the R/W# pin of the LCD module is fixed to low level.

Figure 7.9 shows the pin connections of the LCD module.

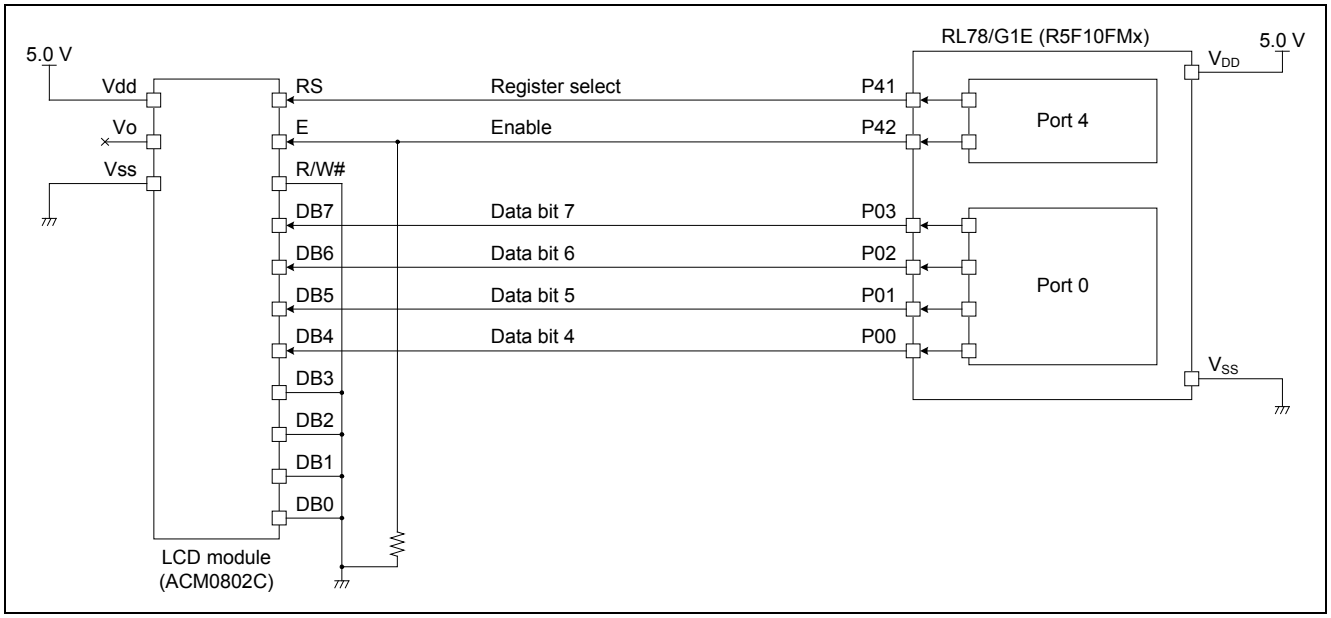


Figure 7.9 Connection of LCD Module

Specify the settings as shown below when using the P41, P42, and P00 to P03 pins as output pins to control the LCD module (ACM0802C).

- Specify the P41 and P42 pins as output pins.
  - Set PMC41 to 0 in port mode control register 4 (PMC4) to specify the P41 pin as a digital I/O pin (alternate function other than analog input).
  - Set P41 to 1 and P42 to 1 in port register 4 (P4) to specify the latched value output from the P41 and P42 pins. (The initial level of the P41 and P42 pin output is set to high.)
  - Set PM41 to 1 and PM42 to 1 in port mode register 4 (PM4) to specify the I/O mode of the P41 and P42 pins as output mode. (The output buffer is turned on.)

- Specify the P00 to P03 pins as output pins.
  - Set PMC02 to 0 and PMC03 to 0 in port mode control register 0 (PMC0) to specify the P02 and P03 pins as digital I/O pins (alternate function other than analog input).
  - Set P01 to 1, P02 to 1, and P03 to 1 in port register 0 (P0) to specify the latched value output from the P00 to P03 pins. (The initial level of the P00 to P03 pin output is set to high.)
  - Set PM03 to 0, PM02 to 0, PM01 to 0, and PM00 to 0 in port mode register 0 (PM0) to specify the I/O mode of the P00 to P03 pins as output mode. (The output buffer is turned on.)

7.3 Software

7.3.1 Timing charts

A chart that shows the timing between power application and initial setup and a chart that shows the timing of A/D conversion performed in the RL78/G1E (R5F10FMx) and LCD module display update used in this application note are shown below.

(1) Timing between power application and initial setup

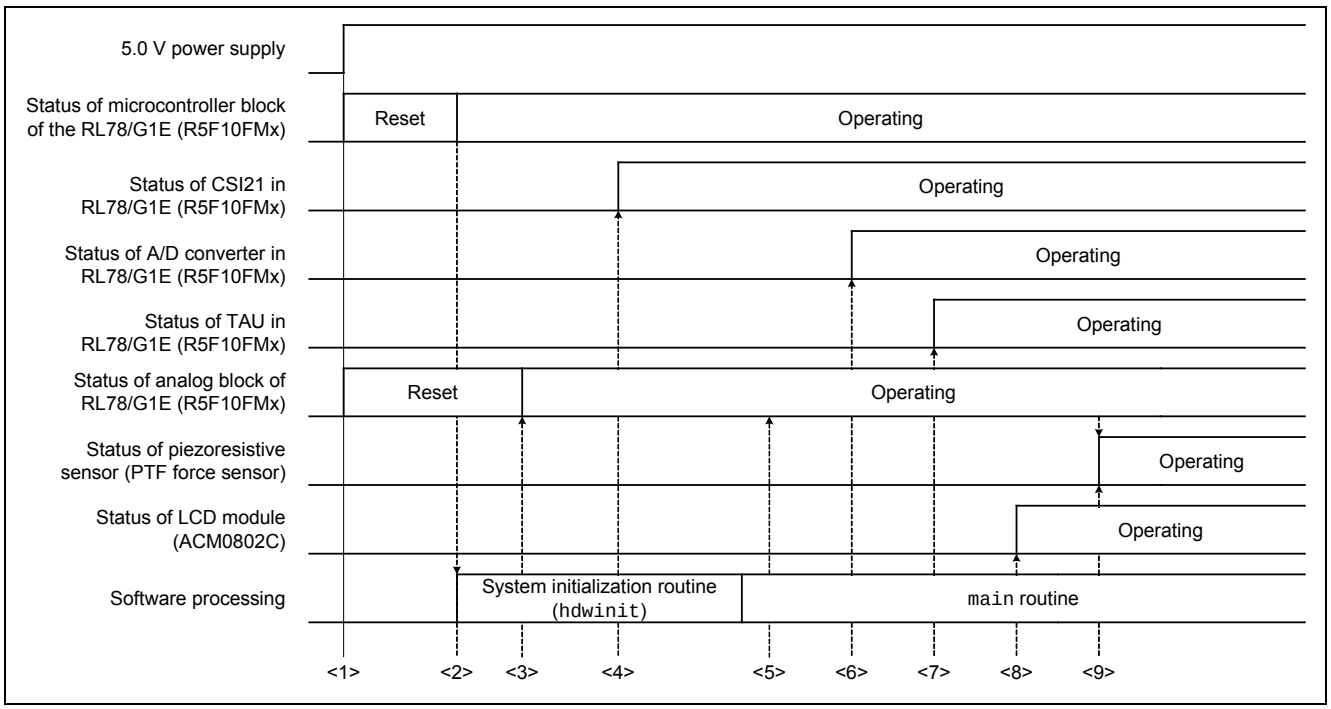


Figure 7.10 Timing Between Power Application and Initial Setup

<1> When power of 5.0 V is applied, the power-on reset circuit in the microcontroller block of the RL78/G1E starts reset processing. In conjunction with the reset processing, a low level is output from the P130 pin, which places the analog block in the reset state.

<2> When the reset state in the RL78/G1E (R5F10FMx) is released, software starts the system initialization routine (`hdwinit`).

<3> During the system initialization routine (`hdwinit`), making the P130 pin output high level ends the reset state in the analog block of the RL78/G1E (R5F10FMx).

<4> During the system initialization routine (`hdwinit`), channel 1 (CSI21) of serial array unit 1 incorporated in the RL78/G1E (R5F10FMx) is initialized.

<5> When the system initialization routine (`hdwinit`) ends, the `main` routine starts and the variable output voltage regulator in the analog block of the RL78/G1E (R5F10FMx) is turned on and 3.3 V is output from the LDO_OUT pin (AV_{DD} pin input = 3.3 V).

<6> The A/D converter is initialized during the `main` routine.

<7> Timer array unit 0 is initialized during the `main` routine.

<8> The LCD module is initialized during the `main` routine. (4-bit interface)

<9> The analog block of the RL78/G1E (R5F10FMx) is initialized during the `main` routine. (The SPI control registers are set up.) Configurable amplifier Ch1 (used as a transimpedance amplifier) in the analog block starts operating and voltage starts to be applied to the piezoresistive sensor (PTF force sensor).

(2) Timing of A/D conversion and LCD module display update

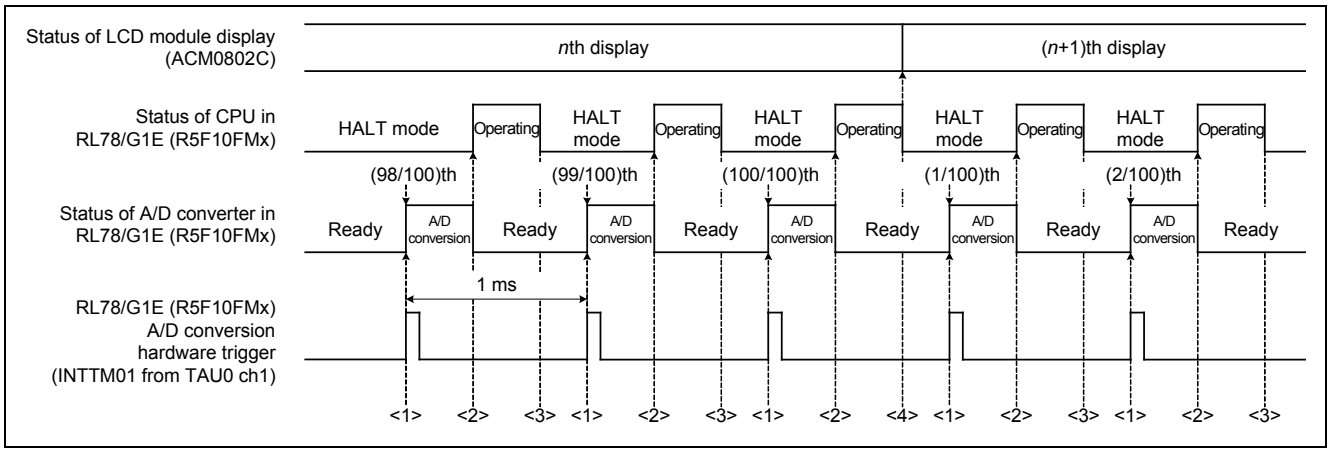


Figure 7.11 Timing of A/D Conversion and LCD Module Display Update

<1> By using channel 1 of timer array unit 0 incorporated in the RL78/G1E (R5F10FMx) as an interval timer, the count end interrupt request signal (INTTM01) is generated at 1 ms intervals. A/D conversion by the A/D converter is started by using INTTM01 as a hardware trigger.

<2> When the A/D converter incorporated in the RL78/G1E (R5F10FMx) finishes A/D conversion of the data input from the ANI2 pin, an A/D conversion end interrupt request signal (INTAD) is generated, and the CPU exits HALT mode.

<3> After exiting HALT mode, the CPU incorporated in the RL78/G1E (R5F10FMx) reads the A/D conversion result and stores it in the internal RAM. The CPU enters HALT mode again.

<4> After A/D conversion is executed 100 times, the CPU calculates the average value of the 100 A/D conversion results, and uses the averaged A/D conversion result to calculate the physical quantity (force). The CPU updates the LCD module display (calculated average value of A/D conversion results and the physical quantity (force)).

7.3.2 Register settings specified for the microcontroller block of the RL78/G1E (R5F10FMx)

The register settings specified for the microcontroller block of the RL78/G1E (R5F10FMx) are shown below.

Caution 1 For how to specify the register settings, see the *RL78/G1E Hardware User's Manual*.
Caution 2 Use the bits for which no description is given with their default values (values following "After reset" on the following pages).

(1) Setting of user option bytes

(a) User option byte 000C0H/010C0H

Address: 000C0H/010C0H Set value: EEH

Address:	7	6	5	4	3	2	1	0
000C0H/ 010C0H	WDTINT	WINDOW 1	WINDOW 0	WDTON	WDCS2	WDCS1	WDCS0	WDSTBY ON
Set value	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**0**

WDTINT	Use of interval interrupt of watchdog timer
0	Interval interrupt is not used.
1	**Interval interrupt is generated when 75% of the overflow time is reached.**

WINDOW 1	WINDOW 0	Watchdog timer window open period
0	0	Setting prohibited
0	1	50%
1	0	75%
1	**1**	**100%**

WDTON	Operation of watchdog timer counter
0	**Counter operation disabled (counting stopped after reset)**
1	Counter operation enabled (counting started after reset)

WDCS2	WDCS1	WDCS0	Watchdog timer overflow time (f_{IL} = 17.25 kHz (Max.))
0	0	0	$2^6/f_{IL}$ (3.71 ms)
0	0	1	$2^7/f_{IL}$ (7.42 ms)
...	...	...	...
1	1	0	$2^{14}/f_{IL}$ (949.80 ms)
1	**1**	**1**	**$2^{16}/f_{IL}$ (3799.19 ms)**

WDSTBY ON	Operation of watchdog timer counter (HALT/STOP mode)
0	**Counter operation stopped in HALT/STOP mode**
1	Counter operation enabled in HALT/STOP mode

(b) User option byte 000C1H/010C1H

Address: 000C1H/010C1H Set value: 73H

Address:	7	6	5	4	3	2	1	0
000C1H/ 010C1H	VPOC2	VPOC1	VPOC0	1	LVIS1	LVIS0	LVIMDS1	LVIMDS0
Set value	**0**	**1**	**1**	**1**	**0**	**0**	**1**	**1**

■ When used in reset mode

Detection voltage (V)		LVIMDS1	LVIMDS0	VPOC2	VPOC1	VPOC0	LVIS1	LVIS0
V_{LVIH}								
Rising edge	Falling edge							
3.13	3.06	**1**	**1**	0	0	1	0	0
3.75	3.67			0	1	0	0	0
4.06	**3.98**			**0**	**1**	**1**	**0**	**0**
Other than above		Setting prohibited						

(c) User option byte 000C2H/010C2H

Address: 000C2H/010C2H Set value: E8H

Address:	7	6	5	4	3	2	1	0
000C2H/ 010C2H	CMODE1	CMODE0	1	0	FRQSEL 3	FRQSEL 2	FRQSEL 1	FRQSEL 0
Set value	**1**	**1**	**1**	**0**	**1**	**0**	**0**	**0**

CMODE1	CMODE0	Setting of flash operation mode		
			Operating frequency range	Operating voltage range
0	0	LV (low voltage main) mode	1 to 4 MHz	1.6 to 5.5 V
1	0	LS (low speed main) mode	1 to 8 MHz	1.8 to 5.5 V
1	**1**	**HS (high speed main) mode**	1 to 16 MHz	2.4 to 5.5 V
			1 to 32 MHz	**2.7 to 5.5 V**
Other than above		Setting prohibited		

FRQSEL 3	FRQSEL 2	FRQSEL 1	FRQSEL 0	Frequency of high-speed on-chip oscillator
1	**0**	**0**	**0**	**32 MHz**
0	0	0	0	24 MHz
...	...	...	...	...
1	1	0	1	1 MHz
Other than above				Setting prohibited

(2) Settings of registers that control the clock generator

(a) Clock operation mode control register (CMC)

Address: FFFA0H After reset: 00H R/W Set value: 10H

Symbol	7	6	5	4	3	2	1	0
CMC	EXCLK	OSCSEL	0	0	0	0	0	AMPH
Set value	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**

EXCLK	OSCSEL	High-speed system clock pin operation mode	X1/P121 pin	X2/EXCLK/P122 pin
0	**0**	**Input port mode**	**Input port**	
0	1	XT1 oscillation mode	Crystal/ceramic resonator connection	
1	0	Input port mode	Input port	
1	1	External clock input mode	Input port	External clock input

(b) Clock operation status control register (CSC)

Address: FFFA1H After reset: C0H R/W Set value: C0H

Symbol	7	6	5	4	3	2	1	0
CSC	MSTOP	1	0	0	0	0	0	HIOSTOP
Set value	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**

MSTOP	High-speed system clock operation		
	XT1 oscillation mode	External clock input mode	Input port mode
0	X1 oscillator operating	External clock from EXCLK pin is valid	**Input port**
1	**X1 oscillator stopped**	**External clock from EXCLK pin is invalid**	

HIOSTOP	High-speed on-chip oscillator clock operation
0	**High-speed on-chip oscillator operating**
1	High-speed on-chip oscillator stopped

(c) System clock control register (CKC)

Address: FFFA4H After reset: 00H R/W Set value: 00H

Symbol	7	6	5	4	3	2	1	0
CKC	CLS	0	MCS	MCM0	0	0	0	0
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

MCM0	Main system clock (f_{MAIN}) operation
0	**The high-speed on-chip oscillator clock (f_{MAIN}) is selected as the main system clock (f_{IH})**
1	The high-speed system clock (f_{MX}) is selected as the main system clock (f_{MAIN})

(d) Peripheral enable register 0 (PER0)

Address: F00F0H After reset: 00H R/W Set value: 29H

Symbol	7	6	5	4	3	2	1	0
PER0	RTCEN	0	ADCEN	0	SAU1EN	SAU0EN	0	TAU0EN
Set value	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**1**

RTCEN	Control of interval timer input clock supply
0	**Stop the input clock supply.** **• SFRs used by the interval timer cannot be written.** **• The interval timer is in the reset status.**
1	Enable the input clock supply. • SFRs used by the interval timer can be written.

ADCEN	Control of A/D converter input clock supply
0	Stop the input clock supply. • SFRs used by the A/D converter cannot be written. • A/D converter is in the reset status.
1	**Enable the input clock supply.** **• SFRs used by the A/D converter can be written.**

SAU1EN	Control of serial array unit 1 input clock supply
0	Stop the input clock supply. • SFRs used by serial array unit 1 cannot be written. • Serial array unit 1 is in the reset status.
1	**Enable the input clock supply.** **• SFRs used by serial array unit 1 can be written.**

SAU0EN	Control of serial array unit 0 input clock supply
0	**Stop the input clock supply.** **• SFRs used by serial array unit 0 cannot be written.** **• Serial array unit 0 is in the reset status.**
1	Enable the input clock supply. • SFRs used by serial array unit 0 can be written.

TAU0EN	Control of timer array unit 0 input clock supply
0	Stop the input clock supply. • SFRs used by timer array unit 0 cannot be written. • Timer array unit 0 is in the reset status.
1	**Enable the input clock supply.** **• SFRs used by timer array unit 0 can be written.**

(3) Settings of registers that control serial array unit 1

(a) Serial mode register 11 (SMR11)

Address: F0152H, F0153H After reset: 0020H R/W Set value: 002*H

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMR11	CKS11	CCS11	0	0	0	0	0	STS11	0	SIS110	1	0	0	MD112	MD111	MD110
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	*

CKS11	Selection of operation clock of channel 1 (f_{MCK})
0	**Operation clock set by the SPS1 register (CK10)**
1	Operation clock set by the SPS1 register (CK11)

CCS11	Selection of transfer clock of channel 1 (f_{TCLK})
0	**Divided clock of operation clock (f_{MCK}) specified by the CKS11 bit**
1	Clock input from the SCK21 pin (slave transfer in CSI mode) (f_{SCK})

STS11	Selection of start trigger source
0	**Only software trigger is valid (selected for CSI, UART transmission, and simplified I^2C)**
1	Valid edge of the RXD2 pin (selected for UART reception)

MD112	MD111	Setting of operation mode of channel 1
0	**0**	**CSI mode**
0	1	UART mode
1	0	Simplified I^2C mode
1	1	Setting prohibited

MD110	Selection of interrupt source of channel 1
0	**Transfer end interrupt**
1	**Buffer empty interrupt (Occurs when data is transferred from the SDR11 register to the shift register.)**

Remark: * = Switch the transfer end interrupt (= 0) and buffer empty interrupt (= 1) by using software.

(b) Serial communication operation setting register 11 (SCR11)

Address: F015AH, F015BH After reset: 0087H R/W Set value: C007H

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCR11	TXE11	RXE11	DAP11	CKP11	0	EOC11	PTC111	PTC110	DIR11	0	0	SLC110	0	1	1	DLS110
Set value	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**

TXE11	RXE11	Setting of operation mode of channel 1
0	0	Disable communication.
0	1	Reception only
1	0	Transmission only
1	**1**	**Transmission and reception**

DAP11	CKP11	Selection of data and clock phase in CSI mode
0	**0**	**Type 1**
0	1	Type 2
1	0	Type 3
1	1	Type 4

DIR11	Selection of data transfer sequence in CSI and UART modes
0	**Input/output data MSB first.**
1	Input/output data LSB first.

DLS110	Setting of data length in CSI and UART modes
0	7-bit data length (stored in bits 0 to 6 of the SDR11 register)
1	**8-bit data length (stored in bits 0 to 7 of the SDR11 register)**

(c) Serial data register 11 (SDR11)

Address: FFF4AH, FFF4BH After reset: 0000H R/W Set value: 1E**H

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDR11																
Set value	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**0**	*	*	*	*	*	*	*	*

SDR11[15:9]							Selection of transfer clock (divided operating clock (f_{MCK}))
0	0	0	0	0	0	0	f_{MCK}/2
0	0	0	0	0	0	1	f_{MCK}/4
...	...	...	...	...	...	...	...
0	**0**	**0**	**1**	**1**	**1**	**1**	**f_{MCK}/32**
...	...	...	...	...	...	...	...
1	1	1	1	1	1	0	f_{MCK}/254
1	1	1	1	1	1	1	f_{MCK}/256

Remark: * = Functions as a transmission/reception buffer register.

(d) Serial channel stop register 1 (ST1)

Address: F0164H, F0165H After reset: 0000H R/W Set value: 000*H

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ST1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ST11	ST10
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	*	**0**

ST11	Operation stop trigger of channel 1
0	**No trigger operation**
1	**Clear the SE11 bit to 0 and stop the communication operation.**

Remark: * = Write 1 to this bit only when finishing serial communication.

(e) Serial clock select register 1 (SPS1)

Address: F0166H, F0167H After reset: 0000H R/W Set value: 0000H

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPS1	0	0	0	0	0	0	0	0	PRS113	PRS112	PRS111	PRS110	PRS103	PRS102	PRS101	PRS100
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

PRS103	PRS102	PRS101	PRS100	Selection of operation clock (CK10)					
					f_{CLK} = 2 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	f_{CLK} = 20 MHz	f_{CLK} = 32 MHz
0	**0**	**0**	**0**	**f_{CLK}**	**2 MHz**	**5 MHz**	**10 MHz**	**20 MHz**	**32 MHz**
0	0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	16 MHz
...	...	...	...	...					
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	305 Hz	610 Hz	1.22 kHz	1.95 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61 Hz	153 Hz	305 Hz	610 Hz	976 Hz

(f) Serial output register 1 (SO1)

Address: F0168H, F0169H After reset: 0F0FH R/W Set value: 0301H

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SO1	0	0	0	0	0	0	CKO11	CKO10	0	0	0	0	0	0	SO11	SO10
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**

CKO11	Serial clock output of channel 1
0	Serial clock output value is “0”.
1	**Serial clock output value is “1”.**

SO11	Serial clock output of channel 1
0	**Serial data output value is “0”.**
1	Serial data output value is “1”.

(g) Serial output enable register 1 (SOE1)

Address: F016AH, F016BH After reset: 0000H R/W Set value: 0002H

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOE1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SOE11	SOE10
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**

SOE11	Serial output enable/stop of channel 1
0	Stop output by using serial communication.
1	**Enable output by using serial communication.**

(h) Serial channel start register 1 (SS1)

Address: F0162H, F0163H After reset: 0000H R/W Set value: 0002H

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SS1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SS11	SS10
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**

SS11	Operation start trigger of channel 1
0	No trigger operation
1	**Clear the SE11 bit to 1 and enter the communication wait status.**

(4) Settings of registers that control the ports

(a) Port mode registers

Address: FFF20H After reset: FFH R/W Set value: 90H

Symbol	7	6	5	4	3	2	1	0
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00
Set value	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**

Address: FFF21H After reset: FFH R/W Set value: BFH

Symbol	7	6	5	4	3	2	1	0
PM1	1	PM16	PM15	PM14	PM13	PM12	PM11	PM10
Set value	**1**	**0**	**1**	**1**	**1**	**1**	**1**	**1**

Address: FFF22H After reset: FFH R/W Set value: 1FH

Symbol	7	6	5	4	3	2	1	0
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20
Set value	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**

Address: FFF24H After reset: FFH R/W Set value: F1H

Symbol	7	6	5	4	3	2	1	0
PM4	1	1	1	1	PM43	PM42	PM41	PM40
Set value	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**1**

Address: FFF26H After reset: FFH R/W Set value: F0H

Symbol	7	6	5	4	3	2	1	0
PM6	1	1	1	1	PM63	PM62	PM61	PM60
Set value	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**

Address: FFF27H After reset: FFH R/W Set value: 02H

Symbol	7	6	5	4	3	2	1	0
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**

Address: FFF2EH After reset: FFH R/W Set value: FDH

Symbol	7	6	5	4	3	2	1	0
PM14	1	1	1	1	1	1	PM141	PM140
Set value	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**1**

Address: FFF2FH After reset: FFH R/W Set value: E0H

Symbol	7	6	5	4	3	2	1	0
PM15	1	1	1	PM154	PM153	PM152	PM151	PM150
Set value	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**

PMmn	PMmn pin I/O mode selection (m = 0 to 2, 4, 6, 7, 14, 15; n = 0 to 7)
0	**Output mode (output buffer on)**
1	**Input mode (output buffer off)**

(b) Port registers

Address: FFF00H After reset: 00H R/W Set value: 0*H

Symbol	7	6	5	4	3	2	1	0
P0	0	0	0	P04	P03	P02	P01	P00
Set value	**0**	**0**	**0**	**0**	*	*	*	*

Address: FFF04H After reset: 00H R/W Set value: 0*H

Symbol	7	6	5	4	3	2	1	0
P4	0	0	0	0	0	P42	P41	P40
Set value	**0**	**0**	**0**	**0**	**0**	*	*	**0**

Address: FFF07H After reset: 00H R/W Set value: 0*H

Symbol	7	6	5	4	3	2	1	0
P7	0	0	0	0	P73	P72	P71	P70
Set value	**0**	**0**	**0**	**0**	*	**1**	**0**	**1**

Address: FFF0DH After reset: Undefined R/W Set value: 01H

Symbol	7	6	5	4	3	2	1	0
P13	P137	0	0	0	0	0	0	P130
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**

Pmn	(m = 0, 4, 7, 13, n = 0 to 4, or 7)	
	Output data control (in output mode)	Input data read (in input mode)
0	**Output 0**	**Input a low level**
1	**Output 1**	**Input a high level**

Remark: * = Write 0 or 1 to switch the output level according to the status.

(c) Port mode control registers

Address: FFF60H After reset: FFH R/W Set value: F3H

Symbol	7	6	5	4	3	2	1	0
PMC0	1	1	1	1	PMC03	PMC02	1	1
Set value	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**1**

Address: FFF64H After reset: FFH R/W Set value: FDH

Symbol	7	6	5	4	3	2	1	0
PMC4	1	1	1	1	1	1	PMC41	1
Set value	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**1**

Address: FFF67H After reset: FFH R/W Set value: FEH

Symbol	7	6	5	4	3	2	1	0
PMC7	1	1	1	1	1	1	1	PMC70
Set value	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**

PMCmn	Pmn pin digital I/O and analog input selection (m = 0, 4, 7; n = 0 to 3)
0	**Digital I/O (alternate function other than analog input)**
1	Analog input

(5) Settings of registers that control A/D converter

(a) A/D converter mode register 0 (ADM0)

Address: FFF30H After reset: 00H R/W Set value: 81H

Symbol	7	6	5	4	3	2	1	0
ADM0	ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
Set value	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**

ADCS	A/D conversion operation
0	Stop conversion operation [When read] Conversion stopped/standby status
1	**Enable conversion operation** [When read] While in the software trigger mode: Conversion operation status While in the hardware trigger wait mode: Stabilization wait status + conversion operation status

ADMD	Specification of the A/D conversion channel selection mode
0	**Select mode**
1	Scan mode

ADCE	A/D voltage comparator operation
0	Stop A/D voltage comparator operation
1	**Enable A/D voltage comparator operation**

■ When performing 12-bit A/D conversion, no stabilization wait time, and hardware trigger no-wait mode are specified

FR2	FR1	FR0	LV1	LV0	Mode	Number of conversion clock cycles (f_{CLK})	Conversion time selection AV_{DD} = 2.7 to 3.6 V f_{CLK} = 32 MHz	Conversion clock (f_{AD})
0	**0**	**0**	**0**	**0**	**Normal 1**	**1728**	**54 μs**	**f_{CLK}/32**
0	0	1				864	27 μs	f_{CLK}/16
...	...	...				...	...	...
1	1	0				108	3.375 μs	f_{CLK}/2
1	1	1				54	Setting prohibited	f_{CLK}/1
0	0	0	0	1	Normal 2	2112	66 μs	f_{CLK}/32
0	0	1				1056	33 μs	f_{CLK}/16
...	...	...				...	...	...
1	1	0				132	4.125 μs	f_{CLK}/2
1	1	1				66	Setting prohibited	f_{CLK}/1
0	0	0	1	0	Low-voltage 1	2432	76 μs	f_{CLK}/32
0	0	1				1216	38 μs	f_{CLK}/16
...	...	...				...	...	...
1	1	0				152	4.75 μs	f_{CLK}/2
1	1	1				76	Setting prohibited	f_{CLK}/1
0	0	0	1	1	Low-voltage 2	7360	230 μs	f_{CLK}/32
0	0	1				3680	115 μs	f_{CLK}/16
...	...	...				...	...	...
1	1	0				460	14.375 μs	f_{CLK}/2
1	1	1				230	Setting prohibited	f_{CLK}/1

(b) A/D converter mode register 1 (ADM1)

Address: FFF32H After reset: 00H R/W Set value: A0H

Symbol	7	6	5	4	3	2	1	0
ADM1	ADTMD1	ADTMD0	ADSCM	0	0	0	ADTRS1	ADTRS0
Set value	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**

ADTMD1	ADTMD0	Selection of the A/D conversion trigger mode
0	×	Software trigger mode
1	**0**	**Hardware trigger no-wait mode**
1	1	Hardware trigger wait mode

ADSCM	A/D conversion operation
0	Sequential conversion mode
1	**One-shot conversion mode**

ADTRS1	ADTRS0	Selection of the hardware trigger signal
0	**0**	**"End of timer channel 1 count or capture" interrupt signal (INTTM01)**
0	1	Setting prohibited
1	0	Setting prohibited
1	1	Interval timer interrupt signal (INTIT)

Remark x: don't care

(c) A/D converter mode register 2 (ADM2)

Address: F0010H After reset: 00H R/W Set value: 00H

Symbol	7	6	5	4	3	2	1	0
ADM2	ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	0	ADTYP
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

AVREFP1	AVREFP0	Selection of the + side reference voltage source of the A/D converter
0	**0**	**Supplied from AV_{DD}**
0	1	Supplied from P20/AV_{REFP}/ANI0
1	0	Supplied from the internal reference voltage source (1.45 V)
1	1	Setting prohibited

ADREFM	Selection of the – side reference voltage source of the A/D converter
0	**Supplied from AV_{SS}**
1	Supplied from P21/AV_{REFM}/ANI1

ADRCK	Checking the upper limit and lower limit conversion result values
0	**The interrupt signal (INTAD) is output when ADLL register ≤ ADCR register ≤ ADUL register.**
1	The interrupt signal (INTAD) is output when ADCR register < ADLL register or ADUL register < ADCR register.

AWC	Specification of SNOOZE mode
0	**Do not use the SNOOZE mode function.**
1	Use the SNOOZE mode function.

ADTYP	Selection of the A/D conversion resolution
0	**12-bit resolution**
1	8-bit resolution

(d) Conversion result comparison upper limit setting register (ADUL)

Address: F0011H After reset: FFH R/W Set value: FFH

Symbol	7	6	5	4	3	2	1	0
ADUL	ADUL7	ADUL6	ADUL5	ADUL4	ADUL3	ADUL2	ADUL1	ADUL0
Set value	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

(e) Conversion result comparison lower limit setting register (ADLL)

Address: F0012H After reset: 00H R/W Set value: 00H

Symbol	7	6	5	4	3	2	1	0
ADLL	ADLL7	ADLL6	ADLL5	ADLL4	ADLL3	ADLL2	ADLL1	ADLL0
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

(f) Analog input channel specification register (ADS)

Address: FFF31H After reset: 00H R/W Set value: 02H

Symbol	7	6	5	4	3	2	1	0
ADS	ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**

■ Select mode (ADMD = 0)

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Selected channel	Input source
0	0	0	0	0	0	ANI0	P20/ANI0/AVREFPpin
0	0	0	0	0	1	ANI1	P21/ANI1/AVREFPpin
0	**0**	**0**	**0**	**1**	**0**	**ANI2**	**P22/ANI2 pin**
0	0	0	0	1	1	ANI3	P23/ANI3 pin
0	0	0	1	0	0	ANI4	P24/ANI4 pin
0	1	0	0	0	0	ANI16	P03/ANI16 pin
0	1	0	0	0	1	ANI17	P02/ANI17 pin
0	1	0	0	1	0	ANI18	P10/ANI18 pin
0	1	0	1	0	0	ANI20	P11/ANI20 pin
0	1	0	1	0	1	ANI21	P12/ANI21 pin
0	1	0	1	1	0	ANI22	P13/ANI22 pin
0	1	0	1	1	1	ANI23	P14/ANI23 pin
0	1	1	0	0	0	ANI24	P15/ANI24 pin
0	1	1	0	0	1	ANI25	P51/ANI25 pin
0	1	1	0	1	0	ANI26	P50/ANI26 pin
0	1	1	1	0	0	ANI28	P70/ANI28 pin
0	1	1	1	1	0	ANI30	P41/ANI30 pin
1	0	0	0	0	0	–	Temperature sensor
1	0	0	0	0	1	–	Internal reference voltage output (1.45 V)
Other than above						Setting prohibited	

(g) A/D port configuration register (ADPC)

Address: F0076H After reset: 00H R/W Set value: 00H

Symbol	7	6	5	4	3	2	1	0
ADPC	0	0	0	0	0	ADPC2	ADPC1	ADPC0
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ADPC2	ADPC1	ADPC0	Switching between analog input (A) and digital I/O (D)				
			ANI4/P24	ANI3/P23	ANI2/P22	ANI1/P21	ANI0/P20
0	**0**	**0**	**A**	**A**	**A**	**A**	**A**
0	0	1	D	D	D	D	D
0	1	0	D	D	D	D	A
0	1	1	D	D	D	A	A
1	0	0	D	D	A	A	A
1	0	1	D	A	A	A	A
Other than above			Setting prohibited				

(6) Settings of registers that control timer array unit 0

(a) Timer channel stop register 0 (TT0)

Address: F01B4H, F01B5H After reset: 0000H R/W Set value: 000*H

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TT0	0	0	0	0	TTH03	0	TTH01	0	TT07	TT06	TT05	TT04	TT03	TT02	TT01	TT00
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	*****	**0**	*****	**0**

TT03	Operation stop trigger of channel 3
0	**No trigger operation**
1	**Operation is stopped (stop trigger is generated).**

TT01	Operation stop trigger of channel 1
0	**No trigger operation**
1	**Operation is stopped (stop trigger is generated).**

Remark: * = Write 1 to this bit during timer operation to stop the timer operation.

(b) Timer clock selection register 0 (TPS0)

Address: F01B6H, F01B7H After reset: 0000H R/W Set value: 0000H

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TPS0	0	0	PRS031	PRS030	0	0	PRS021	PRS020	PRS013	PRS012	PRS011	PRS010	PRS003	PRS002	PRS001	PRS000
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

PRS003	PRS002	PRS001	PRS000		Selection of operation clock (CK00)				
					f_{CLK} = 2 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	f_{CLK} = 20 MHz	f_{CLK} = 32 MHz
0	**0**	**0**	**0**	**f_{CLK}**	**2 MHz**	**5 MHz**	**10 MHz**	**20 MHz**	**32 MHz**
0	0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	16 MHz
...	...	...	...	...			...		
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	305 Hz	610 Hz	1.22 kHz	1.95 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61 Hz	153 Hz	305 Hz	610 Hz	976 Hz

(c) Timer mode registers

Address: F0192H, F0193H After reset: 0000H R/W Set value: 0000H

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMR01	CKS011	CKS010	0	CCS01	SPLIT01	STS012	STS011	STS010	CIS011	CIS010	0	0	MD013	MD012	MD011	MD010
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Address: F0196H, F0197H After reset: 0000H R/W Set value: 0000H

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMR03	CKS031	CKS030	0	CCS03	SPLIT03	STS032	STS031	STS030	CIS031	CIS030	0	0	MD033	MD032	MD031	MD030
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

CKS0n1	CKS0n0	Selection of operation clock (f_{MCK}) of channel n (n = 1, 3)
0	**0**	**Operation clock set by timer clock select register 0 (TPS0) (CK00)**
0	1	Operation clock set by timer clock select register 0 (TPS0) (CK01)
1	0	Operation clock set by timer clock select register 0 (TPS0) (CK02)
1	1	Operation clock set by timer clock select register 0 (TPS0) (CK03)

CCS0n	Selection of count clock (f_{TCLK}) of channel n (n = 1, 3)
0	**Operation clock specified by the CKS0n0 and CKS0n1 bits (f_{MCK})**
1	Valid edge of input signal input from the TI0n pin

SPLIT0n	Selection of 8 or 16-bit timer operation for channel n (n = 1, 3)
0	**Operate as a 16-bit timer. (Operate in independent channel operation mode or as a slave channel in simultaneous channel operation mode.)**
1	Operate as an 8-bit timer.

STS0n2	STS0n1	STS0n0	Setting of start trigger or capture trigger of channel n (n = 1, 3)
0	**0**	**0**	**Only software trigger start is valid (other trigger sources are unselected).**
0	0	1	The valid edge of the T0mn pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TI0n pin input are used as a start trigger and a capture trigger.
1	0	0	The interrupt signal of the master channel is used (when the channel is used as a slave channel in simultaneous channel operation mode).
Other than above			Setting prohibited

MD0n3	MD0n2	MD0n1	MD0n0	Operation mode of channel n (n = 1, 3)	Corresponding function	Count operation of TCR
0	**0**	**0**	**1/0**	**Interval timer mode**	**Interval timer/Square wave output/Divider function/PWM output (master)**	**Counting down**
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter/One-shot pulse output/PWM output (slave)	Counting down
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

Operation mode (Value set by the MD0n3 to MD0n1 bits) (n = 1, 3)	MD0n0	Setting of starting counting and interrupt
• **Interval timer mode (0, 0, 0)** • Capture mode (0, 1, 0)	**0**	**A timer interrupt is not generated when counting is started (the timer output does not change).**
	1	A timer interrupt is generated when counting is started (the timer output also changes).

(d) Timer data registers

Address: FFF1AH, FFF1BH After reset: 0000H R/W Set value: 7CFFH

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDR01																
Set value	**0**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Address: FFF66H, FFF67H After reset: 0000H R/W Set value: ****H

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDR03																
Set value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*

Remark: * = Change the setting by using software to use channel 3 of timer array unit 0 as an interval timer, and to set the interrupt interval to 1 ms or 1 μs.

(e) Timer channel start register 0 (TS0)

Address: F01B2H, F01B3H After reset: 0000H R/W Set value: 000AH

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS0	0	0	0	0	TSH03	0	TSH01	0	TS07	TS06	TS05	TS04	TS03	TS02	TS01	TS00
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**

TS0n	Operation enable (start) trigger of channel n (n = 1, 3)
0	No trigger operation
1	**The TE0n bit is set to 1 and the count operation is enabled.**

7.3.3 Functions

Table 7.2 Functions

Function Name	Overview
main	Main routine function
R5F10FMx_LDO_Enable	Analog block LDO initialization function
R5F10FMx_REG_SET_FORCE_SENSOR	Analog block initialization function
ADC_Get	A/D conversion result average value acquisition function
R_Systeminit	MCU initialization function
hdwinit	System initialization function
R_CGC_Create	Clock generator initialization function
R_PORT_Create	Port initialization function
R_SAU1_Create	SAU1 initialization function
R_CSI21_Create	CSI21 initialization function
R_CSI21_Start	CSI21 operation start function
R_CSI21_Stop	CSI21 operation stop function
R_CSI21_Send_Receive	CSI21 transmission/reception function
r_csi21_interrupt	INTCSI21 interrupt service function
r_csi21_callback_receiveend	CSI21 reception completion function
R5F10FMx_Send_Receive	Function for performing SPI communication with the analog block
R_ADC_Create	ADC initialization function
R_ADC_Start	ADC operation start function
R_ADC_Stop	ADC operation stop function
R_ADC_Set_OperationOn	ADC comparator operation enable function
R_ADC_Set_OperationOff	ADC comparator operation stop function
R_ADC_Get_Result	A/D conversion result read function
r_adc_interrupt	INTAD interrupt service function
ADC_Trigger_Start	ADC trigger operation start function
ADC_Trigger_Stop	ADC trigger operation stop function
ADC_Get_AD_Buffer_Value	A/D conversion result acquisition function
R_TAU0_Create	TAU0 initialization function
R_TAU0_Channel1_Start	TAU0 ch1 counter operation start function
R_TAU0_Channel1_Stop	TAU0 ch1 counter operation stop function
R_TAU0_Channel3_Start	TAU0 ch3 counter operation start function
R_TAU0_Channel3_Stop	TAU0 ch3 counter operation stop function
TAU0_Channel3_ChangeTimerCondition	TAU0 ch3 counter value change function
TAU0_WAIT_1ms	1-ms unit wait function
TAU0_WAIT_1us	1-µs unit wait function
write_lcd	LCD module write function
LCD_Init	LCD module initialization function
lcd_puts	Character string display function
LCD_Sensor_Out	LCD module measurement result display function
LCD_Err_Display	LCD module error display function

7.3.4 Function specifications

Declaration	`void main(void)`
Overview	`Main` routine function
Parameters	None
Return value	None
Description	• Calls the `R5F10FMx_LDO_Enable` function to initialize the variable output voltage regulator in the analog block. (LDO_OUT pin output = 3.3 V) • Calls the `R_ADC_Create` function to initialize the A/D converter. • Calls the `R_TAU0_Create` function to initialize timer array unit 0. • Calls the `LCD_Init` function to initialize the LCD module. • Calls the `R5F10FMx_REG_SET_FORCE_SENSOR` function to initialize the analog block. • Calls the `ADC_Trigger_Start` function to start the A/D converter trigger operation. • Calls the `ADC_Get` function to acquire the averaged value of 100 A/D conversion results. • Calls the `LCD_Sensor_Out` function to display the physical quantity (force) calculated from the A/D conversion result and the averaged value of the A/D conversion results on the LCD module.

Declaration	`static uint8_t R5F10FMx_LDO_Enable(void)`
Overview	Analog block LDO initialization function
Parameters	None
Return value	0: Successful 1: Communication with the analog block failed
Description	• Calls the `R5F10FMx_Send_Receive` function to initialize the variable output voltage regulator. - Sets the variable output voltage regulator voltage to 3.3 V and enables the variable output voltage regulator and the reference voltage generator.

Declaration	`static uint8_t R5F10FMx_REG_SET_FORCE_SENSOR(void)`
Overview	Analog block initialization function
Parameters	None
Return value	0: Successful 1: Communication with the analog block failed
Description	• Calls the `R5F10FMx_Send_Receive` function to initialize the functions in the analog block. - Configures configurable amplifier Ch1 (transimpedance amplifier) and configurable amplifier Ch3 (differential amplifier) as shown in this application note. - Sets the D/A converter channels Ch1 to Ch3 output voltage. - Enables D/A converter channels Ch1 to Ch3 and configurable amplifier channels Ch1 and Ch3.

Declaration	`static float ADC_Get(uint16_t ave_cnt)`
Overview	A/D conversion result average value acquisition function
Parameters	`uint16_t ave_cnt`: Number of A/D conversions over which to average the results
Return value	A/D conversion result average value
Description	Acquires the average of the results of A/D conversion performed the number of times specified by the parameter.

Declaration	`void R_Systeminit(void)`
Overview	MCU initialization function
Parameters	None
Return value	None
Description	• Initializes the peripheral hardware in the MCU used in this application note. - Calls the `R_PORT_Create` function to initialize the ports. - Calls the `R_CGC_Create` function to initialize the clock generator. - Calls the `R_SAU1_Create` function to initialize the 3-wire serial I/O (CSI21) of channel 1 in serial array unit 1.

Declaration	`void hdwinit(void)`
Overview	System initialization function
Parameters	None
Return value	None
Description	• Disables interrupts. • Calls the `R_Systeminit` function to initialize the MCU. • Enables interrupts.

Declaration	`void R_CGC_Create(void)`
Overview	Clock generator initialization function
Parameters	None
Return value	None
Description	Initializes the clock generator.

Declaration	`void R_PORT_Create(void)`
Overview	Port initialization function
Parameters	None
Return value	None
Description	Initializes the ports.

Declaration	`void R_SAU1_Create(void)`
Overview	SAU1 initialization function
Parameters	None
Return value	None
Description	Initializes serial array unit 1.

Declaration	`void R_CSI21_Create(void)`
Overview	CSI21 initialization function
Parameters	None
Return value	None
Description	Initializes the 3-wire serial I/O (CSI21) of channel 1 in serial array unit 1.

Declaration	`void R_CSI21_Start(void)`
Overview	CSI21 operation start function
Parameters	None
Return value	None
Description	• Clears the INTCSI21 interrupt flag. • Enables the INTCSI21 interrupt. • Starts CSI21 operation.

Declaration	`void R_CSI21_Stop(void)`
Overview	CSI21 operation stop function
Parameters	None
Return value	None
Description	• Stops CSI21 operation. • Disables the INTCSI21 interrupt. • Clears the INTCSI21 interrupt flag.

Declaration	`MD_STATUS R_CSI21_Send_Receive(uint8_t * const tx_buf, uint16_t tx_num, uint8_t * const rx_buf)`
Overview	CSI21 transmission/reception function
Parameters	`uint8_t * const tx_buf`: Address of transmission buffer `uint16_t tx_num`: Number of transmitted bytes `uint8_t * const rx_buf`: Address of reception buffer
Return value	`MD_STATUS`: Reception status `MD_OK` (0000H): Successful `MD_ARGERROR` (0081H): Argument input error
Description	Controls transmission and reception via CSI21.

Declaration	`__interrupt static void r_csi21_interrupt(void)`
Overview	INTCSI21 interrupt service function
Parameters	None
Return value	None
Description	Services the CSI21 buffer empty interrupt or reception completion interrupt.

Declaration	`static void r_csi21_callback_receiveend(void)`
Overview	CSI21 reception completion function
Parameters	None
Return value	None
Description	• Controls the operation when CSI21 reception ends. - Outputs a high level from the P73 pin. - Calls the `R_CSI21_Stop` function to stop CSI21 operation.

Declaration	`uint8_t R5F10FMx_Send_Receive(uint8_t *p_read_data, uint8_t addr, uint8_t txdata, uint8_t command)`
Overview	Function for performing SPI communication with the analog block
Parameters	`uint8_t *p_read_data`: Address at which to store the read data `uint8_t addr`: Address of the SPI control register `uint8_t txdata`: Data to transmit `uint8_t command`: Variable to specify read or write 0: Read 1: Write
Return value	0: Successful 1: Communication with the analog block timed out or the analog block is in the reset state.
Description	• Reads the status of the reset pin in the analog block and, if the pin is being reset, returns 1 and ends processing. • Calls the `R_CSI21_Start` function to start CSI21 operation. • Sets the data to be read or written. If the parameter `command` is set to 0 or a value other than 1, returns 1 and ends processing. • Outputs a low level from the P73 pin. • Calls the `R_CSI21_Send_Receive` function to transmit or receive data. • Stores the received data in `*p_read_data`. • Returns 0 if execution finishes successfully and ends processing.

Declaration	`void R_ADC_Create(void)`
Overview	ADC initialization function
Parameters	None
Return value	None
Description	Initializes the A/D converter.

Declaration	`void R_ADC_Start(void)`
Overview	ADC operation start function
Parameters	None
Return value	None
Description	• Clears the INTAD interrupt flag. • Enables the INTAD interrupt. • Enables operation of the D/A converter.

Declaration	`void R_ADC_Stop(void)`
Overview	ADC operation stop function
Parameters	None
Return value	None
Description	• Stops operation of the D/A converter. • Disables the INTAD interrupt. • Clears the INTAD interrupt flag.

Declaration	`void R_ADC_Set_OperationOn(void)`
Overview	ADC comparator operation enable function
Parameters	None
Return value	None
Description	Enables operation of the A/D voltage comparator.

Declaration	`void R_ADC_Set_OperationOff(void)`
Overview	ADC comparator operation stop function
Parameters	None
Return value	None
Description	Stops operation of the A/D voltage comparator.

Declaration	`void R_ADC_Get_Result(uint16_t * const buffer)`
Overview	A/D conversion result read function
Parameters	`uint16_t * const buffer`: Address at which to store the A/D conversion results
Return value	None
Description	Reads the ADCR value and stores it in `* const buffer`.

Declaration	`__interrupt static void r_adc_interrupt(void)`
Overview	INTAD interrupt service function
Parameters	None
Return value	None
Description	Reads the A/D conversion result from the 12-bit A/D conversion result register (ADCR) and stores it in `_ad_buffer`.

Declaration	`void ADC_Trigger_Start(void)`
Overview	ADC trigger operation start function
Parameters	None
Return value	None
Description	• Calls the `R_ADC_Start` function to start operation of the A/D converter. • Calls the `R_TAU0_Channel1_Start` function to start operation of channel 1 in timer array unit 0.

Declaration	`void ADC_Trigger_Stop(void)`
Overview	ADC trigger operation stop function
Parameters	None
Return value	None
Description	• Calls the `R_ADC_Stop` function to stop operation of the A/D converter. • Calls the `R_TAU0_Channel1_Stop` function to stop operation of channel 1 in timer array unit 0.

Declaration	`void ADC_Get_AD_Buffer_Value(uint16_t *dest)`
Overview	A/D conversion result acquisition function
Parameters	`uint16_t *dest`: Address at which to store the A/D conversion results read from the ADCR register.
Return value	None
Description	Reads the A/D conversion results stored in the internal RAM.

Declaration	`void R_TAU0_Create(void)`
Overview	TAU0 initialization function
Parameters	None
Return value	None
Description	Initializes timer array unit 0.

Declaration	`void R_TAU0_Channel1_Start(void)`
Overview	TAU0 ch1 counter operation start function
Parameters	None
Return value	None
Description	Starts counting using channel 1 in timer array unit 0.

Declaration	`void R_TAU0_Channel1_Stop(void)`
Overview	TAU0 ch1 counter operation stop function
Parameters	None
Return value	None
Description	Stops counting using channel 1 in timer array unit 0.

Declaration	`void R_TAU0_Channel3_Start(void)`
Overview	TAU0 ch3 counter operation start function
Parameters	None
Return value	None
Description	Starts counting using channel 3 in timer array unit 0.

Declaration	`void R_TAU0_Channel3_Stop(void)`
Overview	TAU0 ch3 counter operation stop function
Parameters	None
Return value	None
Description	Stops counting using channel 3 in timer array unit 0.

Declaration	`void TAU0_Channel3_ChangeTimerCondition(uint16_t regvalue)`
Overview	TAU0 ch3 counter value change function
Parameters	`uint16_t regvalue`: Counter value set to TDR03
Return value	None
Description	Sets the value of the `regvalue` parameter to TDR03.

Declaration	`void TAU0_WAIT_1ms(uint32_t wait_1ms)`
Overview	1-ms unit wait function
Parameters	`uint32_t wait_1ms`: 1-ms counter
Return value	None
Description	• Calls the `R_TAU0_Channel3_Stop` function to stop counting using channel 3 in timer array unit 0. • Calls the `TAU0_Channel3_ChangeTimerCondition` function to set the interval of channel 3 in timer array unit 0 to 1 ms. • Calls the `R_TAU0_Channel3_Start` function to start counting using channel 3 in timer array unit 0. • Decrements the value of the `wait_1ms` parameter for the interval of channel 3 in timer array unit 0 (1 ms) until the value becomes 0.

Declaration	`void TAU0_WAIT_1us(uint32_t wait_1us)`
Overview	1-µs unit wait function
Parameters	`uint32_t wait_1us`: 1-us counter
Return value	None
Description	• Calls the `R_TAU0_Channel3_Stop` function to stop counting using channel 3 in timer array unit 0. • Calls the `TAU0_Channel3_ChangeTimerCondition` function to set the interval of channel 3 in timer array unit 0 to 1 µs. • Calls the `R_TAU0_Channel3_Start` function to start counting using channel 3 in timer array unit 0. • Decrements the value of the `wait_1us` parameter for the interval of channel 3 in timer array unit 0 (1 µs) until the value becomes 0.

Declaration	`void write_lcd(uint8_t data, uint8_t rs)`
Overview	LCD module write function
Parameters	`uint8_t data`: Data to be written to the LCD module `uint8_t rs`: LCD write mode (0: Command, 1: Data)
Return value	None
Description	Divides the data to be written to the LCD module, which is specified by the `uint8_t data` parameter, into the upper 4 bits and lower 4 bits and writes the data to the LCD module in the mode specified by the `uint8_t rs` parameter.

Declaration	`void LCD_Init(void)`
Overview	LCD module initialization function
Parameters	None
Return value	None
Description	Initializes the LCD module (in 4-bit interface mode)

Declaration	`void lcd_puts(int8_t *str)`
Overview	Character string display function
Parameters	`int8_t *str`: Address of the array in which to store the character string to be displayed on the LCD
Return value	None
Description	Displays the character string stored in the array on the LCD module.

Declaration	`void LCD_Sensor_Out(float result, int8_t *Unit, float adc_result)`
Overview	LCD module measurement result display function
Parameters	`float result`: Calculated physical quantity `int8_t *Unit`: Unit of calculated physical quantity `float adc_result`: A/D conversion result average value
Return value	None
Description	• Calls the LCD module write function to write the data to display on the LCD module. • Displays *XXX.X*[*Y*] on the first line of the LCD. *XXX.X* indicates the calculated physical quantity, and *Y* indicates the unit (g). • Displays ADC:*ZZZ*H on the second line of the LCD. *ZZZ* indicates the A/D conversion result average value in hex.

Declaration	`void LCD_Err_Display(void)`
Overview	LCD module error display function
Parameters	None
Return value	None
Description	• Displays an error message on the LCD module if an SPI communication error occurs when the analog block initialization function is being called. • Displays “PLEASE RESET” on the LCD module.

7.3.5 RAM variables

Table 7.3 RAM Variables

Data Type	Variable Name	Description	Function Used
volatile uint8_t *	gp_csi21_rx_address	Address of CSI21 reception buffer	R_CSI21_Send_Receive r_csi21_interrupt
volatile uint16_t	g_csi21_rx_length	Number of bytes received at CSI21	Not used
volatile uint16_t	g_csi21_rx_count	CSI21 received byte counter	Not used
volatile uint8_t *	gp_csi21_tx_address	Address of CSI21 transmission buffer	R_CSI21_Send_Recieve r_csi21_interrupt
volatile uint16_t	g_csi21_send_length	Number of bytes transmitted from CSI21	R_CSI21_Send_Receive r_csi21_interrupt
volatile uint16_t	g_csi21_tx_count	CSI21 transmitted byte counter	R_CSI21_Send_Receive r_csi21_interrupt
static uint16_t	_ad_buffer	Stores the A/D conversion result.	r_adc_interrupt ADC_Get_AD_Buffer_Value

7.3.6 Flowcharts

Figure 7.12 shows an overview of the processing flow used in this application note. Flowcharts for the major functions are shown in the subsequent figures.

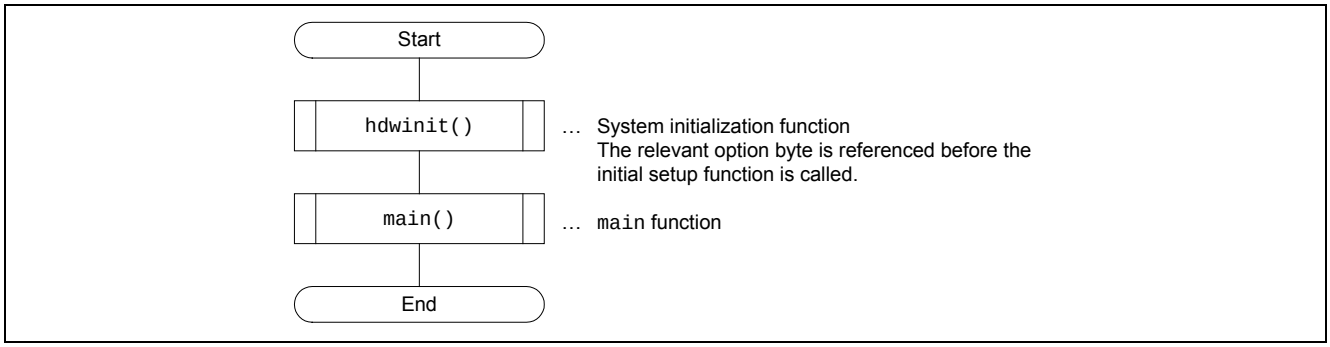


Figure 7.12 Overview of Processing Flow

(1) System initialization function (hdwinit)

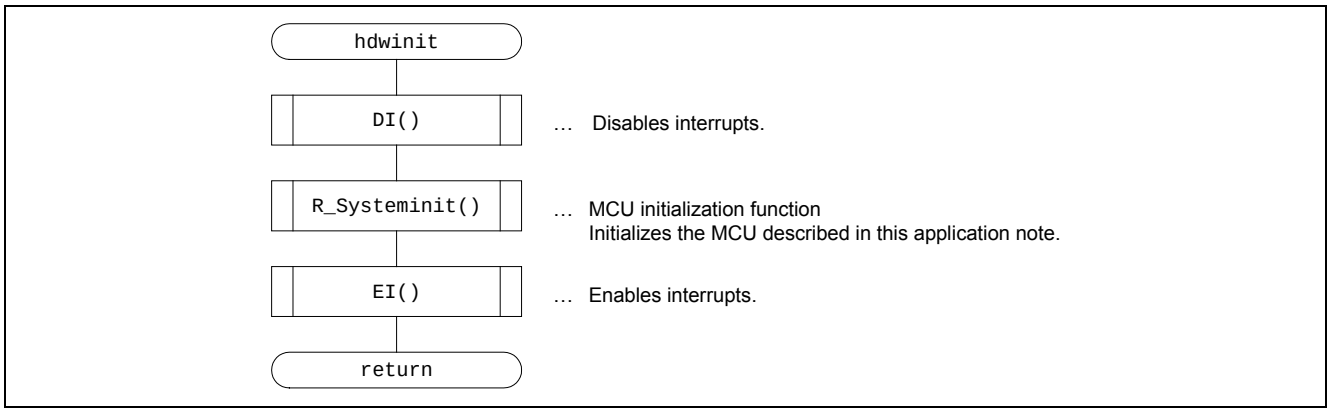


Figure 7.13 Flowchart of hdwinit Function

(2) MCU initialization function (R_Systeminit)

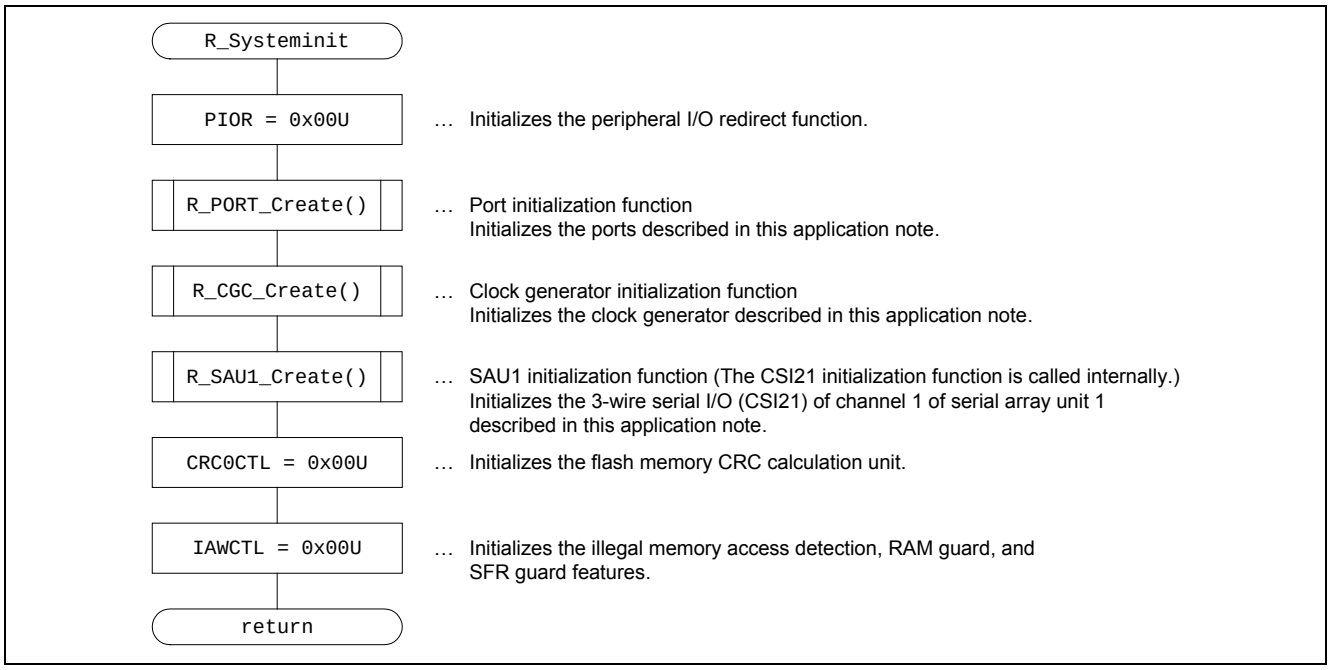


Figure 7.14 Flowchart of R_Systeminit Function

(3) `main` function (`main`)

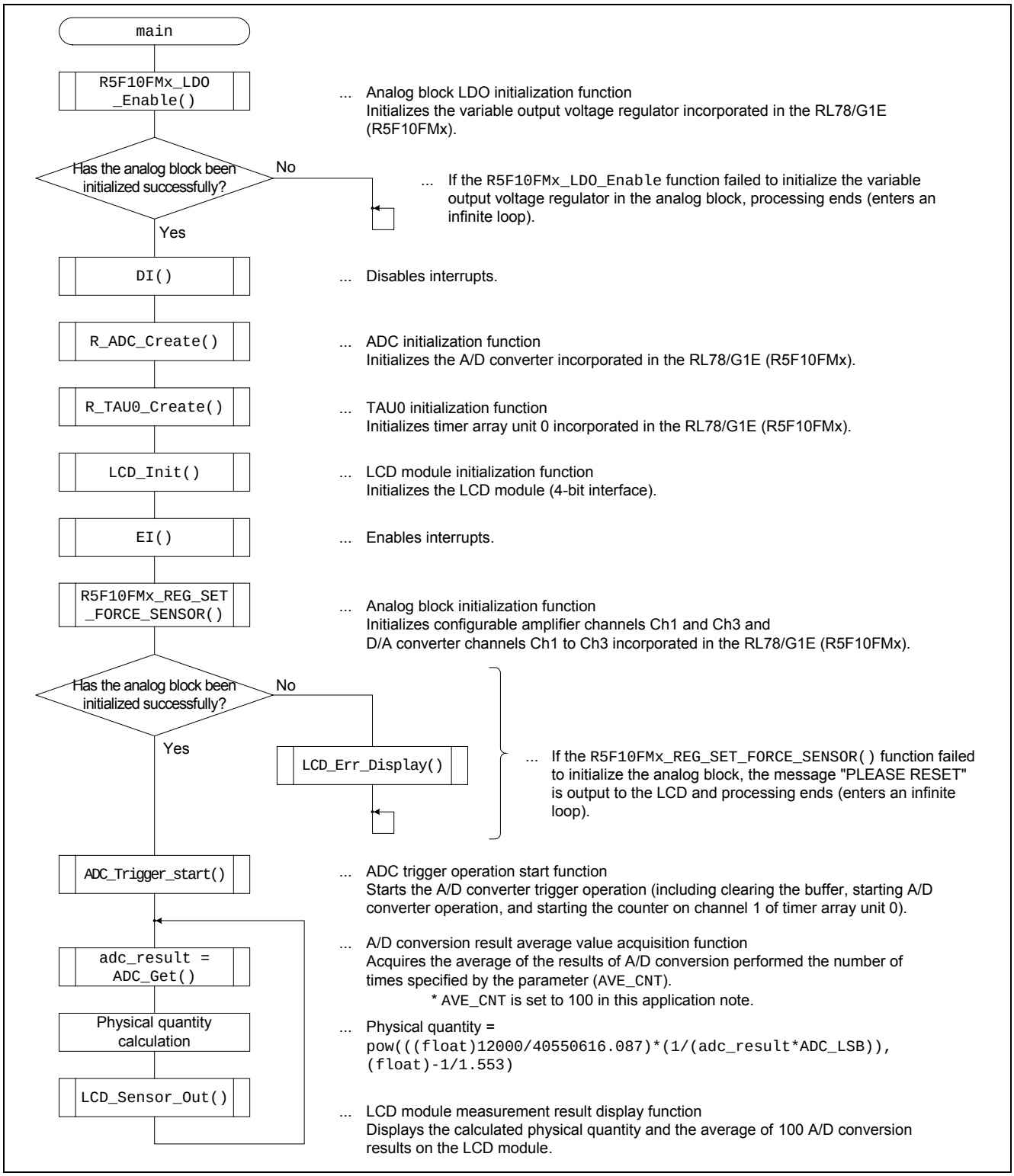


Figure 7.15 Flowchart of `main` Function

(4) Analog block LDO initialization function (R5F10FMx_LDO_Enable)

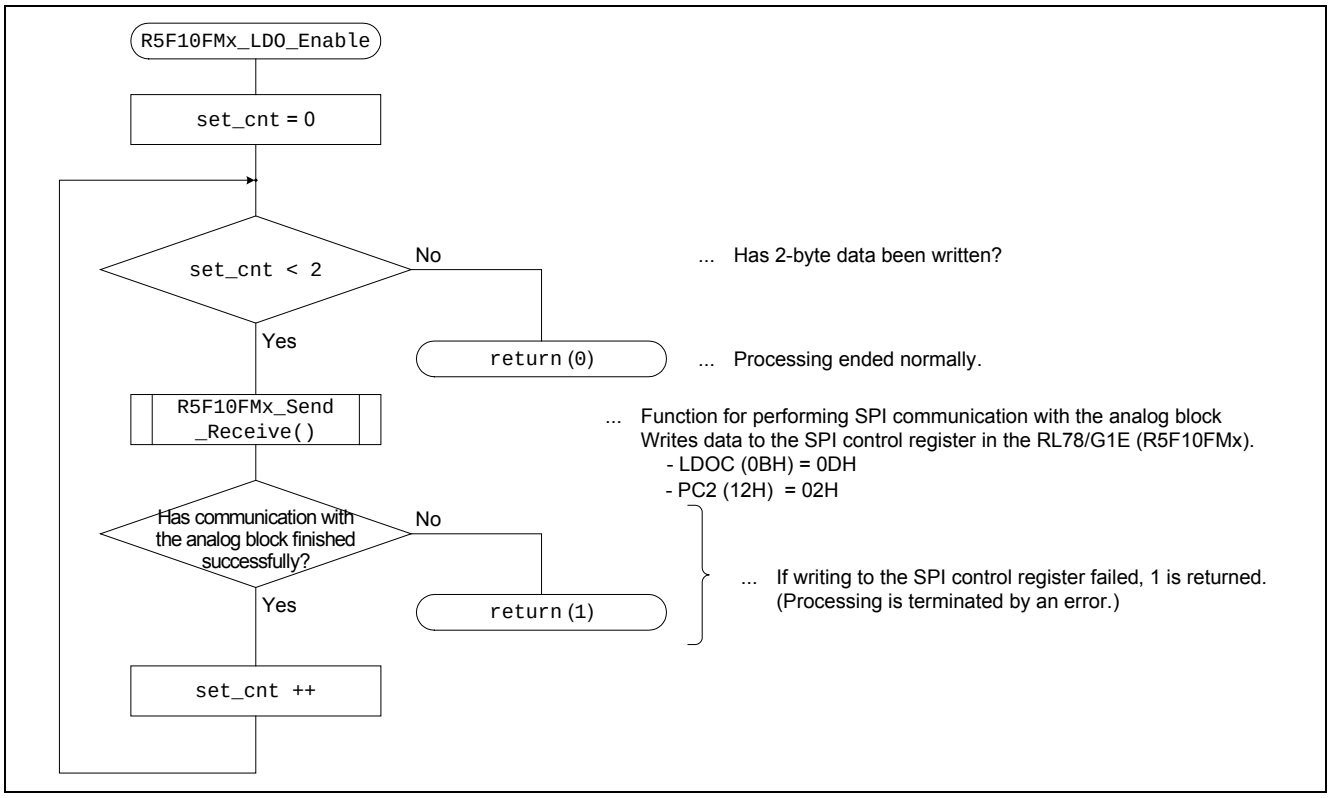


Figure 7.16 Flowchart of R5F10FMx_LDO_Enable Function

(5) Analog block initialization function (R5F10FMx_REG_SET_FORCE_SENSOR)

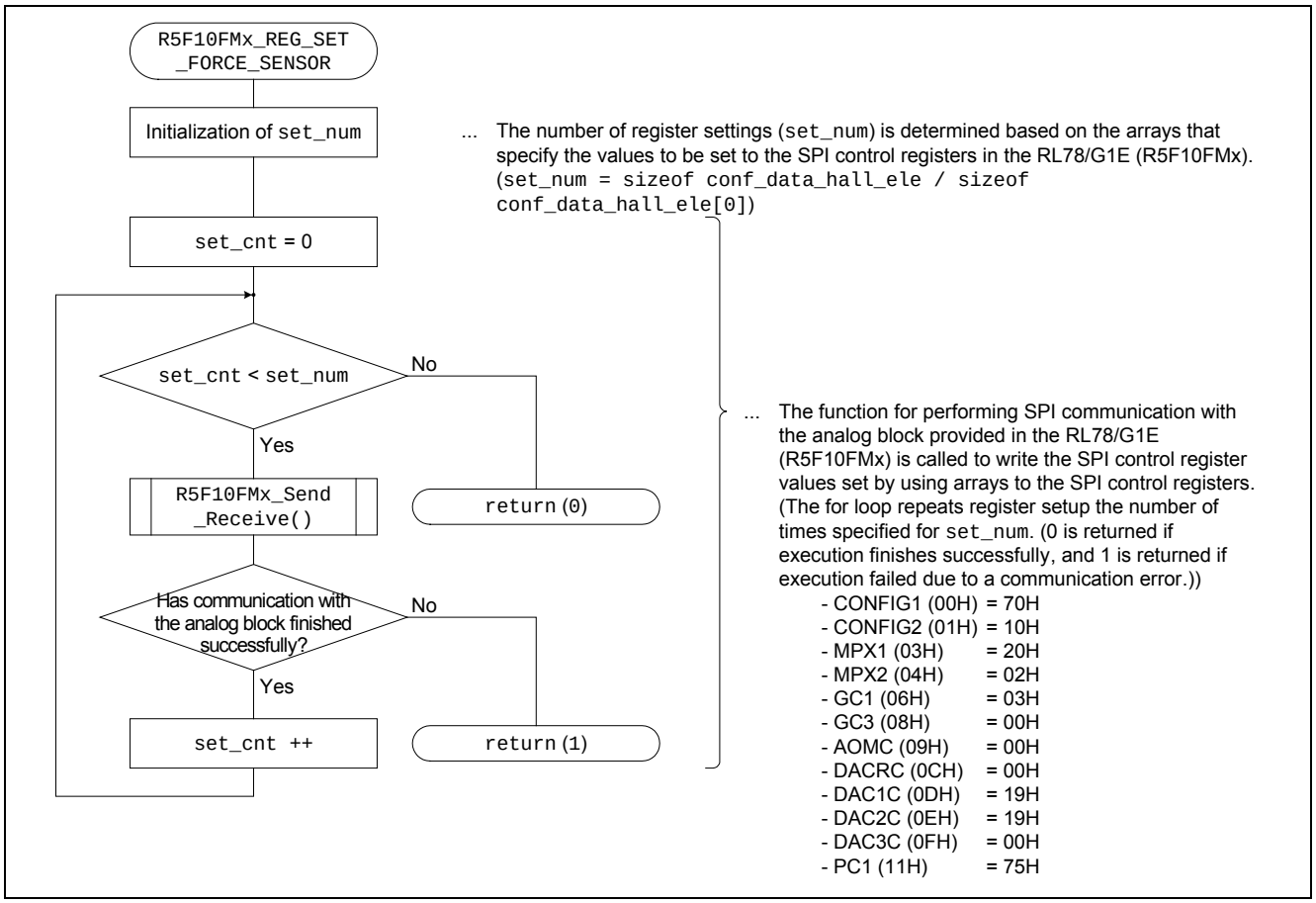


Figure 7.17 Flowchart of R5F10FMx_REG_SET_FORCE_SENSOR Function

(6) Function that performs SPI communication with analog block (R5F10FMx_Send_Receive)

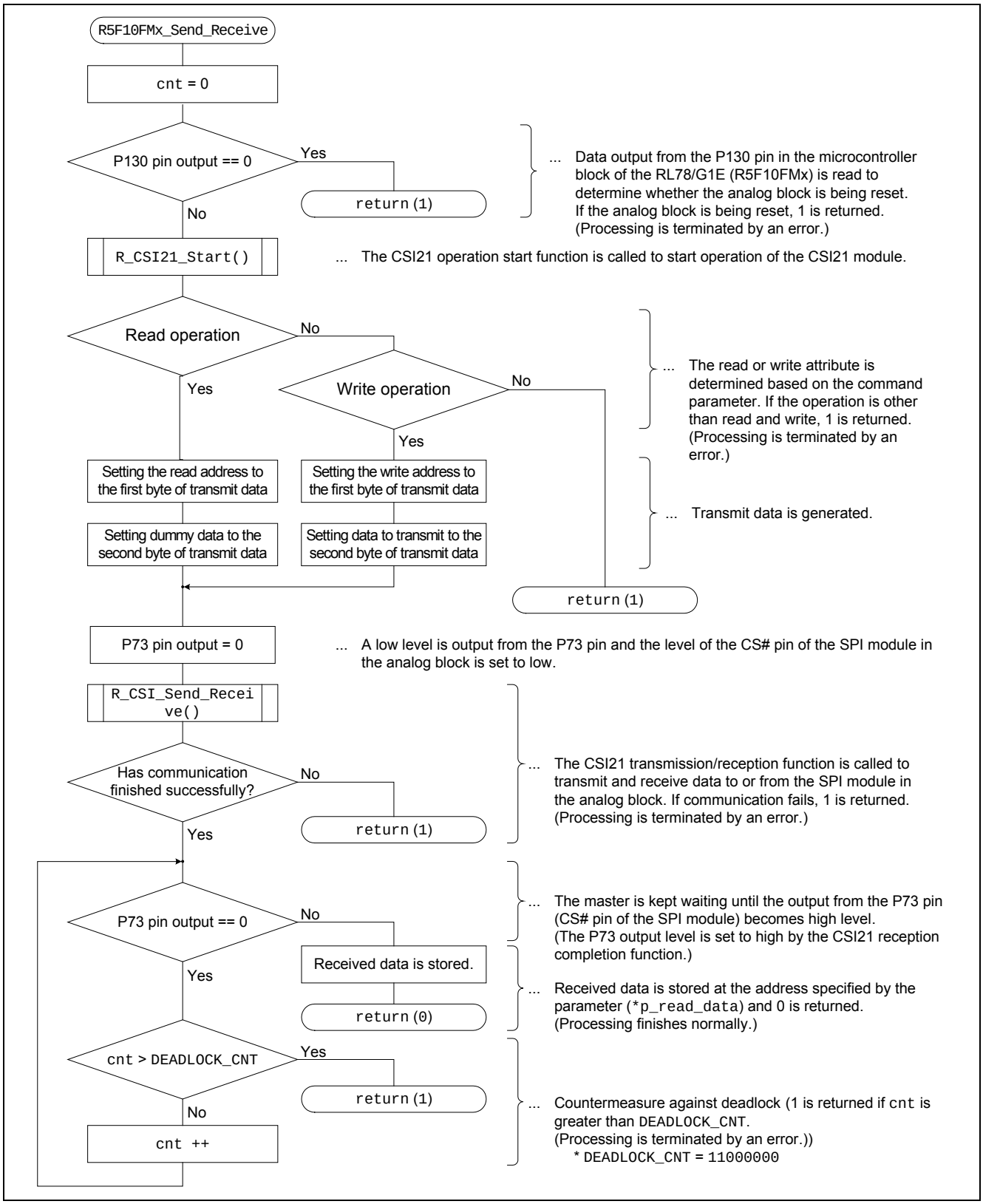


Figure 7.18 Flowchart of R5F10FMx_Send_Receive Function

(7) A/D conversion result average value acquisition function (ADC_Get)

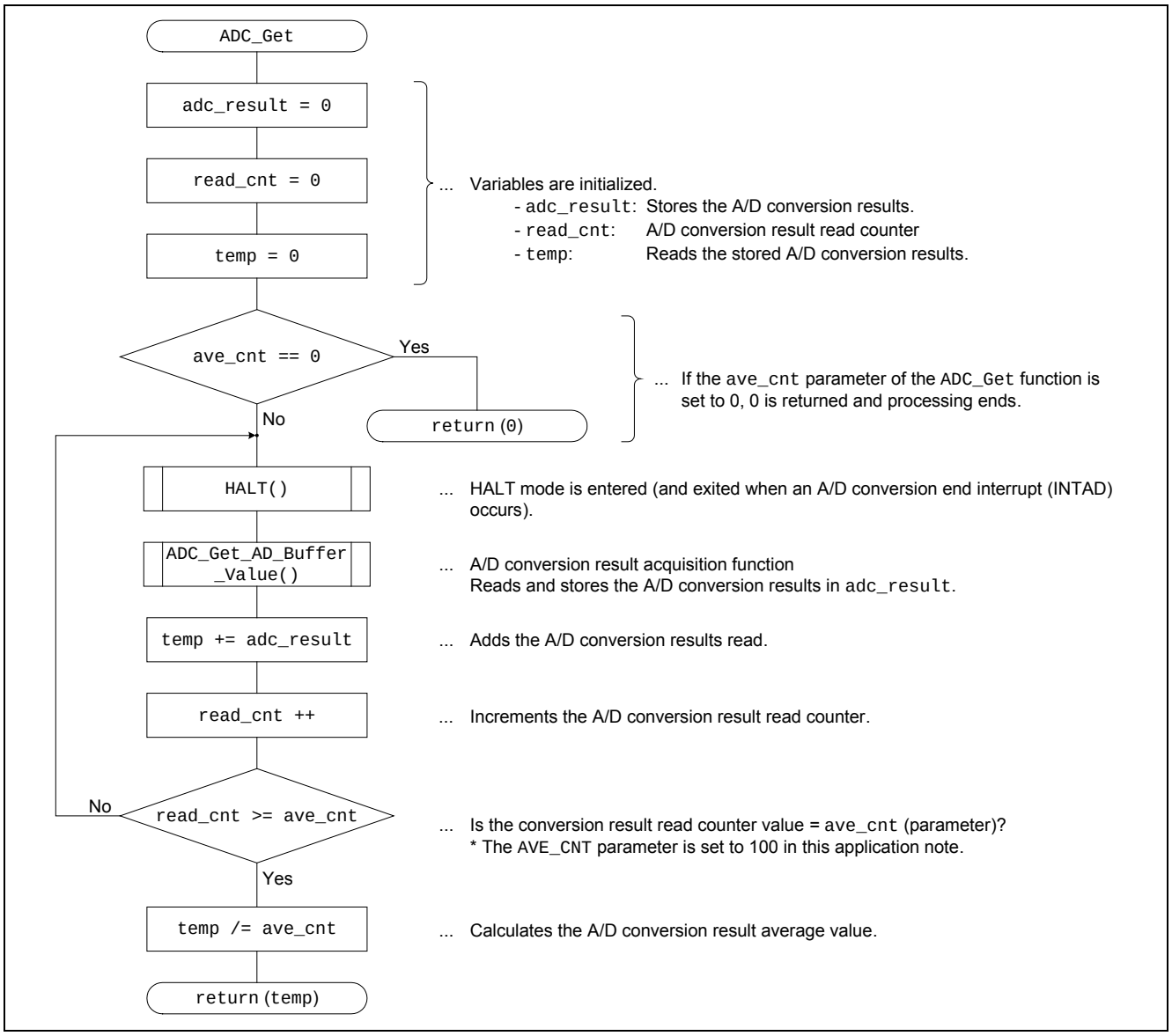


Figure 7.19 Flowchart of ADC_Get Function

(8) CSI21 reception completion function (`r_csi21_callback_receiveend`)

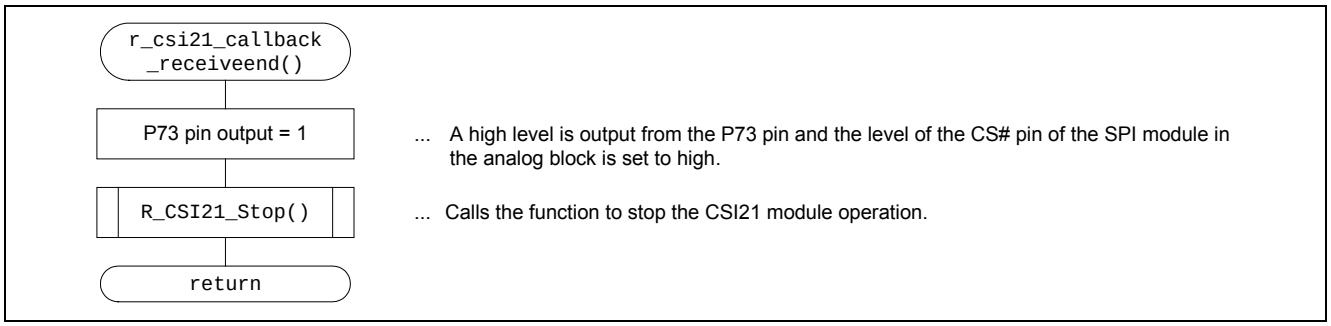


Figure 7.20 Flowchart of `r_csi21_callback_receiveend` Function

7.3.7 Source files and changes applied to the code output from the code generator

The sample code used in this application note was created based on the code for the RL78/G1A group (R5F10ELE) output by the code generator of CubeSuite+.

The output file has been modified to apply the differences between the RL78/G1A (R5F10ELE) and RL78/G1E (R5F10FME) such as incorporated registers. **Table 7.4** shows the changes applied to the code output by the code generator. For details about the differences between the RL78/G1A (R5F10ELE) and RL78/G1E (R5F10FME), see the *RL78/G1E Hardware User's Manual*.

Table 7.4 Source Files and Changes Applied to the Code Output from the Code Generator (1/2)

File Name	Description	Changes Applied to the Code Output by the Code Generator	
		Item	Description
r_main.c	Output by the code generator	–	–
r_systeminit.c	Output by the code generator	R_systeminit function	• Commented out R_ADC_Create();. • Commented out R_TAU0_Create();.
r_cg_cgc.c	Output by the code generator	R_CGC_Create function	• Changed the value set to CMC = ...;. • Commented out XSTOP = ...;. • Commented out CSS = ...;.
r_cg_cgc_user.c	Output by the code generator	–	–
r_cg_port.c	Output by the code generator	R_PORT_Create function	• Commented out P6 = ...;. • Commented out P12 = ...;. • Commented out P15 = ...;. • Commented out PMC4 = ...;. • Changed the value set to ADPC = ...;.
r_cg_port_user.c	Output by the code generator	–	–
r_cg_serial.c	Output by the code generator	R_CSI21_Create function	• Commented out SO1 |= ...;. • Commented out SO1 &= ...;.
r_cg_serial_user.c	Output by the code generator	r_csi21_callback _receiveend function	• Added processing.
r_cg_adc.c	Output by the code generator	R_ADC_Create function	• Commented out PM2 |= ...;. • Commented out PM15 |= ...;. • Commented out PM12 |= ...;. • Commented out PMC3 |= ...;. • Commented out PM3 |= ...;.
r_cg_adc_user.c	Output by the code generator	r_adc_interrupt function	• Added processing.
r_cg_timer.c	Output by the code generator	R_TAU0_Create function	• Commented out TOM0 &= ...;. • Commented out TOL0 &= ...;. • Commented out TO0 &= ...;. • Commented out TOE0 &= ...;.
r_cg_timer_user.c	Output by the code generator	–	–
r_cg_macrodriver.h	Output by the code generator	–	–

Table 7.5 Source Files and Changes Applied to the Code Output from the Code Generator (2/2)

File Name	Description	Changes Applied to the Code Output by the Code Generator	
		Item	Description
r_cg_userdefine.h	Output by the code generator	–	• Added the typedef and define statements.
r_cg_cgc.h	Output by the code generator	–	• Added the extern statement.
r_cg_port.h	Output by the code generator	–	• Added the extern statement.
r_cg_serial.h	Output by the code generator	–	• Added the extern statement.
r_cg_adc.h	Output by the code generator	–	• Added the extern statement.
r_cg_timer.h	Output by the code generator	–	• Added the extern statement.
lcd.c	LCD module control	–	–
lcd.h	Header file for lcd.c	–	–

Website and Support

Renesas Electronics Website
http://www.renesas.com/

Inquires
http://www.renesas.com/contact/

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Sep. 30, 2012	—	First edition issued.
1.10	Sep. 30, 2013	—	Some description are modified.

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   - Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   - The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   - The state of the product is undefined at the moment when power is supplied.
   - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
     In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
     In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   - Access to reserved addresses is prohibited.
   - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   - After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   - Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
   - The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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