RL78/G14, R8C/36M Group

Migration Guide from R8C to RL78: Watchdog Timer

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Abstract

This document describes how to migrate from the R8C/36M Group watchdog timer to the RL78/G14 watchdog timer.

Products

RL78/G14, R8C/36M Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Differences between the R8C/36M Group and RL78/G14

Table 1.1 lists the differences between R8C/36M Group watchdog timer and RL78/G14 watchdog timer.

Table 1.1 Differences in the Watchdog Timer

Item	R8C/36M Group		RL78/G14
	Count Source Protection Mode Disabled	Count Source Protection Mode Enabled	
Count source	CPU clock	Low-speed on-chip oscillator clock for the watchdog timer	Low-speed oscillator clock
Count operation	Decrement		Increment
Count start condition	Set the WDTON bit in the OFS register: • When the WDTON bit is 1, the watchdog timer is stopped (count starts by writing to the WDTS register after a reset) • When the WDTON bit is 0, the watchdog timer is automatically started		Set the WDTON bit in the user option byte (000C0H) • When the WDTON bit is 1, counting starts after a reset • When the WDTON bit is 0, the watchdog timer is stopped
Count stop condition	Stop mode, wait mode	None	HALT mode, STOP mode, SNOOZE mode (1)
Underflow/overflow period setting	Yes (2)		Yes (2)
Operations at underflow/overflow	Interrupt or reset (3)	Reset	Reset
Interrupts	Yes (watchdog timer)	No	Yes (interval interrupt)
Watchdog timer refresh acknowledgment period setting	Yes (set the refresh acknowledgment period)		Yes (set the window open period)
Condition to generate reset or interrupt	• At underflow • When the refresh operation is executed other than the refresh acknowledgment period		• At overflow • When 1-bit manipulation instruction is executed to the WDTE register • When the data other than "ACH" is written to the WDTE register • When data is written to the WDTE register during a window close period
Watchdog timer counter read	Yes		No

Notes 1. The count stop condition varies depending on the setting of the WDSTBYON bit in the user option byte (000C0H).
2. Refer to section 3.2 Setting the Underflow Period and Overflow for the specifiable period.
3. An interrupt or a reset can be specified by setting the PM12 bit in the PM1 register.

2. Register Compatibility

Register compatibility between the R8C/36M Group and the RL78/G14 is listed in Table 2.1.

Table 2.1 Register Compatibility

Item	R8C/36M Group	RL78/G14
Switch between interrupt and reset	• PM1 register PM12 bit	N/A
Watchdog timer refresh	• WDTR register	• WDTE register
Watchdog timer start	• WDTS register	N/A
Prescaler	• WDTC register WDTC7 bit	N/A
Operating mode	• CSPR register CSPRO bit	N/A
Watchdog timer start select	• OFS register WDTON bit	• User option byte (000C0H) Bits WDTON and WDSTBYON
Count source protection mode after a reset	• OFS register CSPROINI bit	N/A
Count stop condition	• OFS register CSPROINI bit	• User option byte (000C0H) WDSTBYON bit
Underflow or overflow period	• OFS2 register Bits WDTUFS1 and WDTUFS0	• User option byte (000C0H) Bits WDCS2 to WDCS0
Watchdog timer refresh acknowledgment period	• OFS2 register Bits WDTRCS1 and WDTRCS0	• User option byte (000C0H) Bits WINDOW1 and WINDOW0
Read the underflow or overflow period value	• WDTC register Bits 6 to 0	N/A
Detect an internal reset request	• RSTFR register WDR bit	• RESF register WDTRF bit
Interval interrupt	N/A	• User option byte (000C0H) WDTINT bit
Interrupt mask flag	N/A	• MK0L register WDTIMK bit
Interrupt request flag	N/A	• IF0L register WDTIIF bit
Maskable interrupt priority level	N/A	• PR00L register WDTIPR0 bit • PR10L register WDTIPR1 bit

3. Comparison of the Watchdog Timer Operation Setting

3.1 Setting the Watchdog Timer

3.1.1 R8C/36M Group

Set the WDTON bit in the OFS register to start or stop the watchdog timer after a reset.

When the WDTON bit is 0, the watchdog timer and the prescaler automatically start counting after a reset.

The watchdog timer and the prescaler are stopped after a reset when the WDTON bit is 1, and they start counting by writing to the WDTS register. Table 3.1 lists the functions of the WDTON bit.

Table 3.1 WDTON Bit in Functions

WDTON Bit	Function
0	Watchdog timer automatically starts after reset
1	Watchdog timer is stopped after reset

Count source protection mode can be disabled or enabled by setting the CSPROINI bit in the OFS register. Table 3.2 lists the functions of the CSPROINI bit.

Table 3.2 CSPROINI Bit Functions

CSPROINI Bit	Function
0	Count source protect mode enabled after reset
1	Count source protect mode disabled after reset

3.1.2 RL78/G14

Set the WDTON bit in the user option byte (000C0H) to select the watchdog timer operation after a reset. Table 3.3 lists the functions of the WDTON bit.

Table 3.3 WDTON Bit Functions

WDTON Bit	Function
0	Counter operation disabled (counting stopped after reset)
1	Counter operation enabled (counting started after reset)

Set the WDSTBYON bit in the user option byte (000C0H) to select the watchdog timer operation in HALT, STOP or SNOOZE mode. Table 3.4 lists the functions of the WDSTBYON bit.

Table 3.4 WDSTBYON Bit Functions

	WDSTBYON = 0	WDSTBYON = 1
In HALT mode	Watchdog timer operation stops	Watchdog timer operation continues
In STOP mode		
In SNOOZE mode		

3.2 Setting the Underflow Period and Overflow Time

3.2.1 R8C/36M Group

The formula to calculate the underflow period differs when the count source protection mode is disabled and enabled. Use the following formulae to calculate the underflow period.

- When the count source protection mode is disabled:
  (Division ratio of prescaler × count value of watchdog timer) ÷ CPU clock

- When the count source protection mode is enabled:
  (Count value of watchdog timer) ÷ (Low-speed on-chip oscillator clock for the watchdog timer)

(1) When the count source protection mode is disabled

When the count source protection mode is disabled, the CPU clock is selected as the count source. Also, the division ratio of the prescaler must be set by the WDTC7 bit in the WDTC register. The division ratio of the prescaler is set to 2 when the low-speed clock is specified.

Table 3.5 lists the functions of the WDTC7 bit.

Table 3.5 WDTC7 Bit Functions

WDTC7 Bit	Function
0	Divided-by-16
1	Divided-by-128

Set bits WDTUFS0 and WDTUFS1 in the OFS2 register to specify the count value.

Table 3.6 lists the functions of bits WDTUFS1 and WDTUFS0.

Table 3.6 Values of Bits WDTUFS1 and WDTUFS0

WDTUFS1	WDTUFS0	Value
0	0	03FFh
0	1	0FFFh
1	0	1FFFh
1	1	3FFFh

(2) When the count source protection mode is enabled

Use the low-speed on-chip oscillator clock for the watchdog timer as the count source when the count source protection mode is enabled. Set bits WDTUFS0 and WDTUFS1 to specify the count value. Refer to Table 3.6 for details on setting the count value.

3.2.2 RL78/G14

Set bits WDCS0 to WDCS2 in the user option byte (000C0H) to select the overflow time.

Table 3.7 lists the selectable overflow time by setting bits WDCS0 to WDCS2.

Table 3.7 Selectable Overflow Time by Setting Bits WDCS2 to WDCS0

WDCS2	WDCS1	WDCS0	Watchdog Timer Overflow Time (f_{IL} = maximum of 17.25 kHz)
0	0	0	$2^6/f_{IL}$ (3.71 ms)
0	0	1	$2^7/f_{IL}$ (7.42 ms)
0	1	0	$2^8/f_{IL}$ (14.84 ms)
0	1	1	$2^9/f_{IL}$ (29.68 ms)
1	0	0	$2^{11}/f_{IL}$ (118.72 ms)
1	0	1	$2^{13}/f_{IL}$ (474.90 ms)
1	1	0	$2^{14}/f_{IL}$ (949.80 ms)
1	1	1	$2^{16}/f_{IL}$ (3799.19 ms)

Remark: f_{IL}: Low-speed on-chip oscillator clock frequency

3.3 Setting the Watchdog Timer Refresh Acknowledgment Period

3.3.1 R8C/36M Group

Set bits WDTRCS1 and WDTRCS0 to select the watchdog timer refresh acknowledgment period.

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, a refresh operation executed during the refresh acknowledgment period for the watchdog timer is acknowledged. Any refresh operation executed during the period other than the above is processed as an incorrect write, and a watchdog timer interrupt or watchdog timer reset is generated.

Table 3.8 lists the values when setting bits WDTRCS1 and WDTRCS0.

Table 3.8 Values When Setting Bits WDTRCS1 and WDTRCS0

WDTRCS1	WDTRCS0	Watchdog Timer Refresh Acknowledgment Period
0	0	25%
0	1	50%
1	0	75%
1	1	100%

3.3.2 RL78/G14

Set bits WINDOW1 and WINDOW0 to select the watchdog timer window open period.

When “ACH” is written to the WDTE register during the window open period, the watchdog timer is cleared and starts counting again.

Even if “ACH” is written to the WDTE register during the window close period, an anomaly is detected and an internal reset signal is generated.

When data is written to the WDTE register for the first time after a reset is released, the watchdog timer can be cleared at any point regardless of the window open time, as long as the register is written before the overflow time. Then the watchdog timer starts counting again.

Table 3.9 lists the values when setting bits WINDOW1 and WINDOW0.

Table 3.9 Values When Setting Bits WINDOW1 and WINDOW0 in the User Option Byte

WINDOW1	WINDOW0	Watchdog Timer Window Open Period
0	0	Setting prohibited
0	1	50%
1	0	75%
1	1	100%

Figure 3.1 shows an example of the watchdog timer when the window open period is 50%.

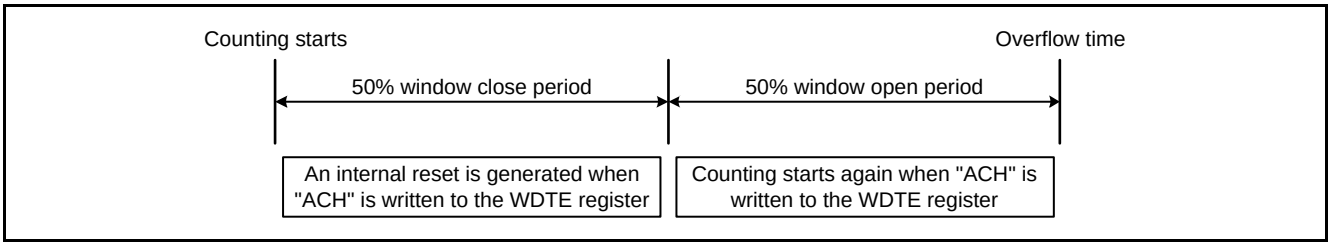

Figure 3.1 Watchdog Timer When the Window Open Period is 50%

3.4 Interval Interrupt

3.4.1 R8C/36M Group

Set the PM12 in the PM1 register to generate a watchdog timer interrupt when the count source protection mode is disabled. Table 3.10 lists the functions of the PM12 bit.

Table 3.10 PM12 Bit Functions

PM12 Bit	Function
0	Watchdog timer interrupt
1	Watchdog timer reset

3.4.2 RL78/G14

Set the WDTINT bit to generate an interval interrupt (INTWDTI) when the watchdog timer reaches 75% of the overflow time. Do not clear the watchdog timer during interrupt handling.

Table 3.11 lists the functions of the WDTINT bit.

Table 3.11 WDTINT Bit Functions

WDTINT	Use of Watchdog Timer Interval Interrupt
0	Interval interrupt is not used
1	Interval interrupt is generated when 75% of the overflow time is reached

4. Terms

Table 4.1 lists the comparison of terms between the R8C/36M Group and the RL78/G14.

Table 4.1 Comparison of Terms between the R8C/36M Group and the RL78/G14

R8C/36M Group	RL78/G14
Refresh acknowledgment period	Window open period

5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

User's Manual: Hardware

RL78/G14 User's Manual: Hardware Rev.1.00

R8C/36M Group User's Manual: Hardware Rev.1.01

The latest versions can be downloaded from the Renesas Electronics website.

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

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Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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