RL78/G13

Timer Array Unit (Pulse Interval Measurement)

R01AN0458EJ0200
Rev. 2.00
Dec. 27, 2013

Introduction

This application note describes how the timer array unit (TAU) measures time intervals between pulses. This unit measures the time elapsed between pulses which arrive at the timer input pin (TI00). Then, it stores the measured value in the on-chip RAM.

Target Device

RL78/G13

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

This application note describes the measurement of time intervals between input pulses on channel 0 of the timer array unit (TAU). Each time a valid edge is detected on the timer input pin (TI00), the count value of the timer is captured to measure the pulse interval. The measurement result is stored in the on-chip RAM.

Table 1.1 shows the required peripheral functions and their uses. Figure 1.1 presents an overview of the pulse interval measurement.

Table 1.1 Required Peripheral Functions and Their Uses

Peripheral function	Use
Timer array unit channel 0	Measurement of the time interval between input pulses on the timer input pin (TI00)
TI00	Input pin for pulse signals

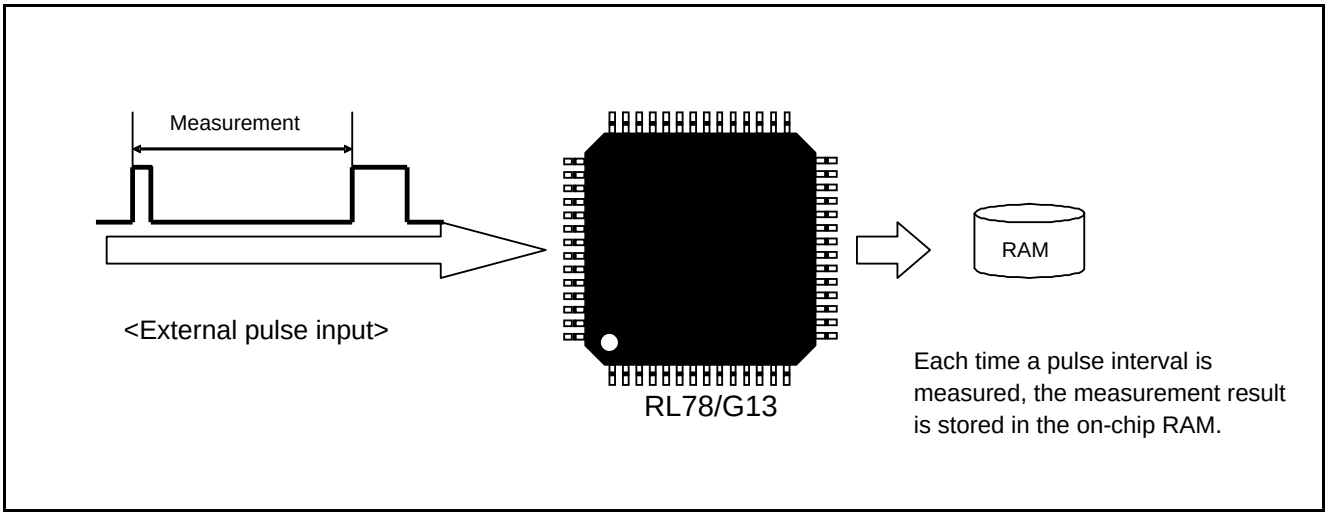

Figure 1.1 Overview of Pulse Interval Measurement

2. Operation Check Conditions

The sample code described in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G13 (R5F100LEA)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 32 MHz • CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0 V (Operation is possible over a voltage range of 2.9 V to 5.5 V.) LVD operation (VLVI): Reset mode which uses 2.81 V (2.76 V to 2.87 V)
Integrated development environment (CubeSuite+)	CubeSuite+ V1.00.01 from Renesas Electronics Corp.
C compiler (CubeSuite+)	CA78K0R V1.20 from Renesas Electronics Corp.
Integrated development environment (e2studio)	e2studio V2.0.1.3 from Renesas Electronics Corp.
C compiler (e2studio)	KPIT GNURL78-ELF Toolchain V13.02 from Renesas Electronics Corp.
Integrated development environment (IAR)	IAR Embedded Workbench for Renesas RL78 V1.30.2
C compiler (IAR)	IAR C/C++ Compiler for Renesas RL78 V1.30.2

3. Related Application Note

The application note that is related to this application note is listed below for reference.

- RL78/G13 Initialization (R01AN0451EJ0100) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of the hardware configuration used for this application note.

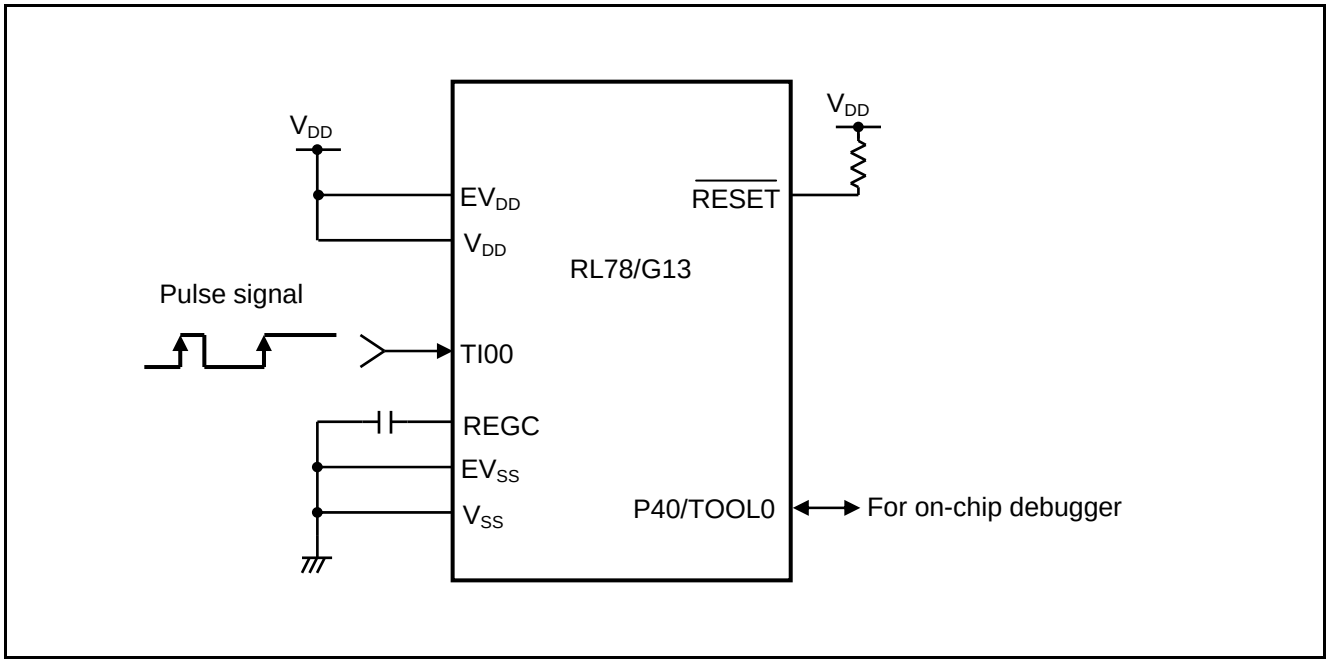

Figure 4.1 Hardware Configuration

Notes: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to VDD or V_{SS} via a resistor).
2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVI}) that is specified as LVD.

4.2 Pin to be Used

Table 4.1 shows the pin to be used and its function.

Table 4.1 Pin to be Used and Its Function

Pin Name	I/O	Description
P00/TI00	Input	Inputs pulse signals to the 16-bit timer 00.

5. Description of the Software

5.1 Operation Outline

Each time a rising edge (valid edge) is detected on the timer input pin (TI00), the sample code described in this application note captures the count value of the timer and measures the time interval between pulses which arrive at the timer input pin (TI00). When a timer interrupt (INTTM00) occurs upon completion of the capture, the sample code calculates the pulse interval and stores the calculation result in the on-chip RAM.

(1) Initialize the TAU.

<Conditions for setting>

- Use the P00/TI00 pin to receive pulses.
- The operation clock for TAU channel 0 should be f_{CLK}.
- Set TAU channel 0 to the capture mode.
- Selects “rising edge detection” as the input edge on the TI00 pin.
- Selects the TI00 pin input valid edge to trigger the capture.

(2) Set the TS00 bit of the timer channel start register 0 (TS0) to 1 to enable count operation. This clears the timer count register (TCR00) to 0000H and starts counting.

(3) When a valid edge is detected, the value of the timer count register (TCR00) is captured and put into the timer data register (TDR00). A timer interrupt (INTTM00) occurs upon completion of the capture. The timer count register (TCR00) is cleared to 0000H and the TAU waits for the next valid edge input.
An invalid value is captured when a timer interrupt (INTTM00) occurs upon completion of the first capture. This data is not used.

(4) In the processing of a timer interrupt (INTTM00) which occurs upon completion of the second capture, the timer data register (TDR00)’s value (pulse width) is stored in the on-chip RAM.

(5) The operation described in (4) above is repeated eight times. Then, the TAU transitions to the HALT state.

5.2 List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

Table 5.1 Option Byte Settings

Address	Value	Description
000C0H/010C0H	01101110B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H/010C1H	01111111B	LVD reset mode 2.81 V (2.76 V to 2.87 V)
000C2H/010C2H	11101000B	HS mode HOCO: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger.

5.3 List of Constants

Table 5.2 lists the constant that is used in this sample program.

Table 5.2 Constant for the Sample Program

Constant	Setting	Description
_0001_TAU_OVERFLOW_OCCURS	0x0001U	Detects an overflow.

5.4 List of Variables

Table 5.3 lists the global variables.

Table 5.3 Global Variables

Type	Variable Name	Contents	Function Used
uint8_t	g_Times	Holds the number of times a pulse interval measurement is to be made.	main() R_TAU0_Channel0_Interrupt()
sreg uint32_t	g_PulseWidth[8]	Holds the measured pulse interval.	main() R_TAU0_Channel0_Interrupt()
volatile uint32_t	g_Tau0Ch0Width	Temporary buffer which holds the measured pulse interval	R_TAU0_Channel0_Interrupt()

5.5 List of Functions

Table 5.4 lists the functions that are used in this sample program.

Table 5.4 Functions

Function Name	Outline
R_TAU0_Channel0_Start	TAU0 channel 0 start processing
R_TAU0_Channel0_Interrupt	INTTM00 interrupt processing

5.6 Function Specifications

This section describes the specifications for the functions that are used in this sample program.

[Function Name] R_TAU0_Channel0_Start	
Synopsis	TAU0 channel 0 start processing
Header	#include "r_cg_macrodriver.h" #include "r_cg_timer.h" #include "r_cg_userdefine.h"
Declaration	void R_TAU0_Channel0_Start(void)
Explanation	This function unmasks TAU0 channel 0 interrupts and starts count operation.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_TAU0_Channel0_Interrupt	
Synopsis	INTTM00 interrupt processing
Header	#include "r_cg_macrodriver.h" #include "r_cg_timer.h" #include "r_cg_userdefine.h"
Declaration	__interrupt void R_TAU0_Channel0_Interrupt(void)
Explanation	This function stores the measured value of the pulse time interval into g_PulseWidth[].
Arguments	None
Return value	None
Remarks	None

5.7 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

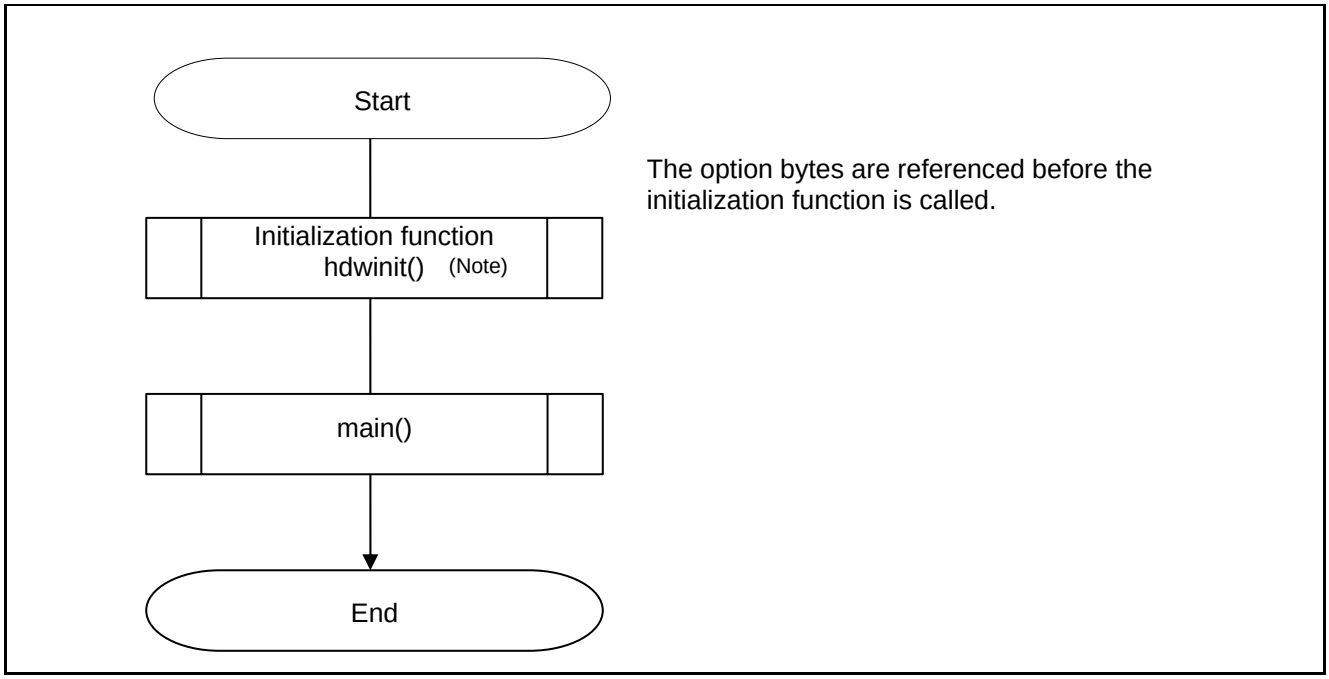

Figure 5.1 Overall Flow

5.7.1 Initialization Function

Figure 5.2 shows the flowchart for the initialization function.

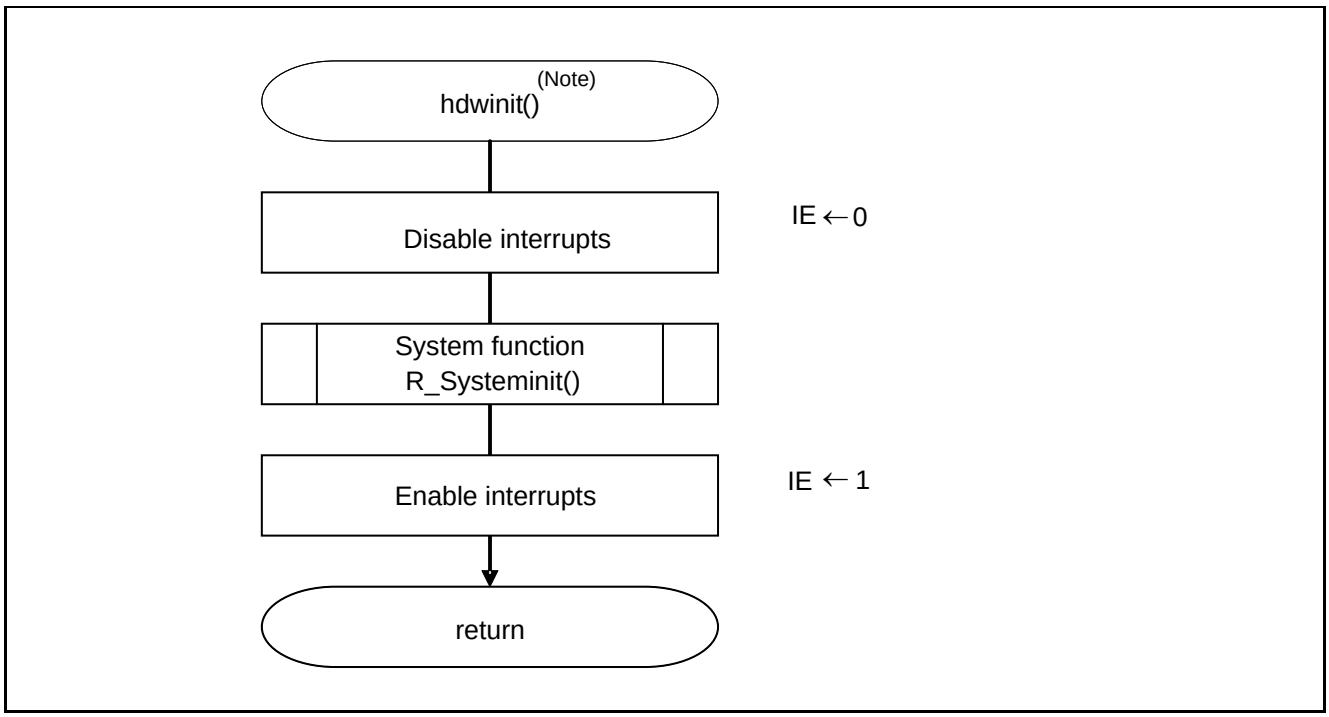

Figure 5.2 Initialization Function

Note: The __low_level_init function initializes the system in the IAR Workbench IDE-Oriented sample code.

5.7.2 System Function

Figure 5.3 shows the flowchart for the system function.

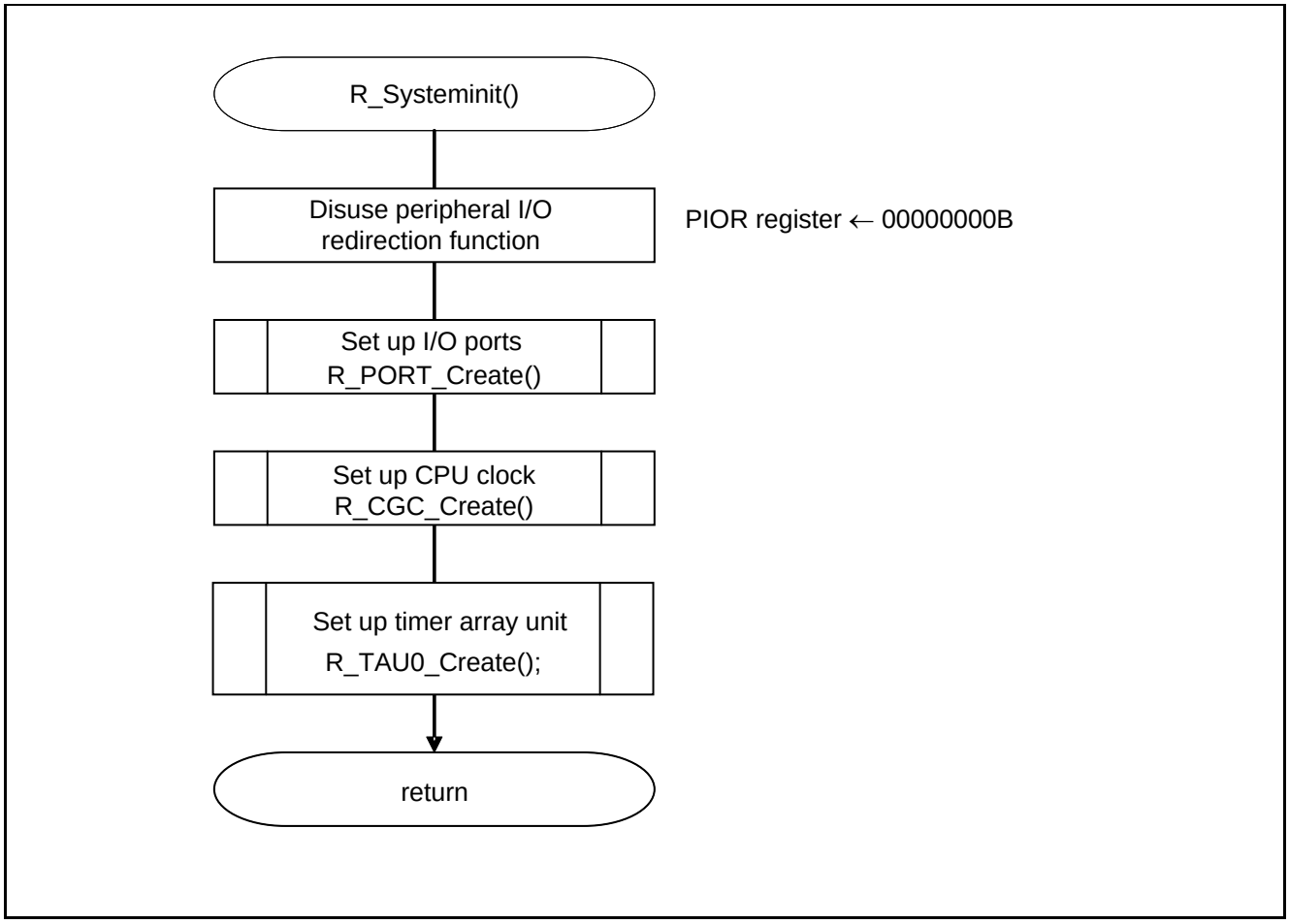

Figure 5.3 System Function

5.7.3 I/O Port Setup

Figure 5.4 shows the flowchart for setting up the I/O ports.

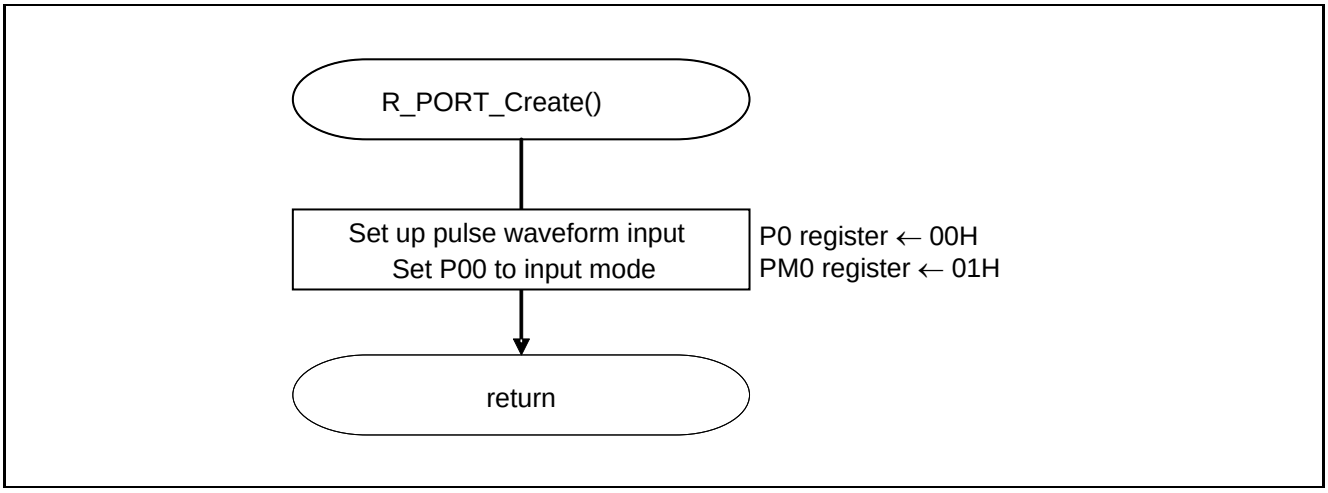

Figure 5.4 I/O Port Setup

Note: Refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN0451EJ0100) for the configuration of the unused ports.

Caution: Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

5.7.4 CPU Clock Setup

Figure 5.5 shows the flowchart for setting up the CPU clock.

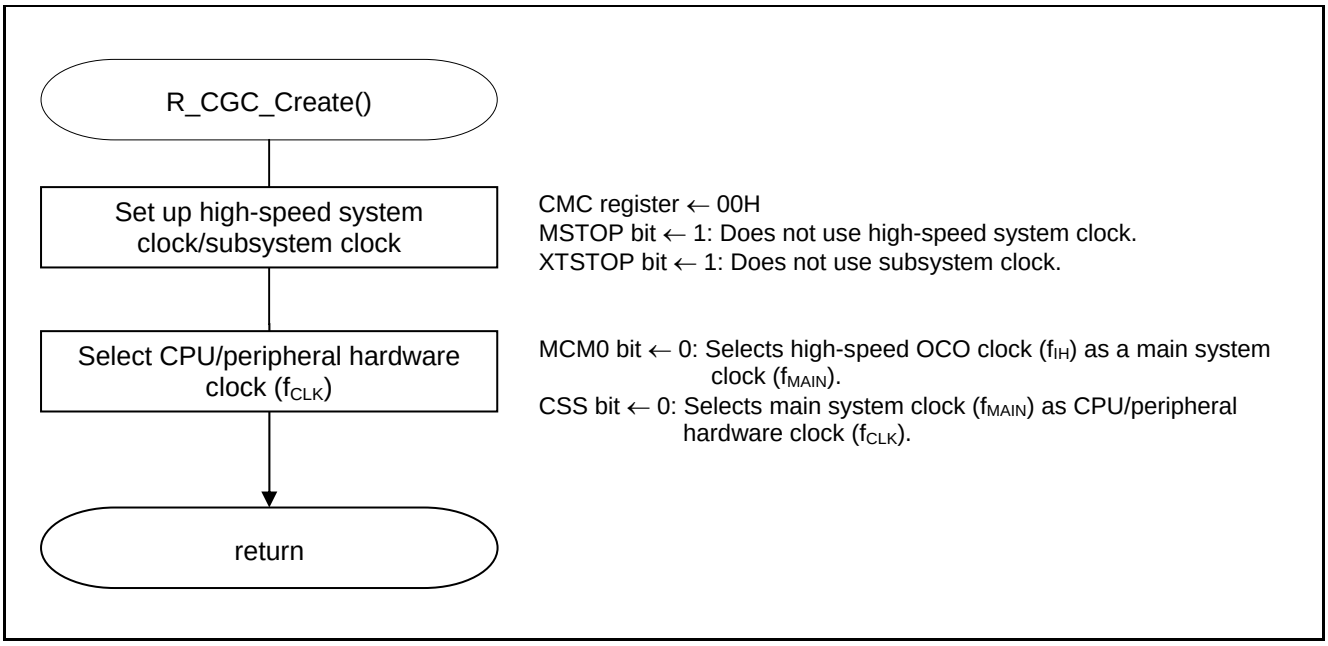

Figure 5.5 CPU Clock Setup

Caution: For details on the procedure for setting up the CPU clock (R_CGC_Create ()), refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN0451EJ0100).

5.7.5 Timer Array Unit Setup

Figure 5.6 shows the flowchart for setting up the timer array unit.

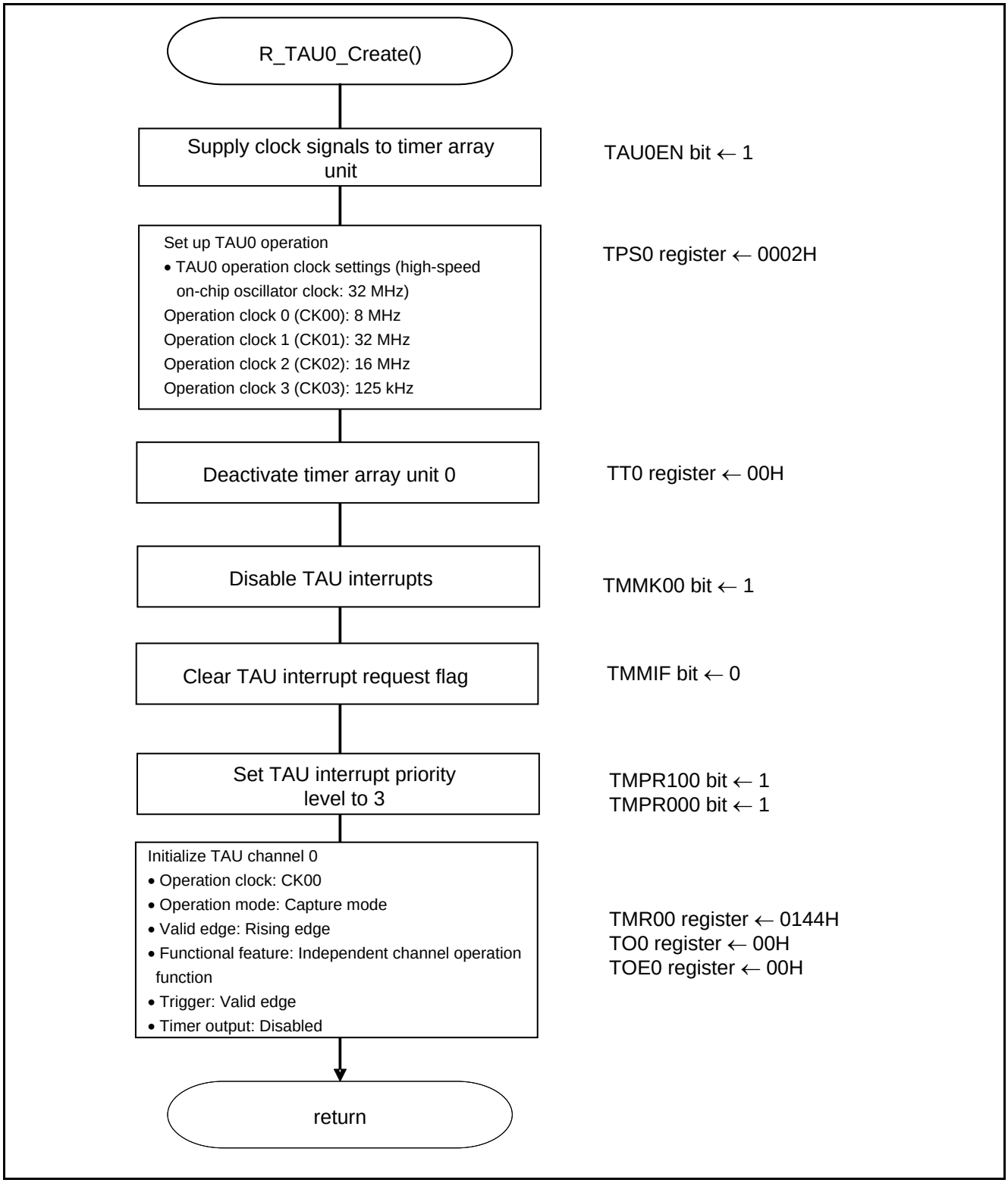

Figure 5.6 Timer Array Unit Setup

Starting clock signal supply to the timer array unit

- Peripheral enable register 0 (PER0)
  Supply clock signals to the timer array unit.

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
0	0	0	0	0	0	0	**1**

Bit 0

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Configuring the clock frequency

- Timer clock select register 0 (TPS0)
  Select the CK00 operation clock.

Symbol: TPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	PRS 031	PRS 030	0	0	PRS 021	PRS 020	PRS 013	PRS 012	PRS 011	PRS 010	PRS 003	PRS 002	PRS 001	PRS 000
0	0	**0**	**0**	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**

PRS 003	PRS 002	PRS 001	PRS 000		Operation clock (CK00) selection				
					f_{CLK} = 2 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	f_{CLK} = 20 MHz	f_{CLK} = 32 MHz
0	0	0	0	f_{CLK}	2 MHz	5 MHz	10 MHz	20 MHz	32 MHz
0	0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	16 MHz
0	**0**	**1**	**0**	**$f_{CLK}/2^2$**	**500 kHz**	**1.25 MHz**	**2.5 MHz**	**5 MHz**	**8 MHz**
0	0	1	1	$f_{CLK}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz	4 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	312.5 kHz	625 kHz	1.25 MHz	2 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	156.2 kHz	312.5 kHz	625 kHz	1 MHz
0	1	1	0	$f_{CLK}/2^6$	31.25 kHz	78.1 kHz	156.2 kHz	312.5 kHz	500 kHz
0	1	1	1	$f_{CLK}/2^7$	15.62 kHz	39.1 kHz	78.1 kHz	156.2 kHz	250 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz	125 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	9.76 kHz	19.5 kHz	39.1 kHz	62.5 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	4.88 kHz	9.76 kHz	19.5 kHz	31.25 kHz
1	0	1	1	$f_{CLK}/2^{11}$	976 Hz	2.44 kHz	4.88 kHz	9.76 kHz	15.63 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz	7.81 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	610 Hz	1.22 kHz	2.44 kHz	3.91 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	305 Hz	610 Hz	1.22 kHz	1.95 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61 Hz	153 Hz	305 Hz	610 Hz	976 Hz

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Controlling the channel trigger operation

- Timer channel stop register 0 (TT0)
  Select the TAU0 stop trigger.

Symbol: TT0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TT H03	0	TT H01	0	TT 07	TT 06	TT 05	TT 04	TT 03	TT 02	TT 01	TT 00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**

Bit 0

TT00	Operation stop trigger of channel 0
0	No trigger operation
1	**Operation is stopped (stop trigger is generated).**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up the channel 0 operation mode

- Timer mode register 00 (TMR00)
  Specify the operation mode, edge, trigger, channel and clocks.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	MAST ER00	STS 002	STS 001	STS 000	CIS 001	CIS 000	0	0	MD 003	MD 002	MD 001	MD 000
0	**0**	0	**0**	**0**	**0**	**0**	**1**	**0**	**1**	0	0	**0**	**1**	**0**	**0**

Bits 3 to 0

MD 003	MD 002	MD 001	MD 000	Channel 0 operation mode setup
0	0	0	0	Interval timer mode. Does not generate a timer interrupt at the start of count operation.
			1	Interval timer mode. Generates a timer interrupt at the start of count operation.
0	**1**	**0**	**0**	**Capture mode** **Does not generate a timer interrupt at the start of count operation.**
			1	Capture mode Generates a timer interrupt at the start of count operation.
0	1	1	0	Event counter mode Does not generate a timer interrupt at the start of count operation.
1	0	0	0	One-count mode Disables the start trigger during count operation.
			1	One-count mode Enables the start trigger during count operation.
1	1	0	0	Capture & one-count mode Does not generate a timer interrupt at the start of count operation. Disables the start trigger during count operation.

Bits 7 and 6

CIS 001	CIS 000	Selection of TI00 pin input valid edge
0	0	Falling edge
0	**1**	**Rising edge**
1	0	Both edges (when low-level width is measured)
1	1	Both edges (when high-level width is measured)

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	MAST ER00	STS 002	STS 001	STS 000	CIS 001	CIS 000	0	0	MD 003	MD 002	MD 001	MD 000
0	**0**	0	**0**	**0**	**0**	**0**	**1**	**0**	**1**	0	0	**0**	**1**	**0**	**0**

Bits 10 to 8

STS 002	STS 001	STS 000	Setting of start trigger or capture trigger of channel 0
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	**0**	**1**	**Valid edge of the TI00 pin input is used as both the start trigger and capture trigger.**
0	1	0	Both the edges of the TI00 pin input are used as a start trigger and capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).

Bit 11

MASTER00	Selection between using channel 0 independently or simultaneously with another channel (as a slave or master)
0	**Operates in independent channel operation function or as slave channel in simultaneous channel operation function.**
1	Operates as master channel in simultaneous channel operation function.

Bit 12

CCS00	Selection of count clock (f_{TCLK}) of channel 0
0	**Operation clock f_{MCK} specified with the CKS000 and CKS001 bits**
1	Valid edge of the input signal from the TI00 pin

Bits 15 and 14

CKS001	CKS000	Selection of operation clock (f_{MCK}) of channel 0
0	**0**	**Operation clock CK00 set by timer clock select register 0 (TPS0)**
1	0	**Operation clock CK01 set by timer clock select register 0 (TPS0)**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.6 Main Processing

Figure 5.7 shows the flowchart for main processing.

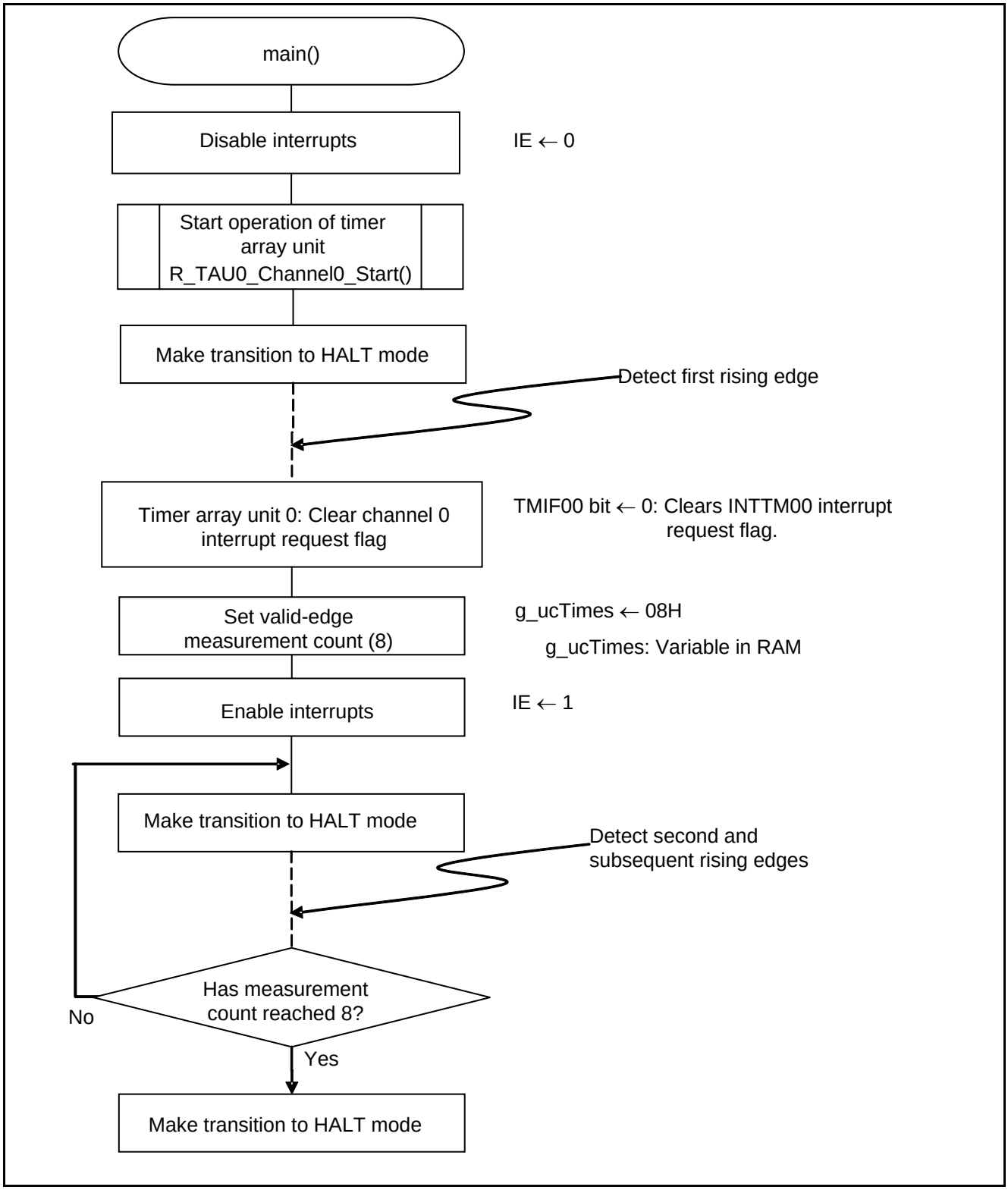

Figure 5.7 Main Processing

5.7.7 Timer Array Unit Startup

Figure 5.8 shows the flowchart for starting the operation of the timer array unit.

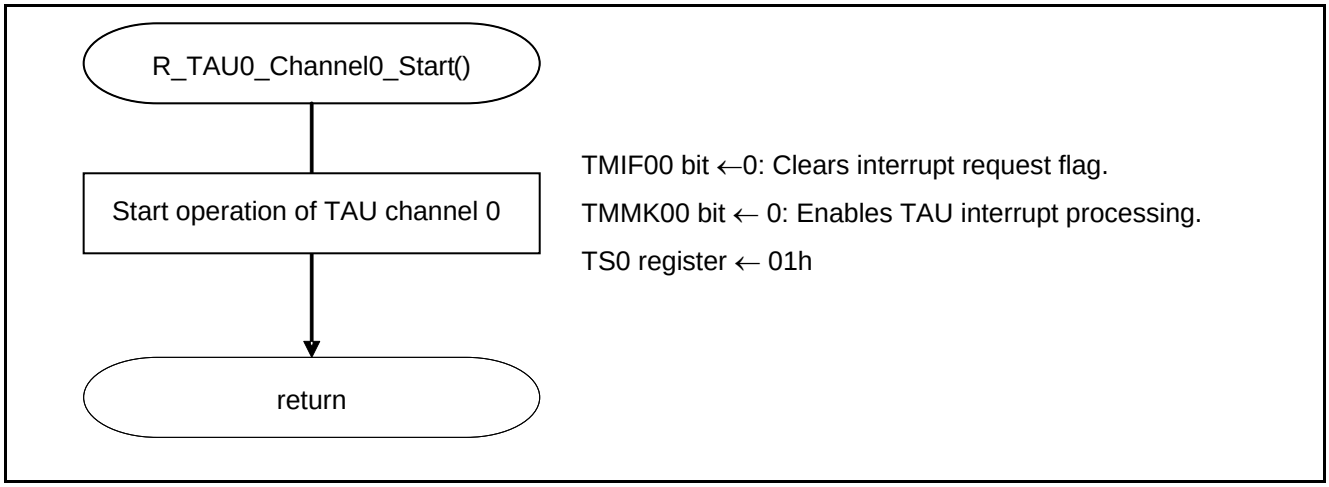

Figure 5.8 Timer Array Unit Startup

Configuring the interrupt request flag

- Clear the timer interrupt request flag.

Symbol: IF1L

7	6	5	4	3	2	1	0
TMIF03	TMIF02	TMIF01	TMIF00	IICAIF0	SREIF1 TMIF03H	SRIF1 CSIIF11 IICIF11	STIF1 CSIIF10 IICIF10
0/1	0/1	0/1	**0**	0/1	0/1	0/1	0/1

Bit 4

TMIF00	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Configuring the interrupt mask

- Unmask timer interrupts.

Symbol: MK1L

7	6	5	4	3	2	1	0
TMMK03	TMMK02	TMMK01	TMMK00	IICAMK0	SREMK1 TMMK03H	SRMK1 CSIMK11 IICMK11	STMK1 CSIMK10 IICMK10
0/1	0/1	0/1	**0**	0/1	0/1	0/1	0/1

Bit 4

TMMK00	Interrupt processing control
0	**Enables interrupt processing.**
1	Disables interrupt processing.

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Configuring the timer channel startup

- Enable timer count operation.

Symbol: TS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TS H03	0	TS H01	0	TS 07	TS 06	TS 05	TS 04	TS 03	TS 02	TS 01	TS 00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**

Bit 0

TS00	Operation enable (start) trigger of channel 0
0	No trigger operation
1	**The TE00 bit is set to 1 and the count operation becomes enabled.**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

User's Manual:

RL78/G13 User's Manual: Hardware (R01UH0146EJ)
RL78 Family User's Manual: Software (R01US0015EJ)
The latest version can be downloaded from the Renesas Electronics website.

Technical Updates/Technical News

The latest information can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics Website

http://www.renesas.com/index.jsp

Inquiries

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REVISION HISTORY	RL78/G13 Timer Array Unit (Pulse Interval Measurement)

Rev.	Date	Description	
		Page	Summary
1.00	Sep. 30, 2011	—	First edition issued
2.00	Dec. 27, 2013	4	Table 2.1: Added e2studio and IAR information
		9	Added note Figure 5.2: Fixed typo in function name
		10	Figure 5.3: Fixed typo in function name
		11	Figure 5.4: Fixed typo in function name

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
  In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
  In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable.
When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal.
  Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different a different part number may differ in terms of the internal memory capacity and layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to products with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
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