RL78/G13, 78K0/Kx2

Migration Guide from 78K0 to RL78: Reset function

Introduction

This application note describes how to migrate the reset function of the 78K0/Kx2 to that of the RL78/G13.

Target Device

RL78/G13, 78K0/Kx2

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Differences in Function Overview

Table 1.1 summarizes the differences between the reset functions of the 78K0/Kx2 and the RL78/G13.

Table 1.1 Differences

Item	78K0/Kx2	RL78/G13
Reset generation sources	- External reset input via RESET pin - Internal reset by watchdog timer program loop detection - Internal reset by comparison of supply voltage and detection voltage of power-on-clear (POC) circuit - Internal reset by comparison of supply voltage and detection voltage of low-power-supply detector (LVI)	- External reset input via RESET pin - Internal reset by watchdog timer program loop detection - Internal reset by comparison of supply voltage and detection voltage of power-on-reset (POR) circuit - Internal reset by comparison of supply voltage of the voltage detector (LVD) and detection voltage - Internal reset by execution of illegal instruction (Note1) - Internal reset by RAM parity error (Note2) - Internal reset by illegal-memory access (Note3)

Note1. The illegal instruction is generated when instruction code FFH is executed.

Note2. A RAM parity error is detected when uninitialized RAM is read.

Note3. An illegal-memory access is detected when a specified illegal access detection area is accessed.

Remark. For details, refer to the appropriate user's manuals (hardware).

The 78K0/Kx2 has four reset sources. When a reset source generates a reset signal, program execution begins from the address specified in the reset vector table (addresses 0000H and 0001H). A reset is applied when a low level is input through the RESET pin, the watchdog timer detects an inadvertent program loop, or the POC or LVI circuit detects a specified voltage. After the MCU is released from the reset state and reset processing is completed, program execution begins with the internal high-speed oscillation clock.

The RL78/G13 has seven reset sources. When a reset source generates a reset signal, program execution begins from the address specified in the reset vector table (addresses 00000H and 00001H). A reset is applied when a low level is input through the RESET pin, the watchdog timer detects an inadvertent program loop, the POR or LVD circuit detects a specified voltage, an illegal instruction(Note1) is executed, a RAM parity error(Note2) occurs, or illegal-memory access(Note3) is attempted. After the MCU is released from the reset state and reset processing is completed, program execution begins with the high-speed on-chip oscillator clock specified by the option byte.

2. Register Compatibilities

Table 2.1 shows the compatibilities of the registers for the reset functions between the 78K0/Kx2 and the RL78/G13. These registers are used to confirm the reset source.

Table 2.1 Register Compatibilities

Item	78K0/Kx2	RL78/G13
Confirming reset source (Note)	RESF register	RESF register
Internal reset request by watchdog timer (WDT)	RESF register WDTRF bit	RESF register WDTRF bit
Internal reset request by low-voltage detector (LVI, LVD)	RESF register LVIRF bit	RESF register LVIRF bit
Internal reset request by execution of illegal instruction	None	RESF register TRAP bit
Internal reset request t by RAM parity	None	RESF register RPERF bit
Internal reset request t by illegal-memory access	None	RESF register IAWRF bit

Note. Do not use a 1-bit memory manipulation instruction to read the RESF register; be sure to use an 8-bit memory manipulation instruction.

Remark. For details, refer to the appropriate user's manuals (hardware).

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	May. 31, 2019	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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