RL78/G10

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Timer Array Unit Controlling Switched-Mode Power Supply with Dual Input One-Shot Pulse Output Function CC-RL

Introduction

This application note explains how to use the dual input one-shot pulse output function to control the switched-mode power supply (SMPS or flyback converter).

Target Device

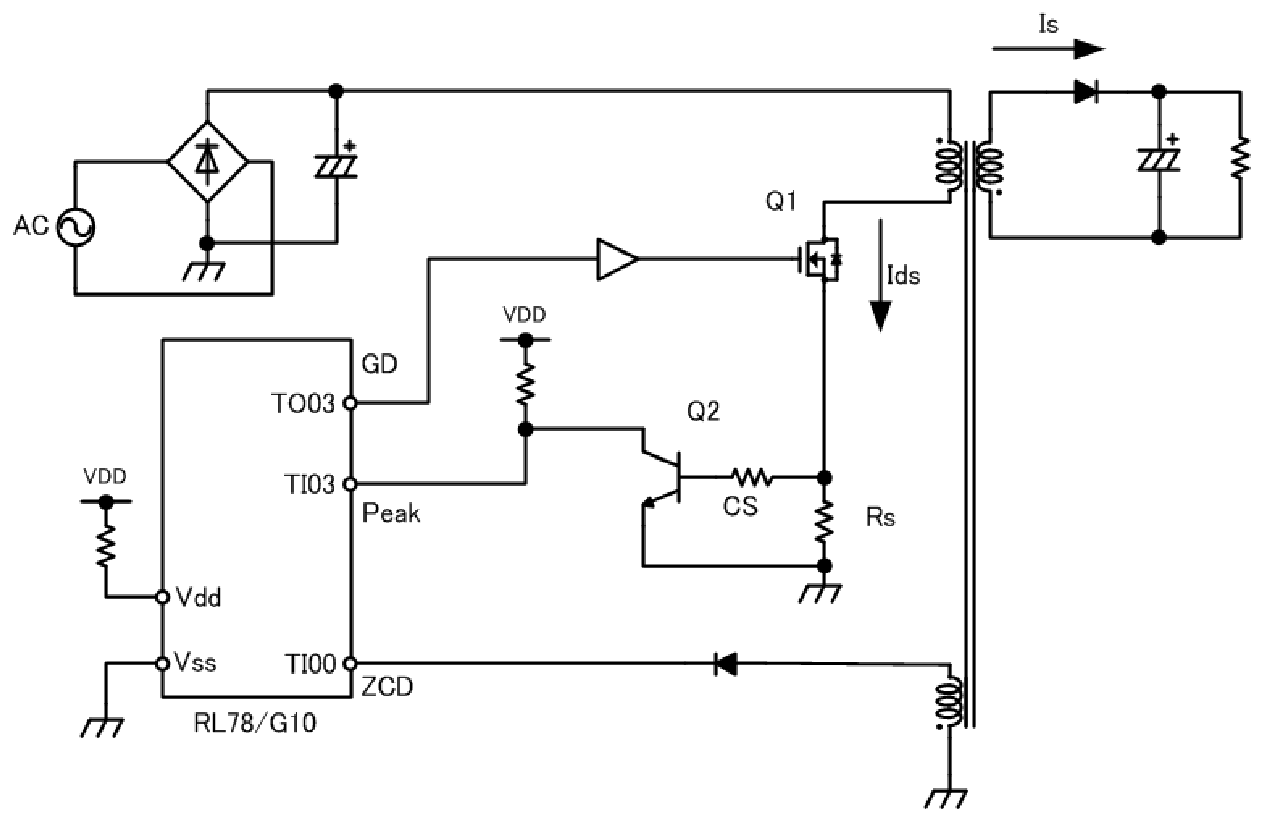
RL78/G10 16-pin (Part name: R5F10Y47, R5F10Y46, R5F10Y44)

Contents

1. Basic Functions

The dual input one-shot pulse output function in the timer array can output a variation of one-shot pulses by changing the pin polarity of the timer output, triggering a valid edge of the timer input pin.

The following is an example of a current-controlled flyback converter using this function.



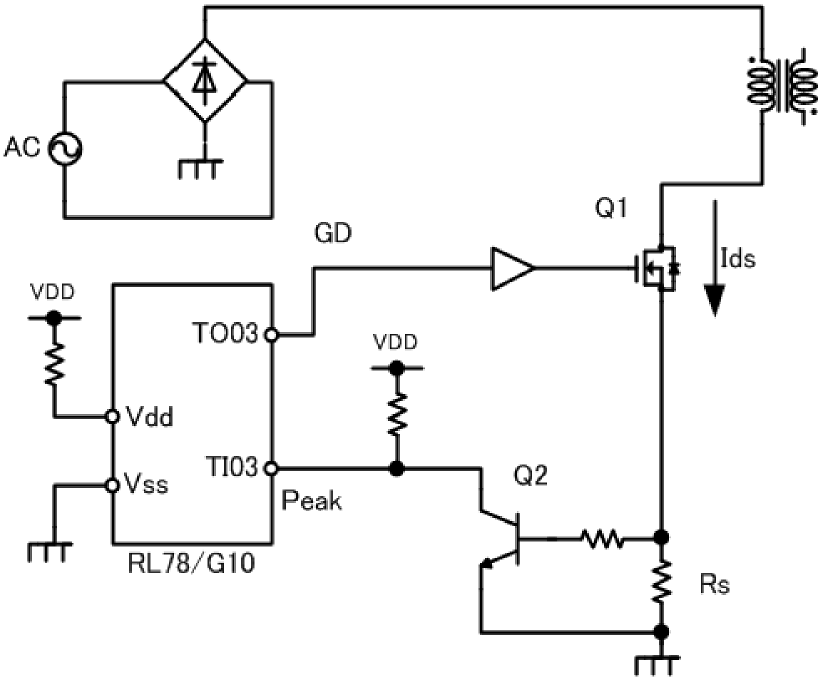
GD: PWM signal
Ids: Drain source current
ZCD: Zero Current Detection signal
Peak: Peak current detection signal
Rs: Shunt resistor
Is: Secondary-side current

Figure 1-1 Circuit Example

The MCU detects the peak signal of the current (Ids) during the ON state of switching device Q1 when the ZCD (Zero Current Detection) signal indicates the current (Is) flowing through the transformer coil is zero. Using these two edge signals for the timer module, the MCU then controls the Ids by outputting the one-shot pulse to Q1.

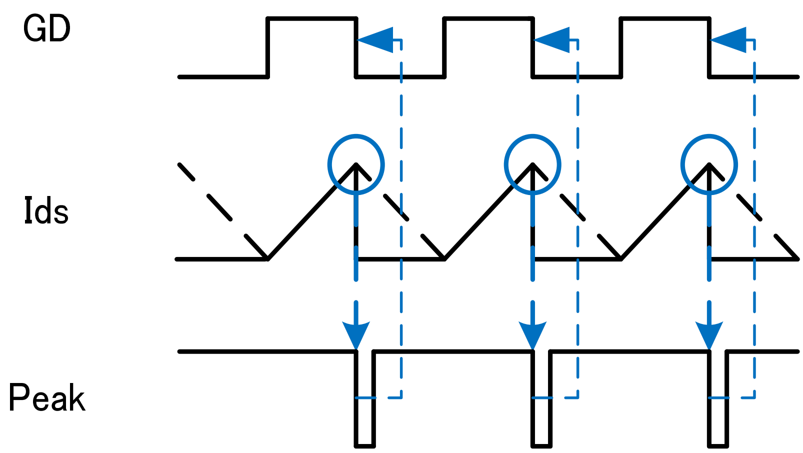
1.1 Peak Current Detection

Transistor Q2 is used to detect the peak current of Ids. Transistor Q2's base and emitter pins are connected to both sides of shunt resistor Rs, which is connected to the Q1 source pin. The Q2 collector pin is connected to timer input pin TI03. As Ids increases, the Rs end-to-end voltage reaches the Vbe voltage of Q2 (≈ 0.6V). This turns Q2 ON and switches the input signal of TI03 to Low. This edge becomes the trigger to switch timer output pin TO03 to Low.
The timing of peak current detection shown in Figures 1-3.



GD: PWM Signal
Peak: Peak current
Q1: Switching device
Q2: Peak current detection transistor
Rs: Shunt resistor

Figure 1-2 Peak Current Output Detection Using External Circuit



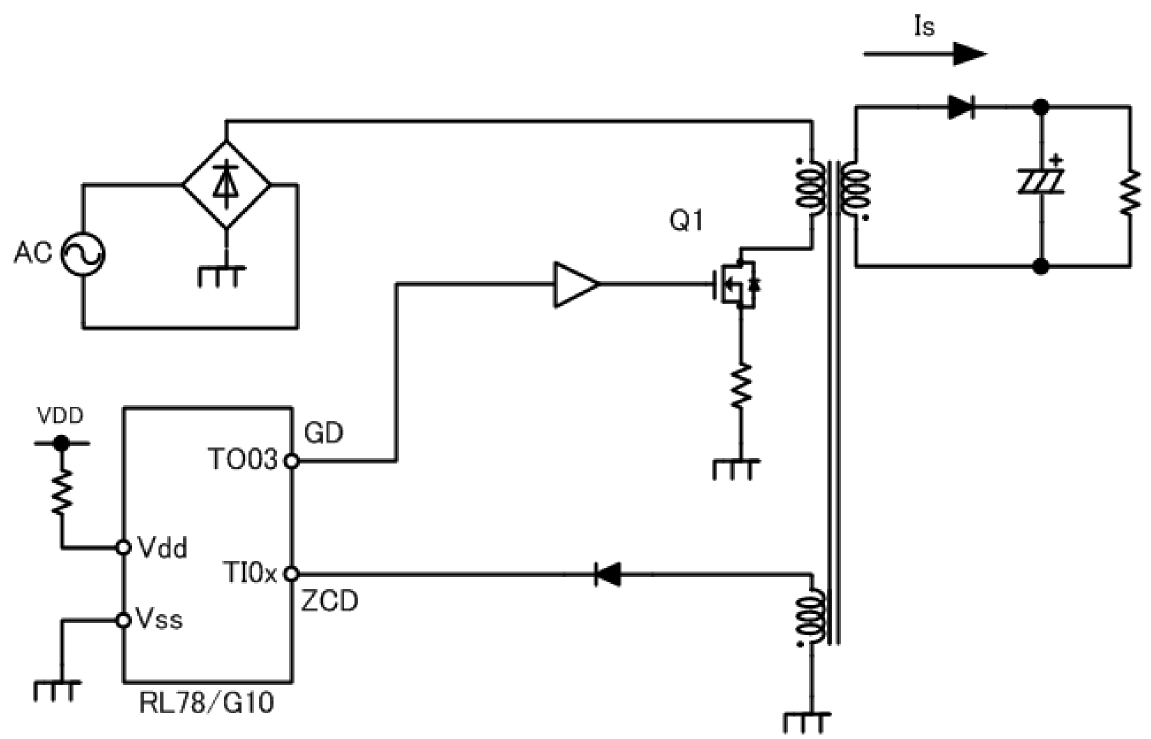
Operation state
Time of operation state

Figure 1-3 Timing Chart (peak current detection)

1.2 ZCD Signal Detection

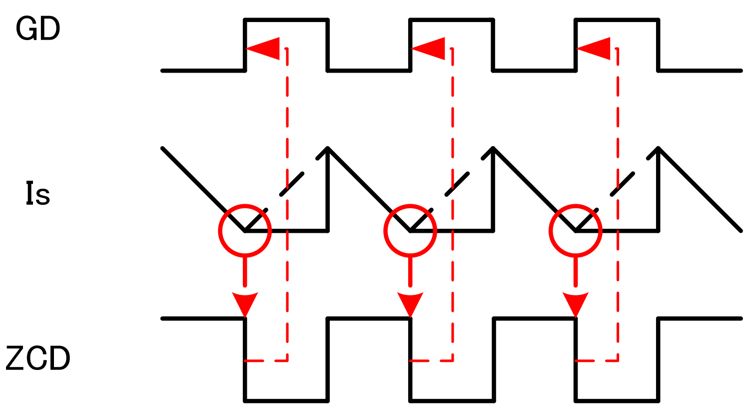
This application detects the zero timing of secondary-side current Is using the winding voltage of the transformer, as shown in Figure 1-4. The method used to detect this zero current Is called Zero Current Detection (ZCD). When Q1 turns OFF, the energy accumulated in the transformer is transferred to the secondary side (winding). Because is flows in the same direction as the diode on the secondary side, power is supplied to the output capacitor and the load. When all of the accumulated energy is transferred from the transformer, the ZCD signal goes to Low. This edge is input to timer input pin T10x and the PWM signal switches to High.

The timing of ZCD signal detection as shown in Figures 1-5.



GD: PWM signal
ZCD: ZCD signal
Is: Secondary-side current

Figure 1-4 ZCD Signal Detection



— Operation state
- - Time of operation state

Figure 1-5 Timing Chart (ZCD signal detection)

2. Pin Assignment Example

Table 2-1 shows RL78/G10 pin assignments for the circuit example described above.

Table 2-1 Pin Assignment Example

Pin	Port	A/D	Comparator	SIF	Timer	External	Other	Function
1	P41				TI03	INTP2		Peak current detection
2	P40				(TI01/ TO01)	KR0	TOOL0/ (PCLBUZ0)	
3	P125					KR1	RESET	Reset
4	P137				TI00	INTP0		ZCD signal detection
5	P122					(INTP2)	X2/ EXCLK	
6	P121					(INTP3)	X1	
7							Vss	GND
8							Vdd	5V
9	P00			SO00/ TXD0		INTP1		
10	P01	ANI0		SI00/ RXD0/ SDA00		KR2		
11	P02	ANI1	VCOUT0	SCK00/ SCL00		KR3	PCLBUZ0	
12	P03	ANI2	IVCMP0		TO00	KR4/ (INTP1)		
13	P04	ANI3	IVREF0		TI01/ TO01	KR5		
14	P05	ANI4		SO01	TI02/ TO02			
15	P06	ANI5		SCLA0/ SIO1		INTP3		
16	P07	ANI6		SDAA0/ SCK01	TO03			PWM signal

3. Operation Check Conditions

The sample code described in this application note has been checked under the conditions listed in the table below.

Table 3.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G10 (R5F10Y47, R5F10Y46, R5F10Y44)
Operating frequency	· High-speed on-chip oscillator (HOCO) clock: 20MHz · CPU/peripheral hardware clock: 20MHz
Operating voltage	5.0 V (can run on a voltage range of 2.9 V to 5.5 V.) SPOR detection voltage: Rising edge voltage: 2.90V : Falling edge voltage: 2.84V
Integrated development environment (CS+)	CS+ for CC V3.01.00 from Renesas Electronics Corp.
Assembler (CS+)	CC-RL V1.01.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V4.1.0.018 from Renesas Electronics Corp.
Assembler (e^2 studio)	CC-RL V1.01.00 from Renesas Electronics Corp.

4. Peripheral Function Settings

The following tables describe the peripheral function settings for RL78/G10.

Table 4-1 Peripheral Function Settings

Function	Ch	Setting
TAU	Ch0,3	• For switching • Operating mode: dual input one-shot pulse output TI00: peak current detection TI03: ZCD signal detection TO03: PWM signal output
12-bit interval timer	-	• For main interval count (200us interval)

Table 4-2 Option Byte Setting

Address	Setting Value	Description
000C0H	1110 1110B	• Watchdog timer not used
000C1H	1111 0111B	• SPOR detection voltage: Falling edge: VDD < 2.84V Rising edge: VDD >= 2.90V
000C2H	1111 1001B	• High-speed on-chip oscillator (20MHz)
000C3H	1000 0101B	• Enables on-chip debug operation

5. Flowcharts

5.1 Main and Peripheral Function Initialization

The following flowchart is an example of main processing and peripheral function initialization.

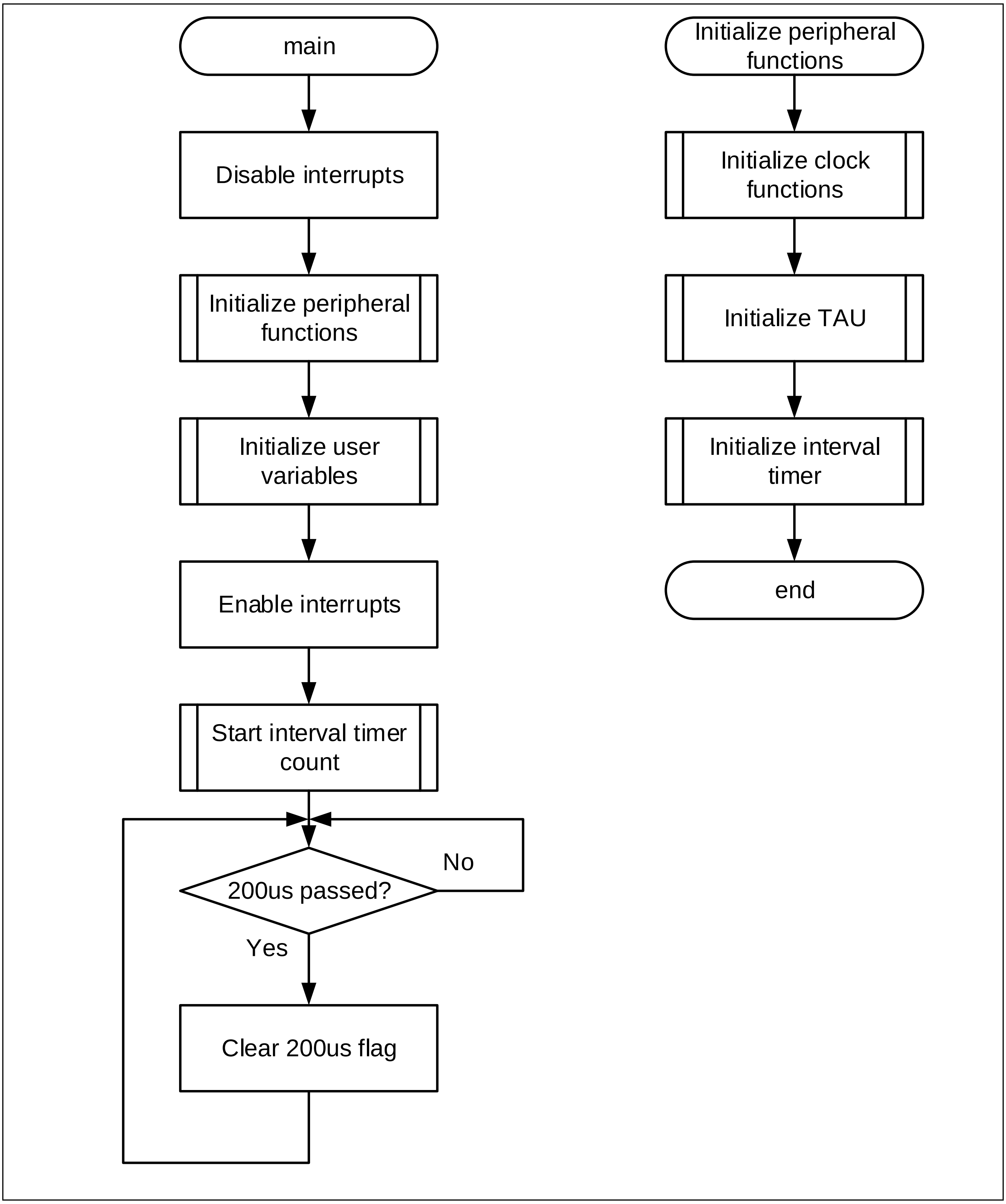


Figure 5-1 Main Processing Flow

5.2 Clock Generation Circuit Initialization

The following flowchart is an example of the clock generation circuit initialization.

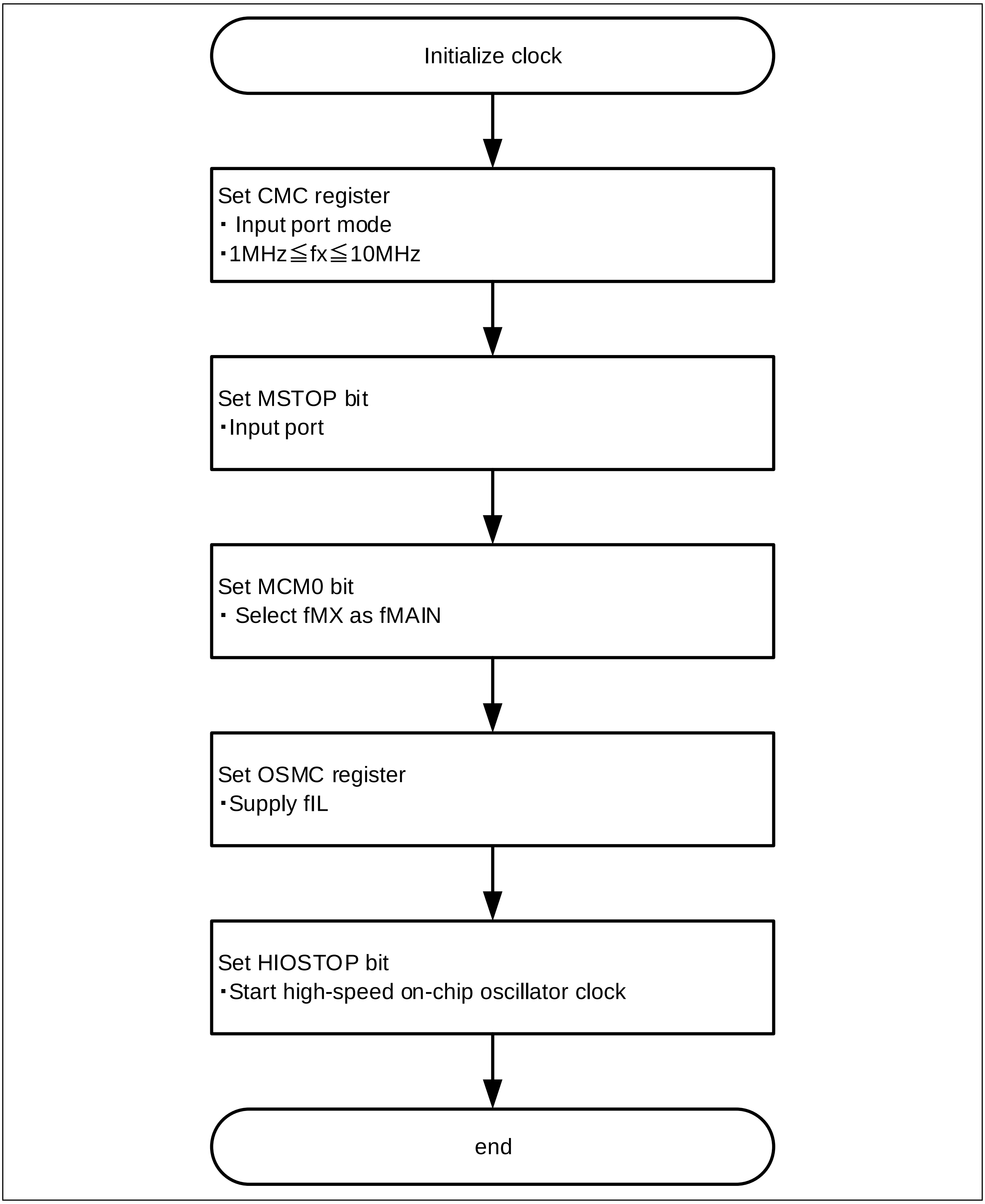


Figure 5-2 Clock Generation Circuit Initialization Flowchart

5.3 TAU Initialization

The following flowchart shows the initialization of the timer array unit (TAU).

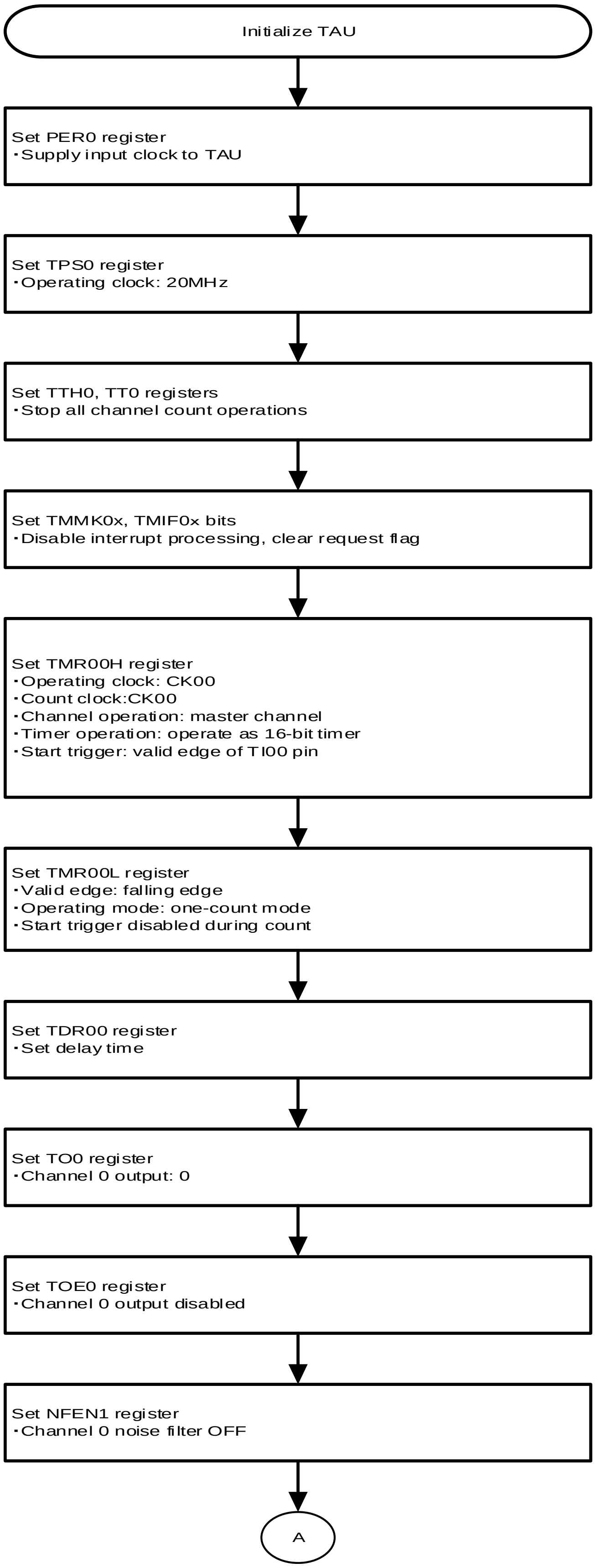


Figure 5-3 TAU Initialization Flowchart (1)

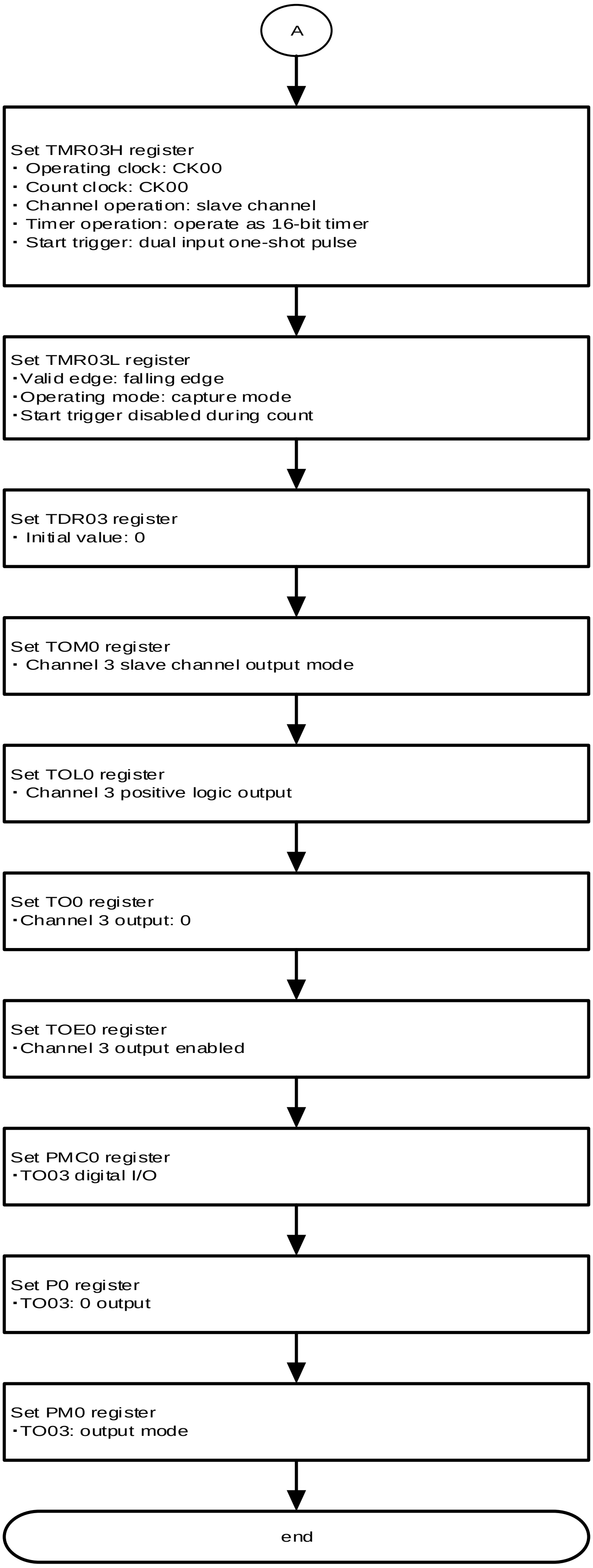


Figure 5-4 TAU Initialization Flowchart (2)

5.4 12-bit Interval Timer Initialization

The following flowchart shows the initialization of the 12-bit interval timer.

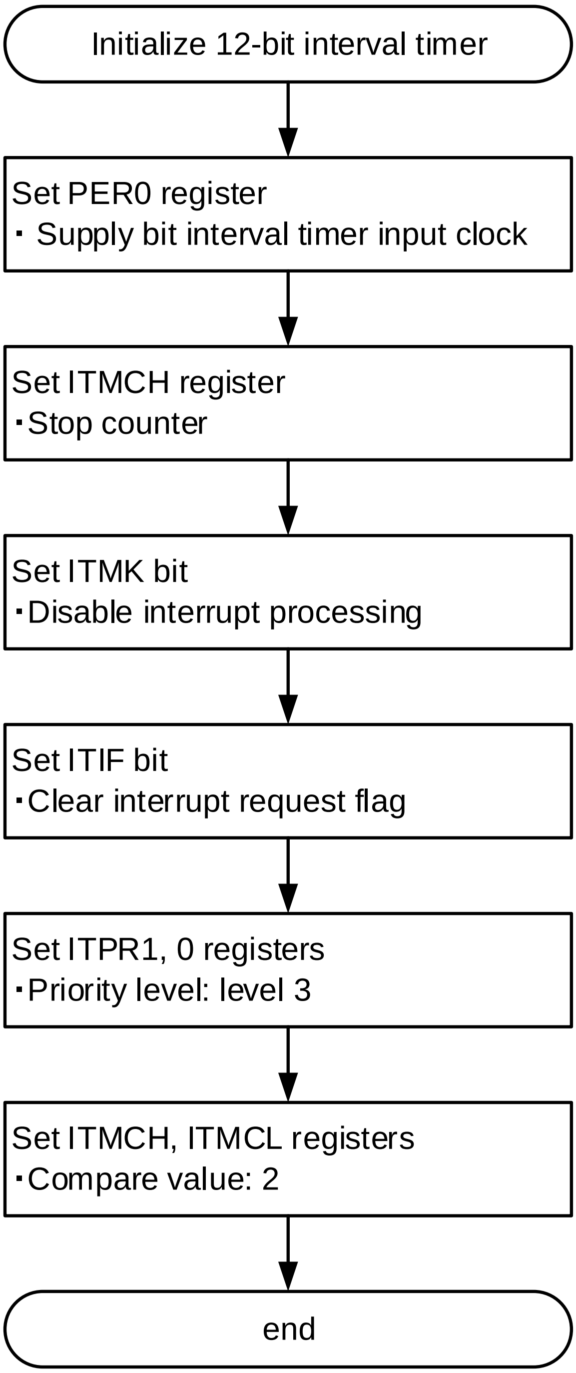
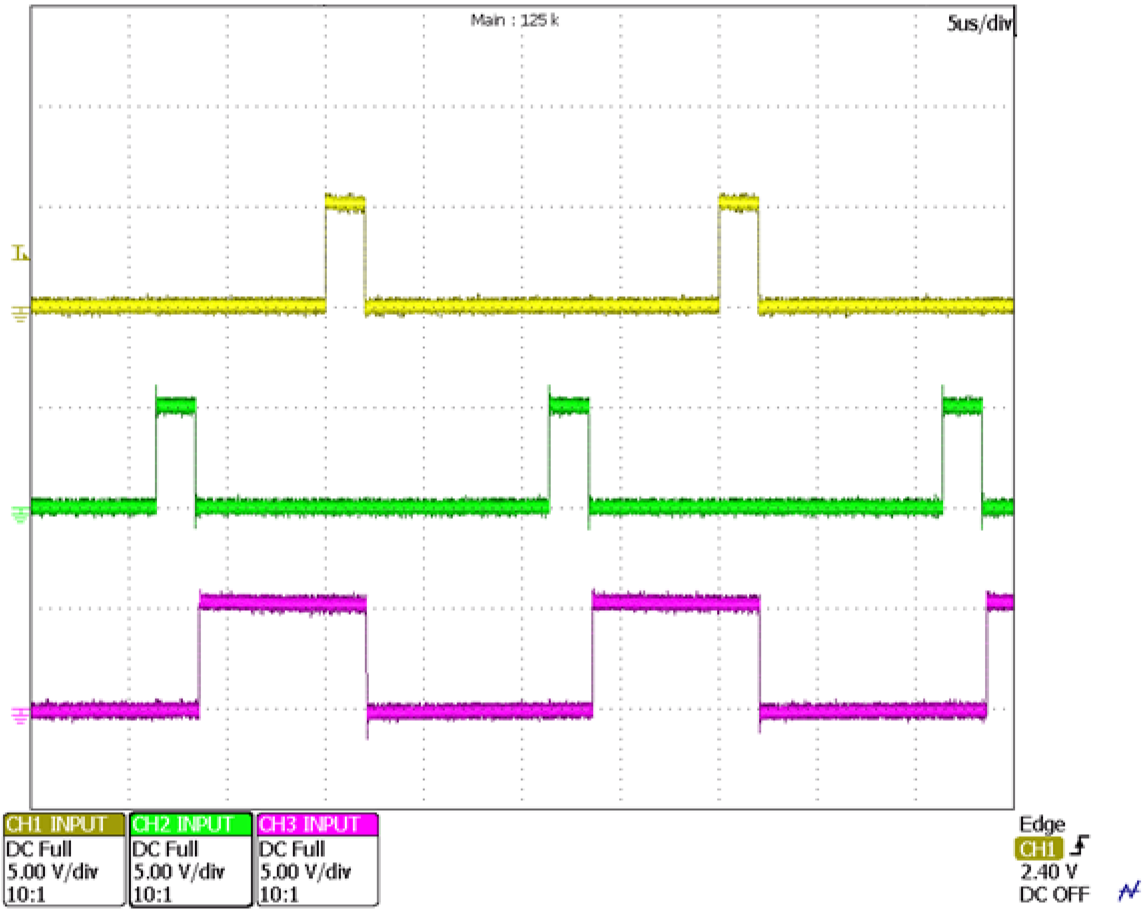


Figure 5-5 12-bit Interval Timer Initialization Flowchart

6. Switching Waveform

The following shows the switching waveform for this example.



CH1: Peak current detection signal (TI03)
CH2: ZCD signal (TI00)
CH3: PWM signal (TO03)

Figure 6-1 Switching Waveform

7. Sample Code

The sample code is available on the Renesas Electronics Website.

8. Documents for Reference

RL78/G10 User's Manual: Hardware (R01UH0384E)

RL78 Family User's Manual: Software (R01US0015E)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

(The latest versions of the documents are available on the Renesas Electronics Website.)

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Revision Record	RL78/G10 Timer Array Unit Controlling Switched-Mode Power Supply with Dual Input One-Shot Pulse Output Function CC-RL

Rev.	Date	Description	
		Page	Summary
1.00	Feb. 03, 2016	—	First edition issued

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   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

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   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
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   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

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