RL78/G10

Serial Array Unit (Baud Rate Correction) CC-RL

R01AN3083EJ0101
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Introduction

This application note describes how to correct the baud rate by UART communication function of the serial array unit (SAU). First, a communication partner's baud rate is computed by the pulse interval measurement function of the timer array unit (TAU). The register of RL78/G10 is set up, and baud rate correction is performed so that a baud rate error may be reduced from the computed result.

Target Device

RL78/G10

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specification

In this application note, measures the data 55H (High and Low come by turns) of LSB first [Note] by the communication partner using the pulse interval measurement function, and calculates the communication partner's baud rate. Moreover, sets up the register of RL78/G10 to reduce a baud rate error with a communication partner (baud rate correction). In addition, an Input switch control register (ISC) is set up for inputting the input signal of RxD0 pin into INTP0 and TM01.
Detects the start bit (falling edge) of the data 55H transmitted by the communication partner by INTP0 interruption, and starts TM01 by the pulse interval measurement function. Measures the pulse interval of the data 55H (4 times of rising edges), and calculates the communication partner's baud rate (bit width of UART data). From the calculation result, adjusts the baud rate of RL78/G10 in SPS0 register and upper 7-bit of SDR register. Sends the data 55H to the communication partner from RL78/G10 as an object for a check after adjustment.

Note: In the case of the MSB first, AAH is used. Moreover, parity is nothing or is taken as odd parity.

Table 1.1 shows the peripheral function to be used and its use.

Figure 1.1 shows the circuit configuration of baud rate measurement.

Figure 1.2 shows the timing chart of baud rate measurement.

Figure 1.3 shows each baud rate adjustment program.

Table 1.1 Peripheral Functions to be Used and Uses

Peripheral Function	Use
Serial array unit 0 (UART0)	Interlocks the channel 0 and the channel 1, and uses a UART function.
External interrupt (INTP0)	The start bit (falling edge) of the signal inputted into RxD0 pin is detected.
Timer array unit 0 (TM01)	The channel 1 is used as the pulse interval measurement function. The pulse interval of the input signal (4 times of rising edges) of RxD0 pin is measured.

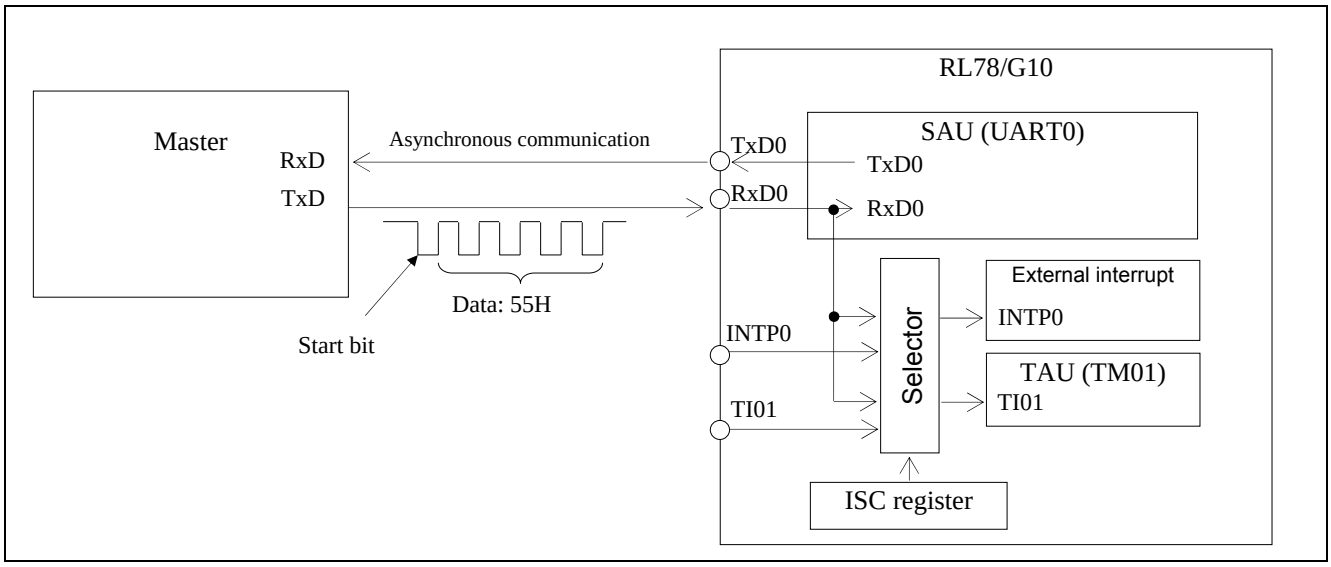

Figure 1.1 Circuit Configuration of Baud Rate Measurement

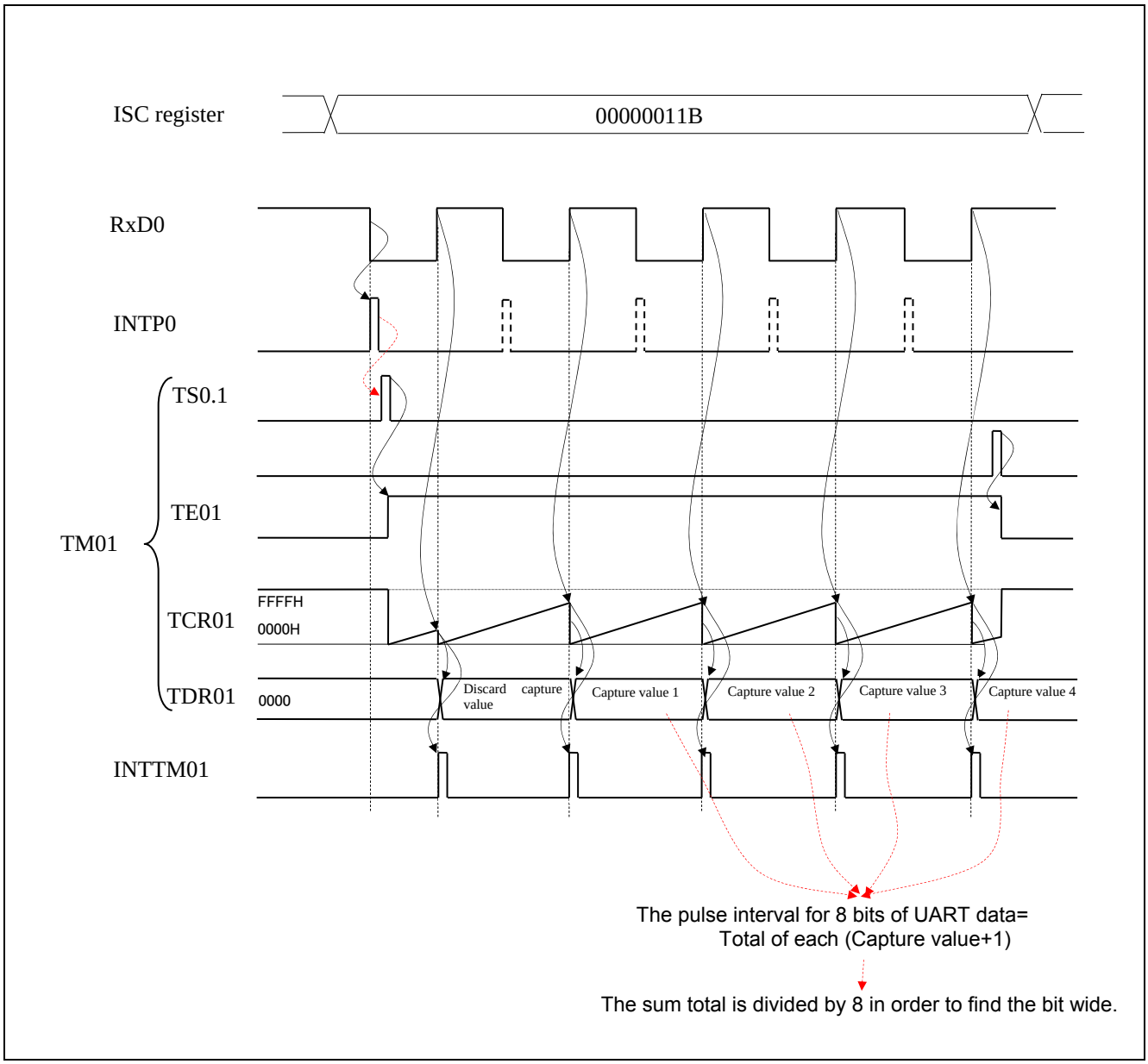

Figure 1.2 Timing Chart of Baud Rate Measurement

As shown in Figure 1.2, calculates the communication partner's baud rate (bit width of UART data) from four capture values of TM01.

Next, adjusts the baud rate of RL78/G10. Sets up the baud rate of RL78/G10 by "dividing of a SPS register", and "dividing of upper 7-bit (SDR0nH) of SDR register." Since SDR0nH can do dividing to a maximum of 256, SPS0 register is specified from the computed result so that it may become the maximum and not greater than 256.

In this application note, subtracts 1 from the value which was made 256 or less in order to make LSB (least significant byte) 0, since the error of the value stored in a SDR0nH [7:1] register is made as small as possible.
(A value of SDR0nH [7:1] register is calculated like that 1 is added to a value which is less than or equal to 256, and it is divided by 2 and subtracted 1.)

Figure 1.3 shows this calculation by actual program. SPSDATA is a variable which stores the value set as SPS0 register. DIVDATA is a variable which stores the value set as SDR0nH.

```
        CLRB    SPSDATA             ; set start data
SHIFTLOOP:
        CMPW    AX、    #0x0101     ; check divide ratio
        BC      $SHIFTEND           ; branch if LT 257
        INC     SPSDATA             ; count up SPS data
        SHRW    AX、    1           ; 1/2
        BR      $SHIFTLOOP          ; continue

SHIFTEND:
        DECW    AX                  ; adjust
        MOV     A、     #0b11111110 ; get 7bits
        AND     A、     X
        MOV     DIVDATA、    A      ; set SDRH data
```

Confirms it has become 256 or less.

If it is not 256 or less, divides it into halves and adds 1 to SPS0 setup value.

The setup value of a SDR register is computed by rounding off.

Figure 1.3 Baud Rate Adjustment Program

2. Operation Check Conditions

The sample code described in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G10 (R5F10Y16)
Operating frequency	High-speed on-chip oscillator (HOCO) clock: 20 MHz CPU/peripheral hardware clock: 20 MHz
Operating voltage	5.0 V (can run on a voltage range of 2.9 V to 5.5 V.) SPOR operating voltage: Rising edge voltage: 2.90V : Falling edge voltage: 2.84V
Integrated development environment (CS+)	CS+ for CC V3.01.00 from Renesas Electronics Corp.
Assembler (CS+)	CC-RL V1.01.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V4.0.2.008 from Renesas Electronics Corp.
Assembler (e^2 studio)	CC-RL V1.01.00 from Renesas Electronics Corp.
Board to be used	RL78/G10 target board (QB-R5F10Y16-TB)

3. Related Application Notes

The application notes related to this application note are listed below for reference.

・ RL78/G10 Initialization (R01AN2668E) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of hardware configuration that is used for this application note.

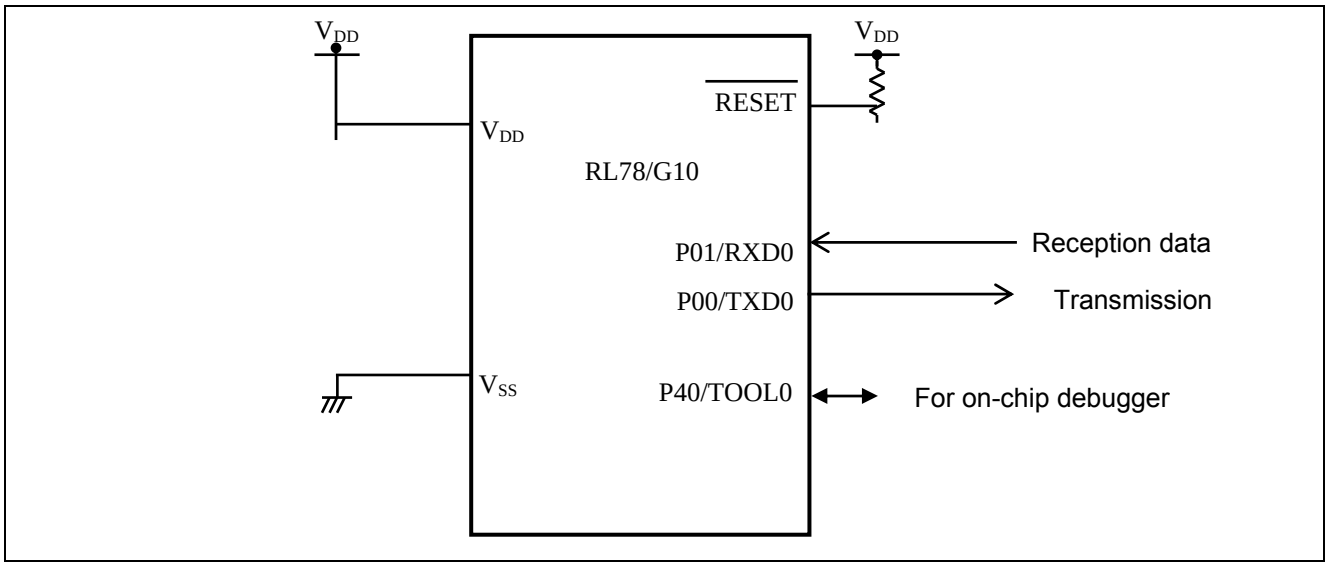

Figure 4.1 Hardware Configuration

Caution: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met. Refer to "2.3 Connection of Unused Pins" of RL78/G14 User's Manual: Hardware (R01UH0384E) for more information about connection of unused pins.

2. V_{DD} must supply not lower than the reset release voltage (V_{SPOR}) that is specified as SPOR.

4.2 List of Pins to be Used

Table 4.1 lists the pins to be used and their function.

Table 4.1 Pins to be Used and their Function

Pin Name	I/O	Description
P01/RXD0	**Input**	Input port for serial receiving data. The following input ports are made to serve a double purpose by an ISC register. ・ISC1=1: Input port of TI01. ・ISC0=1: Input port of INTP0.
P00/TXD0	**Output**	Output port for serial transmission data.

5. Description of the Software

5.1 Operation Outline

The input switch control register (ISC) is set up in order to input the input signal of RxD0 pin into INTP0 and TM01. Waits for the start bit (falling edge) of the data 55H from a communication partner by the falling edge detection function of INTP0. If a start bit is detected, sets the channel 1 (TM01) of TAU as the pulse interval measurement function, and measures the rising edge interval of an input signal 4 times. Calculates the communication partner's baud rate (bit width of UART data) from the sum total of the capture value for 4 times. From the result, sets SPS0 register and a SDR0nH register, and correct the baud rate of RL78/G10.

Notifies a communication partner of completion of communication preparation that the channel 0 and the channel 1 of SAU0 are set as UART mode (with 8 bits, the LSB first, and no parity), and the data 55H is transmitted from TXD0 pin.

(1) Initializes TAU.

<Setting conditions>

- Sets P00/TXD0 pin and P01/RXD0 pin as input.
- Sets the prescaler as CK00: f_{CLK}.
- Sets TM01as the input pulse interval measurement.
- Selects CK00 as a count clock.
  Selects the input edge of TI01 pin as rising edge detection.
  Sets the output of TI00 as disable.

Note: If the baud rate is 1200bps or less, please select LOWRANGE. Correction is made by using CK01:f_{CLK}/128 and adding 7 to the setup value of SPS0 register.

(2) Sets INTP0 to the falling edge detection.

(3) Connects input signal of RXD0 pin to INTP0 and TI01 by ISC register.

(4) Sets the number of times of a capture of TM01 to 5 times.
Enables INTP0 interrupt, and waits for capture completion.

(5) If the start bit of the data 55H is detected by INTP0 interruption, initializes the capture accumulation variable of TM01. Disables INTP0 interruption, starts TM01 and waits for the first INTTM01 generating.

(6) At the first INTTM01 interrupt occurrence, cancels a capture value (for an unfixed value).

(7) Adds captured value 1 to 3 that are obtained by interruption occurrence of the 2nd to 4th time to the accumulation variable of a capture.
Counts down the number of times of a capture and returns.

(8) If the INTTM01 interruption is occurred, makes INTTM00 interruption disable. Adds captured value 4 to the accumulation variable of a capture, and counts down the number of times of capture

(9) Calculates a baud rate from the communication partner's baud rate, and stores the setup value to SPS0 register and SDR0nH register to a variable. Returns from interruption and initializes UART0.

(10) Baud rate correction of RL78/G10 is completed. Transmits 55H to a communication partner.

5.2 List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

Table 5.1 Option Byte Settings

Address	Value	Description
000C0H	11101110B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H	11110111B	Uses P125/RESET pin as RESET input. SPOR detection voltage : Rising edge voltage: 2.90V (typ.) : Falling edge voltage: 2.84V (typ.)
000C2H	11111001B	HOCO: 20MHz
000C3H	10000101B	Enables the on-chip debugger.

5.3 List of Constants

Table 5.2 lists the constants that are used in this sample program.

Table 5.2 Constants for the Sample Program

Constant	Setting	Description
CLKFREQ	**20000**	Expressed fCLK per kHz
CTXMODETxH	**10000000B**	Setting value of SCR00H for transmission
CRXMODERxH	**01000000B**	Setting value of SCR01H for reception
CTRXMODEL	**10010111B**	Setting value of SCR00L and SCR01L
CSMRDATATxH	**00000000B**	Setting value of SMR00H for transmission
CSMRDATARxH	**00000001B**	Setting value of SMR01H for reception
CSMRDATATxL	**00100010B**	Setting value of SMR00L and SMR01L

5.4 List of Variables

Table 5.3 lists variables used by this sample program.

Table 5.3 Variables used for this Sample Program

Variable Name	Outline
capturel	The variable for accumulation of a capture value (lower 16-bit)
captureh	The variable for accumulation of a capture value (upper 8-bit)
spsdata	Stores setup value for SPS0 register
divdata	Stores setup value for SDR0nH register
lpcount	For the number-of-times count of a capture
rxdatabuf	The buffer for received-data storing
rxstatus	Receiving status (00: Receiving successful end, 01 to 07: Receiving error, 80H: No receiving data)
txstatus	Transmission status (00: Complete of transmission)

5.5 List of Functions (Subroutines)

Table 5.4 lists the functions (subroutines).

Table 5.4 Functions (Subroutines)

Function Name	Outline
SINIUART0	Initialization of UART0
STARTUART0	Enabling of UART0
STOPUART0	Disabling of UART0
STxDATAST	Transmission starting of 1 character
STxDATA	Transmission & Wait for transmission complete of 1 character
STxWAIT	Wait for transmission complete of 1 character
SRxDATA	Receiving of 1 character
IINTSR0	Receiving end interrupt
IINTST0	Transfer end interrupt
IINTP0	INTP0 interrupt processing
INTTM01	TM01 capture end interrupt

5.6 Function Specifications (Subroutines)

This section describes the specifications for the functions (subroutines) that are used in this sample program.

[Function Name] SINIUART0

Outline	Initialization of UART0
Explanation	Initializes UART0 according to the communication partner's baud rate.
Arguments	None（spsdata、divdata）
Return value	None
Remarks	None

[Function Name] STARTUART0

Outline	Enabling of UART0
Explanation	Enables UART0 operation and interruption. Sets receiving status (rxstatus) to busy (80H).
Arguments	None
Return value	None
Remarks	None

[Function Name] STOPUART0

Outline	Disabling of UART0
Explanation	Disables UART0 operation and interruption.
Arguments	None
Return value	None
Remarks	None

[Function Name] STxDATAST

Outline	Transmission from UART0 starting
Explanation	Waits for that BFF00 bit becomes 0, and starts transmission by writing data of A register into TXD0 register.
Arguments	A register : Transmit data
Return value	None
Remarks	Sets the bit 7 of transmission status.

[Function Name] STxDATA

Outline	Transmission of UART0
Explanation	Waits for that BFF00 bit becomes 0, starts transmission by writing data of A register into TXD0 register, and waits for the end of transmission.
Arguments	A register : Transmit data
Return value	None
Remarks	The transmission status becomes 00.

[Function Name] STxWAIT

Outline	Wait for transmission complete of UART0
Explanation	Waits for the transmission status becomes 00.
Arguments	None
Return value	None
Remarks	None

[Function Name] SRxDATA

Outline	Wait for receiving complete of UART0
Explanation	Stores received data to A register.
Arguments	None
Return value	A register : Receive data
Remarks	Makes the receiving status (rxstatus) busy (80H).

[Function Name] IINTSR0

Outline	Receiving end interrupt
Explanation	Be activated by INTSR0 interrupt. If the buffer for received-data storing already has data, sets overrun error to the value of SSR01 register, and sets receiving status. If the reception is end normally, sets the receiving status to 00 and stores received data in the buffer for received-data storing.
Arguments	None
Return value	None (rxstatus: Receiving status, rxdatabuf: Normal received data).
Remarks	None

[Function Name] IINTST0

Outline	Transfer end interrupt of UART0
Explanation	Be activated by INTST0 interrupt, and sets the transmission status to 00.
Arguments	None
Return value	None
Remarks	None

[Function Name] IINTP0

Outline	INTP0 interrupt processing
Explanation	Be activated at the leading edge (falling) of start bit. Performs a baud rate measurement setup, and enables operation of TM01. Disables INTP0 interrupt.
Arguments	None
Return value	None
Remarks	None

[Function Name] IINTTM01

Outline	INTTM01 interrupt processing
Explanation	Be activated at the rising edge of RXD0 pin, and performs processing according to the number of times of interruption. 1st time: Counts down the number of times of capture (lpcount). 2nd to 4th times: Adds a capture value to the variable for accumulation. 5th time: Adds a capture value to the variable for accumulation, and stops TM01. Calculates the setup value to SPS0 register and the setup value to SDR0nH register from an accumulation value, and stores in a variable.
Arguments	None
Return value	None
Remarks	Stores the setup value to SPS0 register in Variable spsdata, and the setup value to a SDR0nH register in divdata.

5.7 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

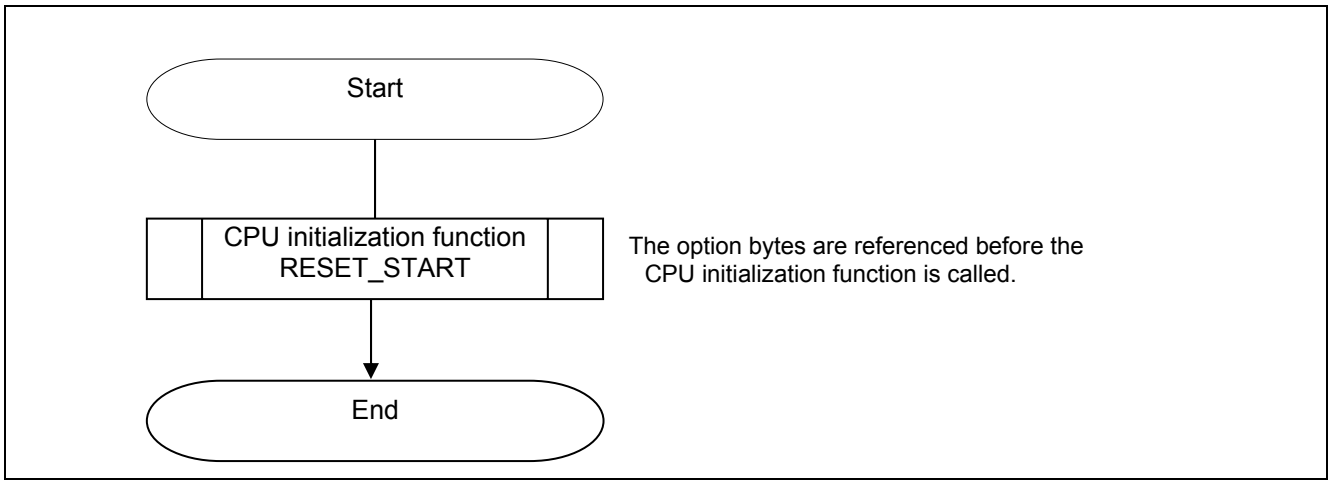

Figure 5.1 Overall Flow

5.7.1 CPU Initialization Function

Figure 5.2 shows the flowchart for the CPU initialization function.

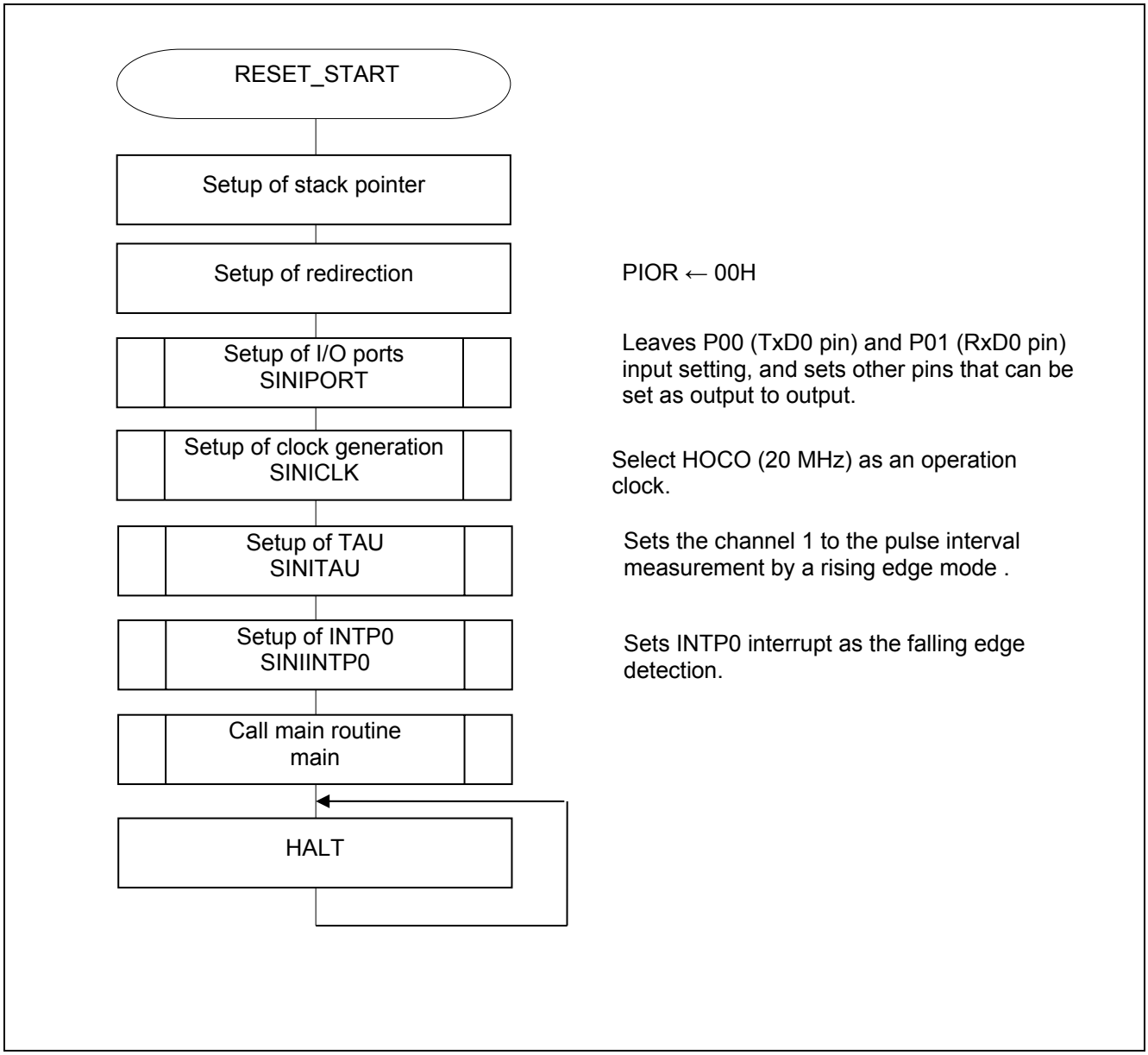

Figure 5.2 CPU Initialization Function

5.7.2 I/O Port Setup

Figure 5.3 shows the flowchart for setting up the I/O ports.

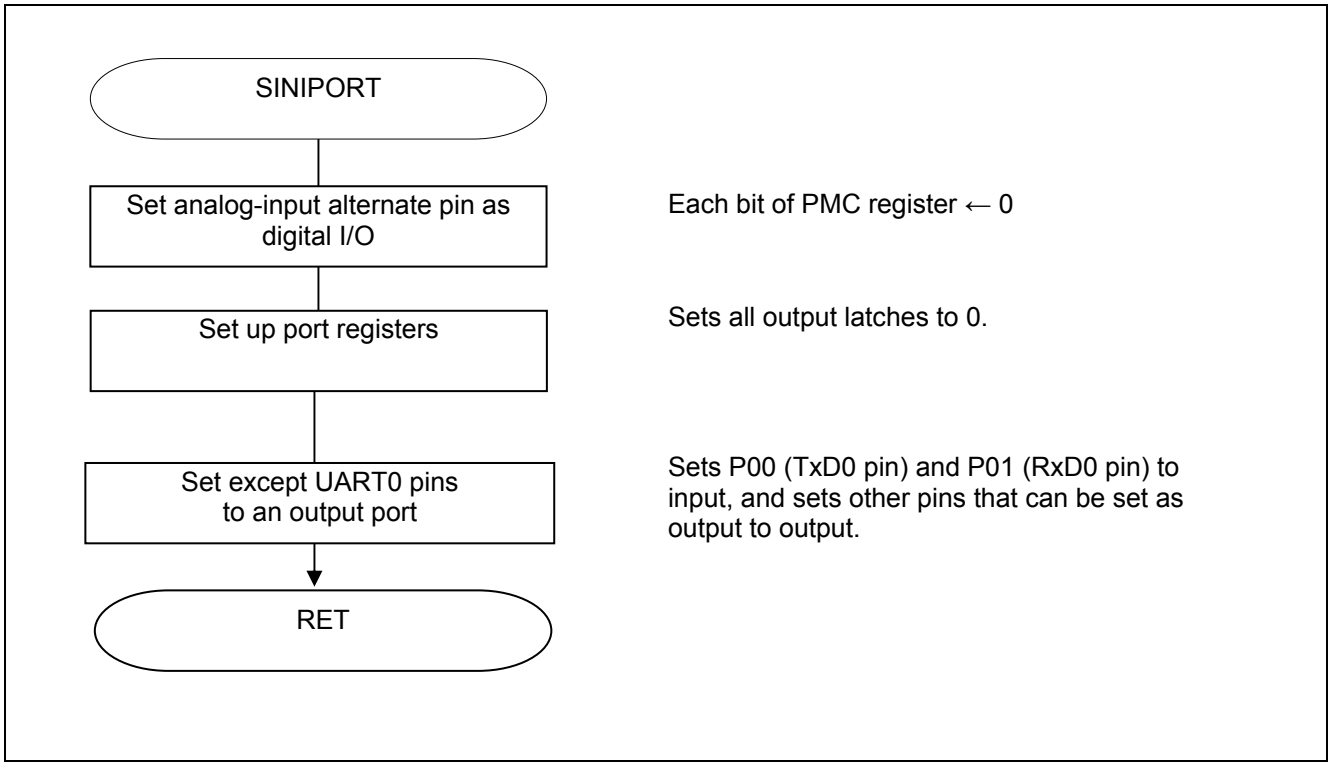

Figure 5.3 I/O Port Setup

Note: Provide proper treatment for unused pins so that their electrical specifications are observed. Refer to RL78/G10 User's Manual: Hardware “2.3 Connection of Unused Pins” for the unused pins processing.

UART0 pin setting

- Port mode register (PM0)

I/O mode of PM00 select

Symbol: PM0

7	6	5	4	3	2	1	0
PM07 Note	PM06 Note	PM05 Note	PM04	PM03	PM02	PM01	PM00
0/1	**0/1**	**0/1**	**0**	**0**	**0**	**1**	**1**

Note: 16-pin products only.

Bit 1

PM01	PM01 input mode selection
0	Output mode (output buffer on)
1	**Input mode (output buffer off)**

Bit 0

PM00	PM00 output mode selection
0	Output mode (output buffer on)
1	**Input mode (output buffer off)**

Note: Refer to RL78/G10 User's Manual: Hardware for more information about the way to set up registers.

5.7.3 Clock Generation Circuit Setup

Figure 5.4 shows the flowchart for clock generation circuit setup.

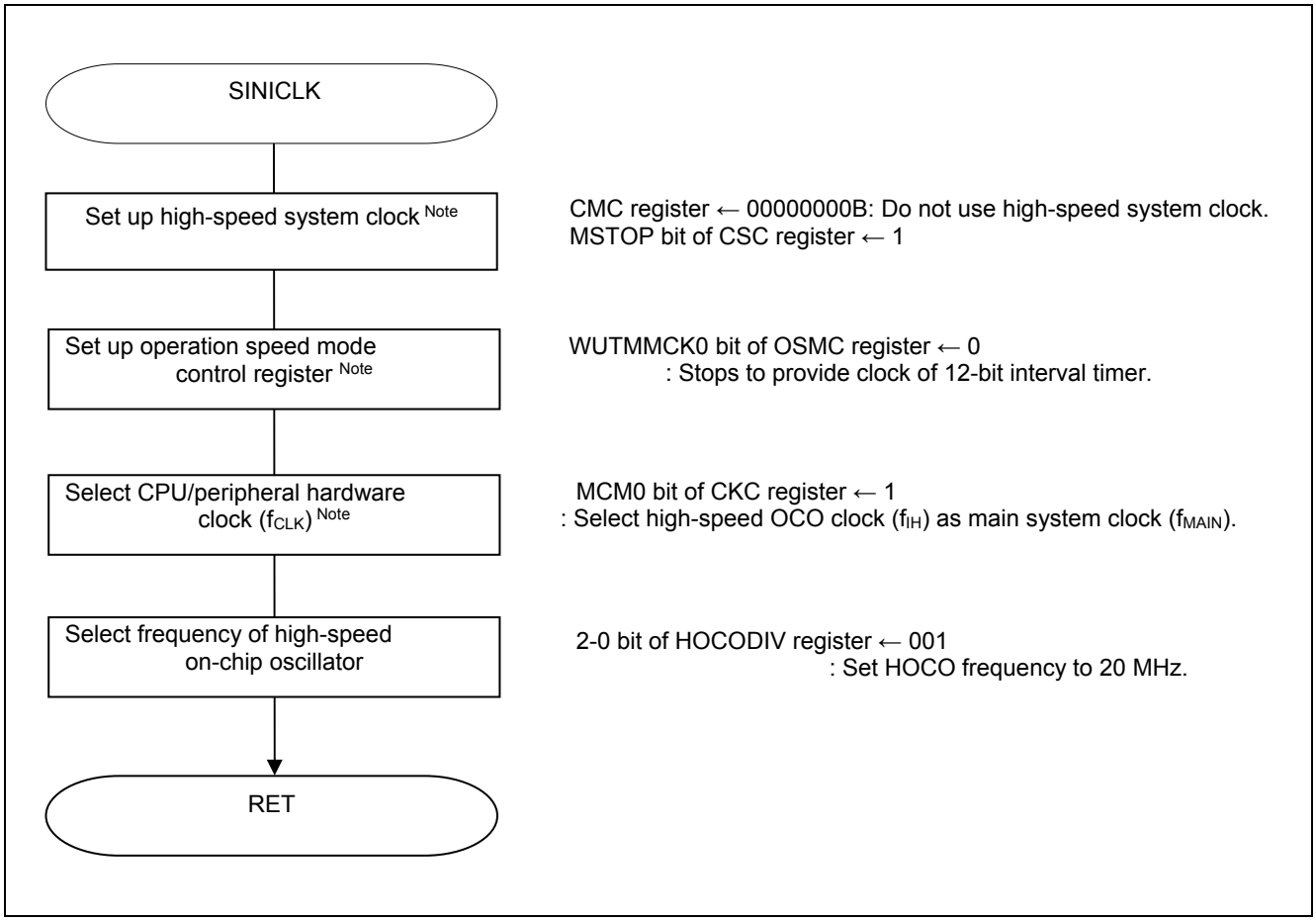

Figure 5.4 Clock Generation Circuit Setup

Note: Set CMC, CKC, CSC, and OSMC register only to 16 pin products. As for10 pin products, the setup of these registers is unnecessary.

Refer to RL78/G10 Initialization (R01AN2668E) Application note “Flowcharts” for CPU clock setup (SINICLK).

5.7.4 Setup of Timer Array Unit

Figure 5.5 shows the flowchart of timer array unit setup.

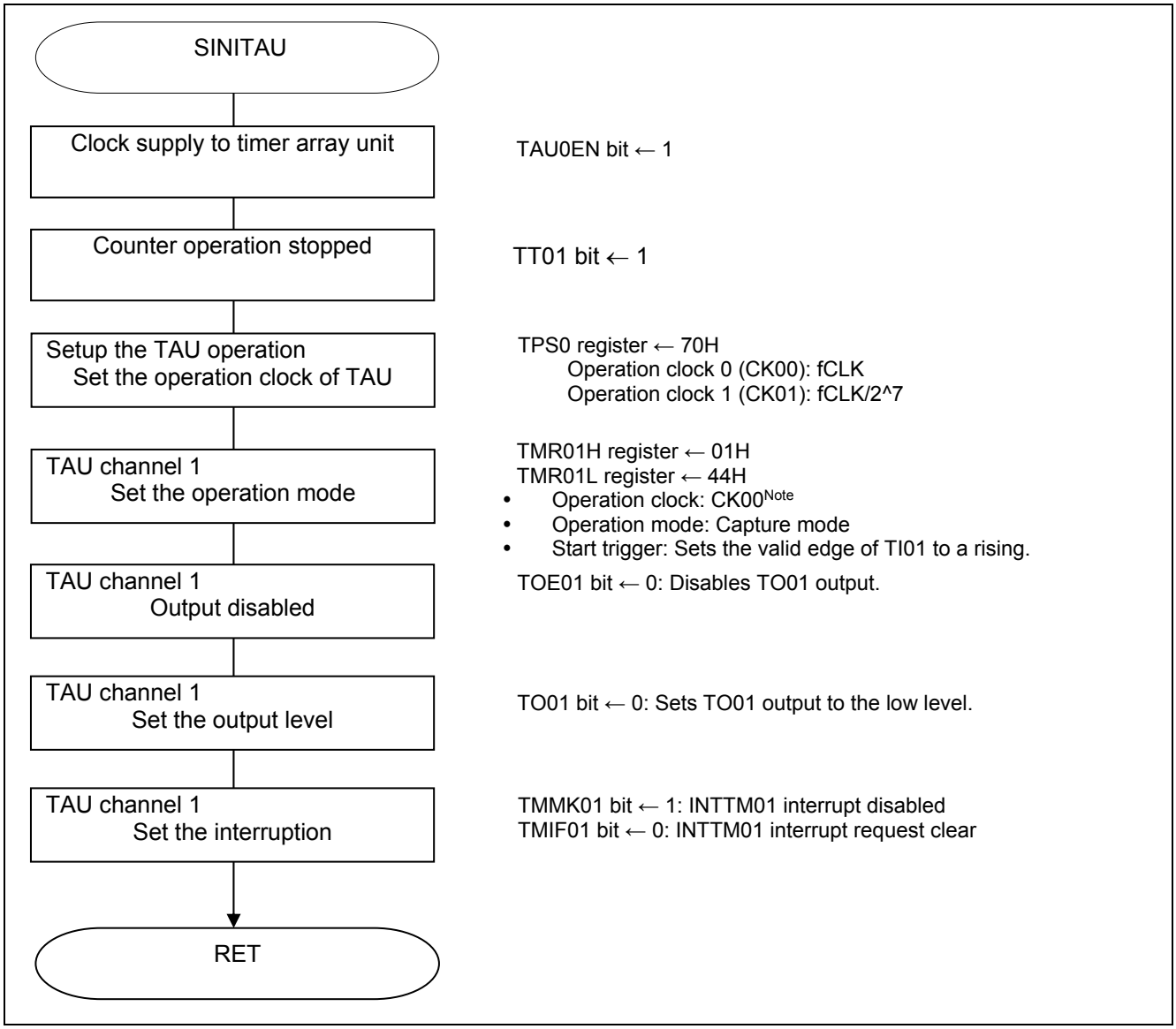

Figure 5.5 Setup of Timer Array Unit

Note: When a baud rate is 1200 bps or less, CK01:fCLK/2^7 are chosen.

In addition, the program of LOWRANGE is used.

Starting clock supply to the timer array unit 0

・Peripheral enable register 0 (PER0)

Starts clock supply to the timer array unit 0.

Symbol: PER0

7	6	5	4	3	2	1	0
TMKAEN[Note]	CMPEN[Note]	ADCEN	IICA0EN[Note]	0	SAU0EN	0	TAU0EN
x	x	x	x	0	x	0	**1**

Bit 0

TAU0EN	Supplies input clock.
0	Stops supply of input clock.
1	Supplies input clock.

Note 16-pin products only.

Setup of the timer clock frequency

・Timer clock select register 0 (TPS0)

Selects the operation clock of timer array unit 0.

Symbol: TPS0

7	6	5	4	3	2	1	0
PRS013	PRS012	PRS011	PRS010	PRS003	PRS002	PRS001	PRS000
0	**1**	**1**	**1**	**0**	**0**	**0**	**0**

Bit 7 - 4, 3 - 0

PRS003	PRS002	PRS001	PRS000	Selection of operation clock (CK00)					
					f_{CLK}= 1.25MHz	f_{CLK}= 2.5MHz	f_{CLK}= 5MHz	f_{CLK}= 10MHz	f_{CLK}= 20MHz
0	**0**	**0**	**0**	**f_{CLK}**	1.25 MHz	2.5 MHz	5 MHz	10 MHz	**20 MHz**
0	0	0	1	$f_{CLK}/2$	625 kHz	1.25 MHz	2.5 MHz	5 MHz	10 MHz
0	0	1	0	$f_{CLK}/2^2$	312.5 kHz	625 kHz	1.25 MHz	2.5 MHz	5 MHz
0	0	1	1	$f_{CLK}/2^3$	156.2 kHz	312.5 kHz	625 kHz	1.25 MHz	2.5 MHz
0	1	0	0	$f_{CLK}/2^4$	78.1 kHz	156.2 kHz	312.5 kHz	625 kHz	1.25 MHz
0	1	0	1	$f_{CLK}/2^5$	39.1 kHz	78.1 kHz	156.2 kHz	312.5 kHz	625 kHz
0	1	1	0	$f_{CLK}/2^6$	19.5 kHz	39.1 kHz	78.1 kHz	156.2 kHz	312.5 kHz
0	**1**	**1**	**1**	**$f_{CLK}/2^7$**	9.76 kHz	19.5 kHz	39.1 kHz	78.1 kHz	**156.2 kHz**
1	0	0	0	$f_{CLK}/2^8$	4.88 kHz	9.76 kHz	19.5 kHz	39.1 kHz	78.1 kHz
1	0	0	1	$f_{CLK}/2^9$	2.44 kHz	4.88 kHz	9.76 kHz	19.5 kHz	39.1 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.22 kHz	2.44 kHz	4.88 kHz	9.76 kHz	19.5 kHz
1	0	1	1	$f_{CLK}/2^{11}$	610 Hz	1.22 kHz	2.44 kHz	4.88 kHz	9.76 kHz
1	1	0	0	$f_{CLK}/2^{12}$	305 Hz	610 Hz	1.22 kHz	2.44 kHz	4.88 kHz
1	1	0	1	$f_{CLK}/2^{13}$	153 Hz	305 Hz	610 Hz	1.22 kHz	2.44 kHz
1	1	1	0	$f_{CLK}/2^{14}$	78Hz	153 Hz	305 Hz	610 Hz	1.22 kHz
1	1	1	1	$f_{CLK}/2^{15}$	39Hz	78Hz	153 Hz	305 Hz	610 Hz

Note: For details on the procedure for setting up the registers, refer to RL78/G10 User's Manual: Hardware.

Setup of channel 0 operation mode

- Timer mode register 01 (TMR01H, TMR01L)
  Selection of the operation clock (f_{MCK}).
  Selection of the count clock.
  Selection of the 16 or 8-bit timer.
  Specifying the start trigger and capture trigger.
  Selection of the valid edge of the timer input.
  Setting of the operation mode.

Symbol: TMR01H

7	6	5	4	3	2	1	0
CKS011	0	0	CCS01	SPLIT01	STS012	STS011	STS010
0Note	0	0	**0**	**0**	**0**	**0**	**1**

Note: Sets 1 when carrying out UART communication by less than baud rate 1200bps.

Bit 7

CKS011	Selection of operation clock (f_{MCK}) of channel 1
0	**Operation clock CK00 set by timer clock select register 0 (TPS0)**
1	Operation clock CK01 set by timer clock select register 0 (TPS0)

Bit 4

CCS01	Selection of count clock (f_{TCLK}) of channel 1
0	**Operation clock (f_{MCK}) specified by the CKS011 bit**
1	Valid edge of input signal from the TI0n pin

Bit 3

SPLIT01	Selection of 8-bit timer/16-bit timer operation of channel 1
0	**Operation as 16-bit timer**
1	Operation as 8-bit timer

Bit 2 - 0

STS012	STS011	STS010	Setting of start trigger or capture trigger of channel 1
0	0	0	Only software trigger start is valid (other trigger sources are unselected)
0	**0**	**1**	**Valid edge of the TI01 pin input is used as the start trigger and capture trigger**
0	1	0	Both the edges of the TI01 pin input are used as a start trigger and a capture trigger.
1	0	0	When the channel is used as a slave channel with the one-shot pulse output,PWM output function,or multiple PWM output function: The interrupt request signal of the master channel is used (at the time of the slave channel of two or more channel linkage operation function）.
1	1	0	When the channel is used as a slave channel in two-channel input with one-shot pulse output function: The interrupt request signal of the master channel (INTTM0n) is used as the start trigger. A valid edge of the TI03 pin input of the slave channel is used as the end trigger.
Other than above			Setting prohibited

Note: Refer to **"**RL78/G10 User's Manual: Hardware" for the setup of the register.

Symbol: TMR01L

7	6	5	4	3	2	1	0
CIS011	CIS010	0	0	MD013	MD012	MD011	MD010
0	**1**	0	0	**0**	**1**	**0**	**0**

Bit 7 - 6

CIS011	CIS010	Selection of TI01 pin input valid edge
0	0	Falling edge
0	**1**	**Rising edge**
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge

Bit 3 - 1

MD 013	MD 012	MD 011	MD 010	Setting of operation mode of channel 1	Corresponding function	Count operation of TCR
0	**0**	**0**	1/**0**	Interval timer mode	Interval timer/Square wave output/Divider function/PWM output (master)	Down count
0	**1**	**0**	1/**0**	**Capture mode**	**Input pulse interval measurement**	**Up count**
0	1	1	0	Event counter mode	External event counter	Down count
1	0	0	1/**0**	One-count mode	Delay counter/One-shot pulse output/PWM output (slave)	Down count
1	1	0	0	Capture & one-count mode	Measurement of high/low-level width of input signal	Up count
Other than above				Setting prohibited		

Note: Refer to **"**RL78/G10 User's Manual: Hardware" for the setup of the register.

Setup of output value of timer output pin

・Timer output register 0 (TO0)

Sets the output value of timer output pin of each channel.

Symbol: TO0

7	6	5	4	3	2	1	0
0	0	0	0	TO03Note	TO02Note	TO01	TO00
x	x	x	x	x	x	**0**	x

Note: 16-pin products only.

Bit 0

TO01	Timer output of channel 1
0	**Timer output value is “0”.**
1	Timer output value is “1”.

Setup of disabling timer output

・Timer output enable register 0 (TOE0)

Sets enabling/disabling timer output of each channel.

Symbol: TOE0

7	6	5	4	3	2	1	0
0	0	0	0	TOE03Note	TOE02Note	TOE01	TOE00
0	0	0	0	x	x	**0**	x

Note: 16-pin products only.

Bit 0

TOE01	Timer output enable/disable of channel 0
0	**Stops TO01 output (timer channel output) operation by count operation.** **The writing to TO01 bits of TO0 register is enabled, and the output level of TO01 pin is able to be controlled by software.** **The output level which is set to TO01 bit is outputted from TO01 pin.**
1	Enables operation of TO01 output (timer channel output) by count operation. Disables writing to TO01 bit (writing is disregarded). The output level of TO01 pin is set/reset by count operation of a timer.

Note: Refer to **“**RL78/G10 User's Manual: Hardware” for the setup of the register.

Setup of the timer capture completion interrupt

- Interrupt request flag register (IF0H)
  Clears the interrupt request flag.
- Interrupt mask flag registers (MK0H)
  Sets the interrupt mask.

Symbol: IF0L

7	6	5	4	3	2	1	0
0	0	0	0	0	KRIF	ADIF	TMIF01
0	0	0	0	0	x	x	**0**

Bit 0

TMIF01	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK0H

7	6	5	4	3	2	1	0
1	1	1	1	1	KRMK	ADMK	TMMK01
1	1	1	1	1	x	x	**1**

Bit 0

TMMK01	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Note: Refer to **"**RL78/G10 User's Manual: Hardware" for the setup of the register.

5.7.5 Main Processing

Figure 5.6 shows the flowchart of main processing.

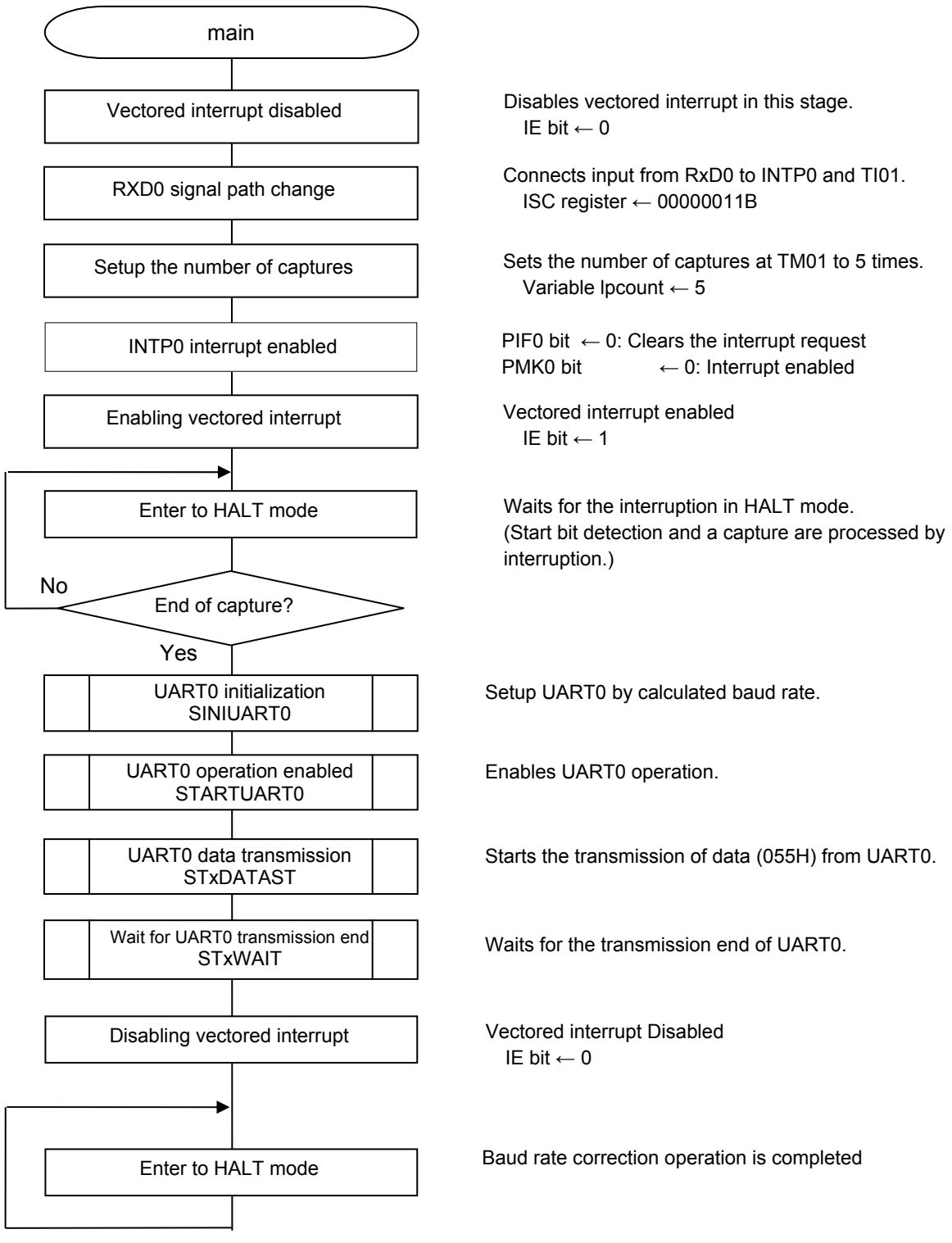

Figure 5.6 Main Processing

Setup of RxD0 signal path

- Input Switch Control Register (ISC)

Connects RxD0 input to INTP0 and TI01.

Symbol: ISC

7	6	5	4	3	2	1	0
0	0	0	0	0	0	ISC1	ISC0
0	0	0	0	0	0	**1**	**1**

Bit 1

ISC1	Switching channel 1 input of timer array unit
0	Uses the input signal of the TI01 pin as a timer input (normal operation).
1	Uses the input signal of the RxD0 pin as a timer input (measures the pulse width for baud rate correction).

Bit 0

ISC0	Switching external interrupt (INTP0) input
0	Uses the input signal of the INTP0 pin as an external interrupt (normal operation).
1	Uses the input signal of the RxD0 pin as an external interrupt (wakeup signal detection: start bit falling edge detection)

Note: Refer to **"**RL78/G10 User's Manual: Hardware" for the setup of the register.

Setup of INTP0 interrupt

- Interrupt request flag register (IF0L)

Clears interrupt request flag.

- Interrupt mask flag register (MK0L)

Releases interrupt mask.

Symbol: IF0L

7	6	5	4	3	2	1	0
TMIF00	TMIF01H	SREIF0	SRIF0	STIF0 CSIIF00 IICIF00	PIF1	PIF0	WDTIIF
x	x	x	x	x	x	**0**	x

Bit 1

PIF0	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Symbol: MK0L

7	6	5	4	3	2	1	0
TMMK00	TMMK01H	SREMK0	SRMK0	STMK0 CSIMK00 IICMK00	PMK1	PMK0	WDTIMK
x	x	x	x	x	x	**0**	x

Bit 1

PMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Note: Refer to **"**RL78/G10 User's Manual: Hardware" for the setup of the register.

5.7.6 INTP0 Interrupt Processing

Figure 5.7 shows INTP0 interrupt processing.

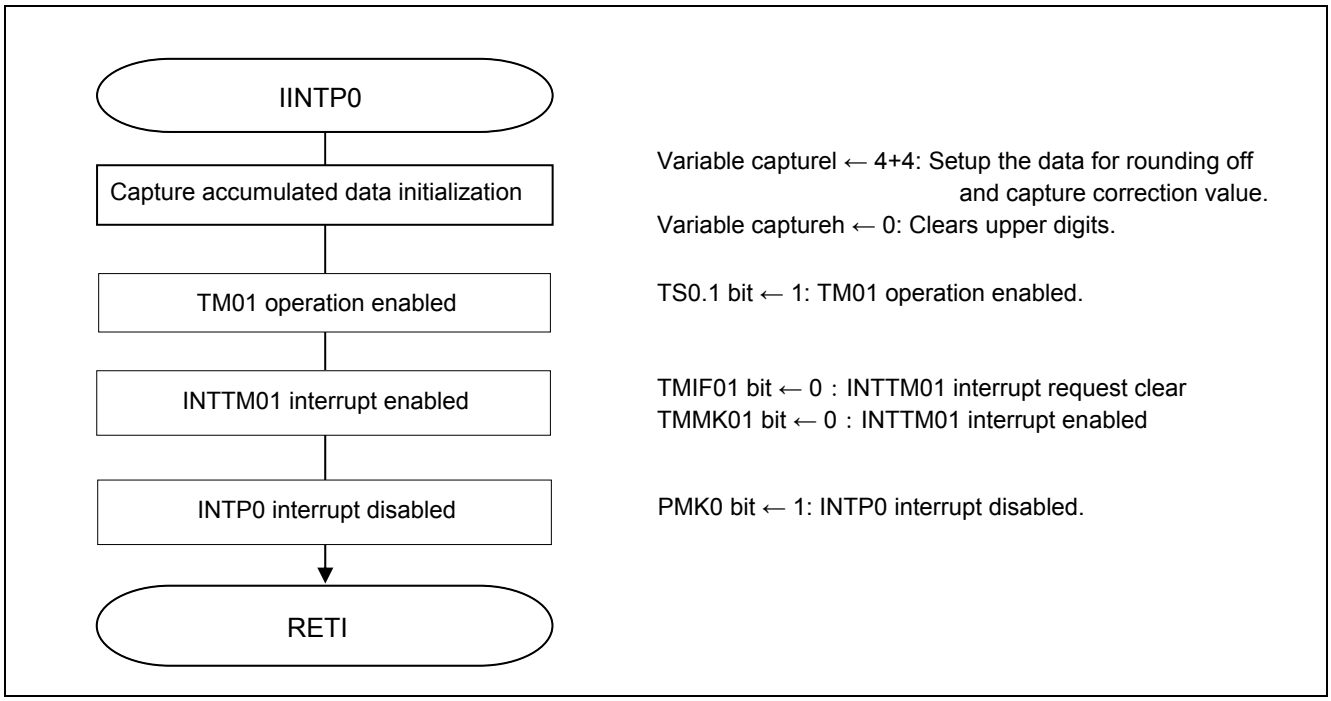

Figure 5.7 NTP0 Interrupt Processing

Setup of timer operation enabled

- Timer channel start register 0 (TS0)
  Count operation of charnel 0 and 1 start setup

Symbol: TS0

7	6	5	4	3	2	1	0
0	0	0	0	TS03[Note]	TS02[Note]	TS01	TS00
0	0	0	0	x	x	**1**	x

Note 16-pin products only.

Bit 1

TS01	Operation enable (start) trigger of channel 1
0	No trigger operation
1	The TE01 bit is set to 1 and the count operation becomes enabled. The TCR01 register count operation start in the count operation enabled state varies depending on each operation mode

Note: Refer to **"**RL78/G10 User's Manual: Hardware" for the setup of the register.

5.7.7 Completion of INTTM01 Capture Interrupt Processing

Figure 5.8 shows the completion of INTTM01 capture interrupt processing.

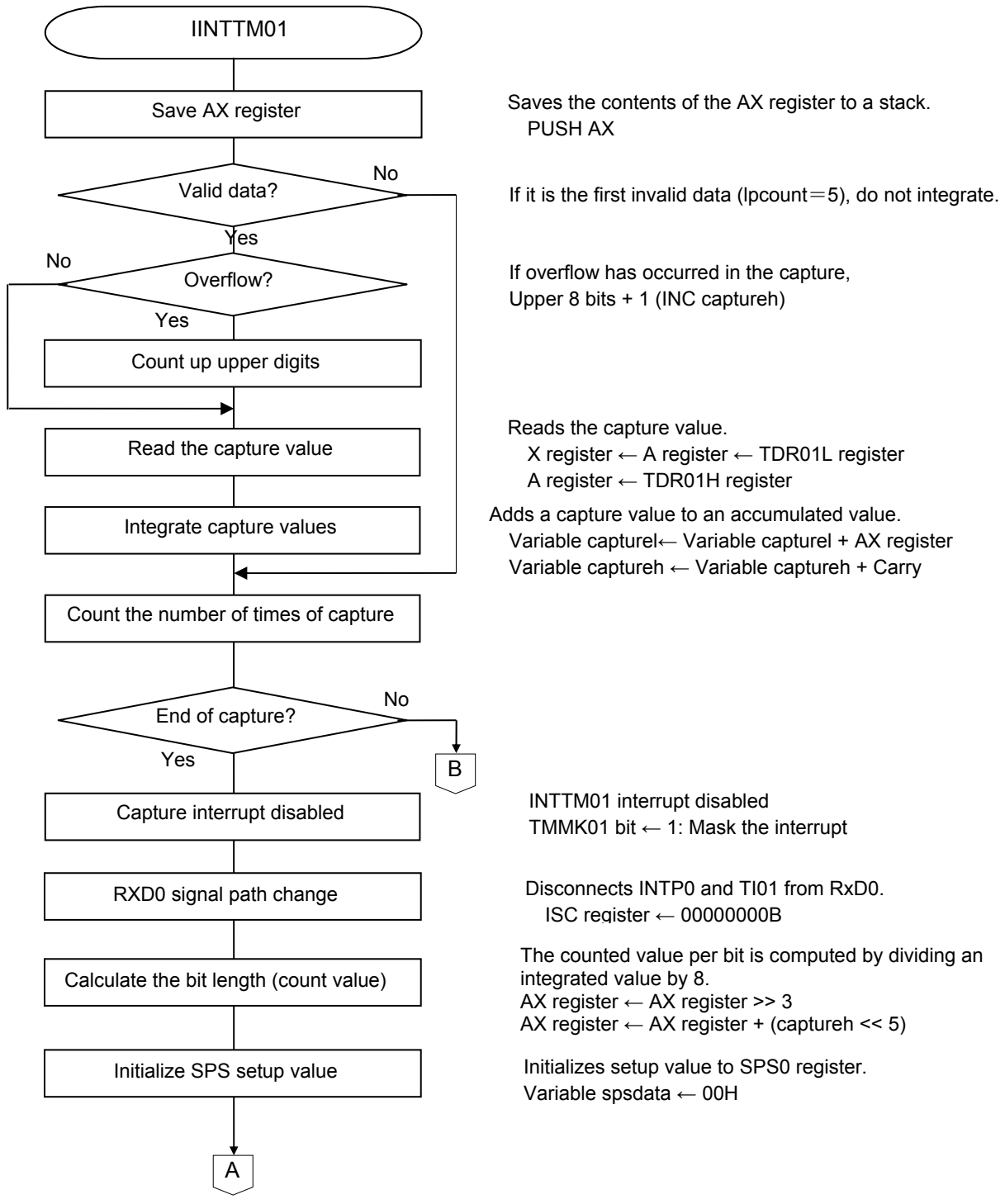

Figure 5.8 Completion of INTTM01 Capture Interrupt Processing (1/2)

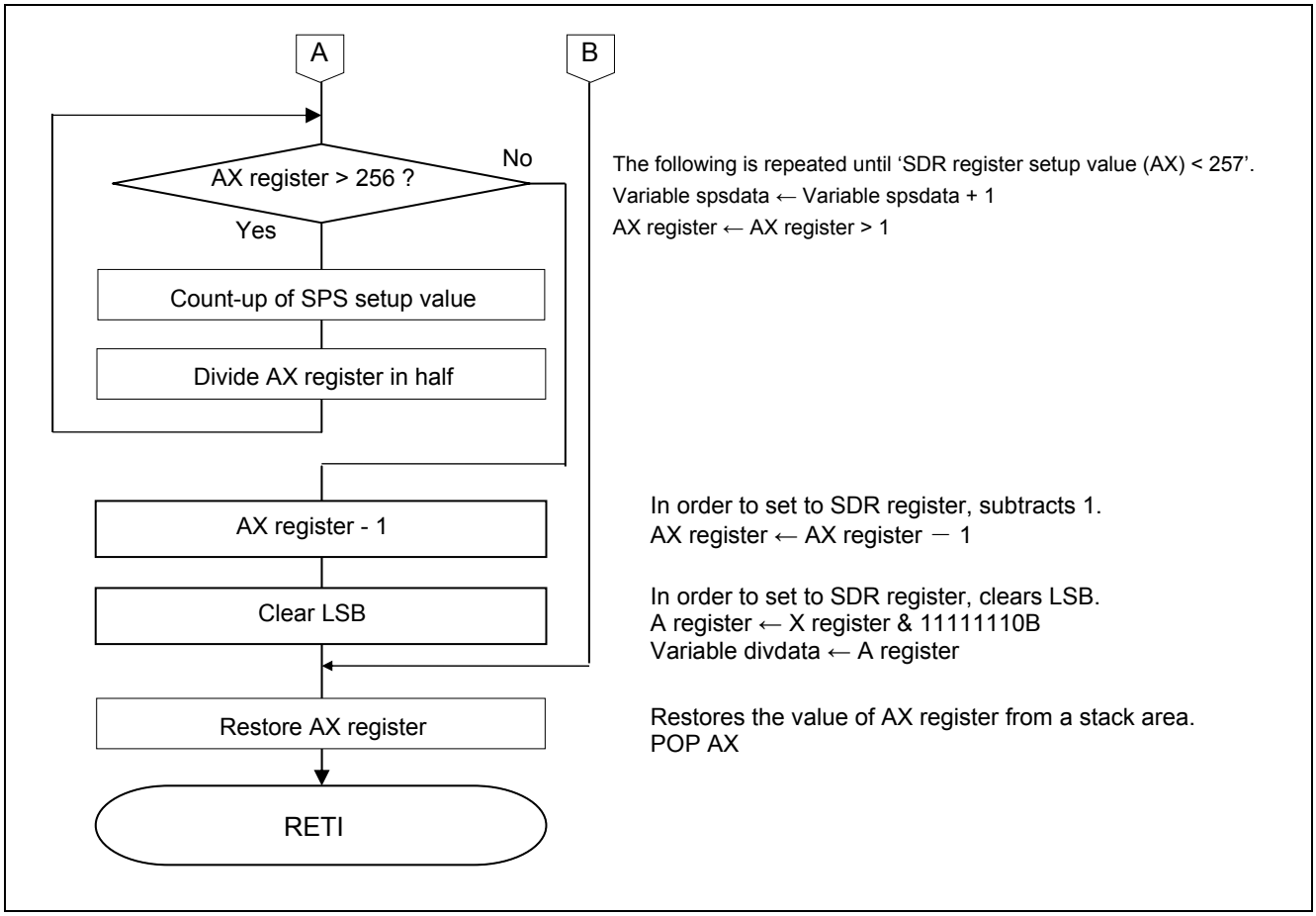

Figure 5.8 Completion of INTTM01 Capture Interrupt Processing (2/2)

5.7.8 Initialization of UART0

Figure 5.9 shows the initialization of UART0.

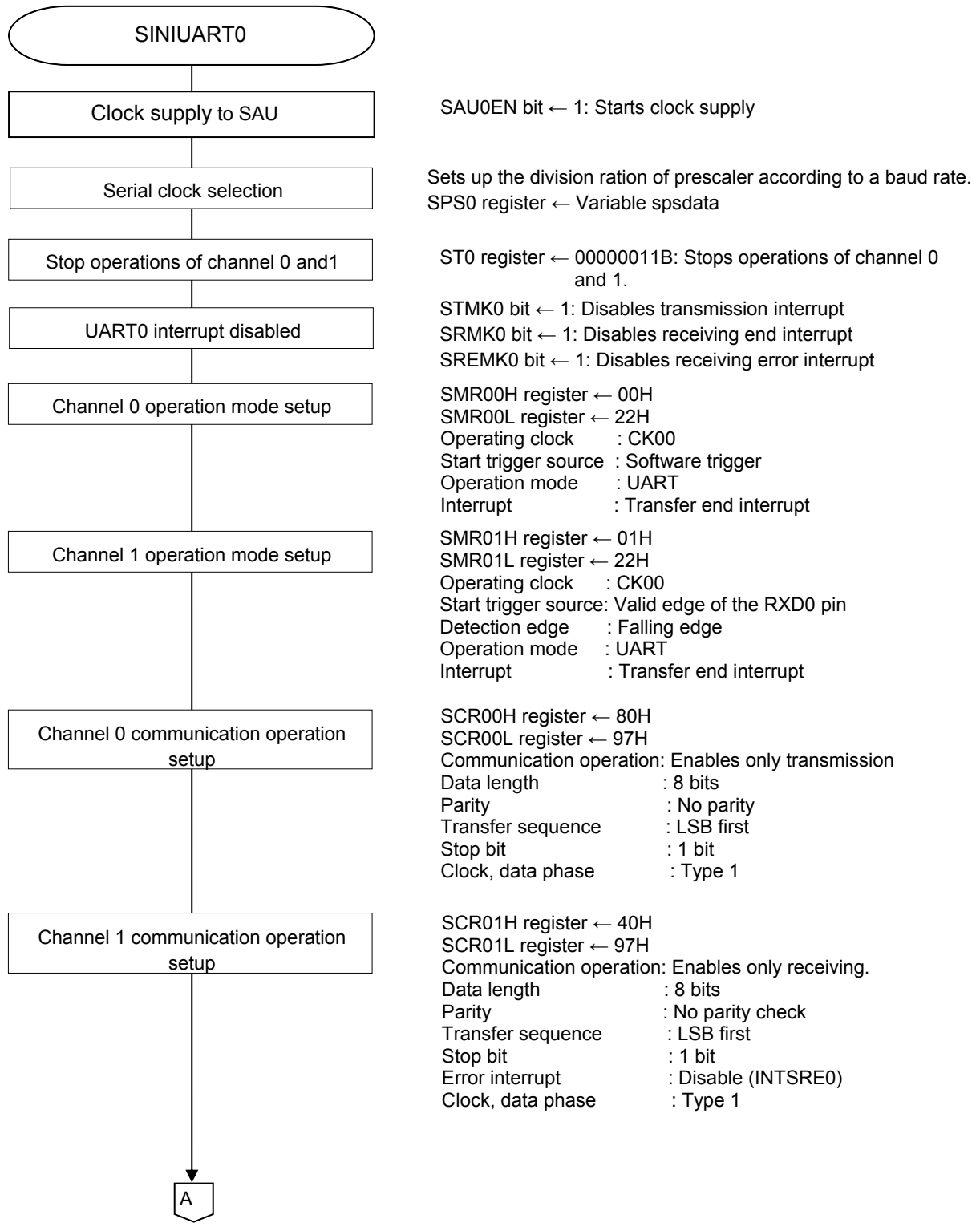

Figure 5.9 Initialization of UART0 (1/2)

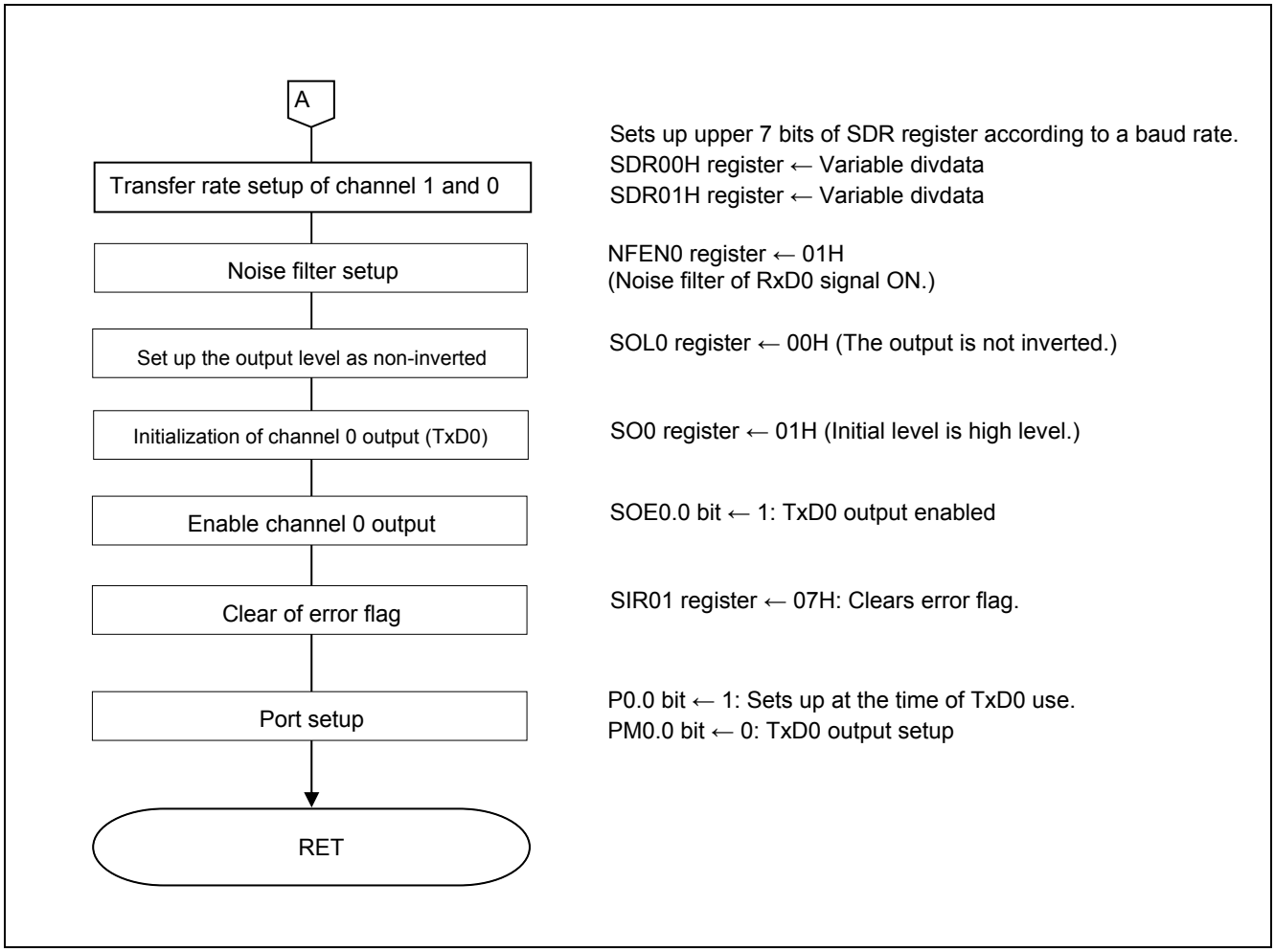

Figure 5.9 Initialization of UART0 (2/2)

Start of supplying clock to the SAU.

- peripheral enable register 0 (PER0)

Clock supply

Symbol: PER0

7	6	5	4	3	2	1	0
TMKAEN	CMPEN	ADCEN	IICA0EN	0	SAU0EN	0	TAU0EN
x	0	x	x	0	**1**	0	x

Bit 2

SAU0EN	Control of serial array unit 0 input clock supply
0	Stops supply of input clock
1	Input clock supply

Serial clock selection.

・Serial clock select register 0 (SPS0)

Operation clock setup.

Symbol: SPS0

7	6	5	4	3	2	1	0
PRS013	PRS012	PRS011	PRS010	PRS003	PRS002	PRS001	PRS000
0	0	0	0	0/1	0/1	0/1	0/1

Bit 3 - 0

PRS 0n3	PRS 0n2	PRS 0n1	PRS 0n0	Selection of operation clock (CKn) (n = 0, 1)					
					f_{CLK} = 1.25MHz	f_{CLK} = 2.5MHz	f_{CLK} = 5MHz	f_{CLK} = 10MHz	f_{CLK} = 20MHz
0	0	0	0	f_{CLK}	1.25 MHz	2.5 MHz	5 MHz	10 MHz	20 MHz
0	0	0	1	$f_{CLK}/2$	625 kHz	1.25 MHz	2.5 MHz	5 MHz	10 MHz
0	0	1	0	$f_{CLK}/2^2$	313 kHz	625 kHz	1.25 MHz	2.5 MHz	5 MHz
0	0	1	1	$f_{CLK}/2^3$	156 kHz	313 kHz	625 kHz	1.25 MHz	2.5 MHz
0	1	0	0	$f_{CLK}/2^4$	78 kHz	156 kHz	313 kHz	625 kHz	1.25 MHz
0	1	0	1	$f_{CLK}/2^5$	39 kHz	78 kHz	156 kHz	313 kHz	625 kHz
0	1	1	0	$f_{CLK}/2^6$	19.5 kHz	39 kHz	78 kHz	156 kHz	313 kHz
0	1	1	1	$f_{CLK}/2^7$	9.8 kHz	19.5 kHz	39 kHz	78 kHz	156 kHz
1	0	0	0	$f_{CLK}/2^8$	4.9 kHz	9.8 kHz	19.5 kHz	39 kHz	78 kHz
1	0	0	1	$f_{CLK}/2^9$	2.5 kHz	4.9 kHz	9.8 kHz	19.5 kHz	39 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.22 kHz	2.5 kHz	4.9 kHz	9.8 kHz	19.5 kHz
1	0	1	1	$f_{CLK}/2^{11}$	625 Hz	1.22 kHz	2.5 kHz	4.9 kHz	9.8 kHz
1	1	0	0	$f_{CLK}/2^{12}$	313 Hz	625 Hz	1.22 kHz	2.5 kHz	4.9 kHz
1	1	0	1	$f_{CLK}/2^{13}$	152 Hz	313 Hz	625 Hz	1.22 kHz	2.5 kHz
1	1	1	0	$f_{CLK}/2^{14}$	78Hz	152 Hz	313 Hz	625 Hz	1.22 kHz
1	1	1	1	$f_{CLK}/2^{15}$	39Hz	78Hz	152 Hz	313 Hz	625 Hz

Note: Refer to **"**RL78/G10 User's Manual: Hardware" for the setup of the register.

Setup of the transmission channel operation mode.

- Serial mode register 00 (SMR00H, SMR00L)

Interrupt source
operation mode
Selection of the transfer clock.
Selection of fMCK.

Symbol: SMR00H

7	6	5	4	3	2	1	0
CKS 00	CCS 00	0	0	0	0	0	STS 00
0	**0**	0	0	0	0	0	**0**

SMR00L

7	6	5	4	3	2	1	0
0	0	1	0	0	MD 002	MD 001	MD 000
0	0	1	0	0	**0**	**1**	**0**

Bit 7 (SMR00H)

CKS00	Selection of operation clock (f_{MCK}) of channel 0
0	**Prescaler operation clock CK00 set by the SPS0 register.**
1	Prescaler operation clock CK01 set by the SPS0 register.

Bit 6 (SMR00H)

CCS00	Selection of transfer clock (f_{TCLK}) of channel 0
0	**Divided operation clock f_{MCK} specified by the CKS00 bit.**
1	Input clock from SCK pin.

Bit 0 (SMR00H)

STS00	Selection of the start trigger source
0	**Only software trigger is valid.**
1	Valid edge of the RXD0 pin (selected for UART reception)

Bit 2 – 1 (SMR00L)

MD002	MD001	Setting of operation mode of channel 0
0	0	CSI mode
0	**1**	**UART mode**
1	0	Simplified I2C mode
1	1	Setting prohibited

Bit 0 (SMR00L)

MD000	Selection of interrupt source of channel 0
0	**Transfer end interrupt**
1	Buffer empty interrupt

Note: Refer to **"**RL78/G10 User's Manual: Hardware" for the setup of the register.

Setup of operation mode of receiving channel

- Serial mode register 01 (SMR01H, SMR01L)

  Interrupt source

  operation mode

  Selection of the transfer clock.

  Selection of f_{MCK}.

Symbol: SMR01H

7	6	5	4	3	2	1	0
CKS 01	CCS 01	0	0	0	0	0	STS 01
0	**0**	0	0	0	0	0	**1**

SMR01L

7	6	5	4	3	2	1	0
0	SIS 010	1	0	0	MD 012	MD 011	MD 010
0	**0**	1	0	0	**0**	**1**	**0**

Bit 7 (SMR01H)

CKS01	Selection of operation clock (fMCK) of channel 1
0	**Prescaler operation clock CK00 set by the SPS0 register.**
1	Prescaler operation clock CK01 set by the SPS0 register.

Bit 6 (SMR01H)

CCS01	Selection of transfer clock (TCLK) of channel 1.
0	**Divided operation clock fMCK specified by the CKS01 bit.**
1	Input clock from the SCK pin.

Bit 0 (SMR01H)

STS01	Selection of the start trigger source
0	Only software trigger is valid.
1	**Valid edge of the RXD0 pin (selected for UART reception).**

Bit 6 (SMR01L)

SIS010	Level inversion control of receiving data of channel 1 in UART mode
0	**Falling edge is detected as the start bit.**
1	Rising edge is detected as the start bit.

Bit 2 – 1 (SMR01L)

MD012	MD011	Setting of operation mode of channel 1
0	0	CSI mode
0	**1**	**UART mode**
1	0	Simplified I2C mode
1	1	Setting prohibited

Bit 0 (SMR01L)

MD010	Selection of interrupt source of channel 1
0	**Transfer end interrupt.**
1	Buffer empty interrupt

Note: Refer to **"**RL78/G10 User's Manual: Hardware" for the setup of the register.

Setup of communication operation setting of transmission channel

- Serial communication operation setting register 00 (SCR00H, SCR00L)

  Data length setup, data transfer sequence, error interrupt signal mask enabled/disabled and operation mode.

Symbol: SCR00H

7	6	5	4	3	2	1	0
TXE00	RXE00	DAP00	CKP00	0	EOC00	PTC001	PTC000
1	**0**	**0**	**0**	0	**0**	**1**	**0**

Bit 7 - 6

TXE00	RXE00	Setting of operation mode of channel 0
0	0	Disable communication
0	1	Reception only
1	**0**	**Transmission only**
1	1	Transmission/reception

Bit 2

EOC00	Selection of masking of error interrupt signal (INTSRE0)
0	Masks error interrupt INTSRE0.
1	Enables generation of error interrupt INTSREx.

Bit 1 - 0

PTC001	PTC000	Setting of parity bit in UART mode	
		Transmission	Reception
0	**0**	**Does not output the parity bit.**	Receives without parity.
0	1	Outputs 0 parity.	No parity judgment.
1	0	Outputs even parity.	Judged as even parity.
	1	Outputs odd parity.	Judges as odd parity.

Note: Refer to **"**RL78/G10 User's Manual: Hardware" for the setup of the register.

Symbol: SCR00L

7	6	5	4	3	2	1	0
DIR00	0	SLC001	SLC000	0	1	1	DLS000
1	0	**0**	**1**	0	1	1	**1**

Bit 7

DIR00	Selection of data transfer sequence in CSI and UART modes
0	Inputs/outputs data with MSB first.
1	**Inputs/outputs data with LSB first.**

Bit 5 - 4

SLC001	SLC000	Setting of stop bit in UART mode
0	0	No stop bit
0	**1**	**Stop bit length = 1 bit**
1	0	Stop bit length = 2 bits
1	1	Setting prohibited

Bit 1 - 0

DLS000	Setting of data length in CSI mode
0	7-bit data length
1	**8-bit data length**

Note: Refer to **"**RL78/G10 User's Manual: Hardware" for the setup of the register.

Communication operation setting of receiving channel

- Serial communication operation register 01(SCR01H, SCR01L)

Data length setup, data transfer sequence, error interrupt signal mask enabled/disabled and operation mode.

Symbol: SCR01H

7	6	5	4	3	2	1	0
TXE01	RXE01	DAP01	CKP01	0	EOC01	PTC011	PTC010
0	**1**	**0**	**0**	0	**0**	**0**	**0**

Bit 7 - 6

TXE01	RXE01	Setting of operation mode of channel 1
0	0	Disable communication.
0	**1**	**Reception only**
1	0	Transmission only
1	1	Transmission/reception

In the case of UART reception, after setting “1” to RXE01 bit of SCR01 register, leaves the 4-clock or more interval of f_{MCK} and sets up SS01 = 1.

Bit 2

EOC01	Selection of masking of error interrupt signal (INTSRE0).
0	**Masks error interrupt INTSRE0.**
1	Enables generation of error interrupt INTSRE0.

Bit 1 - 0

PTC011	PTC010	Setting of parity bit in UART mode	
		Transmission	Reception
0	**0**	**Does not output the parity bit.**	**Receives without parity.**
0	1	Outputs 0 parity.	No parity judgment.
1	0	Outputs even parity.	Judged as even parity.
1	1	Outputs odd parity.	Judges as odd parity.

Note: Refer to **“**RL78/G10 User's Manual: Hardware” for the setup of the register.

Symbol: SCR01

7	6	5	4	3	2	1	0
DIR01	0	SLC011	SLC010	0	1	1	DLS010
1	0	**0**	**1**	0	1	1	**1**

Bit 7

DIR01	Selection of data transfer sequence in CSI and UART modes
0	Inputs/outputs data with MSB first.
1	**Inputs/outputs data with LSB first.**

Bit 5 - 4

SLC011	SLC010	Setting of stop bit in UART mode
0	0	No stop bit
0	**1**	**Stop bit length = 1 bit**
1	0	Stop bit length = 2 bits
1	1	Setting prohibited

Bit 0

DLS010	Setting of data length in CSI mode
0	7-bit data length
1	**8-bit data length**

Note: Refer to **“**RL78/G10 User's Manual: Hardware” for the setup of the register.

Setup of transmission channel transfer clock

- Serial data register 00 (SDR00H)

Transfer clock frequency: Undefined

Symbol: SDR00H

7	6	5	4	3	2	1	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0

Bit 7 - 1

SDR00H[7:1]							Transfer clock setting by dividing the operating clock (f_{MCK})
0	0	0	0	0	0	0	f_{MCK} /2
0	0	0	0	0	0	1	f_{MCK} /4
0	0	0	0	0	1	0	f_{MCK} /6
0	0	0	0	0	1	1	f_{MCK} /8
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	1	1	1	1	1	0	f_{MCK} /254
1	1	1	1	1	1	1	f_{MCK} /256

Setup of receiving transfer clock

- Serial data register 0n (SDR0nH)

Transfer clock frequency: Undefined

Symbol: SDR01H

7	6	5	4	3	2	1	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0

Bit 7 - 1

SDR01H[7:1]							Transfer clock setting by dividing the operating clock (f_{MCK})
0	0	0	0	0	0	0	f_{MCK} /2
0	0	0	0	0	0	1	f_{MCK} /4
0	0	0	0	0	1	0	f_{MCK} /6
0	0	0	0	0	1	1	f_{MCK} /8
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	1	1	1	1	1	0	f_{MCK} /254
1	1	1	1	1	1	1	f_{MCK} /256

Note: Refer to **"**RL78/G10 User's Manual: Hardware" for the setup of the register.

Setup of output level

・Serial output level register 0 (SOL0)

Output: Non-inversion

Symbol: SOL0

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SOL00
0	0	0	0	0	0	0	**0**

Bit 0

SOL00	Selects inversion of the level of the transmit data of channel 0 in UART mode
0	**Communication data is output as is.**
1	Communication data is inverted and output.

Setup of initial output level

・Serial output register 0 (SO0)

Initial output: 1

Symbol: SO0

7	6	5	4	3	2	1	0
0	0	0	0	0	0	SO01	SO00
0	0	0	0	0	0	x	**1**

Bit 0

SO00	Serial data output of channel 0
0	Serial data output value is “0”.
1	**Serial data output value is “1”.**

Data output enabling of target channel

・Serial output enable register 0 (SOE0/SOE0L)

Output is enabled.

Symbol: SOE0

7	6	5	4	3	2	1	0
0	0	0	0	0	0	SOE01	SOE00
0	0	0	0	0	0	x	**1**

Bit 0

SOE00	Serial output enable or stop of channel 0
0	Stops output by serial communication operation.
1	**Enables output by serial communication operation.**

Note: Refer to **“**RL78/G10 User's Manual: Hardware” for the setup of the register.

Noise filter enabled

- Noise filter enable register 0 (NFEN0)

Noise filter of RxD0 pin on.

Symbol: NFEN0

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SNFEN00
0	0	0	0	0	0	0	**1**

Bit 0

SNFEN00	Use of noise filter of RxD0 pin (RxD0/P01)
0	Noise filter OFF
1	**Noise filter ON**

Clear of error flag

- Serial flag clear trigger register 01 (SIR01)

Clear of error flag.

Symbol: SIR01

7	6	5	4	3	2	1	0
0	0	0	0	0	FECT01	PECT01	OVCT01
0	0	0	0	0	**1**	**1**	**1**

Bit 2

FECT01	Clear trigger of framing error of channel 1
0	Not cleared
1	**Clears the FEF01 bit of the SSR01 register to 0.**

Bit 1

PECT01	Clear trigger of parity error flag of channel 1
0	Not cleared
1	**Clears the PEF01 bit of the SSR01 register to 0.**

Bit 0

OVCT01	Clear trigger of overrun error flag of channel 1
0	Not cleared
1	**Clears the OVF01 bit of the SSR01 register to 0.**

Note: Refer to **"**RL78/G10 User's Manual: Hardware" for the setup of the register.

5.7.9 Enabling UART0 Operation

Figure 5.10 shows the enabling UART0 operation.

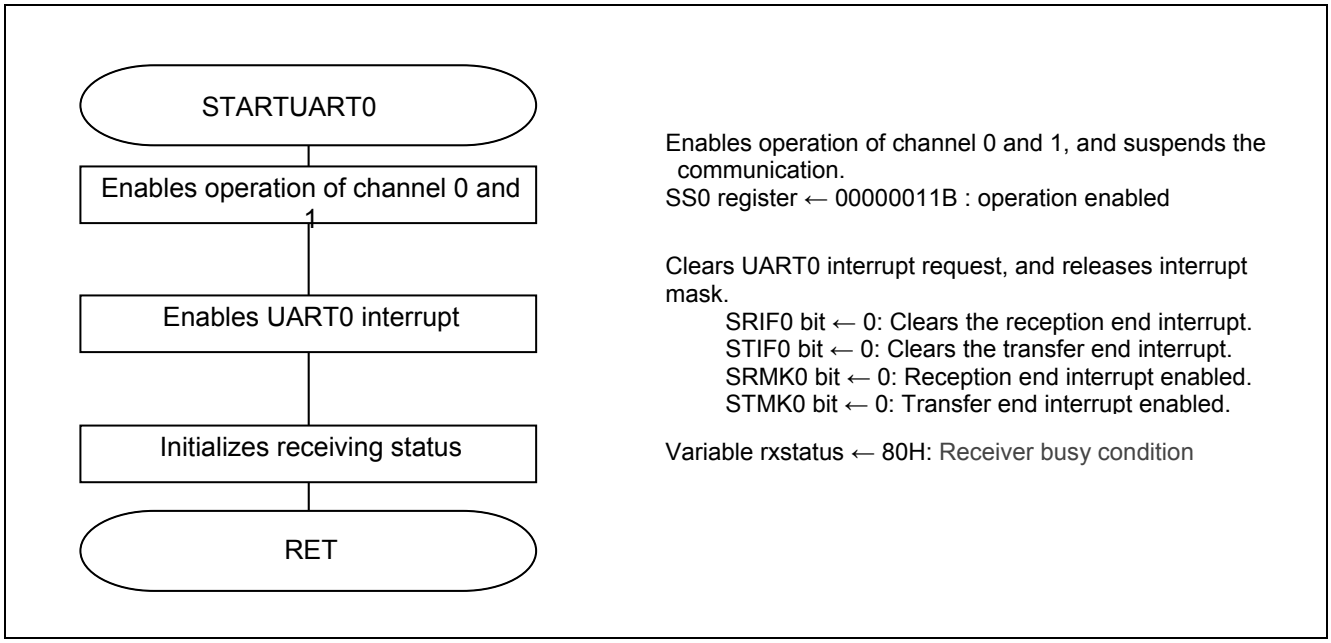

Figure 5.9 Enabling UART0 Operation

Entering the communication wait status

- Serial channel start register 0 (SS0)
  Starts the operation.

Symbol: SS0

7	6	5	4	3	2	1	0
0	0	0	0	0	0	SS01	SS00
0	0	0	0	0	0	**1**	**1**

Bit 1 - 0

SS0n	Sets the SE0n bit to 1 to suspend communication.
0	No trigger operation
1	**Sets the SE0n bit to 1 to suspend communication.**

Note: In the case of UART reception, after setting “1” to RXE01 bit of SCR01 register, leaves the 4-clock or more interval of f_{MCK} and sets up SS01 = 1.

5.7.10 UART0 Operation Disabled

Figure 5.11 shows the UART0 operation disabled processing.

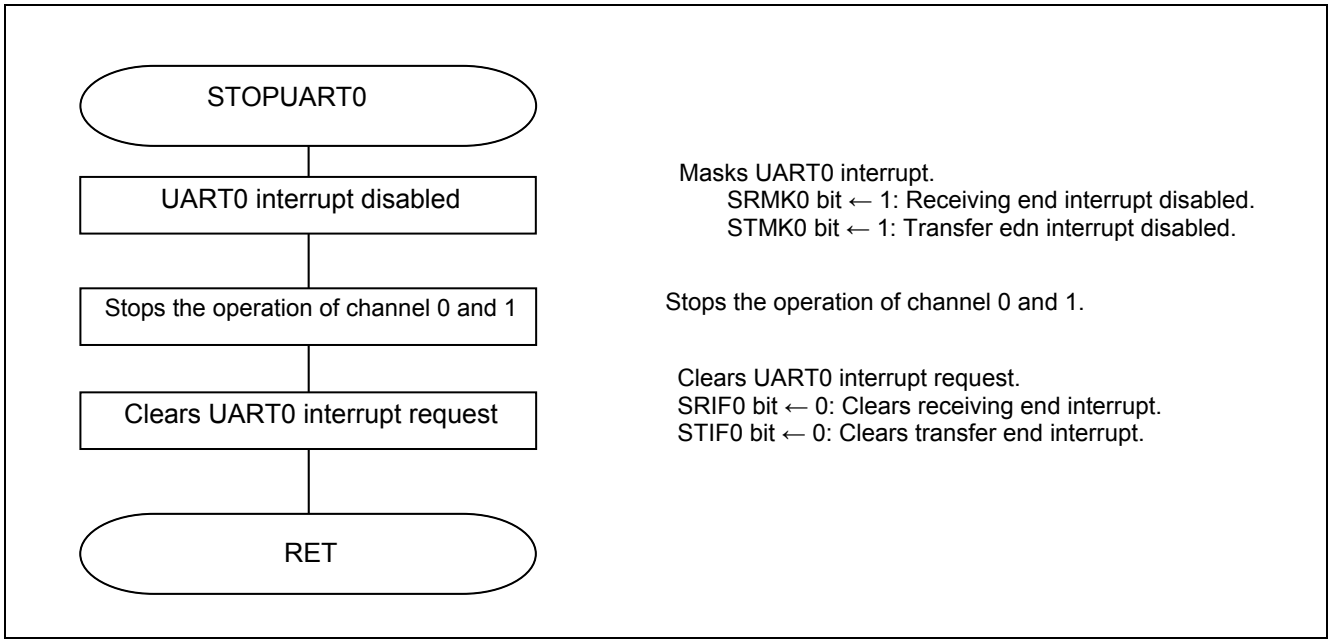

Figure 5.11 UART0 Operation Disabled

Release communication suspended state

- Serial channel stop register 0 (ST0)

  Stops UART0 operation.

Symbol: ST0

7	6	5	4	3	2	1	0
0	0	0	0	0	0	ST01	ST00
0	0	0	0	0	0	**1**	**1**

Bit 1 - 0

ST0n	Operation stop trigger of channel n.
0	No trigger operation.
1	**Clears the SE0n bit to 0 and stops the communication operation.**

Note: Followings keep the state; the value of control register and shift register, the pin of SCK0n and SO0n, and the flag of FEF0n, PEF0n, and OVF0n.

Note: Refer to “RL78/G10 User's Manual: Hardware” for the setup of the register.

5.7.11 1 Character Transmission Start Processing

Figure 5.12 shows the 1 character transmission start processing.

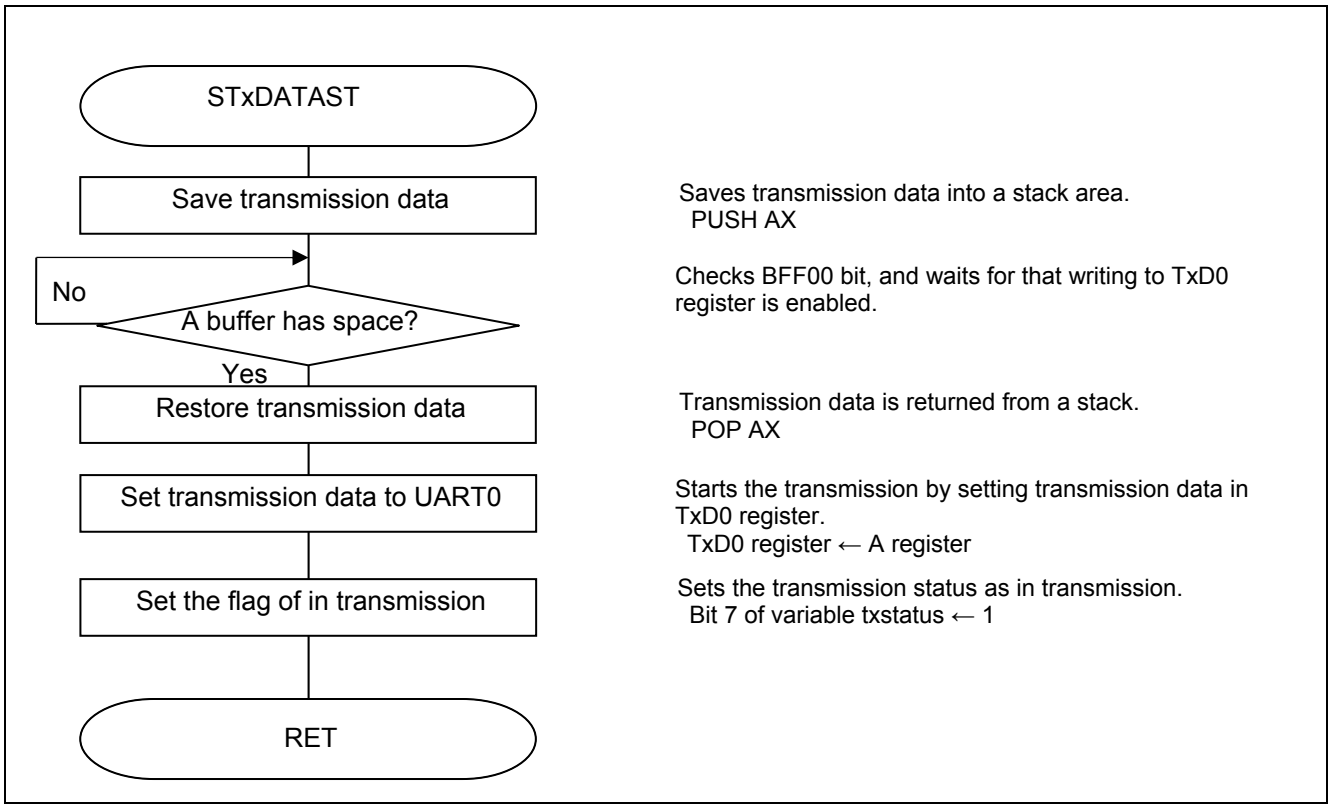

Figure 5.12 1 Character Transmission Start Processing

Transmission state check

- Serial status register 00 (SSR00)
  Checks transmission buffer state.

Symbol: SSR00

7	6	5	4	3	2	1	0
0	TSF00	BFF00	0	0	FEF00	PEF00	OVF00
0	x	**0/1**	0	0	x	x	x

Bit 5

BFF00	Buffer register status indication flag of channel 0
0	**Valid data is not stored in the SDR00L register.**
1	**Valid data is stored in the SDR00L register.**

Note: Refer to **"**RL78/G10 User's Manual: Hardware" for the setup of the register.

5.7.12 1 Character Transmission/Wait for the End of Transmission Processing

Figure 5.13 shows the 1 character transmission/wait for the end of transmission processing.

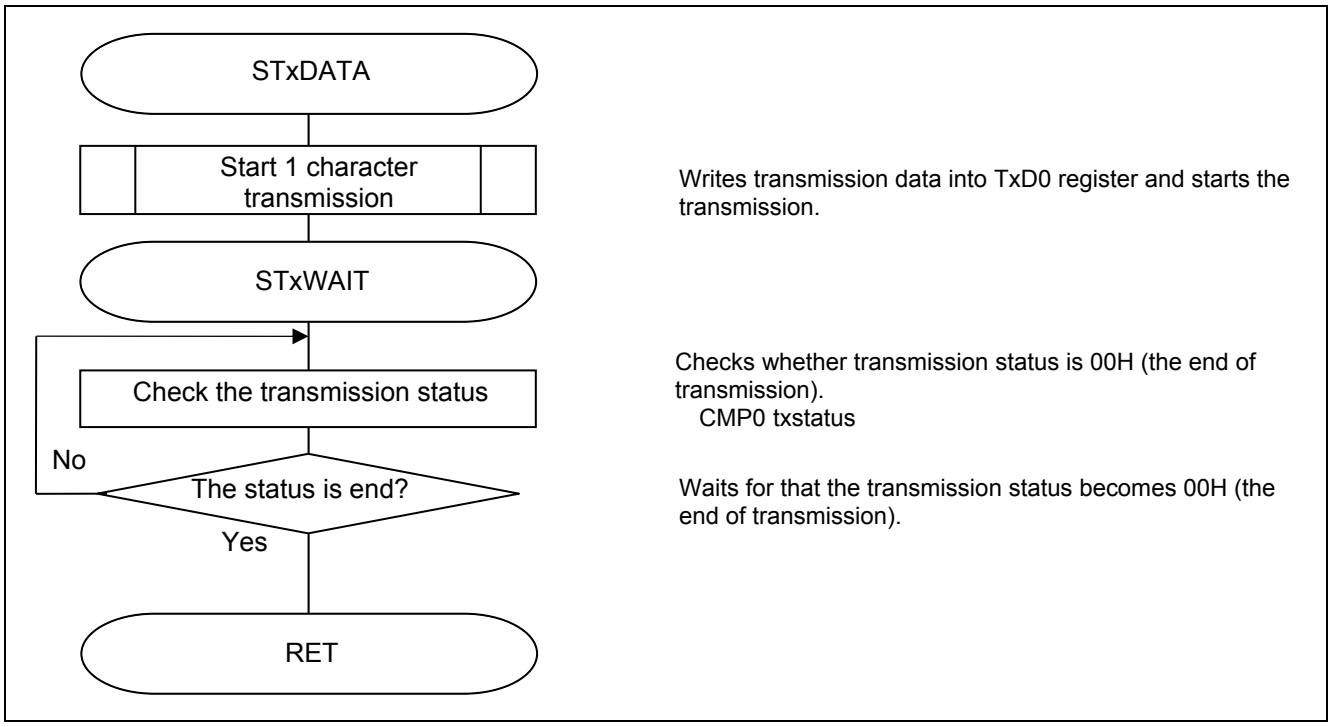

Figure 5.13 1 Character Transmission/Wait for the End of Transmission Processing

5.7.13 1 Character Receiving Processing

Figure 5.14 shows the 1 character receiving processing.

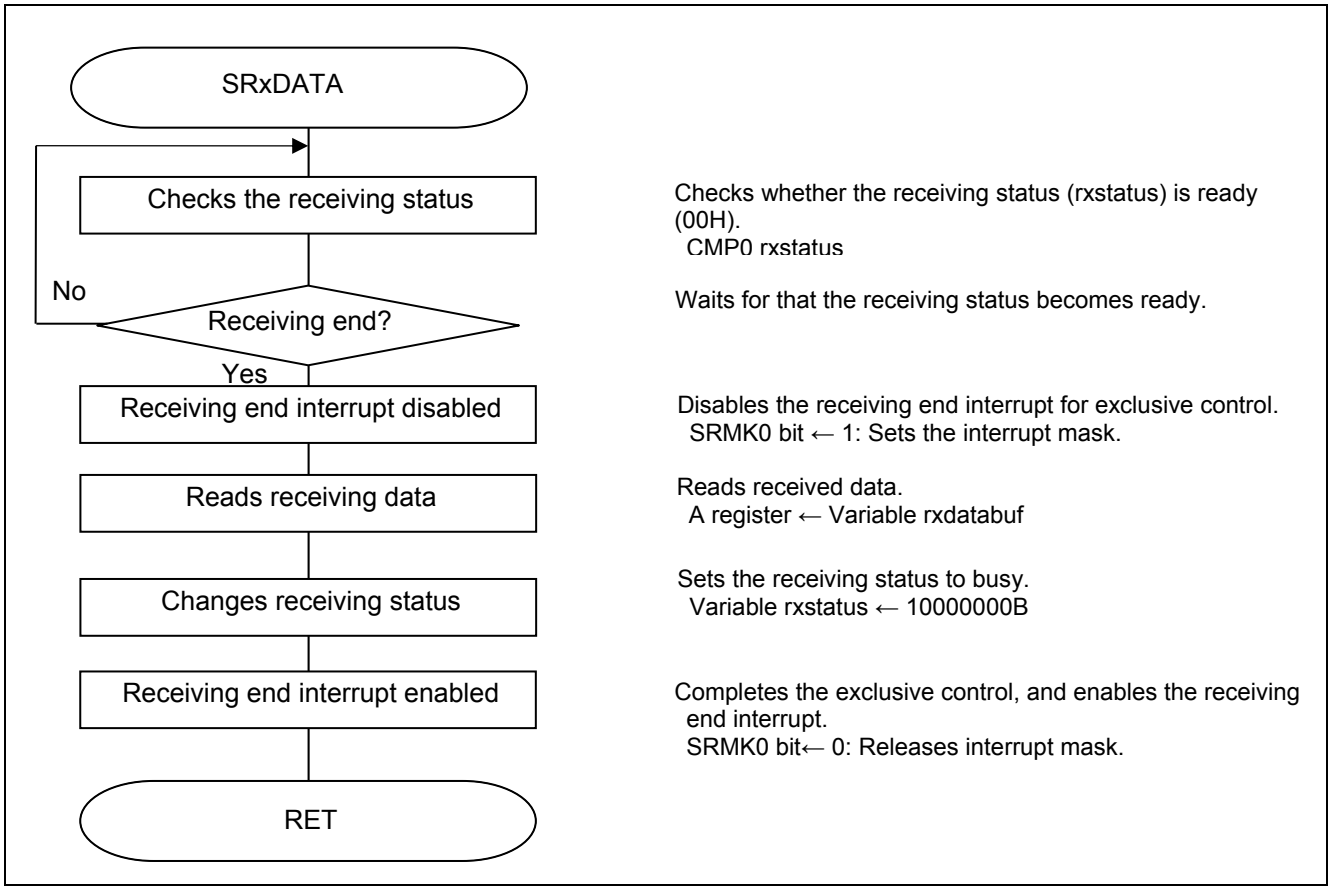

Figure 5.14 1 Character Receiving Processing

5.7.14 Receiving End Interrupt Processing

Figure 5.15 shows the receiving end interrupt processing.

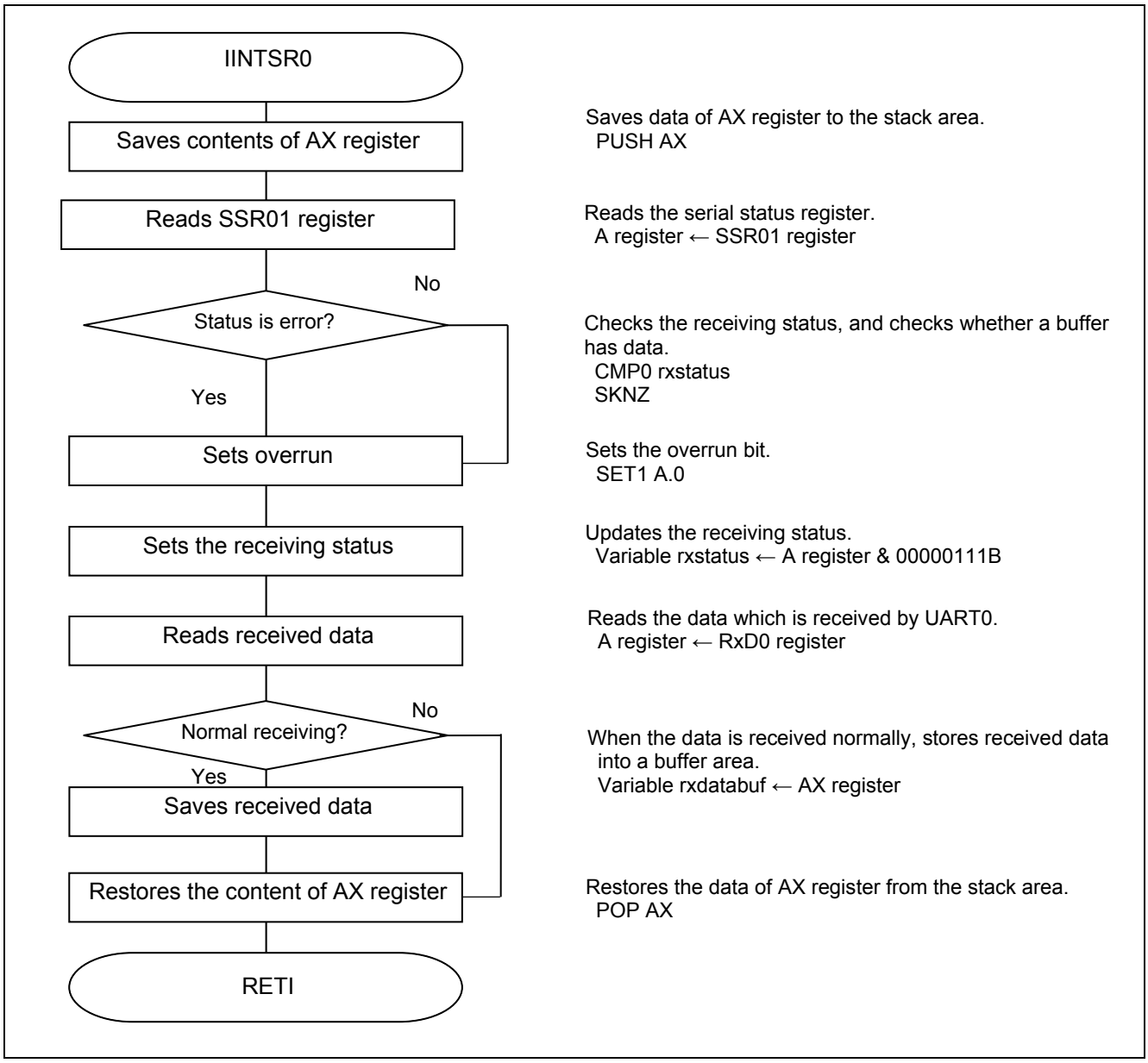

Figure 5.15 Receiving End Interrupt Processing

Note: Refer to **"**RL78/G10 User's Manual: Hardware" for the setup of the register.

5.7.15 Transfer End Interrupt Processing

Figure 5.16 shows the transfer end interrupt processing.

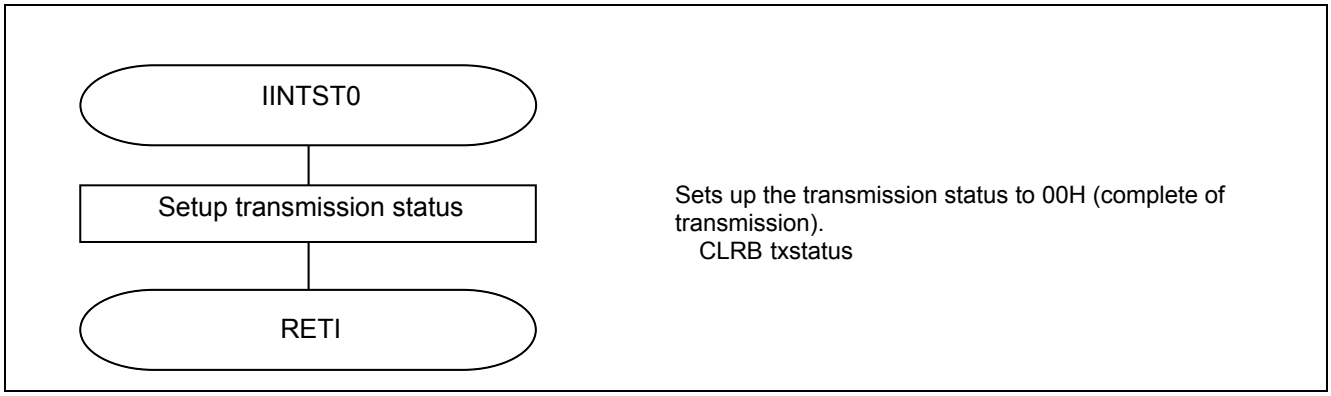

Figure 5.16 Transfer End Interrupt Processing

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

RL78/G10 User's Manual: Hardware (R01UH0384E)
RL78 Family User's Manual: Software (R01US0015E)
(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

(The latest versions of the documents are available on the Renesas Electronics Website.)

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Revision Record	RL78/G10 Serial Array Unit (Baud Rate Correction) CC-RL

Rev.	Date	Description	
		Page	Summary
1.00	Nov. 20, 2015	—	First edition issued
1.01	Oct. 05, 2016	—	Errors Correction

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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