RL78/F23, F24

Interrupt Source Determination Procedure

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Introduction

Some interrupt vector tables of the target devices (RL78/F23, F24) share multiple interrupt sources with one interrupt vector table as shown in the following **Table 1-1**. When using multiple interrupt sources assigned to the same interrupt vector table at the same time, it is necessary to determine which interrupt has occurred in the interrupt handler, or whether both interrupts have occurred.

This application note describes how to determine the interrupt source when using both interrupt sources simultaneously.

Table 1-1 List of Multiple Interrupt Sources that are Shared in One Interrupt Vector Table

Vector Table Address	Interrupt Source Note1		Reference Section
	Name	Trigger	
0008H	INTP0	Pin input edge detection 0	Cannot use both simultaneously.Note2
	-	RXD0 reception pin input detection	
0010H	INTP4	Pin input edge detection 4	**Section 1.1**
	INTSPM	Stack pointer overflow/underflow detection	
0012H	INTP5	Pin input edge detection 5	**Section 1.2**
	INTCMP0	Comparator detection 0	
0014H	INTP13	Pin input edge detection 13	**Section 1.3**
	INTCLM	PLL clock stop detection	
002AH	INTP8	Pin input edge detection 8	**Section 1.4**
	INTRTC	RTC pretimed signal or alarm match detection	
0036H	INTP6	Pin input edge detection 6	Cannot identify both interrupt sources.
	INTTM11H	Upper 8-bit interval timer interrupt of TAU1 channel 1	
0038H	INTP7	Pin input edge detection 7	
	INTTM13H	Upper 8-bit interval timer interrupt of TAU1 channel 3	
003AH	INTP9	Pin input edge detection 9	
	INTTM01H	Upper 8-bit interval timer interrupt of TAU0 channel 1	
003CH	INTP10	Pin input edge detection 10	
	INTTM03H	Upper 8-bit interval timer interrupt of TAU0 channel 3	
004AH	INTP11	Pin input edge detection 11	Cannot use both simultaneously .Note2
	INTLIN0WUP	LIN0 reception pin input detection	
004CH	INTKR	Key interrupt detection	Cannot identify both interrupt sources.
	INTRCANGRVC	CAN global receive message buffer interrupt	
0064H	INTP12	Pin input edge detection 12	Cannot use both simultaneously.Note2
	INTLIN1WUP	LIN1 reception pin input detection	

Note 1: It depends on the product. For details, show the user's manual.
2: Select the interrupt to use with the ISC0, ISC2, and ISC3 bits in the ISC register.

Contents

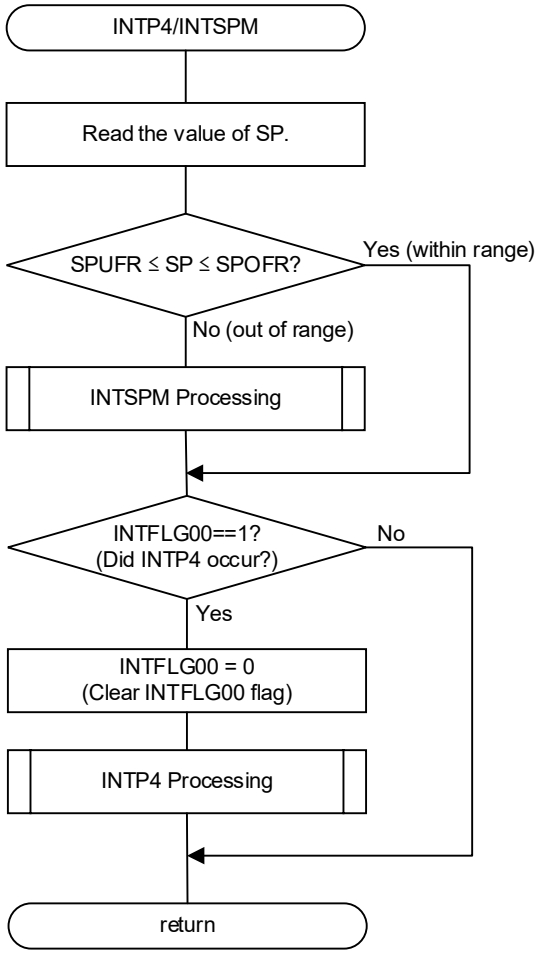
1. Interrupt Source Determination Procedure

In some interrupt vector tables of the target devices (RL78/F23, F24), multiple interrupt sources share one interrupt vector table. This chapter explains how to determine interrupt sources when using interrupts assigned to the same vector table at the same time.

1.1 Determination between INTP4 and INTSPM

Figure 1-1 shows an interrupt processing example in case of both INTP4 (Pin input edge detection 4) and INTSPM (Stack pointer overflow/underflow) are enabled.

Interrupt by INTP4 can be determined from INTFLG00 bit of INTFLG0. And interrupt by INTSPM can be determined by reading stack pointer from user software.



Caution: When both INTP4 and INTSPM are enabled, enable multiple interrupt servicing (before each interrupt request is acknowledged, the EI instruction must be issued.).

Remarks: SPOFR: SP overflow address setting register
SPUFR: SP underflow address setting register

Figure 1-1 INTP4/INTSPM Interrupt Judgement Example

1.2 Determination between INTP5 and INTCMP0

Figure 1-2 shows an interrupt processing example in case of both INTP5 (Pin input edge detection 5) and INTCMP0 (Comparator detection 0) are enabled.

Interrupt by INTP5 can be determined from INTFLG01 bit of INTFLG0. And interrupt by INTCMP0 can be determined from INTFLG06 bit of INTFLG0.

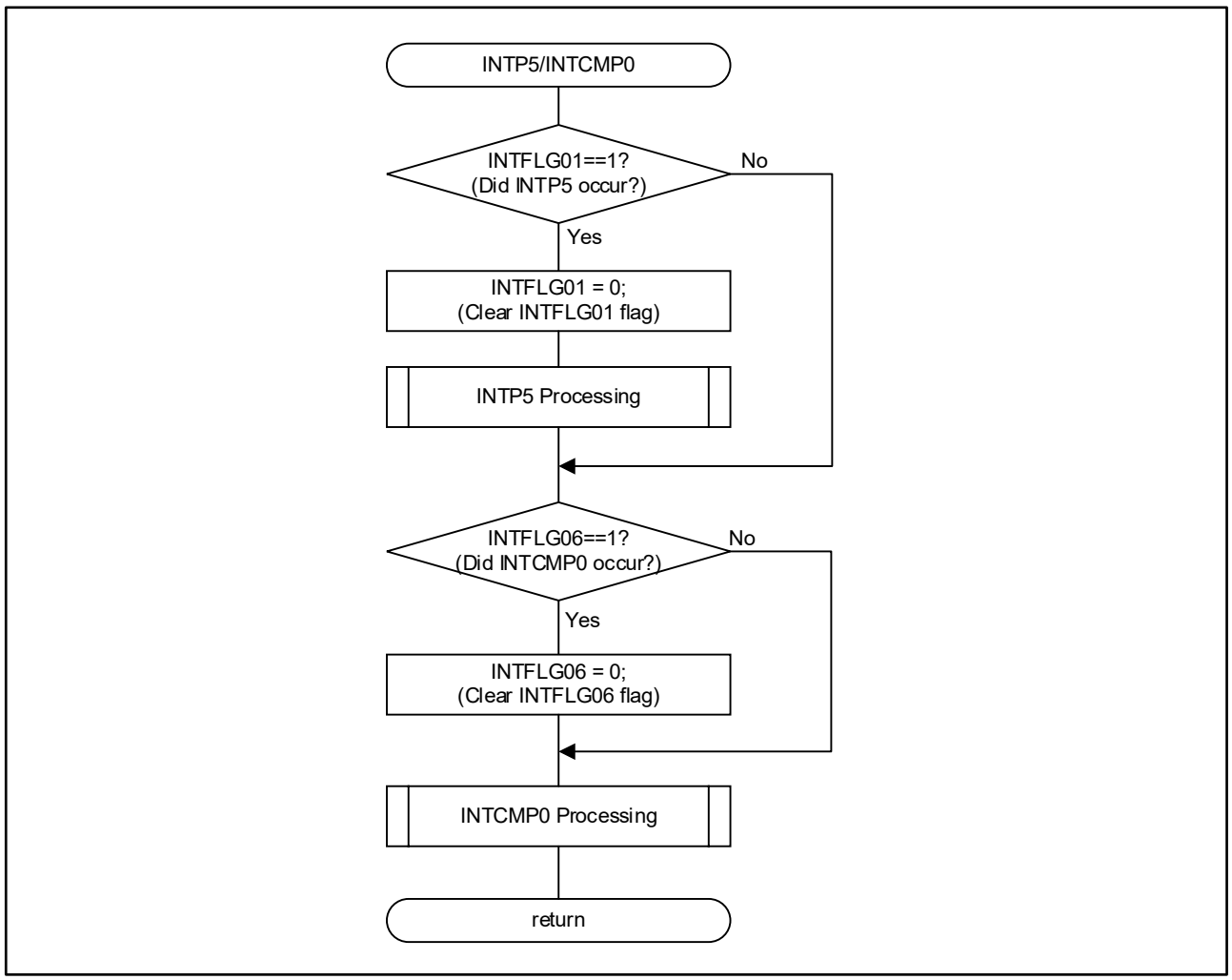
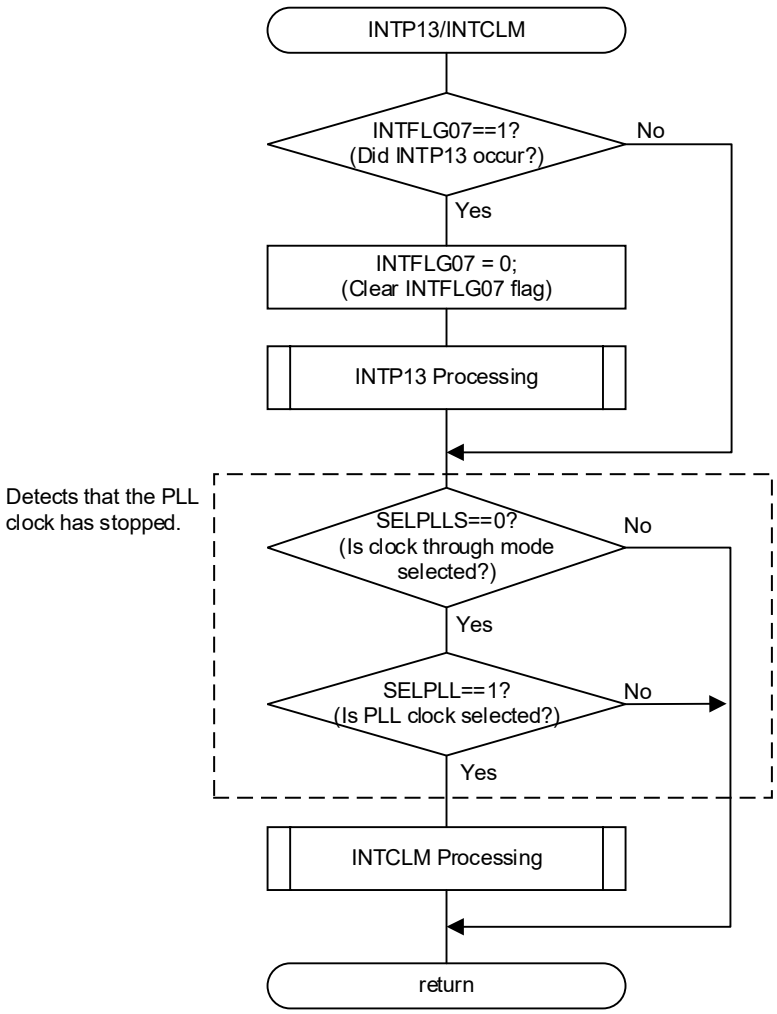


Figure 1-2 INTP5/INTCMP0 Interrupt Judgement Example

1.3 Determination between INTP13 and INTCLM

Figure 1-3 shows an interrupt processing example in case of both INTP13 (Pin input edge detection 13) and INTCLM (PLL clock stop detection) are enabled.

Interrupt by INTP13 can be determined from INTFLG07 bit of INTFLG0. And interrupt by INTCLM can be determined from SELPLLS bit of PLLSTS and SELPLL bit of PLLCTL.



Caution: Be sure to switch the main / PLL selection clock (f_{MP}) to PLL clock frequency (f_{PLL}) before enabling both INTP13 and INTCLM interrupts.

Figure 1-3 INTP13/INTCLM Interrupt Judgement Example

1.4 Determination between INTP8 and INTRTC

Figure 1-4 shows an interrupt processing example in case of both INTP8 (Pin input edge detection 8) and INTRTC (RTC pretimed signal or alarm match detection) are enabled.

Interrupt by INTP8 can be determined from INTFLG02 bit of INTFLG0. And interrupt by INTRTC can be determined from WAFG bit and RIFG bit of RTCC1.

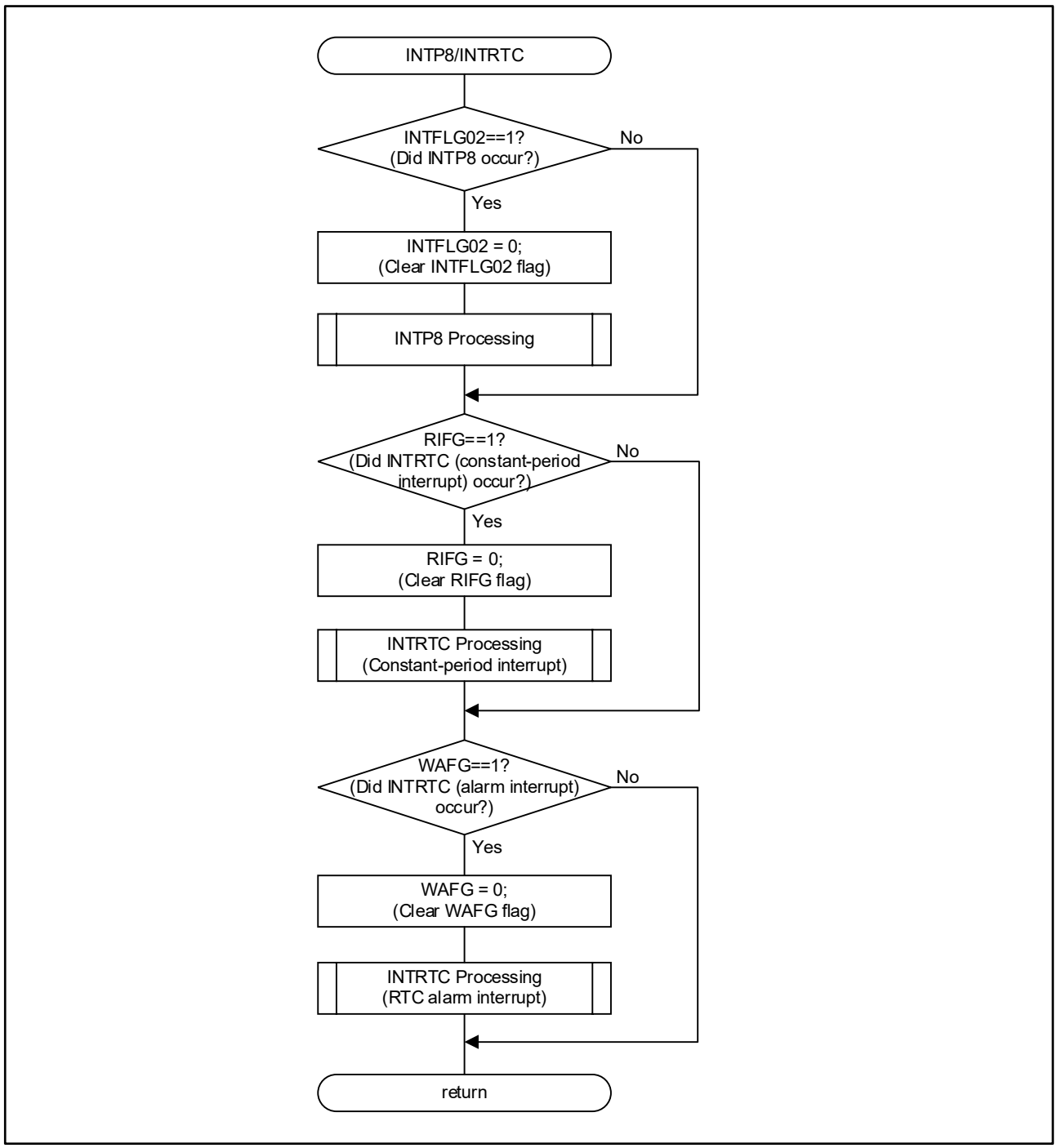


Figure 1-4 INTP8/INTRTC Interrupt Judgement Example

2. Notes on Interrupt Source Determination

2.1 Notes when Clearing bit of INTFLGn Register

If a new interrupt of the same source occurs during interrupt processing, the interrupt request (IF bit) may become "1" even if the INTFLGnm bit of INTFLGn register is cleared. In this case, the interrupt is generated, but its interrupt factor INTFLGnm bit is “0” (no interrupt request), so its interrupt is terminated without processing.

The above case will be explained using the INTP4 / INTSPM interrupt as an example. After the INTFLG00 bit is determined to be “1” (INTP4 request is occurred) in the interrupt processing shown in **Figure 2-1** and if a new effective edge is input to the INTP4 pin before the INTFLG00 bit is cleared, the PIF4 bit of the IF0L register is set to “1”. After that, the INTFLG00 bit is cleared and the INTP4 interrupt processing ends. And the INTP4 / INTSPM interrupt occurs again as the PIF4 bit is “1”. However, at this time, since the INTFLG00 bit has already been cleared to “0”, the next processing is executed without executing INTP4 Processing.

When using multiple interrupts with them enabled, consider the above notes when designing.

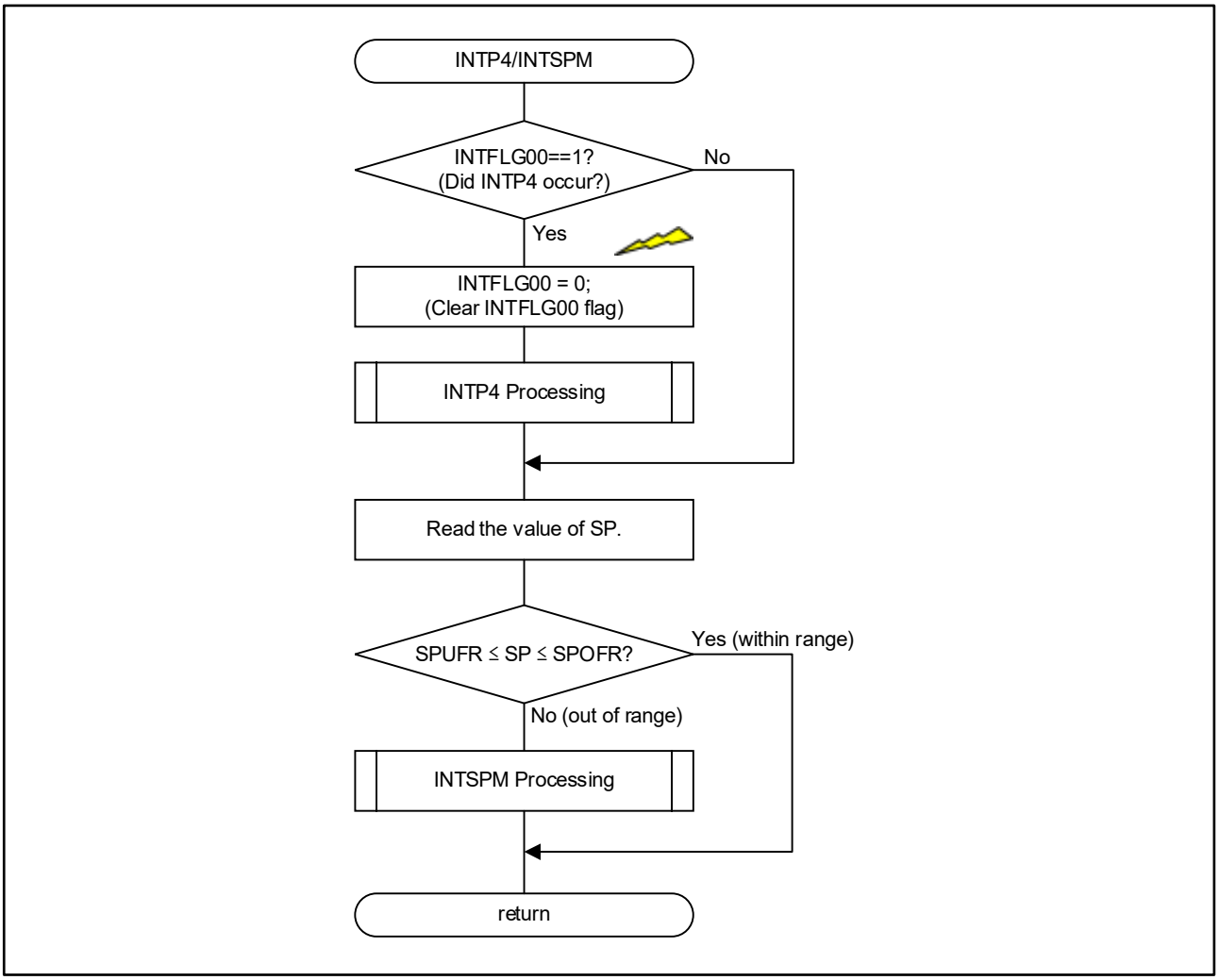


Figure 2-1 INTP4/INTSPM Interrupt Judgement Example (INTP4 occurs continuously)

2.2 Notes when Using INTSPM and INTCLM

The CPU stack pointer monitor function or Clock monitor function are a safety function, it is recommended to set those interrupt priority level high.

3. References

Documents referenced in this application note are shown below. When referring to these documents, make sure to obtain the latest version of each document from Renesas Electronics website.

- RL78/ F23, F24 User's Manual: Hardware Rev. 1.00

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2023. 7.30	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

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1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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