RL78 Family

RL78 Microcontroller (RL78 Protocol A) Serial Programming Guide

Introduction

This application note describes the specifications of the boot firmware in RL78 microcontrollers. If the firmware is used in a way that does not conform with the descriptions in this document, correct operation is not guaranteed.

Target Device

RL78 Family

Please refer to the following site for target devices compatible with RL78 protocol A.

https://en-support.renesas.com/knowledgeBase/16979203

CONTENTS

CHAPTER 1 FLASH MEMORY PROGRAMMING

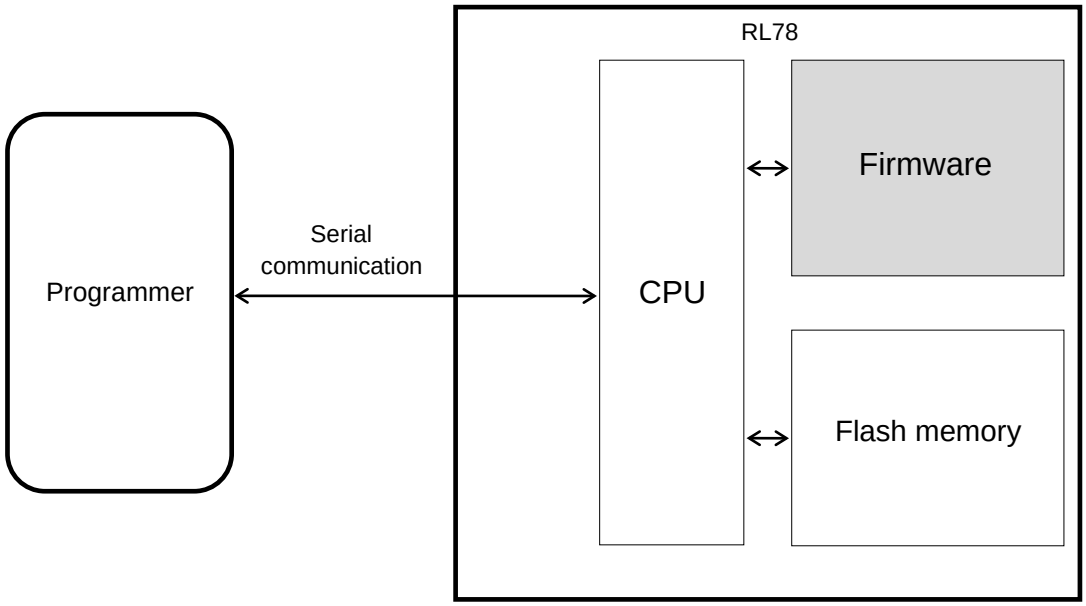
To rewrite the contents of the internal flash memory of the RL78, a dedicated flash memory programmer (hereafter referred to as the “programmer”) is usually used.

This Application Note explains how to develop a dedicated programmer.

1.1 Overview

The RL78 incorporates firmware that controls flash memory programming. The programming to the internal flash memory is performed by transmitting/receiving commands between the programmer and the RL78 via serial communication.

Figure 1-1. System Outline of Flash Memory Programming in RL78

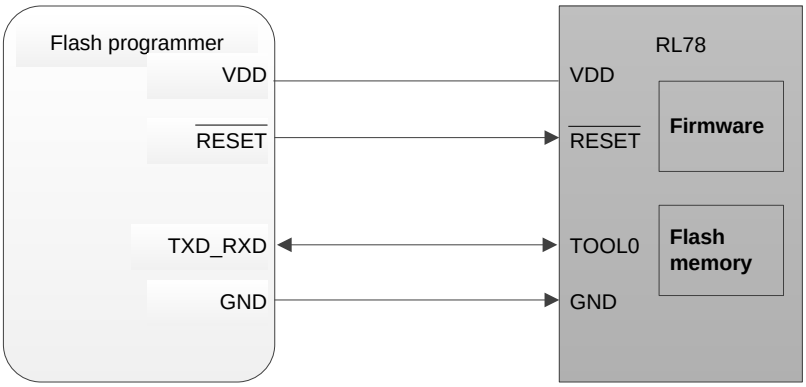


1.2 Communication Modes

As serial communications for writing the flash memory, single-wire UART communication or two-wire UART communication can be used. By exchanging the master and slave, an optimum communication can be realized.

1.2.1 Single-wire UART communication

Figure 1-2. Single-wire UART Communication



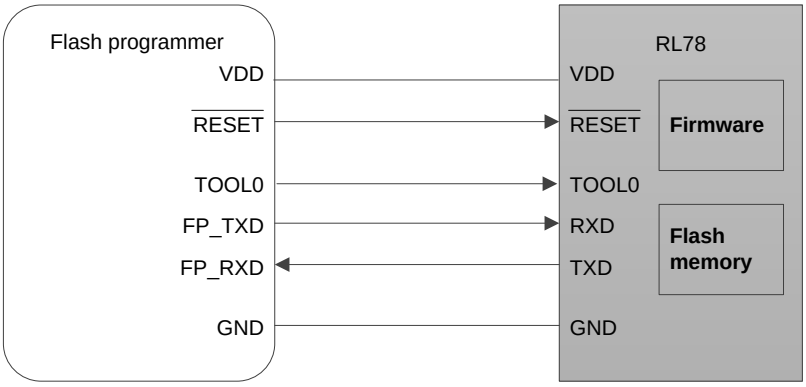
The TOOL0 pin is used for single-wire UART communication. The communication conditions are shown below.

Table 1-1. Single-wire UART Communication Conditions

Item	Description
Baud rate	Communication is performed at 115,200 bps until the Baud Rate Set command for baud rate setting command processing is transmitted. The transmission rate is changed to the baud rate set by the Baud Rate Set command from the transmission of the Reset command for baud rate command processing. For details of the settable baud rate, refer to **3.2 Baud Rate Set Command**.
Parity bit	None
Data length	8 bits (LSB first)
Start bit	1 bit
Stop bit	2 bits (programmer → RL78)/1 bit (RL78 → programmer)

1.2.2 Two-wire UART communication

Figure 1-3. Two-wire UART Communication



TxD and RxD pins are used for two-wire UART communication. The communication conditions are shown below.

Table 1-2. Two-wire UART Communication Conditions

Item	Description
Baud rate	Communication is performed at 115,200 bps until the Baud Rate Set command for baud rate setting command processing is transmitted. The transmission rate is changed to the baud rate set by the Baud Rate Set command from the transmission of the Reset command for baud rate command processing. For details of the settable baud rate, refer to **3.2 Baud Rate Set Command**.
Parity bit	None
Data length	8 bits (LSB first)
Start bit	1 bit
Stop bit	2 bits (programmer → RL78)/1 bit (RL78 → programmer)

1.3 Command List and Status List

The flash memory incorporated in the RL78 can be rewritten by using the commands listed in Table 1-2. The programmer transmits commands to control these functions to the RL78, and checks the response status sent from the RL78, to manipulate the flash memory.

1.3.1 Command list

The commands used by the programmer and their functions are listed below.

Table 1-3. List of Commands Transmitted from Programmer to RL78

Command Number	Command Name	Function
00H	Reset	Detects synchronization in communication.
22H	Block Erase	Erases a specified area in the flash memory.
40H	Programming	Writes data to a specified area in the flash memory.
13H	Verify	Compares the contents in a specified area in the flash memory with the data transmitted from the programmer.
32H	Block Blank Check	Checks the erase status of a specified block in the flash memory.
9AH	Baud Rate Set	Sets a baud rate and a voltage.
C0H	Silicon Signature	Reads RL78 information (such as product name and flash memory configuration).
A0H	Security Set	Sets a security flag, boot block cluster block number, and FSW.
A1H	Security Get	Reads a security flag, boot block cluster block number, boot area exchange flag, and FSW (flash option).
A2H	Security Release	Initializes all flash options.
B0H	Checksum	Reads the checksum value of data in a specified area.

1.3.2 Status list

The following table lists the status codes the programmer receives from the RL78.

Table 1-4. Status Code List

Status Code	Status	Description
04H	Command number error	Error returned if a command not supported is received
05H	Parameter error	Error returned if the value of a parameter to be appended to a command is not appropriate.
06H	Normal acknowledgment (ACK)	Normal acknowledgment
07H	Checksum error	Error returned if transmitted data frame has an abnormality
0FH	Verify error	Error returned if a verify error has occurred upon verifying data transmitted from the programmer
10H	Protect error	Error returned if an attempt is made to execute processing that is prohibited by the Security Set command
15H	Negative acknowledgment (NACK)	Negative acknowledgment
1AH	Erase error	Erase error
1BH	IVerify error/Blank error	Internal verify error or blank check error
1CH	Write error	Write error

Reception of a checksum error or NACK is treated as an immediate abnormal end in this manual. When a dedicated programmer is developed, however, the processing may be retried without problem from the wait immediately before transmission of the command that results a checksum error or NACK. In this event, limiting the retry count is recommended for preventing infinite repetition of the retry operation.

Although not listed in the above table, if a time-out error (BUSY time-out or time-out in data frame reception during UART communication) occurs, it is recommended to shutdown the power supply to the RL78 (refer to **1.5 Shutting Down Target Power Supply**) and then connect the power supply again.

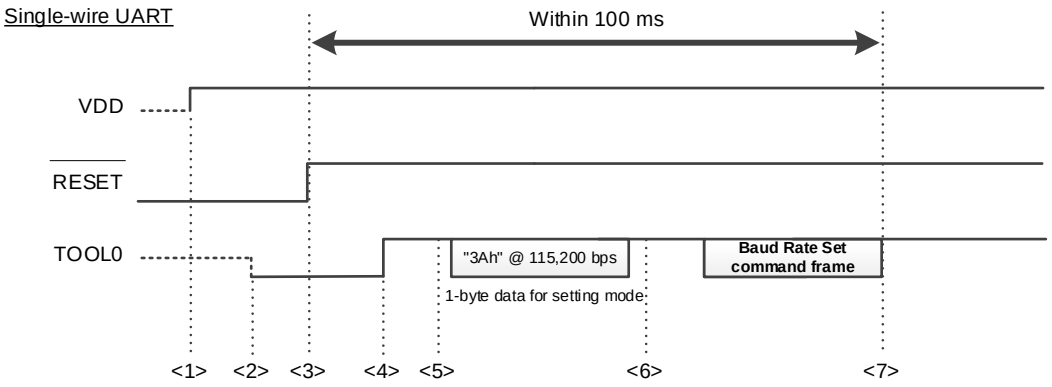
1.4 Power Application and Setting Flash Memory Programming Mode

To rewrite the contents of the flash memory with the programmer, the RL78 must first be set to the flash memory programming mode (serial programming mode).

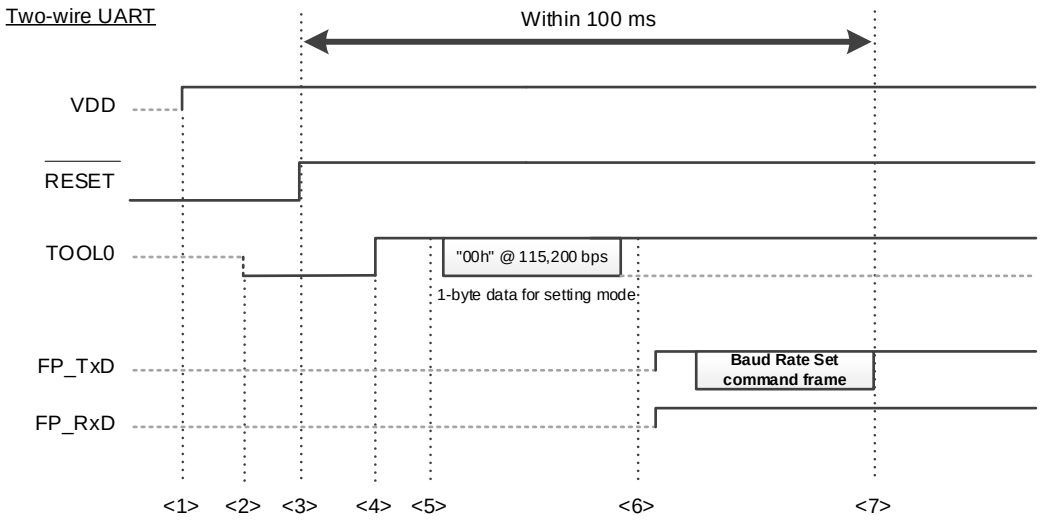
If the TOOL0 pin is at the low level on reset release, the RL78 is first set to the pre-mode. After data for setting a communication mode and the Baud Rate Set command have been transmitted, the RL78 is set to an operation mode of the serial programming mode.

The following figure illustrates a timing chart for setting the flash memory programming mode and selecting the communication mode.

Figure 1-4. Setting Flash Memory Programming Mode and Selecting Communication Mode



<1>: Power (VDD) application
<2>: TOOL0 = Low level
<3>: Reset release
<4>: TOOL0 = High level
<5>: Start of 1-byte data transmission
<6>: End of 1-byte data transmission
<7>: Completion of Baud Rate Set command



<1>: Power (VDD) application
<2>: TOOL0 = Low level
<3>: Reset release
<4>: TOOL0 = High level
<5>: Start of 1-byte data transmission
<6>: End of 1-byte data transmission
<7>: Completion of Baud Rate Set command

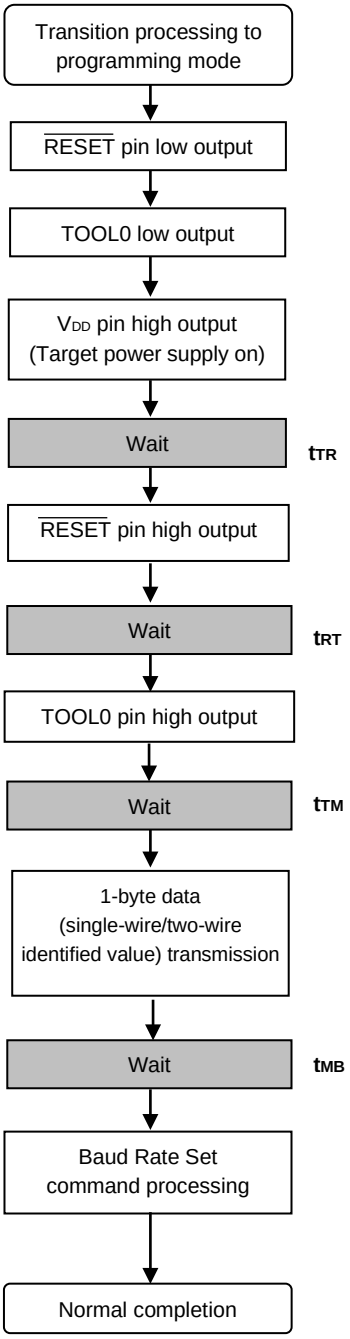
After reset release, 1-byte data is transmitted at 115,200 bps to set the RL78 to the serial programming mode and determine a communication mode. (Note, however, that this data can be set to 00H in the two-wire UART mode even by low-level control at 78.125 µs).

The relationship between the 1-byte data and communication interface is shown below.

Table 1-5. 1-byte Data and Communication Interface of RL78

1-byte Data	Communication Interface
3AH	Single-wire UART
00H	Two-wire UART

1.4.1 Mode setting flowchart



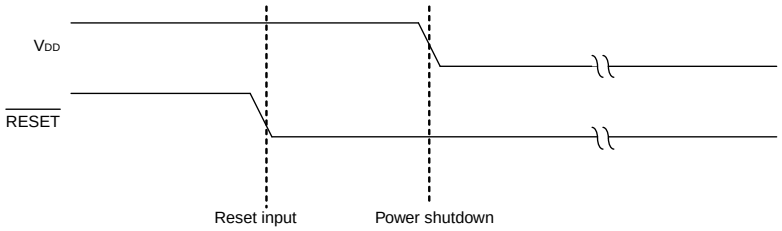
1.5 Shutting Down Target Power Supply

After each command execution is completed, shut down the power supply to the target after setting the $\overline{\text{RESET}}$ pin to low level, as shown below.

Set other pins to Hi-Z when shutting down the power supply to the target.

Caution Shutting down the power supply and inputting a reset during command processing are prohibited.

Figure 1-5. Timing for Terminating Flash Memory Programming Mode

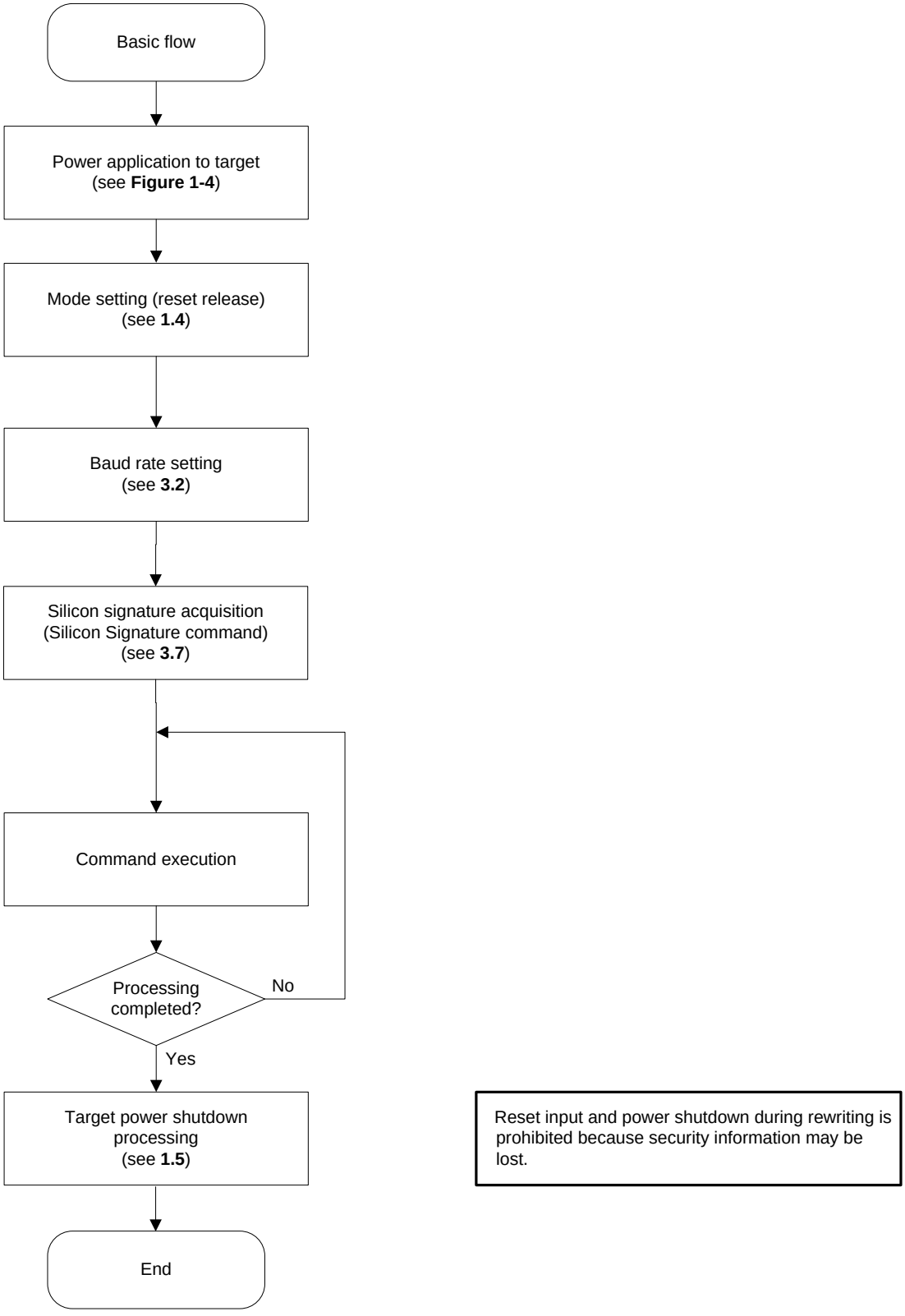


1.6 Command Execution Flow at Flash Memory Rewriting

Figure 1-6 illustrates the basic flowchart when flash memory rewriting is performed with the programmer.

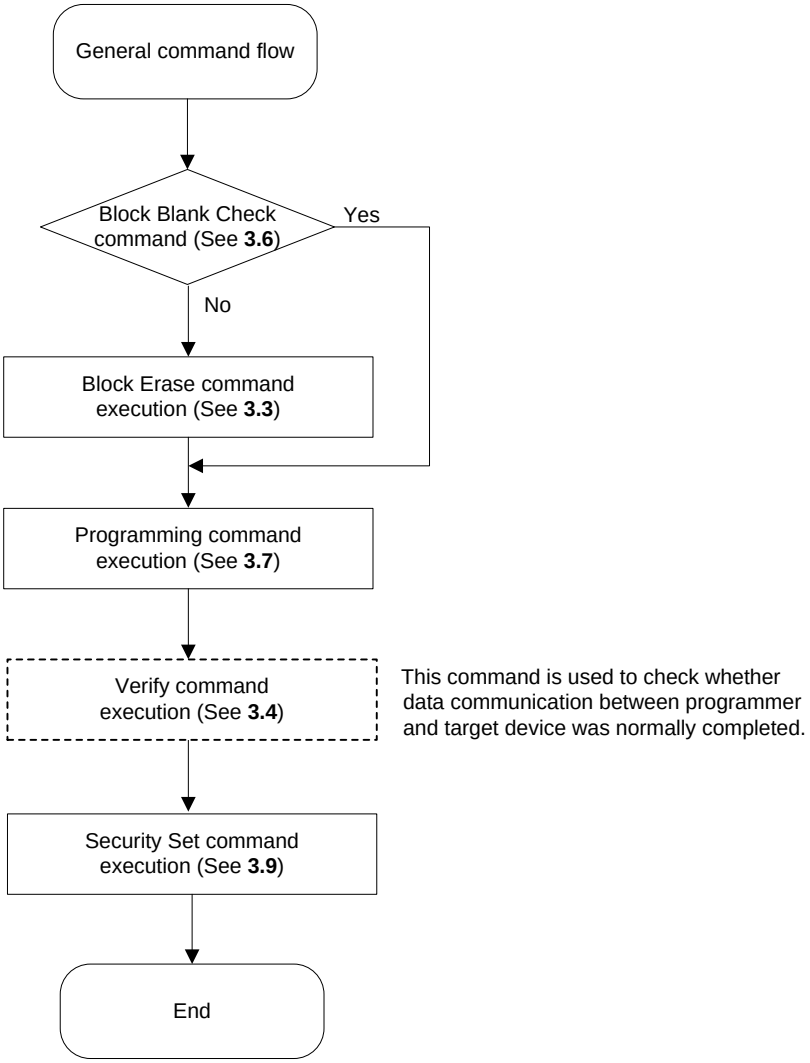
Other than commands shown in Figure 1-6, the Verify command and Checksum command are also supported.

Figure 1-6. Basic Flowchart for Flash Memory Rewrite Processing



Remark The example of each command execution is shown in Figure 1-7.

Figure 1-7. General Command Execution Flow at Flash Memory Rewriting



CHAPTER 2 COMMAND/DATA FRAME FORMAT

The programmer uses the command frame to transmit commands to the RL78. The RL78 uses the data frame to transmit write data or verify data to the programmer. A header, footer, data length information, and checksum are appended to each frame to enhance the reliability of the transferred data.

The following shows the format of a command frame and data frame.

Figure 2-1. Command Frame Format

SOH (1 byte)	LEN (1 byte)	COM (1 byte)	Command information (variable length) (Max. 255 bytes)	SUM (1 byte)	ETX (1 byte)

Figure 2-2. Data Frame Format

STX (1 byte)	LEN (1 byte)	Data (variable length) (Max. 256 bytes)	SUM (1 byte)	ETX or ETB (1 byte)

Table 2-1. Description of Symbols in Each Frame

Symbol	Value	Description
SOH	01H	Command frame header
STX	02H	Data frame header
LEN	–	Data length information (00H indicates 256). Command frame: COM + command information length Data frame: Data field length
COM	–	Command number
SUM	–	Checksum data for a frame Obtained by sequentially subtracting all of calculation target data from the initial value (00H) in 1-byte units (borrow is ignored). The calculation targets are as follows. Command frame: LEN + COM + all of command information Data frame: LEN + all of data
ETB	17H	Footer of data frame other than the last frame
ETX	03H	Command frame footer, or footer of last data frame

The following shows examples of calculating the checksum (SUM) for a frame.

[Command frame]

No command information is included in the following example of a Security Get command frame, so LEN and COM are targets of checksum calculation.

SOH	LEN	COM	SUM	ETX
01H	01H	A1H	Checksum	03H
	Checksum calculation targets			

For this command frame, checksum data is obtained as follows.

00H (initial value) – 01H (LEN) – A1H (COM) = 5EH (Borrow ignored. Lower 8 bits only.)

The Security Get command frame finally transmitted is as follows.

SOH	LEN	COM	SUM	ETX
01H	01H	A1H	5EH	03H

[Data frame]

To transmit a data frame as shown below, LEN and D1 to D4 are targets of checksum calculation.

STX	LEN	D1	D2	D3	D4	SUM	ETX
02H	04H	FFH	80H	40H	22H	Checksum	03H
	Checksum calculation targets						

For this data frame, checksum data is obtained as follows.

00H (initial value) – 04H (LEN) – FFH (D1) – 80H (D2) – 40H (D3) – 22H (D4)
= 1BH (Borrow ignored. Lower 8 bits only.)

The data frame finally transmitted is as follows.

STX	LEN	D1	D2	D3	D4	SUM	ETX
02H	04H	FFH	80H	40H	22H	1BH	03H

When a data frame is received, the checksum data is calculated in the same manner, and the obtained value is used to detect a checksum error by judging whether the value is the same as that stored in the SUM field of the receive data. When a data frame as shown below is received, for example, a checksum error is detected.

STX	LEN	D1	D2	D3	D4	SUM	ETX
02H	04H	FFH	80H	40H	22H	1AH	03H
						↑ Normally 1BH	

2.1 Command Frame Transmission Processing

For details of the flowchart of processing to transmit command frames, read **4.1 Command Frame Transmission Processing Flowchart**.

2.2 Data Frame Transmission Processing

The write data frame (user program), verify data frame (user program), and security data frame (security flag) are transmitted as a data frame.

For details of the flowchart of processing to transmit data frames, read **4.2 Data Frame Transmission Processing Flowchart**.

2.3 Data Frame Reception Processing

The status frame, silicon signature data frame, security data frame, and checksum data frame are received as a data frame.

For details of the flowchart of processing to receive data frames, read **4.3 Data Frame Reception Processing Flowchart**.

CHAPTER 3 DESCRIPTION OF COMMAND PROCESSING

3.1 Reset Command

3.1.1 Description

This command follows the Baud Rate Set command and is used to check if synchronization is performed at the baud rate that has been newly set by the Baud Rate Set command.

3.1.2 Command frame and status frame

Figure 3-1 shows the format of a command frame for the Reset command, and Figure 3-2 shows the status frame for the command.

Figure 3-1. Reset Command Frame (from Programmer to RL78)

SOH	LEN	COM	SUM	ETX
01H	01H	00H (Reset)	Checksum	03H

Figure 3-2. Status Frame for Reset Command (from RL78 to Programmer)

STX	LEN	Data	SUM	ETX
02H	01H	ST1	Checksum	03H

Remark ST1: Synchronization detection result

See **4.4 Reset Command** for details on the flowchart of the processing sequence between the programmer and the RL78, and the flowchart of command processing.

3.2 Baud Rate Set Command

3.2.1 Description

This command is used to set a baud rate (115,200 bps by default) for UART communication and input information on the data that sets a voltage.

The RL78 determines the operating frequency and programming mode by using voltage setting data and option byte.

3.2.2 Command frame and status frame

Figure 3-3 shows the format of a command frame for the Baud Rate Set command, and Figure 3-4 shows the status frame for the command.

Figure 3-3. Baud Rate Set Command Frame (from Programmer to RL78)

SOH	LEN	COM	Command Information[Note]		SUM	ETX
01H	03H	9AH	D01	D02	Checksum	03H

Note For details of the command information setting, refer to **Table 3-1**. If data other than in Table 3-1 is set, a time-out error will occur.
If a time-out error has occurred, execute a hardware reset and re-set the flash memory programming mode.

Remark D01: Baud rate setting data
D02: Voltage setting data. Data on the voltage supplied to the target when the flash memory is written is rounded off at the first place below decimal point and transmitted as hexadecimal data.
Example: Voltage D02
3.69 V → 36 → 24H
2.11 V → 21 → 15H

Table 3-1. Baud Rate Setting Data Format

Data	Set Baud Rate (bps)
00H	115,200
01H	250,000
02H	500,000
03H	1,000,000

Figure 3-4. Status Frame for Baud Rate Set Command (from RL78 to Programmer)

STX	LEN	Data			SUM	ETX
02H	03H	ST1	D01	D02	checksum	03H

Remark ST1: Synchronization detection result
D01: Transmitted as hexadecimal data. Wait time and time-out are set based on this frequency.
Example: 32 MHz: 20H
20 MHz: 14H
D02: Sets a programming mode.
To write in the full-speed mode: 00H
To write in the wide-voltage mode: 01H

See **4.5 Baud Rate Set Command** for details on the flowchart of the processing sequence between the programmer and the RL78, and the flowchart of command processing.

3.3 Block Erase Command

3.3.1 Description

This command is used to erase the content of flash memory of the block with the specified number.

A block can be specified by specifying the first address of arbitrary block in block units.

Erasing cannot be performed, however, if execution of this command is prohibited due to the security setting (see **3.9 Security Set Command**).

3.3.2 Command frame and status frame

Figure 3-7 shows the format of a command frame for the Block Erase command, and Figure 3-8 shows the status frame for the command.

Figure 3-7. Block Erase Command Frame (from Programmer to RL78)

SOH	LEN	COM	Command Information			SUM	ETX
01H	04H	22H (Block Erase)	SAL	SAM	SAH	Checksum	03H

Remark SAH to SAL: Block erase start address (start address of any block)
SAH: Start address, high (bits 23 to 16)
SAM: Start address, middle (bits 15 to 8)
SAL: Start address, low (bits 7 to 0)

Figure 3-8. Status Frame for Block Erase Command (from RL78 to Programmer)

STX	LEN	Data	SUM	ETX
02H	01H	ST1	Checksum	03H

Remark ST1: Block erase result

See **4.6 Block Erase Command** for details on the flowchart of the processing sequence between the programmer and the RL78, and the flowchart of command processing.

3.4 Programming Command

3.4.1 Description

This command is used to write the user program to the flash memory by transmitting write data after having transmitted the write start address and the write end address. Internal verification is then executed after the last data has been transmitted and writing has been completed.

The write start/end address can be set only in the block start/end address units.

Addresses must not be specified extending from the code flash memory to data flash memory.

If both of the status frames (ST1 and ST2) after the last data transmission indicate ACK, the RL78 firmware automatically executes internal verify. Therefore, the Status command for this internal verify must be transmitted.

3.4.2 Command frame and status frame

Figure 3-9 shows the format of a command frame for the Programming command, and Figure 3-10 shows the status frame for the command.

Figure 3-9. Programming Command Frame (from Programmer to RL78)

SOH	LEN	COM	Command Information						SUM	ETX
01H	07H	40H (Programming)	SAL	SAM	SAH	EAL	EAM	EAH	Checksum	03H

Remark SAH to SAL: Write start addresses
EAH to EAL: Write end addresses

Figure 3-10. Status Frame for Programming Command (from RL78 to Programmer)

STX	LEN	Data	SUM	ETX
02H	01H	ST1 (a)	Checksum	03H

Remark ST1 (a): Command reception result

3.4.3 Data frame and status frame

Figure 3-11 shows the format of a frame that includes data to be written, and Figure 3-12 shows the status frame for the data.

Figure 3-11. Data Frame to Be Written (from Programmer to RL78)

STX	LEN	Data	SUM	ETX/ETB
02H	00H (= 256)	Write Data	Checksum	03H/17H

Remark Write Data: User program to be written

Figure 3-12. Status Frame for Data Frame (from RL78 to Programmer)

STX	LEN	Data		SUM	ETX
02H	02H	ST1 (b)	ST2 (b)	Checksum	03H

Remark ST1 (b): Data reception check result
ST2 (b): Write result

3.4.4 Completion of transferring all data and status frame

Figure 3-13 shows the status frame after transfer of all data is completed.

Figure 3-13. Status Frame After Completion of Transferring All Data (from RL78 to Programmer)

STX	LEN	Data	SUM	ETX
02H	01H	ST1 (c)	Checksum	03H

Remark ST1 (c): Internal verify result

See **4.7 Programming Command** for details on the flowchart of the processing sequence between the programmer and the RL78, and the flowchart of command processing.

3.5 Verify Command

3.5.1 Description

This command is used to compare the data transmitted from the programmer with the data read from the RL78 (read level) in the specified address range, and check whether they match.

The verify start/end address can be set only in the block start/end address units.

Addresses must not be specified extending from the code flash memory to data flash memory.

3.5.2 Command frame and status frame

Figure 3-14 shows the format of a command frame for the Verify command, and Figure 3-15 shows the status frame for the command.

Figure 3-14. Verify Command Frame (from Programmer to RL78)

SOH	LEN	COM	Command Information						SUM	ETX
01H	07H	13H (Verify)	SAL	SAM	SAH	EAL	EAM	EAH	Checksum	03H

Remark SAH to SAL: Verify start addresses
EAH to EAL: Verify end addresses

Figure 3-15. Status Frame for Verify Command (from RL78 to Programmer)

STX	LEN	Data	SUM	ETX
02H	01H	ST1 (a)	Checksum	03H

Remark ST1 (a): Command reception result

3.5.3 Data frame and status frame

Figure 3-16 shows the format of a frame that includes data to be verified, and Figure 3-17 shows the status frame for the data.

Figure 3-16. Data Frame of Data to Be Verified (from Programmer to RL78)

STX	LEN	Data	SUM	ETX/ETB
02H	00H (= 256)	Verify Data	Checksum	03H/17H

Remark Verify Data: User program to be verified

Figure 3-17. Status Frame for Data Frame (from RL78 to Programmer)

STX	LEN	Data		SUM	ETX
02H	02H	ST1 (b)	ST2 (b)	Checksum	03H

Remark ST1 (b): Data reception check result
ST2 (b): Verify result[Note]

Note Even if a verify error occurs in the specified address range, ACK is always returned as the verify result. The status of all verify errors are reflected in the verify result for the last data. Therefore, the occurrence of verify errors can be checked only when all the verify processing for the specified address range is completed.

See **4.8 Verify Command** for details on the flowchart of the processing sequence between the programmer and the RL78, and the flowchart of command processing.

3.6 Block Blank Check Command

3.6.1 Description

This command is used to check if a block in the flash memory, with a specified block number, is blank (erased state).

A block can be specified with the start address of the blank check start block and the last address of the blank check end block. Successive multiple blocks can be specified. However, blocks must not be specified extending from the code flash memory to data flash memory.

To execute the Block Blank Check command alone, set the blank check area specification field (D01) to “00H” regardless of the specified range. Set D01 to “01H” to execute the Block Blank Check command with all the blocks specified and before the flash memory is erased.

3.6.2 Command frame and status frame

Figure 3-18 shows the format of a command frame for the Block Blank Check command, and Figure 3-19 shows the status frame for the command.

Figure 3-18. Block Blank Check Command Frame (from Programmer to RL78)

SOH	LEN	COM	Command Information							SUM	ETX
01H	08H	32H (Block Blank Check)	SAL	SAM	SAH	EAL	EAM	EAH	D01	Checksum	03H

Remark SAH to SAL: Block blank check start address (start address of any block)
SAM: Start address, middle (bits 15 to 8)
SAL: Start address, low (bits 7 to 0)
SAH: Start address, high (bits 23 to 16)
EAH to EAL: Block blank check end address (last address of any block)
EAM: End address, middle (bits 15 to 8)
EAL: End address, low (bits 7 to 0)
EAH: End address, high (bits 23 to 16)
D01: Blank check specification area
00H: Specified block (When performing a block blank check for a single block)
01H: Specified block and flash option (When performing a blank check for the complete area before erasing the chip)

Figure 3-19. Status Frame for Block Blank Check Command (from RL78 to Programmer)

STX	LEN	Data	SUM	ETX
02H	01H	ST1	Checksum	03H

Remark ST1: Block blank check result

See **4.9 Block Blank Check Command** for details on the flowchart of the processing sequence between the programmer and the RL78, and the flowchart of command processing.

3.7 Silicon Signature Command

3.7.1 Description

This command is used to read information (silicon signature) of the RL78.

3.7.2 Command frame and status frame

Figure 3-20 shows the format of a command frame for the Silicon Signature command, and Figure 3-21 shows the status frame for the command.

Figure 3-20. Silicon Signature Command Frame (from Programmer to RL78)

SOH	LEN	COM	SUM	ETX
01H	01H	C0H (Silicon Signature)	Checksum	03H

Figure 3-21. Status Frame for Silicon Signature Command (from RL78 to Programmer)

STX	LEN	Data	SUM	ETX
02H	01H	ST1	Checksum	03H

Remark ST1: Command reception result

3.7.3 Silicon signature data frame

Figure 3-22 shows the format of a frame that includes silicon signature data.

Figure 3-22. Silicon Signature Data Frame (from RL78 to Programmer)

STX	LEN	Data					SUM	ETX
02H	16H	DEC (3 bytes)	DEV (10 bytes)	CEN (3 bytes)	DEN (3 bytes)	VER (3 bytes)	checksum	03H

Remark DEC: Device code
DEV: Device name
CEN: Last address of code flash ROM
Example) In the case of 00FFFFH: FFH, FFH, 00H
DEN: Last address of data flash ROM
Example) In the case of 0F1FFFH: FFH, 1FH, 0FH
000000H is transmitted with a model not supporting the data flash memory.
VER: Firmware version
Example) If version is V1.23: 01H, 02H, 03H

Table 3-2. Example of Silicon Signature Data (R5F100LE (RL78/G13))

Field Name	Content	Length (Byte)	Example of Silicon Signature Data
DEC	Device code	3	10H
			00H
			06H
DEV	Device name	10	52H = ‘R’
			35H = ‘5’
			46H = ‘F’
			31H = ‘1’
			30H = ‘0’
			20H = ‘0’
			4CH = ‘L’
			45H = ‘E’
			20H = ‘ ’
			20H = ‘ ’
CEN	Code flash ROM last address (00FFFFh)	3	FFH
			FFH
			00H
DEN	Data flash ROM last address (001FFFh)	3	FFH
			1FH
			00H
VER	Firmware version (V1.23)	3	01H
			02H
			03H

See **4.10 Silicon Signature Command** for details on the flowchart of the processing sequence between the programmer and the RL78, and the flowchart of command processing.

3.8 Checksum Command

3.8.1 Description

This command is used to acquire the checksum data in the specified area.

For the checksum calculation start/end address, specify a fixed address in block units (1 KB) starting from the top of the flash memory.

Addresses must not be specified extending from the code flash memory to data flash memory.

Checksum data is obtained by sequentially subtracting data in the specified address range from the initial value (0000H) in 1-byte units.

3.8.2 Command frame and status frame

Figure 3-26 shows the format of a command frame for the Checksum command, and Figure 3-27 shows the status frame for the command.

Figure 3-26. Checksum Command Frame (from Programmer to RL78)

SOH	LEN	COM	Command Information						SUM	ETX
01H	07H	B0H (Checksum)	SAL	SAM	SAH	EAL	EAM	EAH	Checksum	03H

Remark SAH to SAL: Checksum calculation start addresses
EAH to EAL: Checksum calculation end addresses

Figure 3-27. Status Frame for Checksum Command (from RL78 to Programmer)

STX	LEN	Data	SUM	ETX
02H	01H	ST1	Checksum	03H

Remark ST1: Command reception result

3.8.3 Checksum data frame

Figure 3-28 shows the format of a frame that includes checksum data.

Figure 3-28. Checksum Data Frame (from RL78 to Programmer)

STX	LEN	Data		SUM	ETX
02H	02H	CK1	CK2	Checksum	03H

Remark CK1: Lower 8 bits of checksum data
CK2: Higher 8 bits of checksum data

See **4.11 Checksum Command** for details on the flowchart of the processing sequence between the programmer and the RL78, and the flowchart of command processing.

3.9 Security Set Command

3.9.1 Description

This command is used to perform security settings (enabling/disabling of write, block erase, and boot block cluster rewriting, and setting of flash shield window and others). By performing these settings with this command, rewriting of the flash memory by an unauthorized party can be restricted. The security settings performed by this command are also valid for the data flash memory.

Caution Even after the security setting, additional setting of changing from enable to disable can be performed; however, changing from disable to enable is not possible. If an attempt is made to perform such a setting, a protect error (10H) will occur. If such setting is required, the Security Release command must first be executed.
If block erase or boot block cluster rewriting has been disabled, however, the Security Release command cannot be executed. Re-confirmation of security setting execution is therefore recommended before disabling block erase or boot block cluster rewriting, due to this programmer specification.

3.9.2 Command frame and status frame

Figure 3-29 shows the format of a command frame for the Security Set command, and Figure 3-30 shows the status frame for the command.

Figure 3-29. Security Set Command Frame (from Programmer to RL78)

SOH	LEN	COM	SUM	ETX
01H	01H	A0H (Security Set)	Checksum	03H

Figure 3-30. Status Frame for Security Set Command (from RL78 to Programmer)

STX	LEN	Data	SUM	ETX
02H	01H	ST1 (a)	Checksum	03H

Remark ST1 (a): Command reception result

3.9.3 Data frame and status frame

Figure 3-31 shows the format of a security data frame, and Figure 3-32 shows the status frame for the data.

Figure 3-31. Security Data Frame (from Programmer to RL78)

STX	LEN	Data							SUM	ETX
02H	08H	FLG	BOT	SSL	SSH	SEL	SEH	RES (FFFFH)	Checksum	03H

Remarks 1. FLG: Security flag
BOT: Boot block cluster block number
RL78 with boot cluster size of 4KB (03H) RL78/G13 etc.
RL78 with boot cluster size of 8KB (07H) RL78/F13 etc.
RL78 with boot cluster size of 16KB (0FH)
SSL: Flash shield window start block number (Lower)
SSH: Flash shield window start block number (Higher)
SEL: Flash shield window end block number (Lower)
SEH: Flash shield window end block number (Higher)
RES: (Reserve)

2. If the flash shield window is not to be set, set SSL/SSH to 0000H and SEL/SEH to the target device end block number.

Figure 3-32. Status Frame for Security Data Writing (from RL78 to Programmer)

STX	LEN	Data	SUM	ETX
02H	01H	ST1 (b)	Checksum	03H

Remark ST1 (b): Security data write result

The following table shows the contents in the security flag field.

Table 3-3. Contents of Security Flag Field

Item	Contents
Bit 7	Fixed to “1”
Bit 6	Fixed to “1”
Bit 5	Fixed to “1”
Bit 4	Programming disable flag (1: Enables programming, 0: Disable programming)
Bit 3	Fixed to “1”
Bit 2	Block erase disable flag (1: Enables block erase, 0: Disable block erase)
Bit 1	Boot block cluster rewrite disable flag (1: Enables boot block cluster rewrite, 0: Disable boot block cluster rewrite)
Bit 0	Fixed to “1”

The following table shows the relationship between the security flag field settings and the enable/disable status of each operation.

Table 3-4. Security Flag Field and Enable/Disable Status of Each Operation

Command / Security Setting Item	Command Operation After Security Setting √: Execution possible, ×: Execution impossible △: Writing and erase in boot block cluster are impossible Writing and block erase in boot block cluster are impossible				
	Block Erase		Programming		Security Release
Target Area	Code flash memory	Data flash memory	Code flash memory	Data flash memory	–
Disable programming	√	√	×	×	√
Disable block erase	×	×	√	√	×
Boot block cluster rewrite disable flag	△	√	△	√	×

For the relationship between the security function and command, and for security in the self-programming mode, refer to the User's Manual of each product.

See **4.12 Security Set Command** for details on the flowchart of the processing sequence between the programmer and the RL78, and the flowchart of command processing.

3.10 Security Get Command

3.10.1 Description

This command is used to acquire security information set to the RL78 (such as writing, block erasure, enabling/disabling rewriting of boot block cluster, and setting of flash shield window).

3.10.2 Command frame and status frame

Figure 3-33 shows the format of a command frame for the Security Get command, and Figure 3-34 shows the status frame for the command.

Figure 3-33. Security Get Command Frame (from Programmer to RL78)

SOH	LEN	COM	SUM	ETX
01H	01H	A1H (Security Set)	Checksum	03H

Figure 3-34. Status Frame for Security Get Command (from RL78 to Programmer)

STX	LEN	Data	SUM	ETX
02H	01H	ST1	Checksum	03H

Remark ST1: Command reception result

3.10.3 Data frame and security flag

Figure 3-35 shows the format of a security data frame.

Figure 3-35. Security Data Frame (from RL78 to Programmer)

STX	LEN	Data							SUM	ETX
02H	08H	FLG	BOT	SSL	SSH	SEL	SEH	RES (FFFFH)	Checksum	03H

Remark FLG: Security flag
BOT: Boot block cluster block number
RL78 with boot cluster size of 4KB (03H) RL78/G13 etc.
RL78 with boot cluster size of 8KB (07H) RL78/F13 etc.
RL78 with boot cluster size of 16KB (0FH)
SSL: Flash shield window start block number (Lower)
SSH: Flash shield window start block number (Higher)
SEL: Flash shield window end block number (Lower)
SEH: Flash shield window end block number (Higher)
RES: (Reserve)

The following table shows the contents in the security flag field.

Table 3-5. Contents of Security Flag Field

Item	Contents
Bit 7	Fixed to “1”
Bit 6	Fixed to “1”
Bit 5	Fixed to “1”
Bit 4	Programming disable flag (1: Enables programming, 0: Disable programming)
Bit 3	Fixed to “1”
Bit 2	Block erase disable flag (1: Enables block erase, 0: Disable block erase)
Bit 1	Boot block cluster rewrite disable flag (1: Enables boot block cluster rewrite, 0: Disable boot block cluster rewrite)
Bit 0	Boot area exchange flag (“1”: Provided, “0”: None)

See **4.13 Security Get Command** for details on the flowchart of the processing sequence between the programmer and the RL78, and the flowchart of command processing.

3.11 Security Release Command

3.11.1 Description

This command is used to initialize the security information set to the RL78 (such as writing, block erasure, enabling/disabling rewriting of boot block cluster, and setting of flash shield window).

The Security Release command can be executed only when all the following conditions are satisfied.

- “Block erase” and “Boot block cluster rewrite” are not prohibited.
  If these are prohibited, a Protect error occurs.
- The code flash memory and data flash memory[Note] are blank.
  If they are not blank, a Blank error occurs.

Note Only with a model with data flash memory

3.11.2 Command frame and status frame

Figure 3-36 shows the format of a command frame for the Security Release command, and Figure 3-37 shows the status frame for the command.

Figure 3-36. Security Release Command Frame (from Programmer to RL78)

SOH	LEN	COM	SUM	ETX
01H	01H	A2H (Security Release)	Checksum	03H

Figure 3-37. Status Frame for Security Release Command (from RL78 to Programmer)

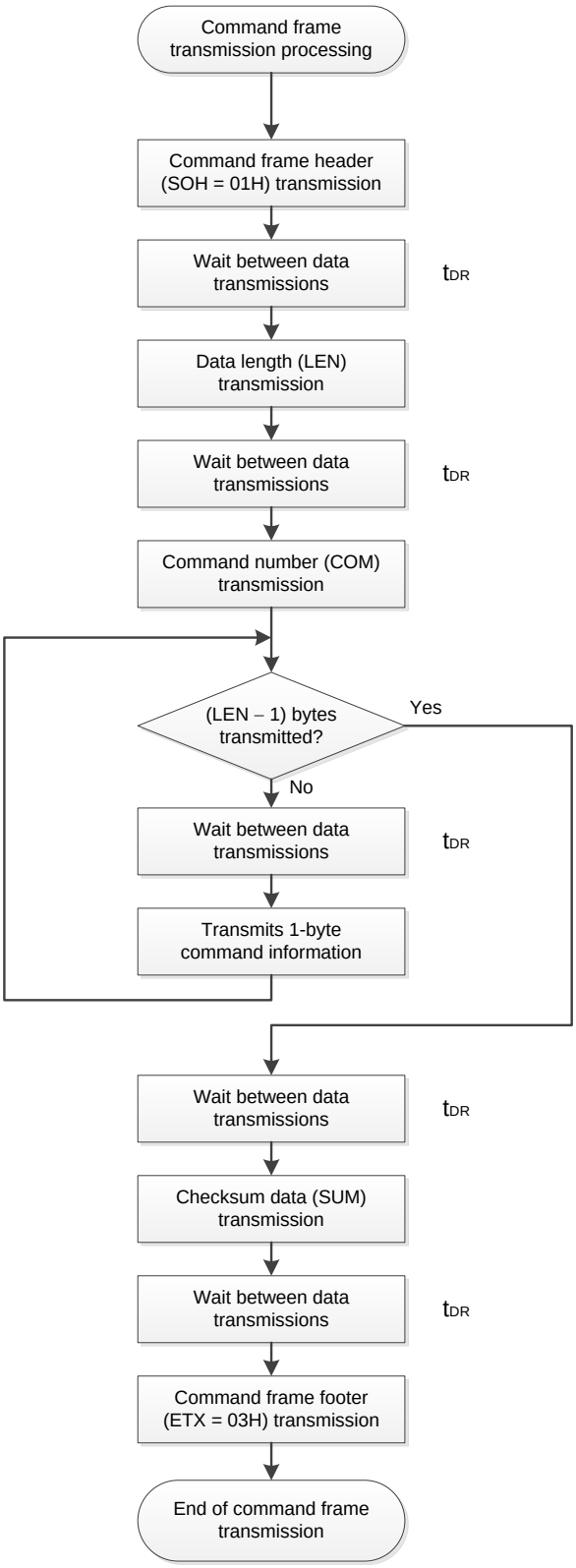
STX	LEN	Data	SUM	ETX
02H	01H	ST1	Checksum	03H

Remark ST1: Command reception result

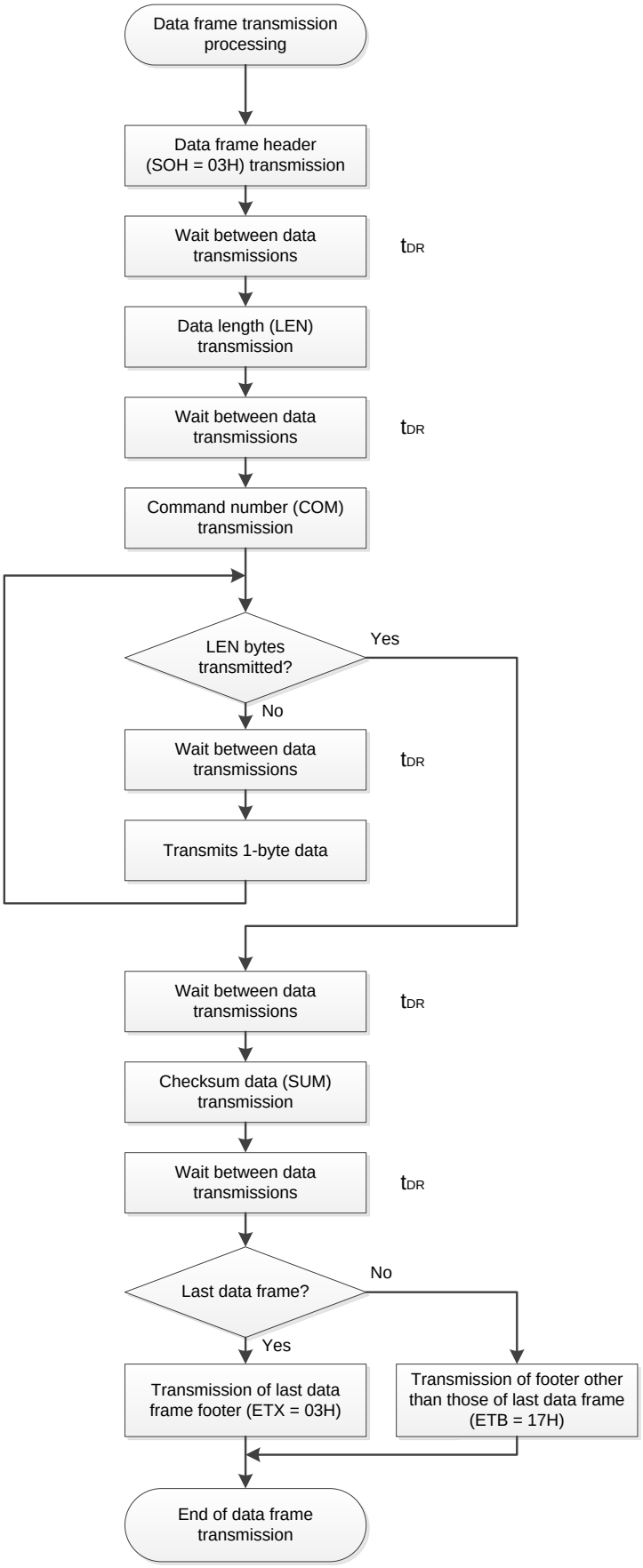
See **4.14 Security Release Command** for details on the flowchart of the processing sequence between the programmer and the RL78, and the flowchart of command processing.

CHAPTER 4 UART COMMUNICATION MODE

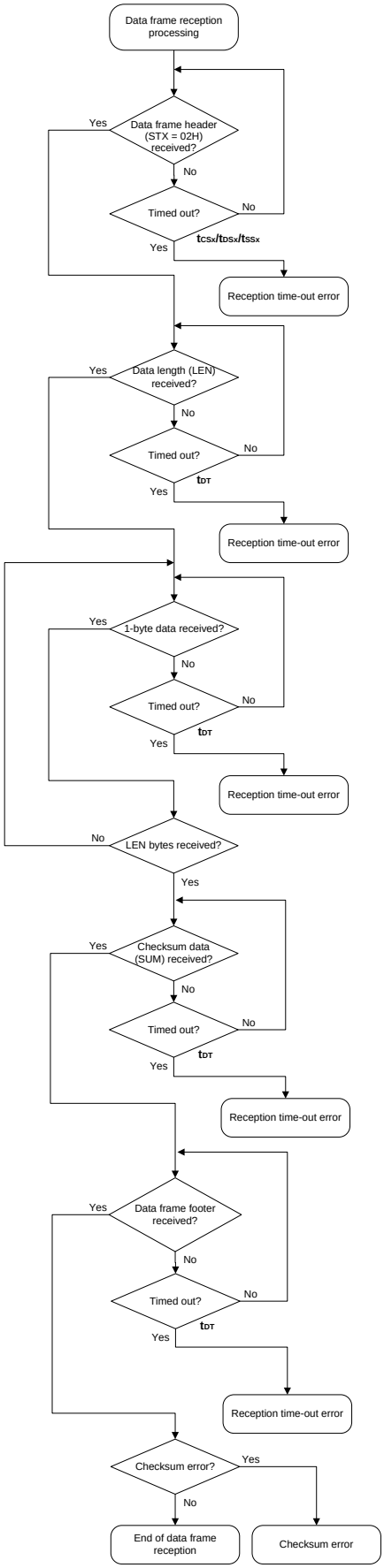
4.1 Command Frame Transmission Processing Flowchart



4.2 Data Frame Transmission Processing Flowchart



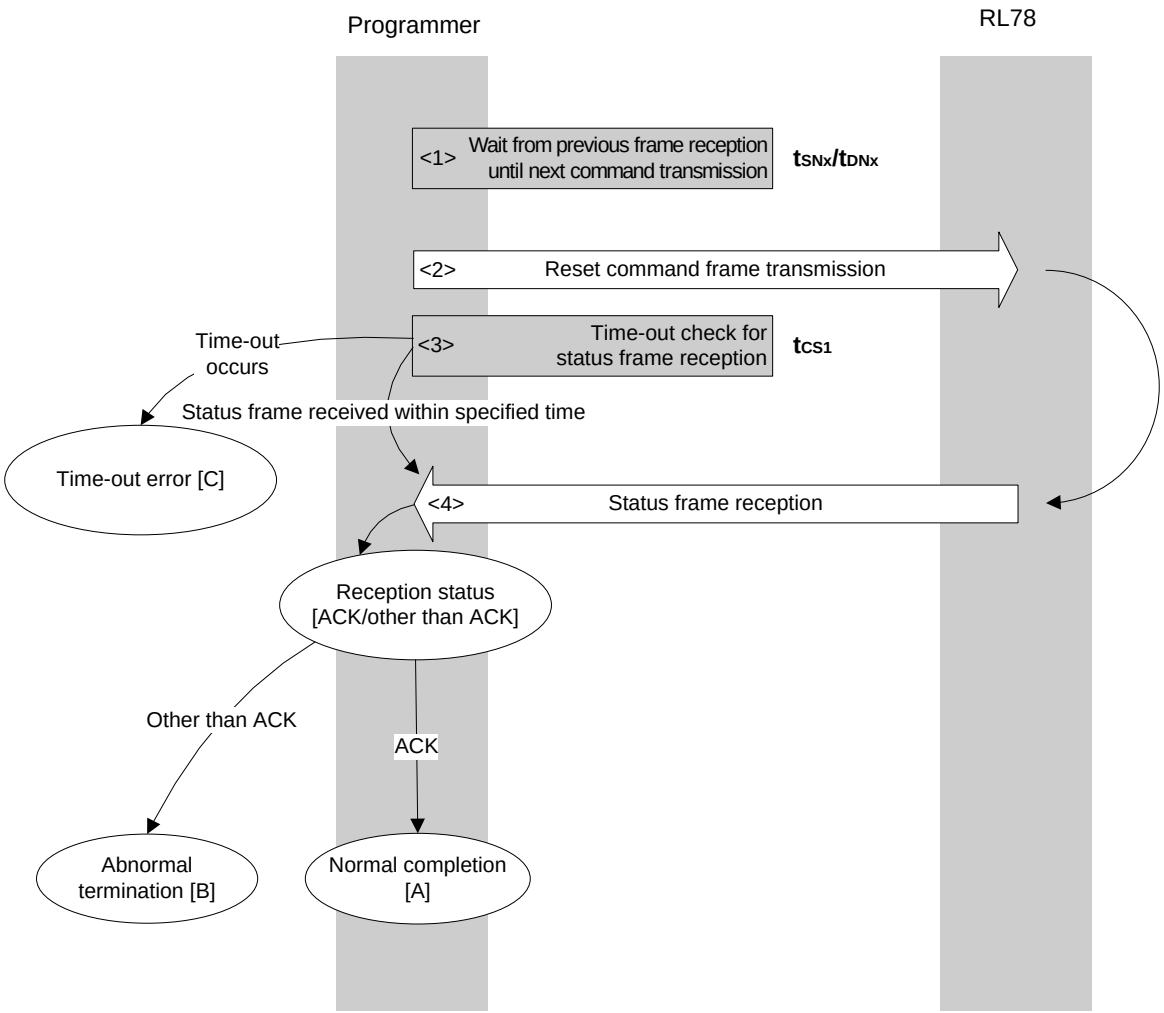
4.3 Data Frame Reception Processing Flowchart



4.4 Reset Command

4.4.1 Processing sequence chart

Reset command processing sequence



4.4.2 Description of processing sequence

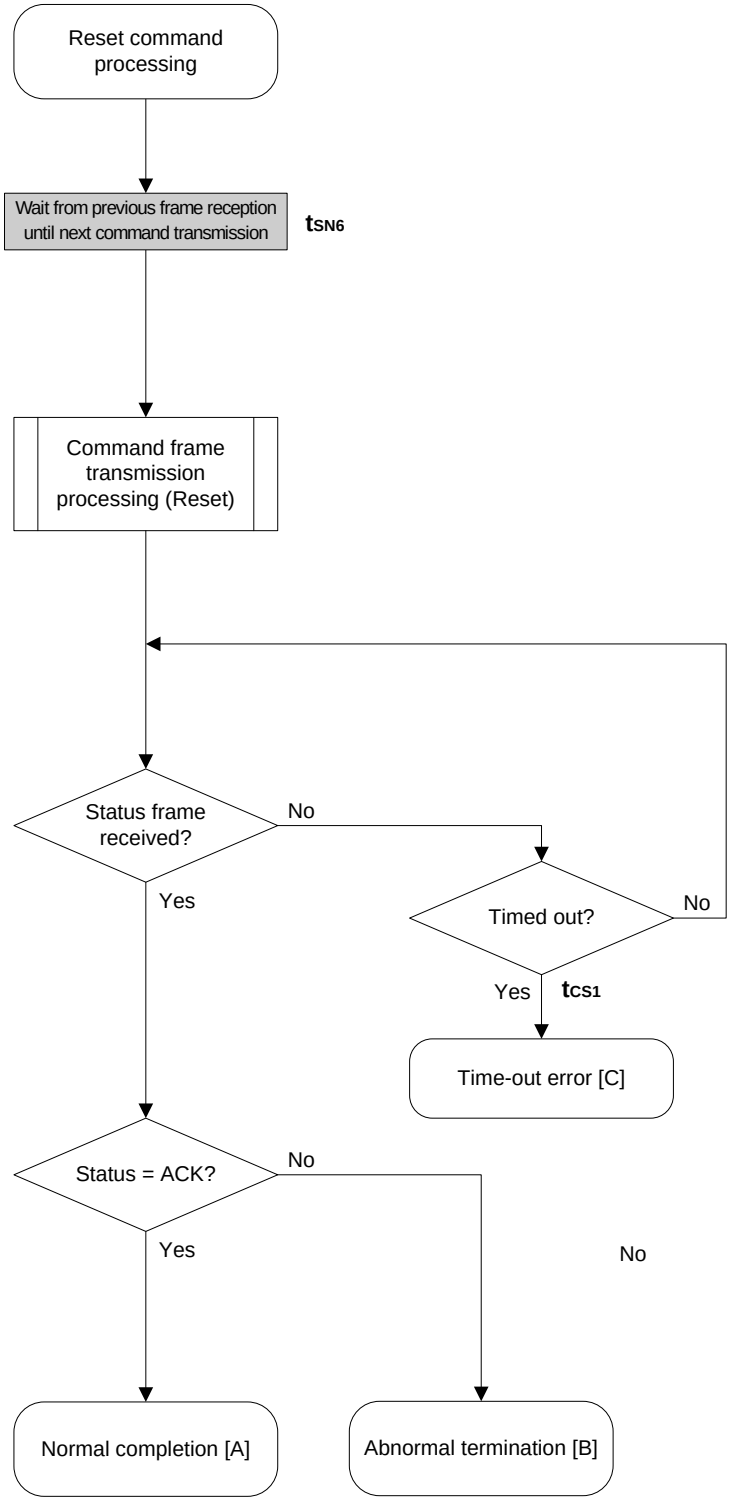
<1> Waits from the previous frame reception until the next command processing starts (wait time t_{SN6}).
<2> The Reset command is transmitted by command frame transmission processing.
<3> A time-out check is performed from command transmission until status frame reception.
If a time-out occurs, a time-out error [C] is returned (time-out time t_{CS1}).
<4> The status code is checked.

When ST1 = ACK: Normal completion [A]
When ST1 ≠ ACK: Abnormal termination [B]

4.4.3 Status at processing completion

Status at Processing Completion		Status Code	Description
Normal completion [A]	Normal acknowledgment (ACK)	06H	The command was executed normally and synchronization between the programmer and the RL78 has been established.
Abnormal termination [B]	Checksum error	07H	The checksum of the transmitted command frame does not match.
	Negative acknowledgment (NACK)	15H	Command frame data is abnormal (such as invalid data length (LEN) or no ETX).
Time-out error [C]		–	The status frame was not received within the specified time.

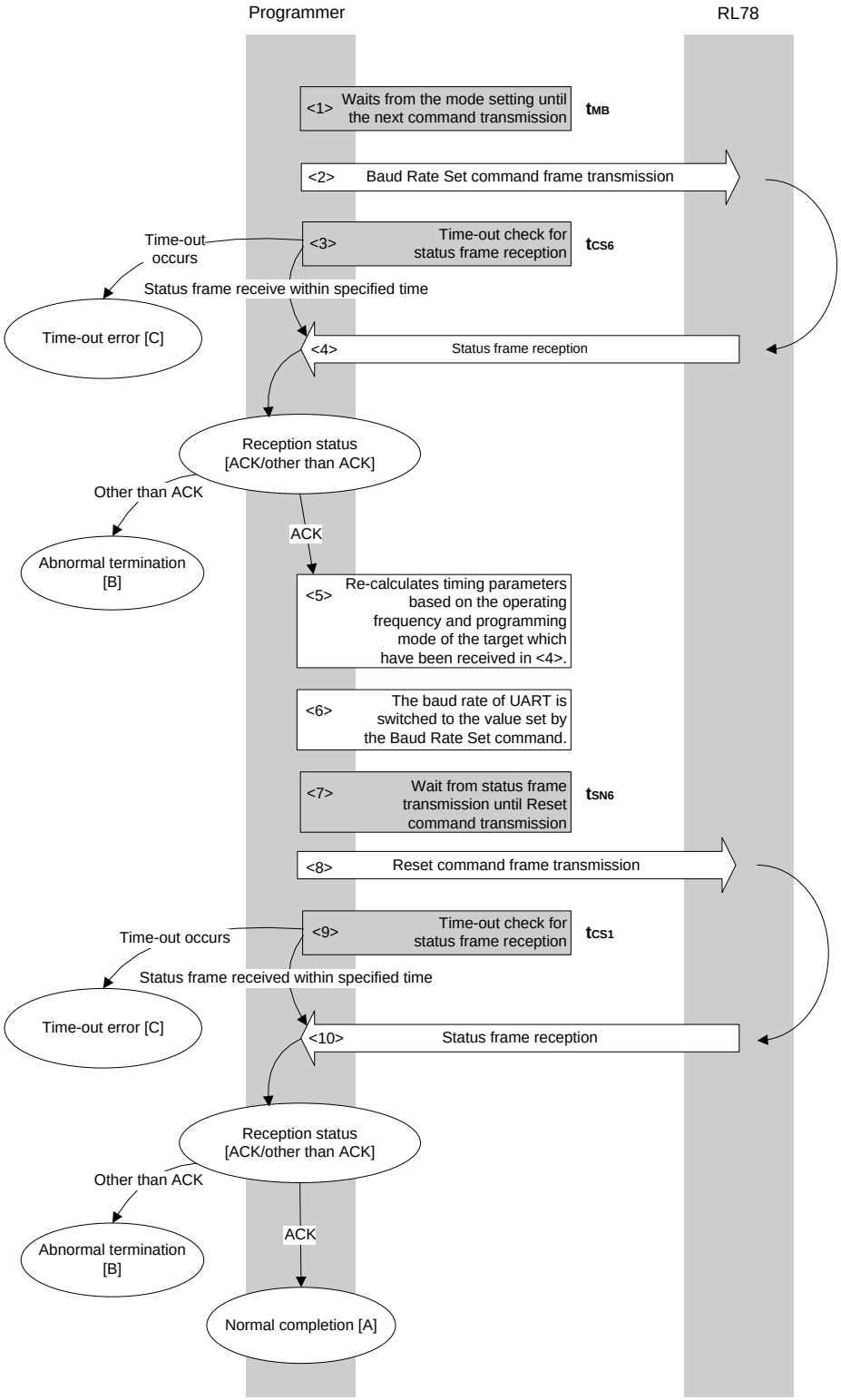
4.4.4 Flowchart



4.5 Baud Rate Set Command

4.5.1 Processing sequence chart

Baud Rate Set command processing sequence



4.5.2 Description of processing sequence

<1> Waits from the mode setting until the next command transmission (wait time t_{MB}).
<2> The Baud Rate Set command is transmitted by command frame transmission processing.
<3> A time-out check is performed from command transmission until status frame reception.
If a time-out occurs, a time-out error [C] is returned (time-out time t_{CS6}).
<4> The status code is checked.

When ST1 = ACK: Proceeds to <5>.
When ST1 ≠ ACK: Abnormal termination [B]

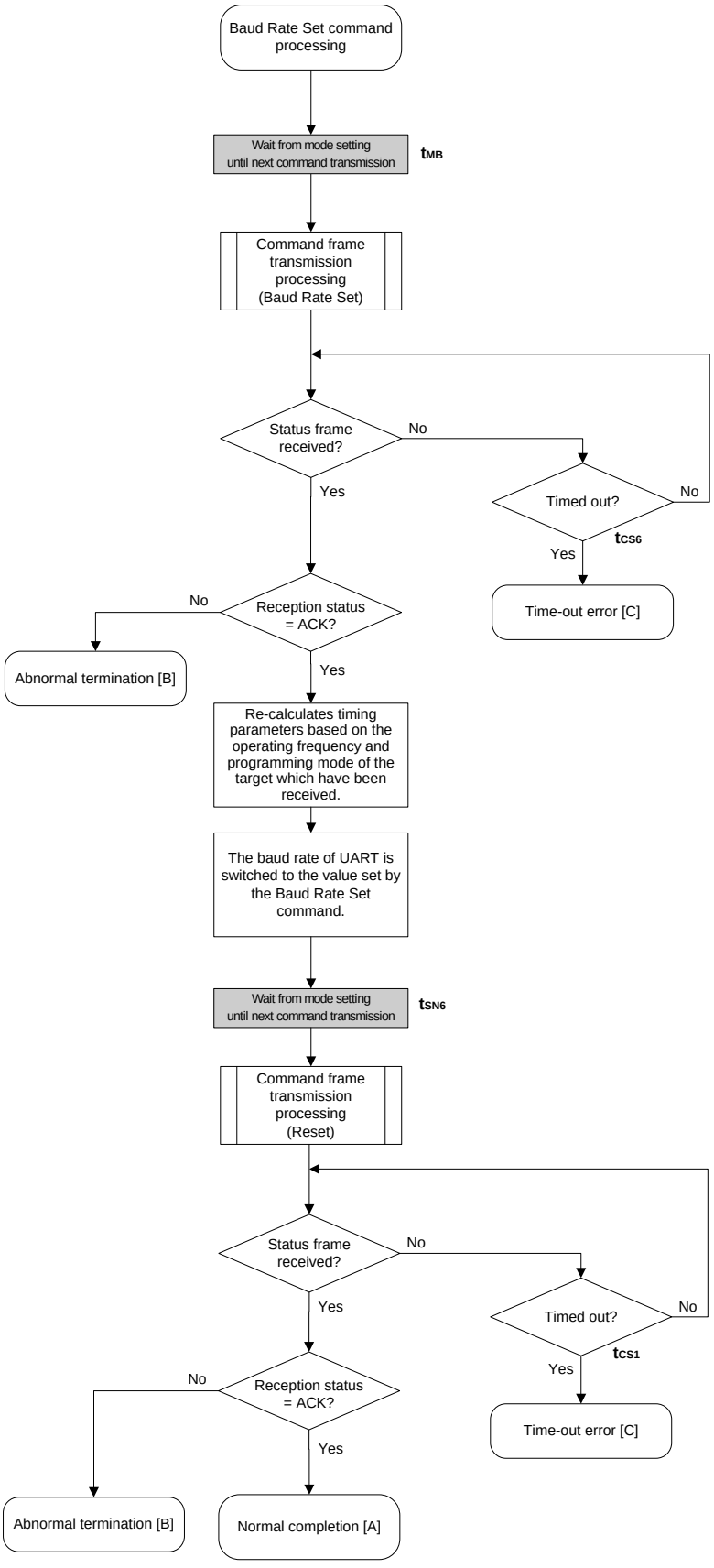
<5> Re-calculates timing parameters based on the operating frequency and programming mode of the target which have been received.
<6> Switches the baud rate for UART communication to the value set by the Baud Rate Set command.
<7> Waits from the command transmission until the Reset command transmission (wait time t_{SN6}).
<8> The Reset command is transmitted by command frame transmission processing.
<9> A time-out check is performed from command transmission until status frame reception.
If a time-out occurs, a time-out error [C] is returned (time-out time t_{CS1}).
<10> The status code is checked.
When ST1 = ACK: Normal completion [A]
When ST1 ≠ ACK: Abnormal termination [B]

4.5.3 Status at processing completion

Status at Processing Completion		Status Code	Description
Normal completion [A]	Normal acknowledgment (ACK)	06H	The command was executed normally and the synchronization of the UART communication speed has been established between the programmer and the RL78.
Abnormal termination [B]	Checksum error	07H	The checksum of the transmitted command frame does not match.
	Command number error	04H	Command other than Baud Rate Set command has been received.
	Parameter error	05H	Command information (D01) is illegal. Or, command information (D02) indicates less than 1.8 V.
	Negative acknowledgment (NACK)	15H	Command frame data is abnormal (such as invalid data length (LEN) or no ETX).
Time-out error [C]Note		–	Data frame reception was timed out.

Note If the Baud Rate Set command has not been completed normally, execute a hardware reset and re-set to the flash memory programming mode.

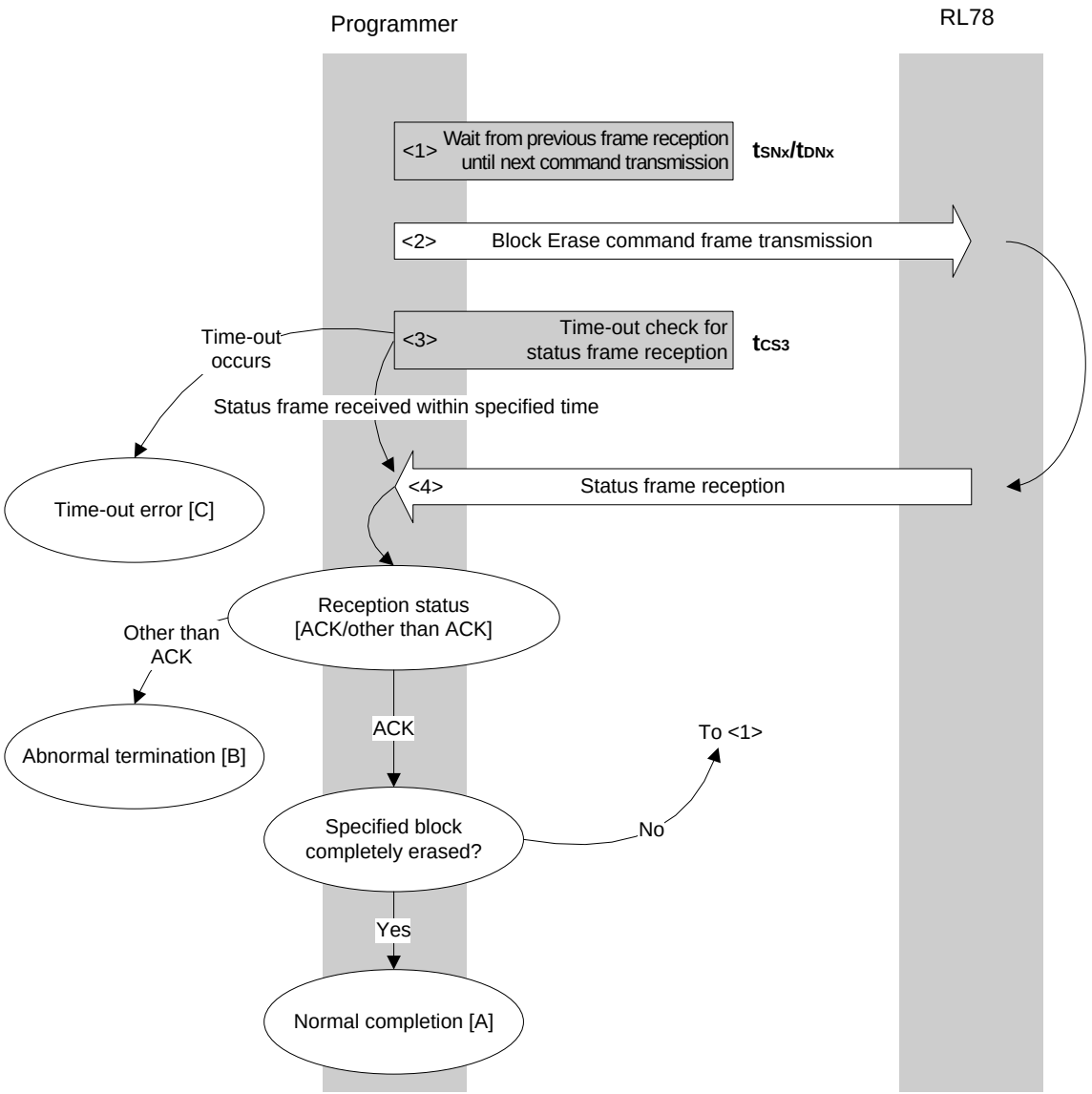
4.5.4 Flowchart



4.6 Block Erase Command

4.6.1 Processing sequence chart

Block Erase command processing sequence



4.6.2 Description of processing sequence

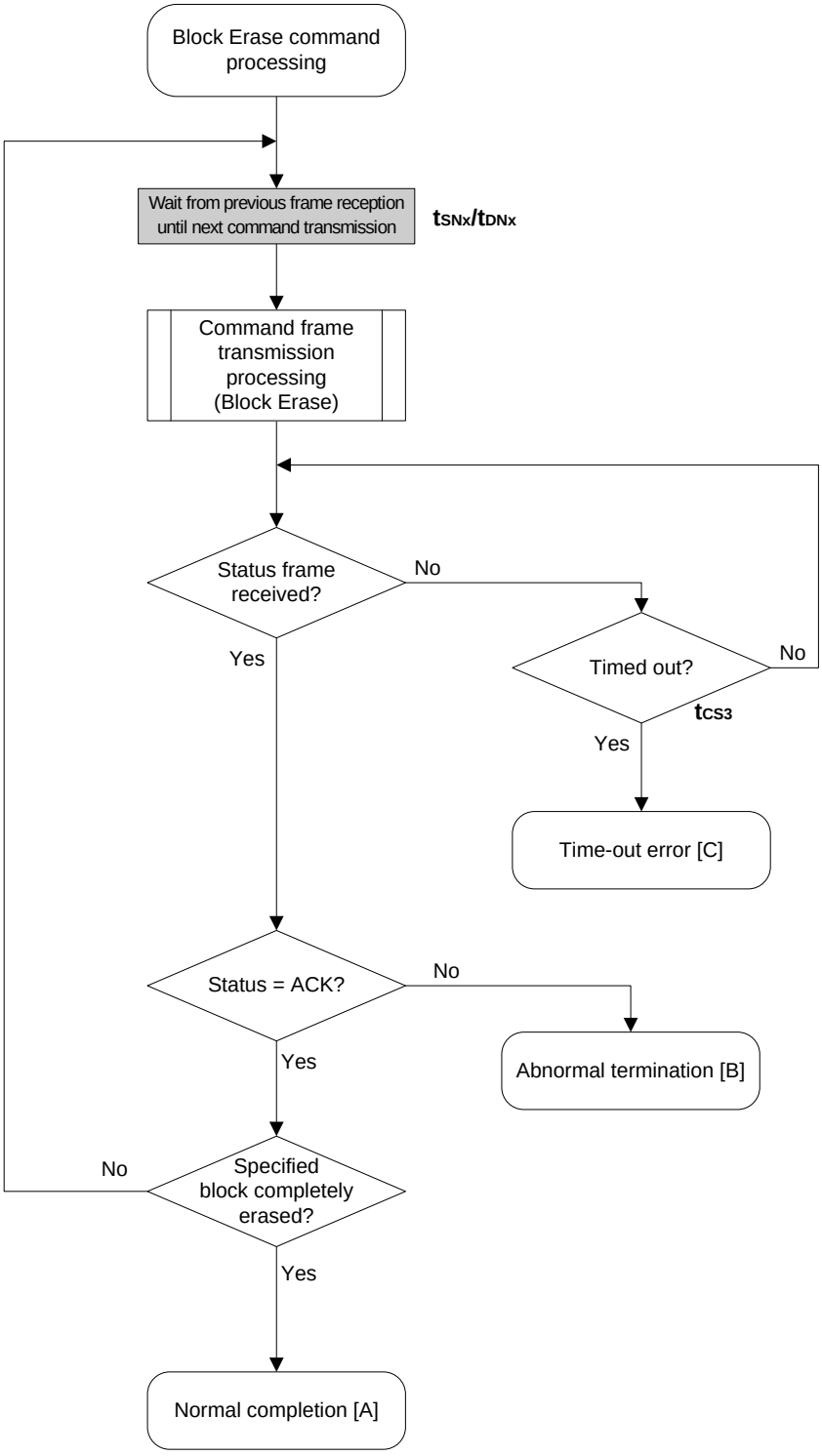
<1> Waits from the previous frame reception until the next command transmission (wait time t_{SNx}/t_{DNx}).
<2> The Block Erase command is transmitted by command frame transmission processing.
<3> A time-out check is performed from command transmission until status frame reception.
If a time-out occurs, a time-out error [C] is returned (time-out time t_{CS3}).
<4> The status code is checked.

When ST1 = ACK: Normal completion [A] if the specified block has been erased.
Returns to <1> if the specified block has not been erased.
When ST1 ≠ ACK: Abnormal termination [B]

4.6.3 Status at processing completion

Status at Processing Completion		Status Code	Description
Normal completion [A]	Normal acknowledgment (ACK)	06H	The command was executed normally and block erase was performed normally.
Abnormal termination [B]	Parameter error	05H	The specified start address is not the first address of the block.
	Checksum error	07H	The checksum of the transmitted command frame does not match.
	Protect error	10H	Block erase is prohibited in the security setting. A boot block is included in the specified range and boot block rewrite is prohibited.
	Negative acknowledgment (NACK)	15H	Command frame data is abnormal (such as invalid data length (LEN) or no ETX).
	Erase error	1AH	An erase error has occurred.
Time-out error [C]		–	The status frame was not received within the specified time.

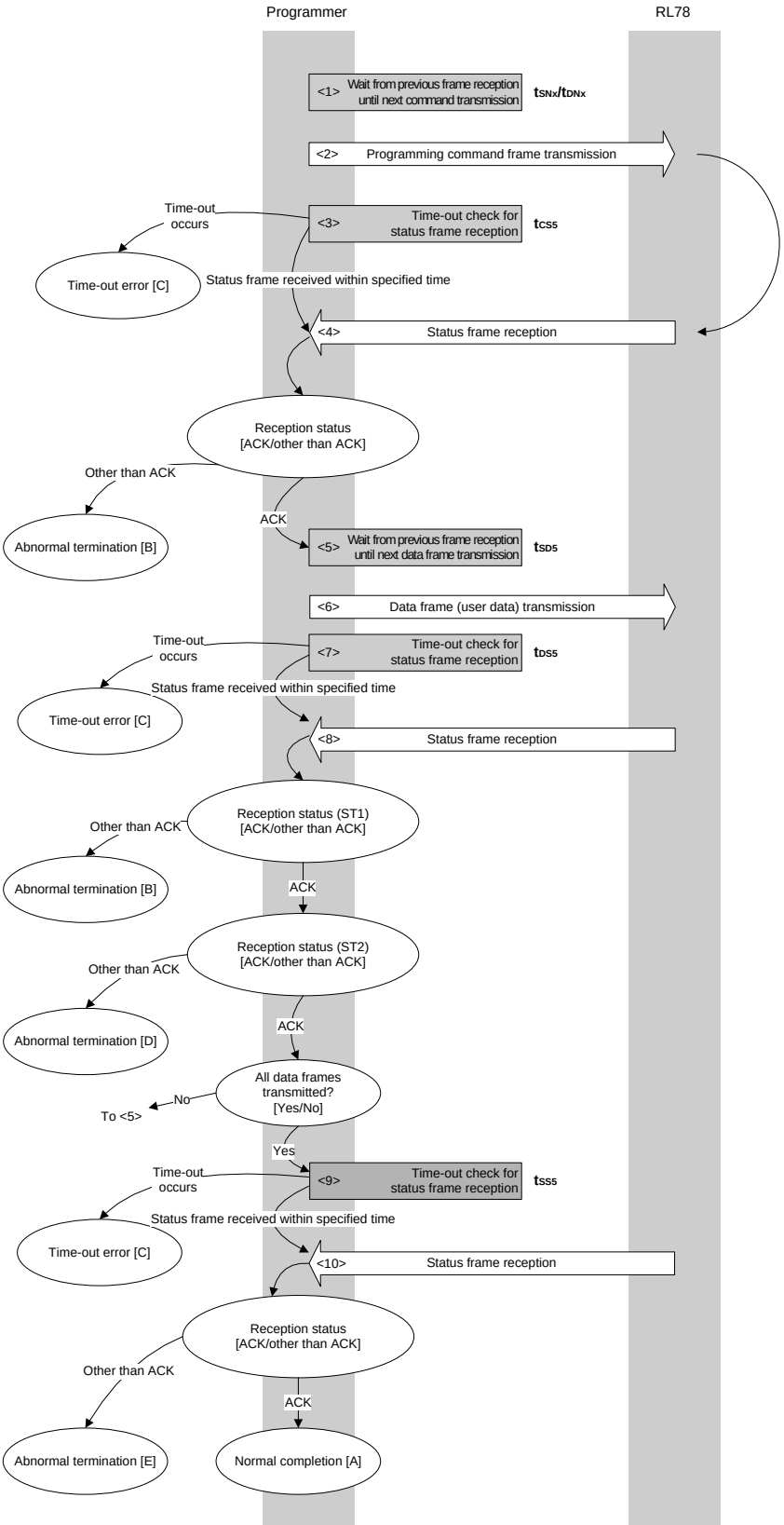
4.6.4 Flowchart



4.7 Programming Command

4.7.1 Processing sequence chart

Programming command processing sequence



4.7.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time t_{SNx}/t_{DNx}).
<2> The Programming command is transmitted by command frame transmission processing.
<3> A time-out check is performed from command transmission until status frame reception.
If a time-out occurs, a time-out error [C] is returned (time-out time t_{CS5}).
<4> The status code is checked.

When ST1 = ACK: Proceeds to <5>.
When ST1 ≠ ACK: Abnormal termination [B]

<5> Waits from the previous frame reception until the next data frame transmission (wait time t_{SD5}).
<6> User data is transmitted by data frame transmission processing.
<7> A time-out check is performed from user data transmission until data frame reception.
If a time-out occurs, a time-out error [C] is returned (time-out time t_{DS5}).
<8> The status code (ST1/ST2) is checked (also refer to the processing sequence chart and flowchart).

When ST1 ≠ ACK: Abnormal termination [B]
When ST1 = ACK: The following processing is performed according to the ST2 value.
- When ST2 = ACK: Proceeds to <9> when transmission of all data frames is completed.
  If there still remain data frames to be transmitted, the processing re-executes the sequence from <5>.
- When ST2 ≠ ACK: Abnormal termination [D]

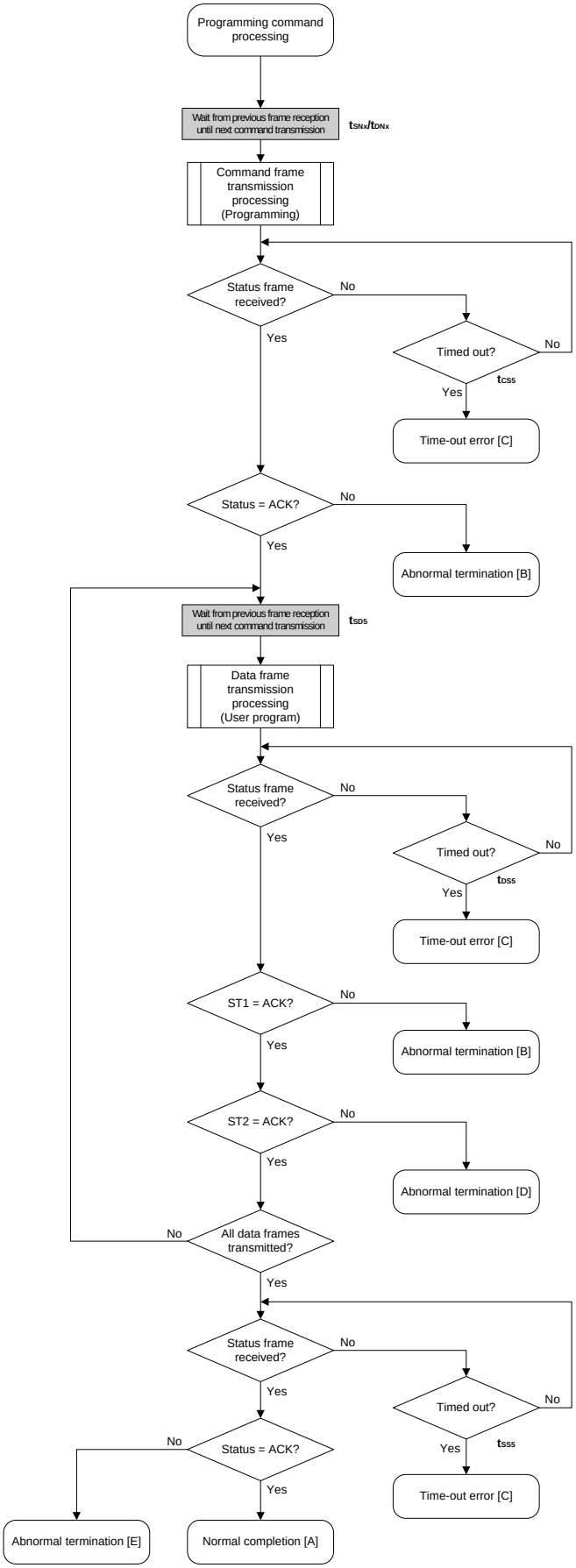
<9> A time-out check is performed until status frame reception.
If a time-out occurs, a time-out error [C] is returned (time-out time t_{SS5}).
<10> The status code is checked.

When ST1 = ACK: Normal completion [A]
When ST1 ≠ ACK: Abnormal termination [E]

4.7.3 Status at processing completion

Status at Processing Completion		Status Code	Description
Normal completion [A]	Normal acknowledgment (ACK)	06H	The command was executed normally and the user data was written normally.
Abnormal termination [B]	Parameter error	05H	The start/end address is out of the flash memory range, the specified start/end address is not the first/end address of the block, or the write start address is larger than the end address. Or, the address range specified by the start/end address extends from the code flash memory to the data flash memory.
	Checksum error	07H	The checksum of the transmitted command frame or data frame does not match.
	Protect error	10H	Write is prohibited in the security setting. A boot block is included in the specified range and boot block rewrite is prohibited.
	Negative acknowledgment (NACK)	15H	Command frame data or data frame data is abnormal (such as invalid data length (LEN) or no ETX).
Time-out error [C]		–	The status frame was not received within the specified time.
Abnormal termination [D], [E]	IVerify error	1BH	A write error has occurred.
	Write error	1CH	

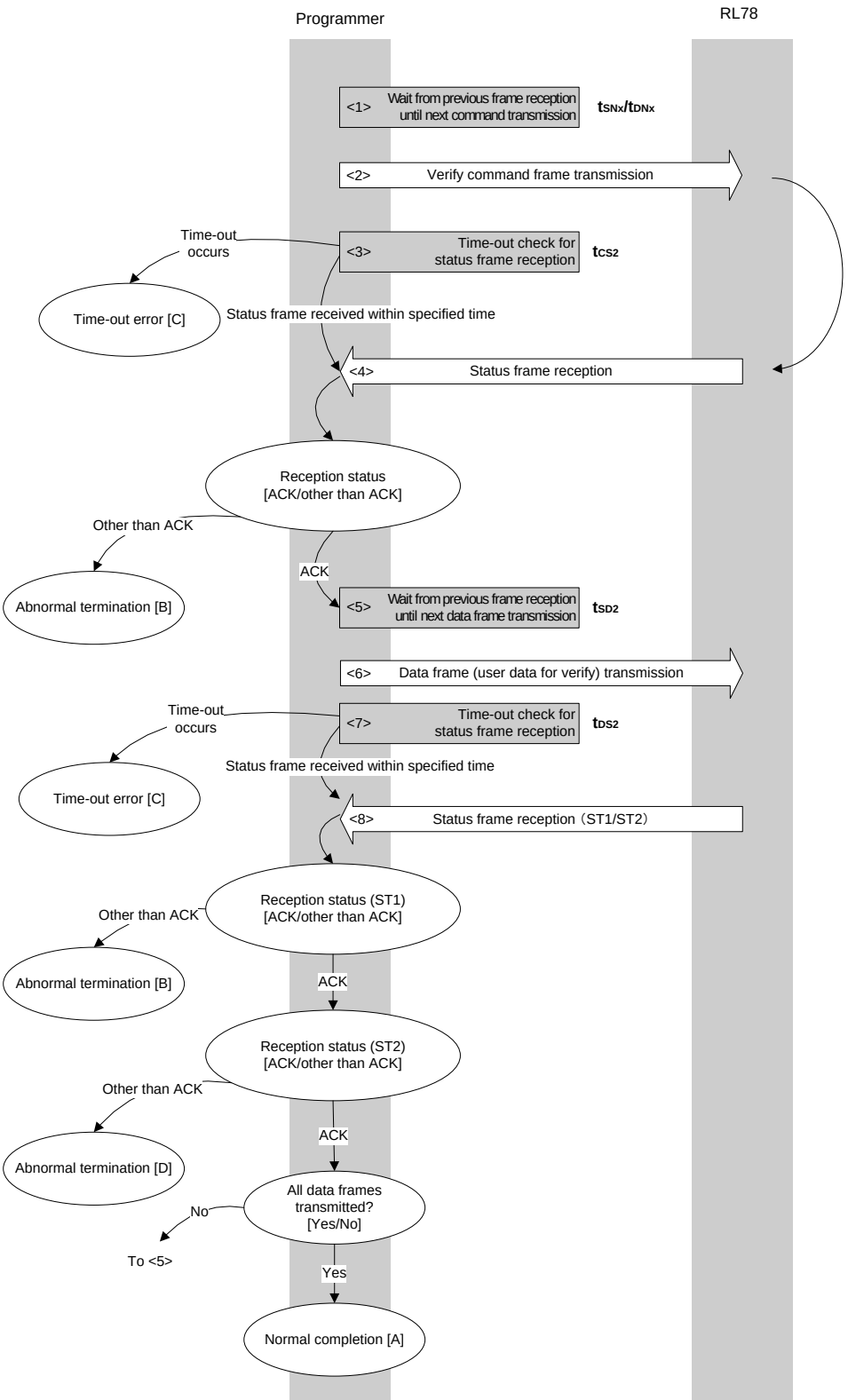
4.7.4 Flowchart



4.8 Verify Command

4.8.1 Processing sequence char

Verify command processing sequence



4.8.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time t_{SNx}/t_{DNx}).
<2> The Verify command is transmitted by command frame transmission processing.
<3> A time-out check is performed from command transmission until status frame reception.
If a time-out occurs, a time-out error [C] is returned (time-out time t_{CS2}).
<4> The status code is checked.

When ST1 = ACK: Proceeds to <5>.
When ST1 ≠ ACK: Abnormal termination [B]

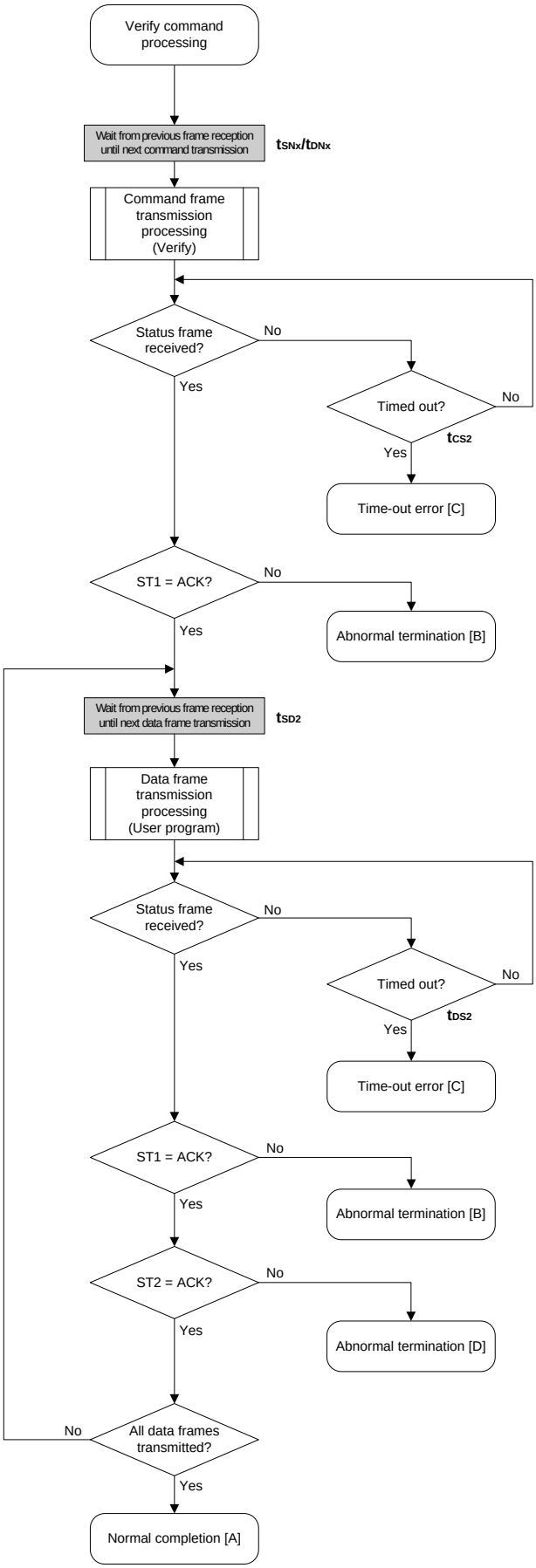
<5> Waits from the previous frame reception until the next data frame transmission (wait time t_{SD2}).
<6> User data for verifying is transmitted by data frame transmission processing.
<7> A time-out check is performed from user data transmission until status frame reception.
If a time-out occurs, a time-out error [C] is returned (time-out time t_{DS2}).
<8> The status code (ST1/ST2) is checked (also refer to the processing sequence chart and flowchart).

When ST1 ≠ ACK: Abnormal termination [B]
When ST1 = ACK: The following processing is performed according to the ST2 value.
- When ST2 = ACK: If transmission of all data frames is completed, the processing ends normally [A].
  If there still remain data frames to be transmitted, the processing re-executes the sequence from <5>.
- When ST2 ≠ ACK: Abnormal termination [D]

4.8.3 Status at processing completion

Status at Processing Completion		Status Code	Description
Normal completion [A]	Normal acknowledgment (ACK)	06H	The command was executed normally and the verify was completed normally.
Abnormal termination [B]	Parameter error	05H	The start/end address is out of the flash memory range, the start/end address is not the start/end address of the block, or the verify start address is larger than the end address. Or, the address range specified by the start/end address extends from the code flash memory to the data flash memory.
	Checksum error	07H	The checksum of the transmitted command frame or data frame does not match.
	Negative acknowledgment (NACK)	15H	Command frame data or data frame data is abnormal (such as invalid data length (LEN) or no ETX).
Time-out error [C]		–	The status frame was not received within the specified time.
Abnormal termination [D]	Verify error	0FH (ST2)	A verify error has occurred.

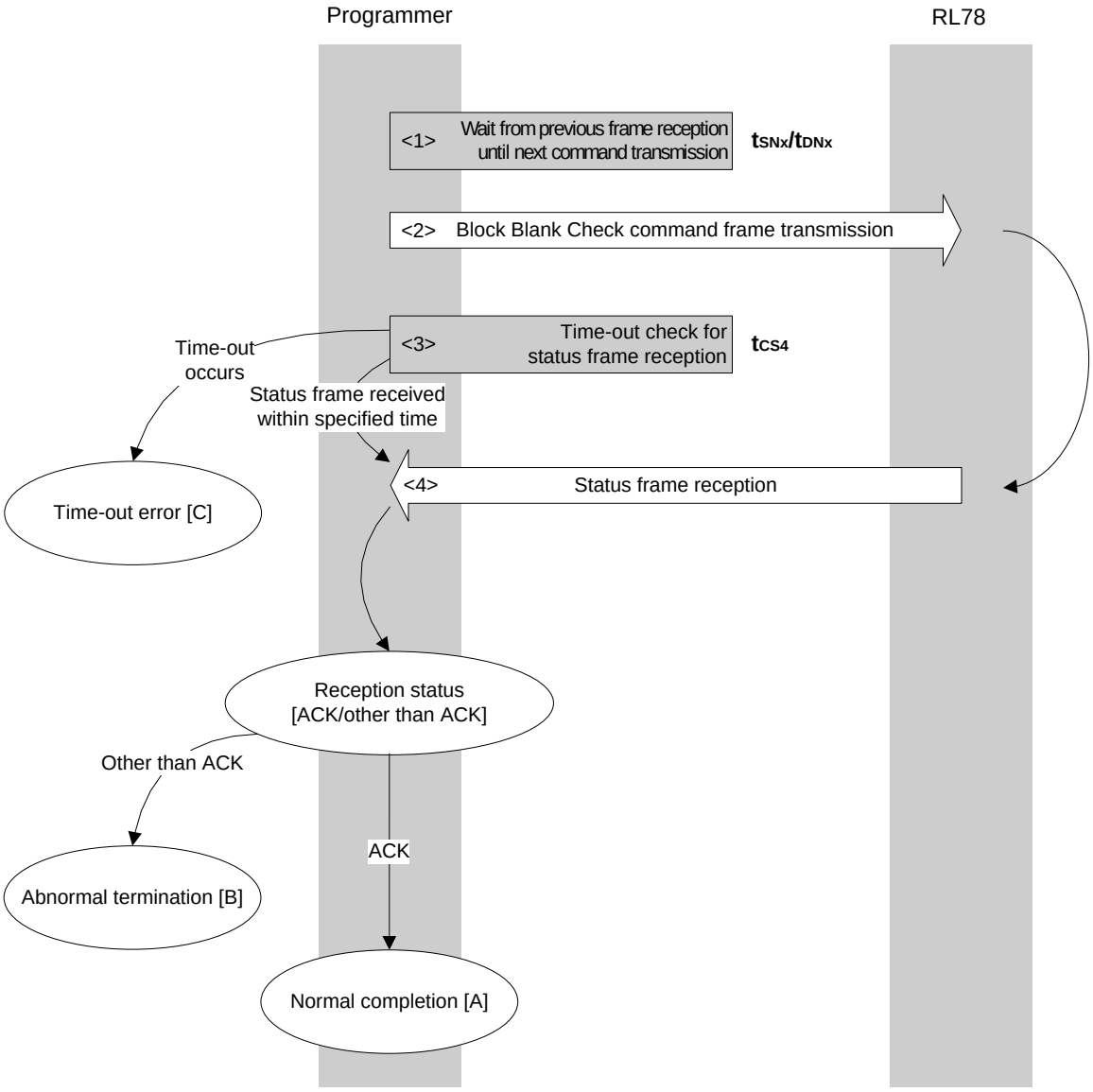
4.8.4 Flowchart



4.9 Block Blank Check Command

4.9.1 Processing sequence chart

Block Blank Check command processing sequence



4.9.2 Description of processing sequence

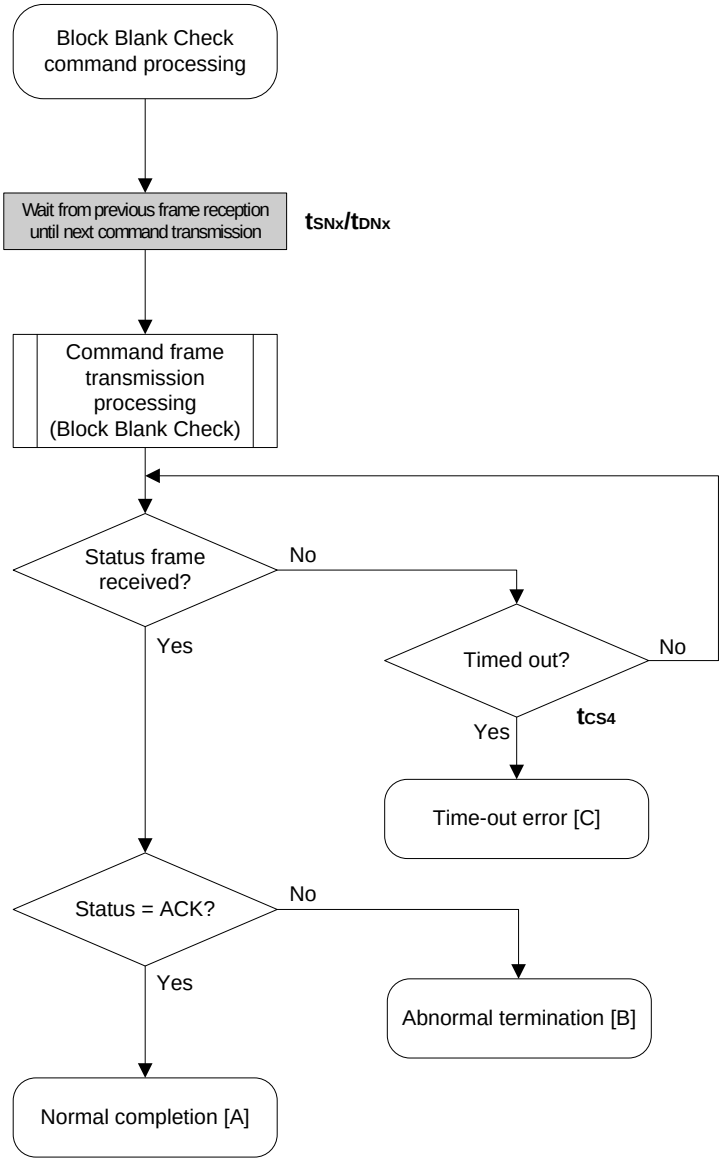
<1> Waits from the previous frame reception until the next command transmission (wait time t_{SNx}/t_{DNx}).
<2> The Block Blank Check command is transmitted by command frame transmission processing.
<3> A time-out check is performed from command transmission until status frame reception.
If a time-out occurs, a time-out error [C] is returned (time-out time t_{CS4}).
<4> The status code is checked.

When ST1 = ACK: Normal completion [A]
When ST1 ≠ ACK: Abnormal termination [B]

4.9.3 Status at processing completion

Status at Processing Completion		Status Code	Description
Normal completion [A]	Normal acknowledgment (ACK)	06H	The command was executed normally and block blank check was executed normally.
Abnormal termination [B]	Parameter error	05H	The end address is out of the flash memory range, or the start/end address is not the start/end address of the block. The start address is larger than the end address or the value of parameter D01 is other than 00H or 01H. Or, the address range specified by the start/end address extends from the code flash memory to the data flash memory.
	Checksum error	07H	The checksum of the transmitted command frame does not match.
	Negative acknowledgment (NACK)	15H	Command frame data is abnormal (such as invalid data length (LEN) or no ETX).
	Blank error	1BH	The flash memory of the specified block is not blank.
Time-out error [C]		–	The status frame was not received within the specified time.

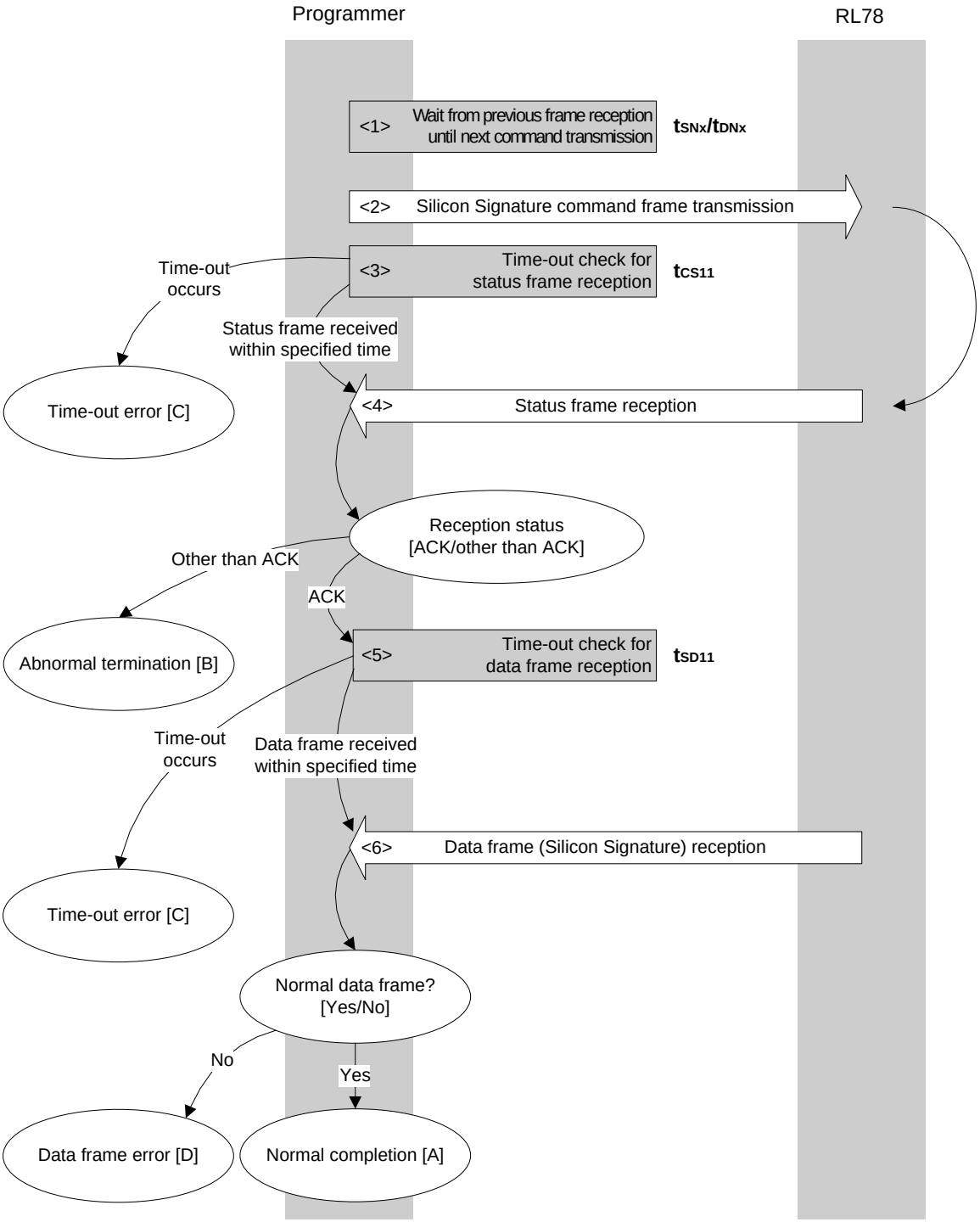
4.9.4 Flowchart



4.10 Silicon Signature Command

4.10.1 Processing sequence chart

Silicon Signature command processing sequence



4.10.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time t_{SNx}/t_{DNx}).
<2> The Silicon Signature command is transmitted by command frame transmission processing.
<3> A time-out check is performed from command transmission until status frame reception.
If a time-out occurs, a time-out error [C] is returned (time-out time t_{CS11}).
<4> The status code is checked.

When ST1 = ACK: Proceeds to <5>.
When ST1 ≠ ACK: Abnormal termination [B]

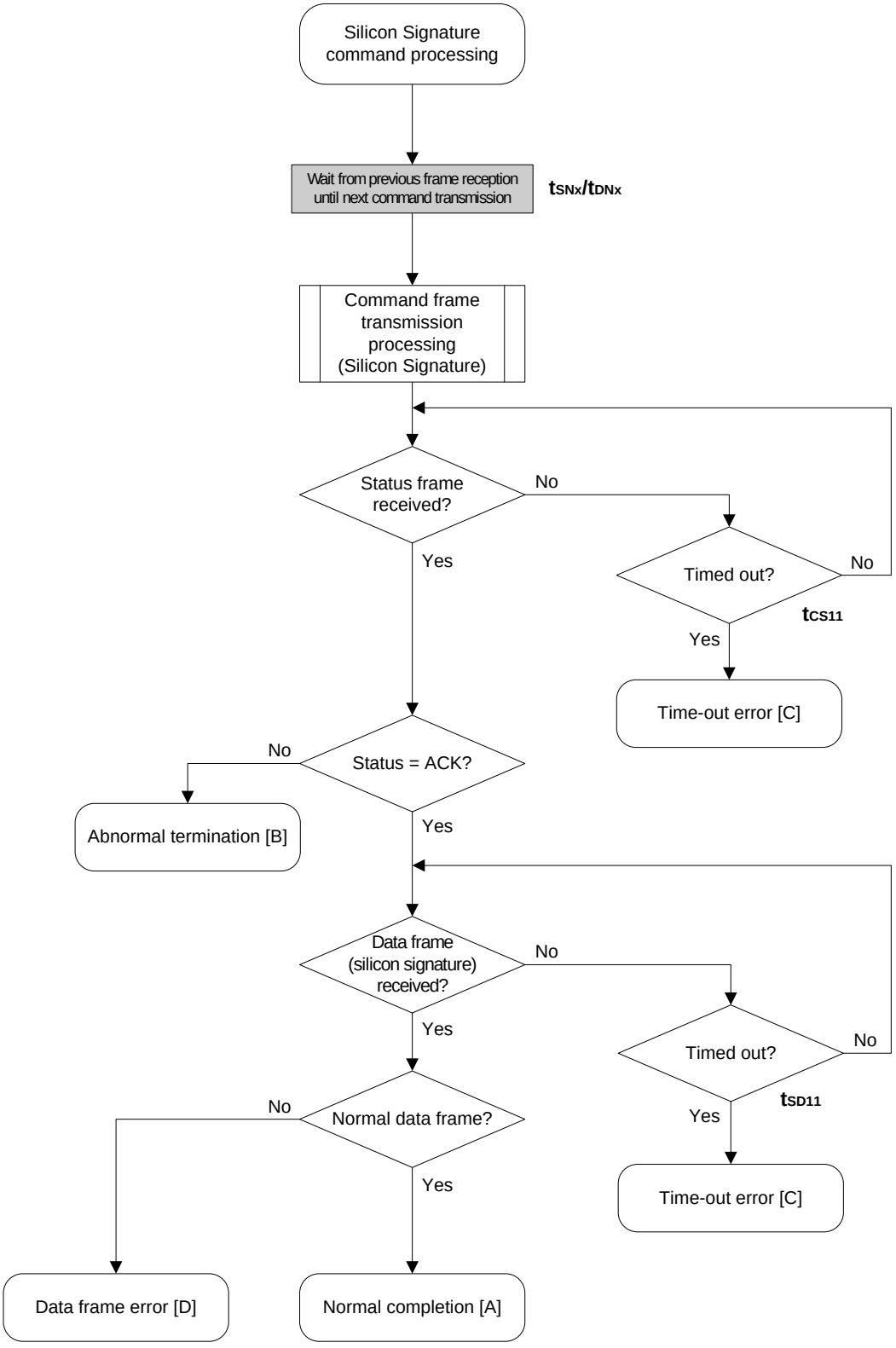
<5> A time-out check is performed until data frame (silicon signature data) reception.
If a time-out occurs, a time-out error [C] is returned (time-out time t_{SD11}).
<6> The received data frame (silicon signature data) is checked.

If data frame is normal: Normal completion [A]
If data frame is abnormal: Data frame error [D]

4.10.3 Status at processing completion

Status at Processing Completion		Status Code	Description
Normal completion [A]		–	The command was executed normally and silicon signature was acquired normally.
Abnormal termination [B]	Checksum error	07H	The checksum of the transmitted command frame does not match.
	Negative acknowledgment (NACK)	15H	Command frame data is abnormal (such as invalid data length (LEN) or no ETX).
Time-out error [C]		–	The status frame or data frame was not received within the specified time.
Data frame error [D]		–	The checksum of the data frame received as silicon signature data does not match.

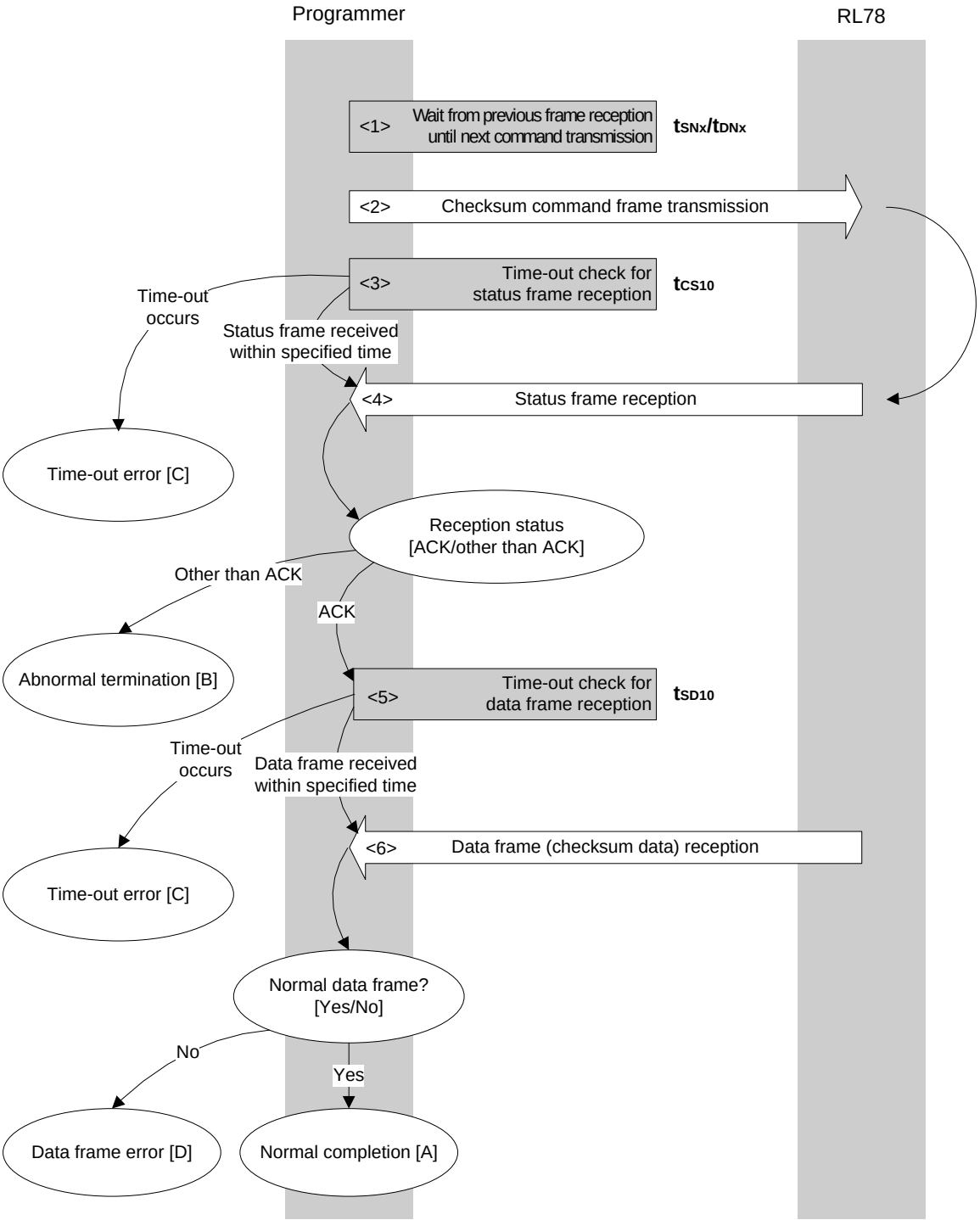
4.10.4 Flowchart



4.11 Checksum Command

4.11.1 Processing sequence chart

Checksum command processing sequence



4.11.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time t_{SNx}/t_{DNx}).
<2> The Checksum command is transmitted by command frame transmission processing.
<3> A time-out check is performed from command transmission until status frame reception.
If a time-out occurs, a time-out error [C] is returned (time-out time t_{CS10}).
<4> The status code is checked.

When ST1 = ACK: Proceeds to <5>.
When ST1 ≠ ACK: Abnormal termination [B]

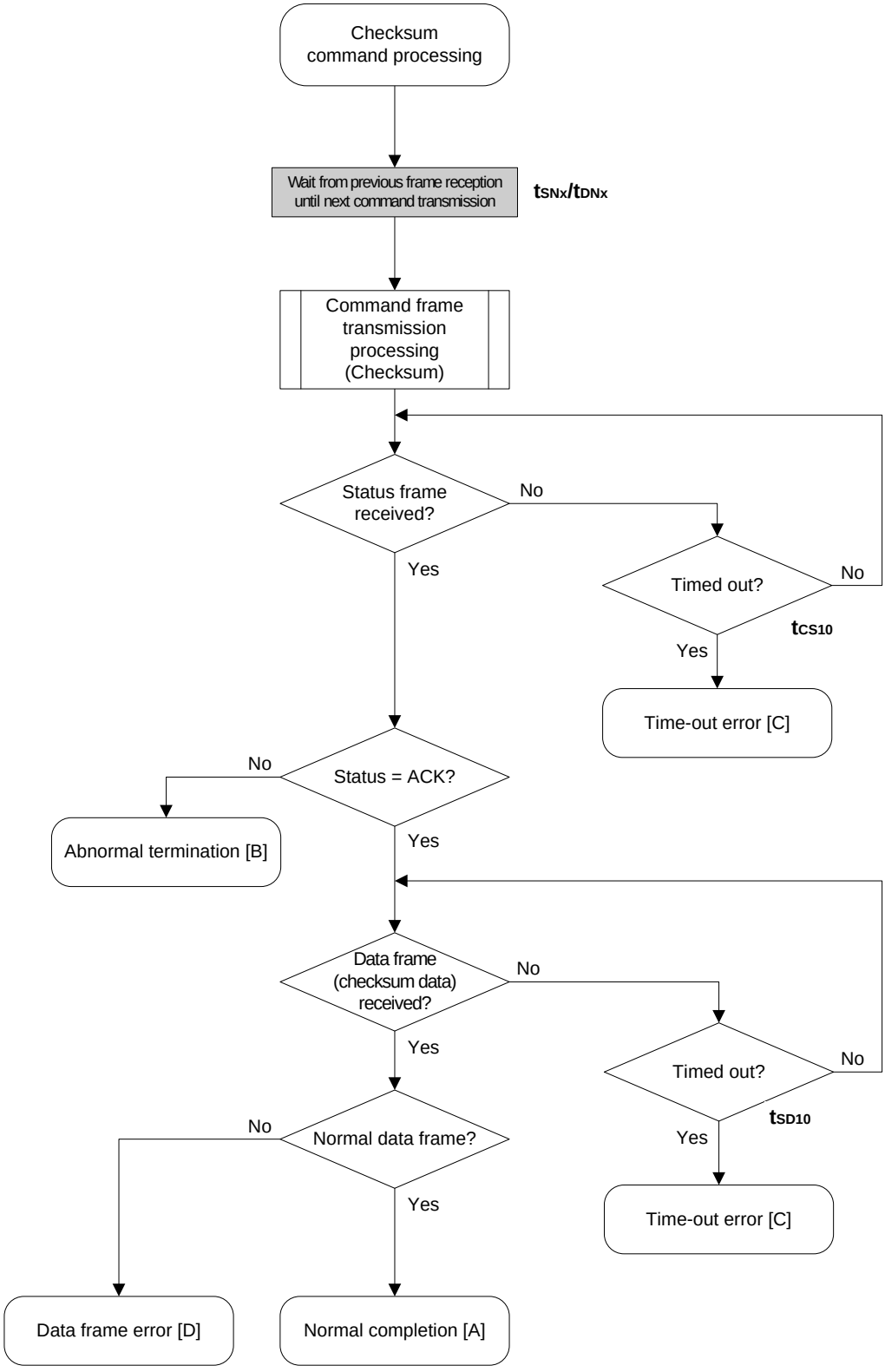
<5> A time-out check is performed until data frame (checksum data) reception.
If a time-out occurs, a time-out error [C] is returned (time-out time t_{SD10}).
<6> The received data frame (checksum data) is checked.

If data frame is normal: Normal completion [A]
If data frame is abnormal: Data frame error [D]

4.11.3 Status at processing completion

Status at Processing Completion		Status Code	Description
Normal completion [A]		–	The command was executed normally and checksum data was acquired normally.
Abnormal termination [B]	Parameter error	05H	The start/end address is out of the flash memory range. The specified start/end address is not the start/end address of the block. The start address is larger than the end address. Or, the address range specified by the start/end address extends from the code flash memory to the data flash memory.
	Checksum error	07H	The checksum of the transmitted command frame does not match.
	Negative acknowledgment (NACK)	15H	Command frame data is abnormal (such as invalid data length (LEN) or no ETX).
Time-out error [C]		–	The status frame or data frame was not received within the specified time.
Data frame error [D]		–	The checksum of the data frame received as checksum data does not match.

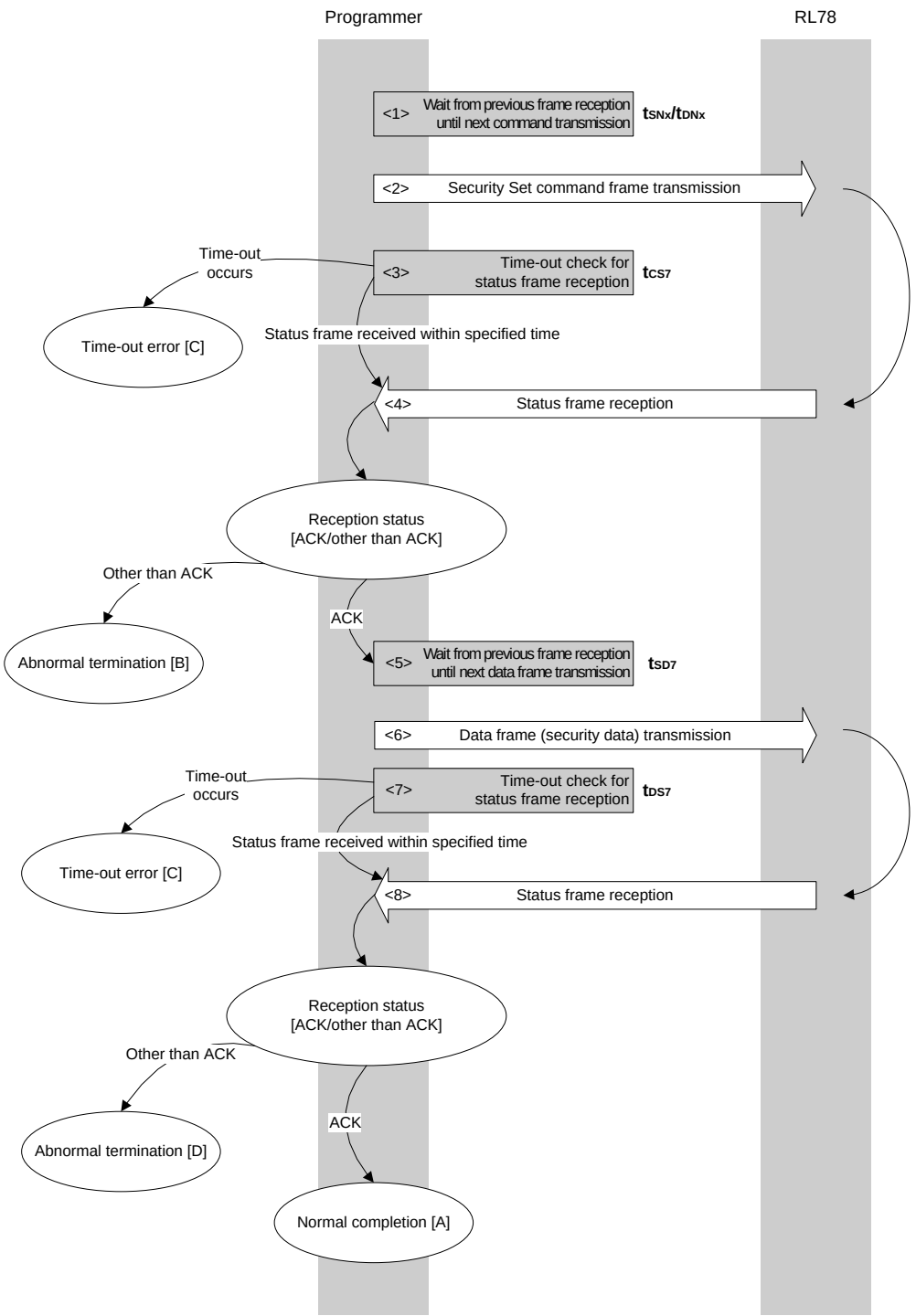
4.11.4 Flowchart



4.12 Security Set Command

4.12.1 Processing sequence chart

Security Set command processing sequence



4.12.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time t_{SNx}/t_{DNx}).
<2> The Security Set command is transmitted by command frame transmission processing.
<3> A time-out check is performed from command transmission until status frame reception.
If a time-out occurs, a time-out error [C] is returned (time-out time t_{CS7}).
<4> The status code is checked.

When ST1 = ACK: Proceeds to <5>.
When ST1 ≠ ACK: Abnormal termination [B]

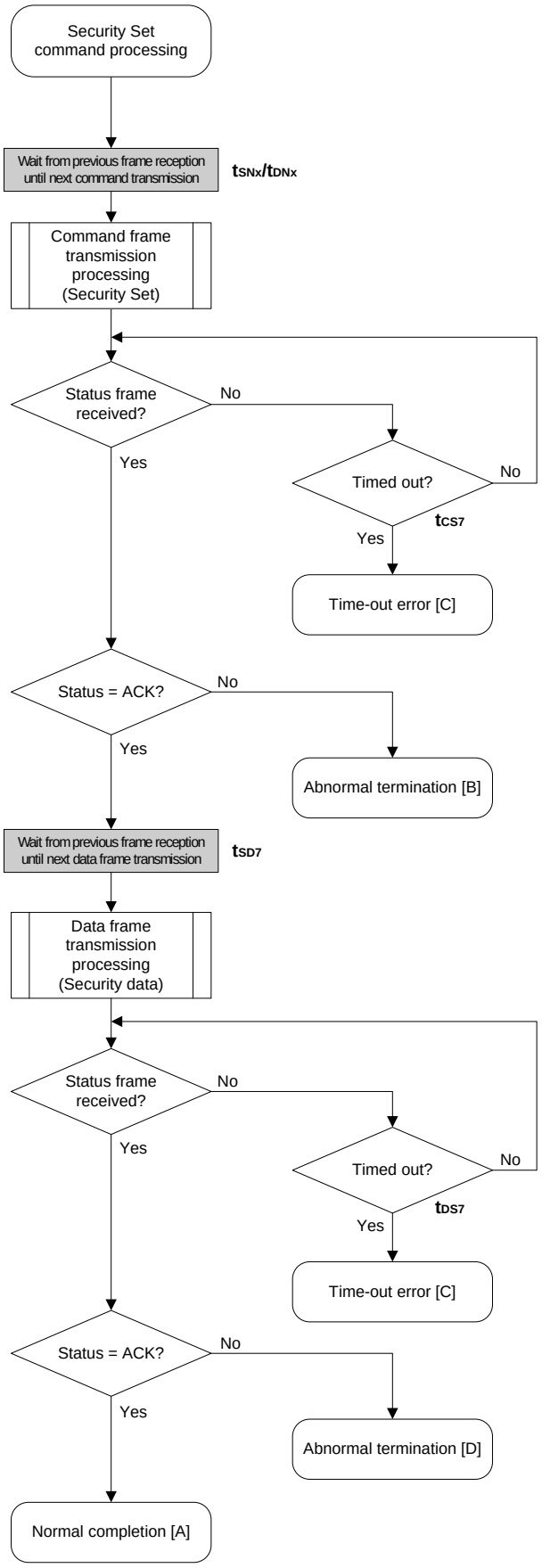
<5> Waits from the previous frame reception until the next data frame transmission (wait time t_{SD7}).
<6> The data frame (security setting data) is transmitted by data frame transmission processing.
<7> A time-out check is performed until status frame reception.
If a time-out occurs, a time-out error [C] is returned (time-out time t_{DS7}).
<8> The status code is checked.

When ST1 = ACK: Normal completion [A]
When ST1 ≠ ACK: Abnormal termination [D]

4.12.3 Status at processing completion

Status at Processing Completion		Status Code	Description
Normal completion [A]	Normal acknowledgment (ACK)	06H	The command was executed normally and security setting data was set normally.
Abnormal termination [B]	Parameter error	05H	Parameter BOT does not match the specifications of the RL78. The FSW setting block number is not set so that the start block number is larger than the end block number. Or, the FSW end block number is larger than the last block number of the code flash memory.
	Checksum error	07H	The checksum of the transmitted command frame or data frame does not match.
	Protect error	10H	An already prohibited flag is to be enabled.
	Negative acknowledgment (NACK)	15H	Command frame data is abnormal (such as invalid data length (LEN) or no ETX).
Time-out error [C]		–	The status frame or data frame was not received within the specified time.
Abnormal termination [D]	Erase error	1AH	Writing security data has failed.
	IVerify error	1BH	
	Write error	1CH	

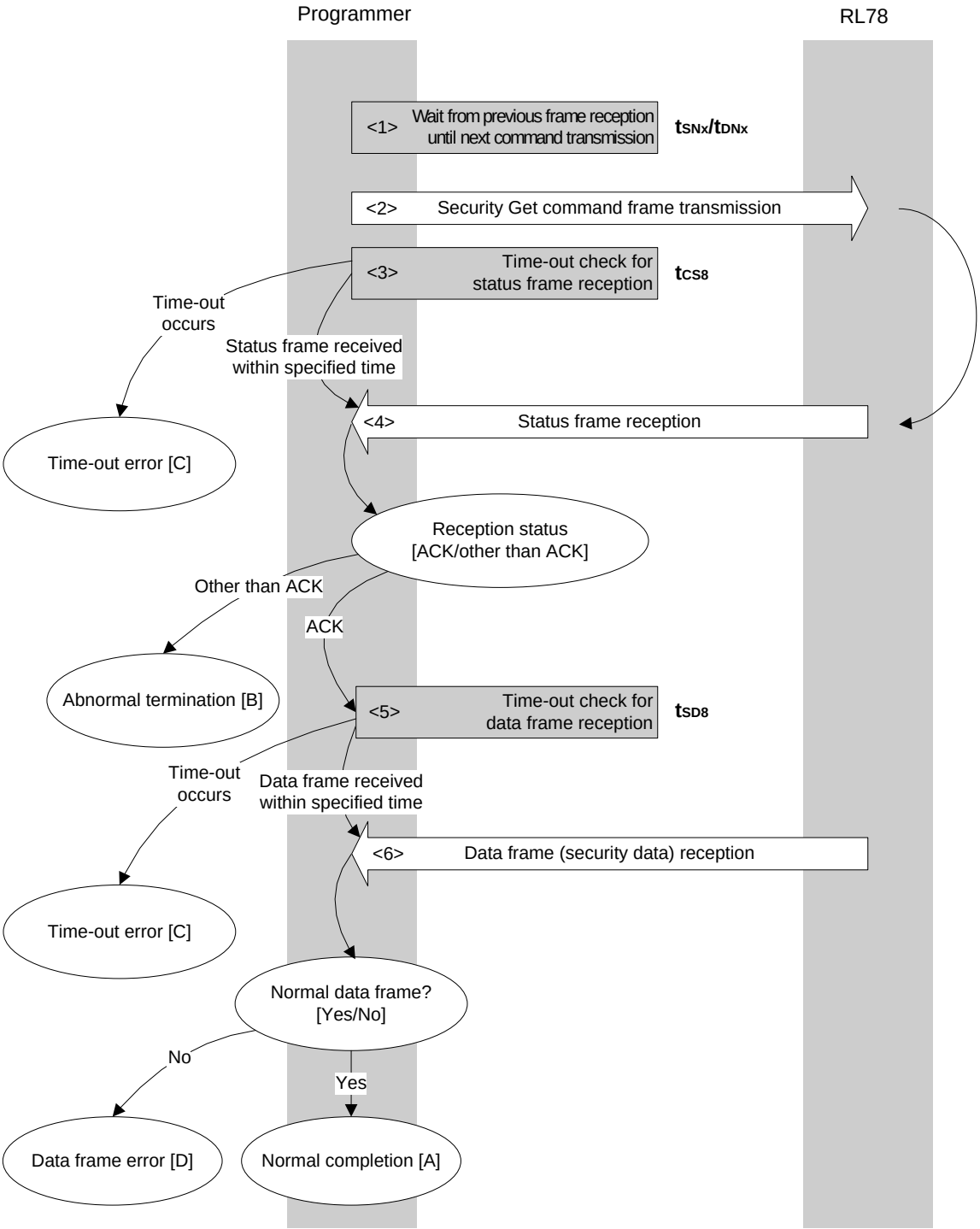
4.12.4 Flowchart



4.13 Security Get Command

4.13.1 Processing sequence chart

Security Get command processing sequence



4.13.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time t_{SNx}/t_{DNx}).
<2> The Security Get command is transmitted by command frame transmission processing.
<3> A time-out check is performed from command transmission until status frame reception.
If a time-out occurs, a time-out error [C] is returned (time-out time t_{CS8}).
<4> The status code is checked.

When ST1 = ACK: Proceeds to <5>.
When ST1 ≠ ACK: Abnormal termination [B]

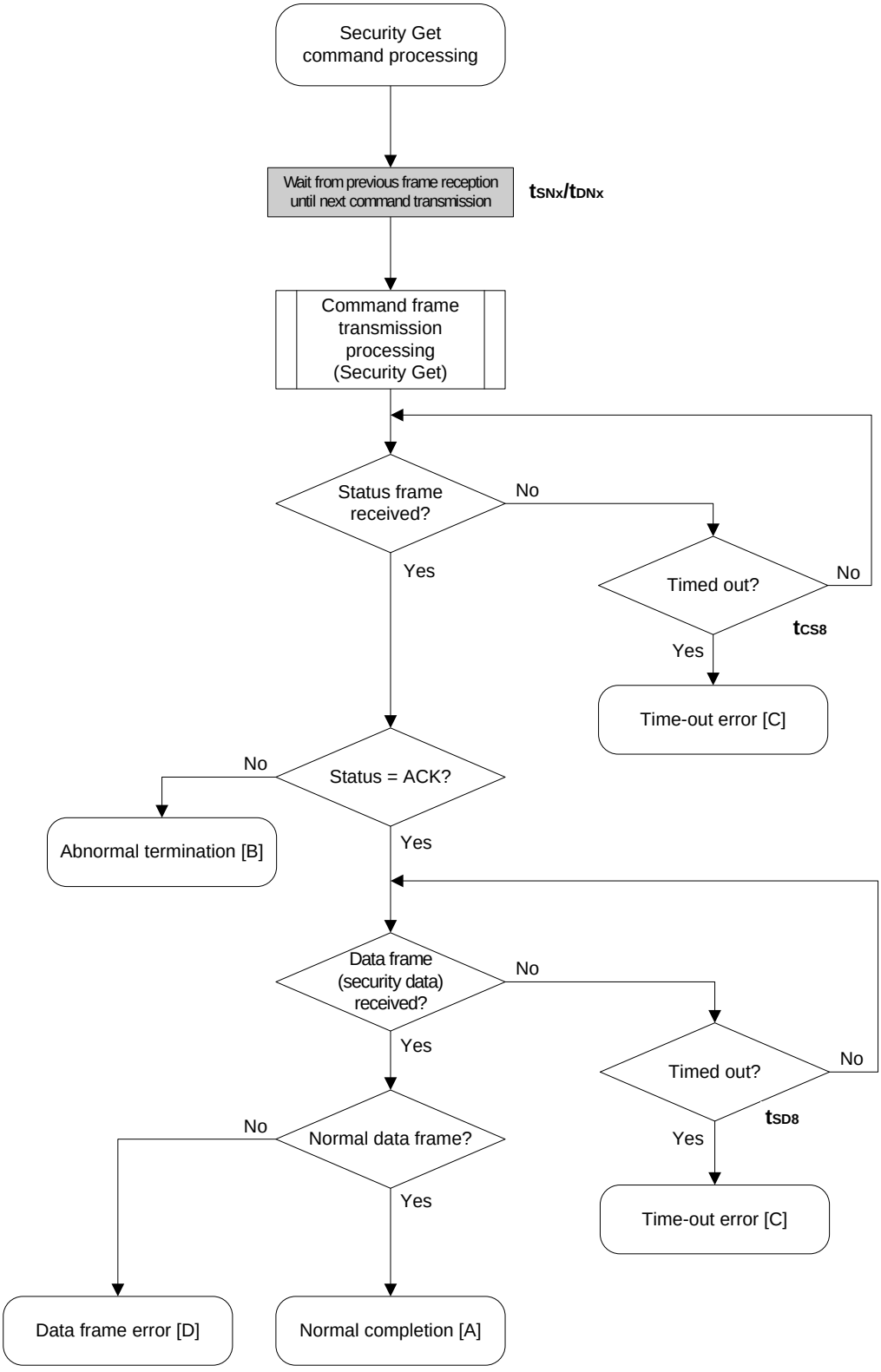
<5> A time-out check is performed until data frame (security data) reception.
If a time-out occurs, a time-out error [C] is returned (time-out time t_{SD8}).
<6> The received data frame (version data) is checked.

If data frame is normal: Normal completion [A]
If data frame is abnormal: Data frame error [D]

4.13.3 Status at processing completion

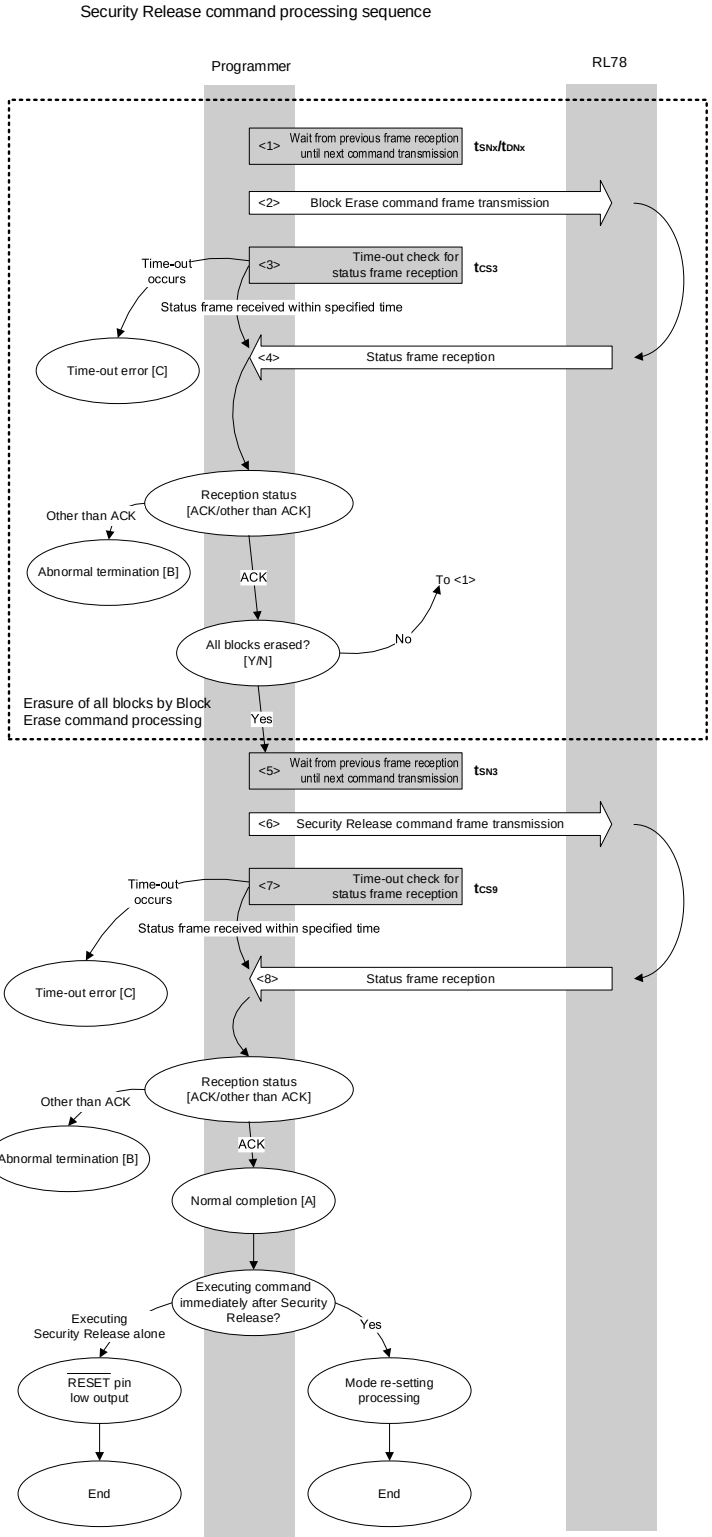
Status at Processing Completion		Status Code	Description
Normal completion [A]		–	The command was executed normally and security setting data was set normally.
Abnormal termination [B]	Checksum error	07H	The checksum of the transmitted command frame does not match.
	Negative acknowledgment (NACK)	15H	Command frame data is abnormal (such as invalid data length (LEN) or no ETX).
Normal acknowledgment (ACK)		06H	The command was transmitted normally.
Time-out error [C]		–	The status frame or data frame was not received within the specified time.
Data frame error [D]		–	The checksum of the data frame received as security data does not match.

4.13.4 Flowchart



4.14 Security Release Command

4.14.1 Processing sequence chart



The Security Release command can be executed only when all the code flash area and data flash area are blank. Therefore, the block erase processing indicated by the dotted line above must be executed in advance.

4.14.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time t_{SNx}/t_{DNx}).
<2> The Block Erase command is transmitted by command frame transmission processing.
<3> A time-out check is performed from command transmission until status frame reception.
If a time-out occurs, a time-out error [C] is returned (time-out time t_{CS3}).
<4> The status code is checked.

When ST1 = ACK: Proceed to <5> if all the blocks have been erased.
Return to <1> if the specified block has not been erased.
When ST1 ≠ ACK: Abnormal termination [B]

<5> Waits from the previous frame reception until the next command transmission (wait time t_{SN3}).
<6> The Security Release command is transmitted by command frame transmission processing.
<7> A time-out check is performed from command transmission until status frame reception.
If a time-out occurs, a time-out error [C] is returned (time-out time t_{CS9}).
<8> The status code is checked.

When ST1 = ACK: Normal completion [A]
Execute the following processing.
To execute Security Release command alone:
Output the low level to the Reset pin and terminate.
To execute a command immediately after Security Release command:
Execute mode re-setting processing.

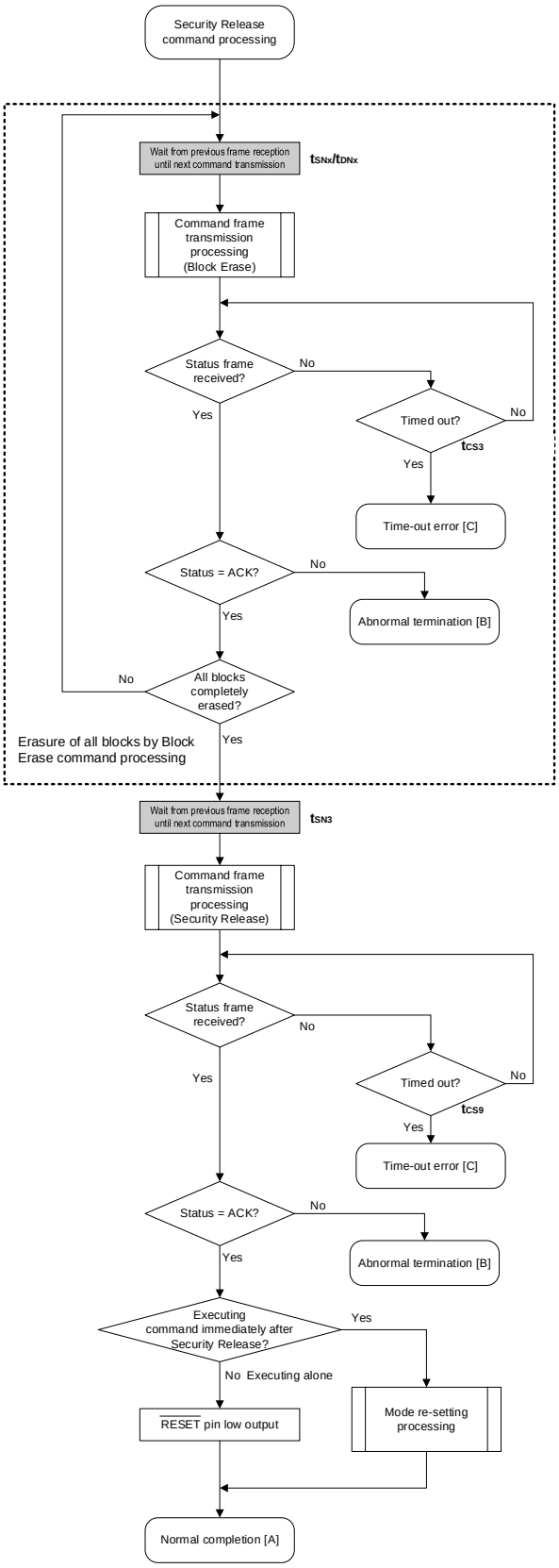
When ST1 ≠ ACK: Abnormal termination [B]

4.14.3 Status at processing completion

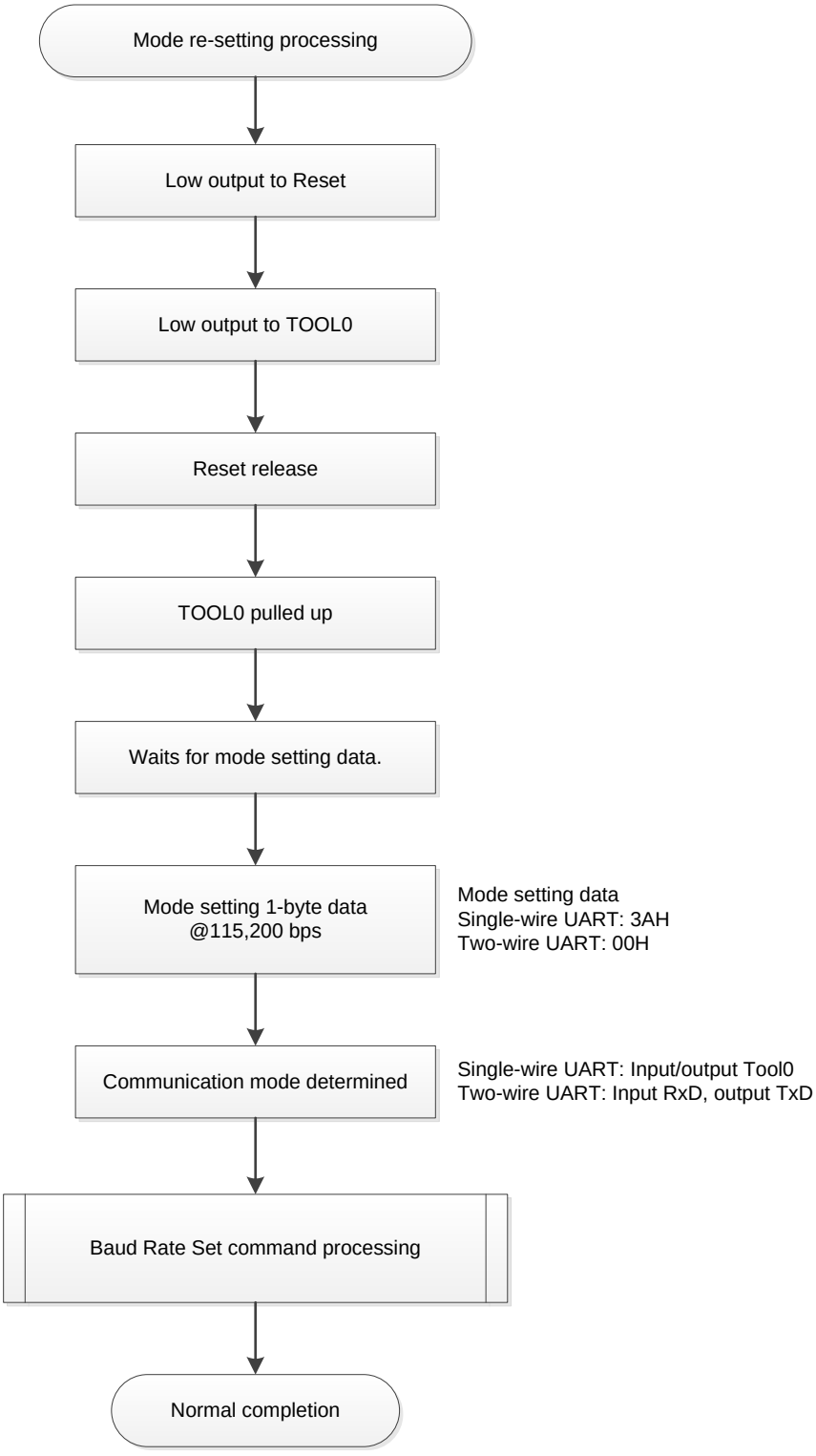
The following table shows the status codes that may be output after the Security Release command has been executed.

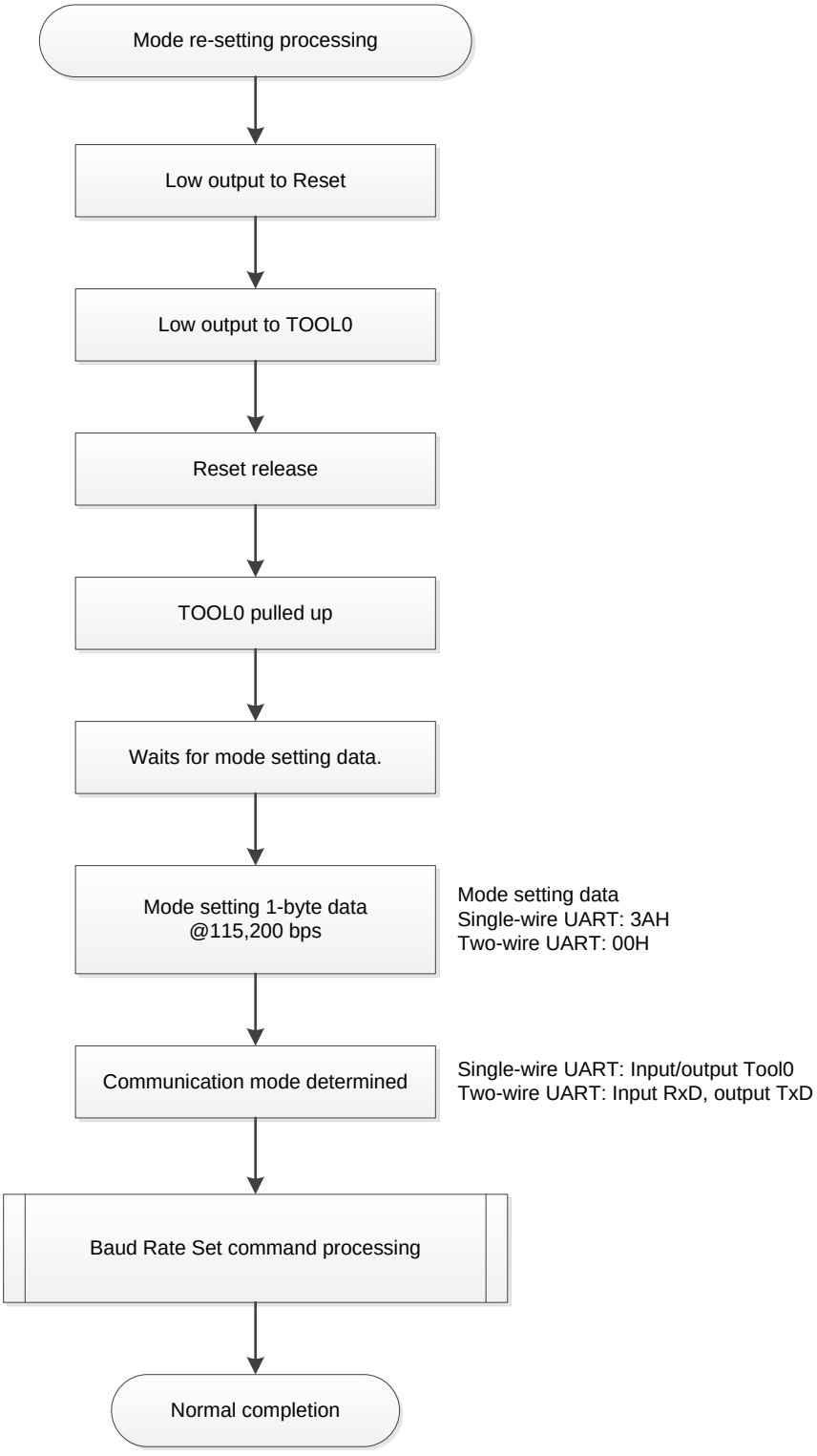
Status at Processing Completion		Status Code	Description
Normal completion [A]	Normal acknowledgment (ACK)	06H	The command was executed normally and the security setting was initialized normally.
Abnormal termination [B]	Checksum error	07H	The checksum of the transmitted command frame or data frame does not match.
	Protect error	10H	Block erase or boot block rewrite is prohibited in the security setting.
	Negative acknowledgment (NACK)	15H	Command frame data is abnormal (such as invalid data length (LEN) or no ETX).
	Blank error	1BH	The code flash memory and/or data flash memory is not blank.
	Erase error/ IVerify error/ Write error	1AH/1BH/1CH	The security setting could not be initialized normally.
Time-out error [C]		–	The status frame was not received within the specified time.

4.14.4 Flowchart



The Security Release command can be executed only when all the code flash area and data flash area are blank. Therefore, the block erase processing indicated by the dotted line above must be executed in advance.


Mode re-setting processing
Low output to Reset
Low output to TOOL0
Reset release
TOOL0 pulled up
Waits for mode setting data.
Mode setting 1-byte data
@115,200 bps
Mode setting data
Single-wire UART: 3AH
Two-wire UART: 00H
Communication mode determined
Single-wire UART: Input/output Tool0
Two-wire UART: Input RxD, output TxD
Baud Rate Set command processing
Normal completion


Mode re-setting processing
Low output to Reset
Low output to TOOL0
Reset release
TOOL0 pulled up
Waits for mode setting data.
Mode setting 1-byte data
@115,200 bps
Mode setting data
Single-wire UART: 3AH
Two-wire UART: 00H
Communication mode determined
Single-wire UART: Input/output Tool0
Two-wire UART: Input RxD, output TxD
Baud Rate Set command processing
Normal completion

CHAPTER 5 FLASH MEMORY PROGRAMMING PARAMETER CHARACTERISTICS

This chapter describes the characteristics of parameter transmitted between the programmer and the devices (RL78) in the flash memory programming mode. Refer to the user's manual of the devices (RL78) for electrical specifications when designing a programmer.

5.1 Flash Memory Parameter Characteristics of RL78

5.1.1 Flash memory parameter characteristics in full-speed mode

(1) Flash memory programming mode setting time

Parameter	Symbol	MIN.	TYP.	MAX.
TOOL0↓ to $\overline{\text{RESET}}$↑	t_{TR}	t_{SU}		
$\overline{\text{RESET}}$↑ to TOOL0↑	t_{RT}	723 μs+t_{HD} Note 2		
TOOL0↑ to Receive mode info	t_{TM}	16 μs Note 2		
Receive mode info to Receive Baud Rate Set Command	t_{MB}	62 μs Note 2		
$\overline{\text{RESET}}$↑ to Receive Baud Rate Set Command	t_{RB}			100 ms Note 1

Notes 1. The location indicated differs depending on the setting of the option byte.
Option byte (0000C3H.bit6) = 0: $\overline{\text{RESET}}$↑ to Baud Rate Set Command reception: within 100 ms
= 1: TOOL0↑ to Baud Rate Set command reception: within 100 ms
To permit both of the option byte settings, complete the reception of the Baud Rate Set command within 100 ms from $\overline{\text{RESET}}$↑ (refer to the User's Manual of each device (t_{SUINIT})).

2. The flash memory programmer needs the specified wait time before transmission.

(2) Programming characteristic

Wait	Condition		Symbol	MIN.	MAX.
Between data transmissions	Data reception[Note 5]	16 MHz≤f_{CLK}≤32 MHz	t_{DR}	0 μs[Note 3]	
		0.75 MHz≤f_{CLK}<16 MHz		136/f_{CLK} – 8 μs[Note 3]	
	Data transmission[Note 5]		t_{DT}	6/f_{CLK}[Note 2]	10/f_{CLK}[Notes 1]
From status frame transmission until data frame transmission	Check Sum command		t_{SD10}	48/f_{CLK}+ 15564/f_{CLK} ×BLK[Notes 2, 4]	72/f_{CLK}+ 30720/f_{CLK} ×BLK[Notes 1, 4]
From status frame transmission until data frame reception (1)	Programming command		t_{SD5}	41/f_{CLK}[Note 3]	
From status frame transmission until data frame reception (2)	Verify command		t_{SD2}	41/f_{CLK}[Note 3]	
From status frame transmission until data frame reception (3)	Security Set command		t_{SD7}	32/f_{CLK}[Note 3]	
From status frame transmission until data frame reception (4)	Security Get command		t_{SD8}	139/f_{CLK}[Note 2]	212/f_{CLK}[Note 1]
From status frame transmission until data frame reception (5)	Signature command		t_{SD11}	340/f_{CLK}[Note 2]	512/f_{CLK}[Note 1]
From status frame transmission until next command frame reception	Reset command		t_{SN1}	51/f_{CLK}[Note 3]	
	Verify command		t_{SN2}	54/f_{CLK}[Note 3]	
	Block Erase command		t_{SN3}	51/f_{CLK}[Note 3]	
	Block Blank Check command		t_{SN4}	51/f_{CLK}[Note 3]	
	Programming command		t_{SN5}	51/f_{CLK}[Note 3]	
	Baud Rate Set command		t_{SN6}	67 μs[Note 3]	
	Security Set command		t_{SN7}	51/f_{CLK}[Note 3]	
	Security Release command		t_{SN9}	51/f_{CLK}[Note 3]	
From data frame transmission until next command frame reception	Security Get command		t_{DN8}	44/f_{CLK}[Note 3]	
	Checksum command		t_{DN10}	44/f_{CLK}[Note 3]	
	Signature command		t_{DN11}	44/f_{CLK}[Note 3]	

Notes 1. This is as a guide of the time-out time.

2. The Flash memory programmer must be ready for receiving communication data within the specified time.

3. The Flash memory programmer needs the specified time before transmission.

4. The detail of the symbol is as follows.
BLK: Number of blocks (in 1024-byte units)

5. The device operates at either 0.75 MHz or 1 MHz since reset release until reception of the Baud Rate Set command. Calculate the time on the assumption that fclk = 0.75 MHz so that communication can be executed during this period.

(3) Command characteristics

Command	Symbol	Condition	MIN.	MAX.
Reset	t_{CS1}	–	$58/f_{CLK}$ Note 2	$255/f_{CLK}$ Note 1
Verify	t_{CS2}	Code flash	$58/f_{CLK}$ Note 2	$335/f_{CLK}$ Note 1
		Data flash	$58/f_{CLK}$ Note 2	$351/f_{CLK}$ Note 1
	t_{DS2}	Code flash	$64/f_{CLK}$ Note 2	$11981/f_{CLK}$ Note 1
		Data flash	$64/f_{CLK}$ Note 2	$11980/f_{CLK}$ Note 1
Block Erase	t_{CS3}	Code flash	$58/f_{CLK}$ Note 2	$67731/f_{CLK}+255098\ \mu s$ Note 1
		Data flash	$58/f_{CLK}$ Note 2	$281423/f_{CLK}+264790\ \mu s$ Note 1
Block Blank Check	t_{CS4}	Code flash	$58/f_{CLK}$ Note 2	$3805/f_{CLK}+91\ \mu s+$ $(1457/f_{CLK}+80\ \mu s)\times BLK+$ $(203/f_{CLK}+18\ \mu s)\times N$ Notes 1, 3
		Data flash	$58/f_{CLK}$ Note 2	$2503/f_{CLK}+86\ \mu s+$ $(5827/f_{CLK}+318\ \mu s)\times BLK$ Notes 1, 3
Programming	t_{CS5}	Code flash	$58/f_{CLK}$ Note 2	$1432/f_{CLK}$ Note 1
		Data flash	$58/f_{CLK}$ Note 2	$346/f_{CLK}$ Note 1
	t_{DS5}	Code flash	$64/f_{CLK}$ Note 2	$113502/f_{CLK}+71753\ \mu s$ Note 1
		Data flash	$64/f_{CLK}$ Note 2	$309870/f_{CLK}+219761\ \mu s$ Note 1
	t_{SS5}	Code flash	$1294/f_{CLK}+37\ \mu s$ Note 2	$1732/f_{CLK}+36\ \mu s+$ $(7096/f_{CLK}+892\ \mu s)\times BLK+$ $(182/f_{CLK}+17\ \mu s)\times N$ Notes 1, 3
		Data flash	$282/f_{CLK}+22\ \mu s$ Note 2	$397/f_{CLK}+30\ \mu s+$ $(28382/f_{CLK}+3568\ \mu s)\times BLK$ Notes 1, 3
Baud Rate Set	t_{CS6}	–	$58\ \mu s$ Note 2	$4735\ \mu s$ Note 1
Security Set	t_{CS7}	–	$58/f_{CLK}$ Note 2	$168/f_{CLK}$ Note 1
	t_{DS7}	–	$60/f_{CLK}$ Note 2	$277095/f_{CLK}+1027564\ \mu s$ Note 1
Security Get	t_{CS8}	–	$58/f_{CLK}$ Note 2	$154/f_{CLK}$ Note 1
Security Release	t_{CS9}	Model with data flash	$58/f_{CLK}$ Note 2	$146110/f_{CLK}+511868\ \mu s+$ $(1457/f_{CLK}+80\ \mu s)\times CBLK+$ $(5827/f_{CLK}+318\ \mu s)\times DBLK+$ $(203/f_{CLK}+18\ \mu s)\times N$ Notes 1, 4
		Model without data flash	$58/f_{CLK}$ Note 2	$145783/f_{CLK}+511837\ \mu s+$ $(1457/f_{CLK}+80\ \mu s)\times CBLK+$ $(203/f_{CLK}+18\ \mu s)\times N$ Notes 1, 4
Checksum	t_{CS10}	Code flash	$58/f_{CLK}$ Note 2	$203/f_{CLK}$ Note 1
		Data flash	$58/f_{CLK}$ Note 2	$219/f_{CLK}$ Note 1
Signature Get	t_{CS11}	–	$58/f_{CLK}$ Note 2	$111/f_{CLK}$ Note 1

Notes 1. This is as a guide of the time-out time.

2. The Flash memory programmer must be ready for receiving communication data within the specified time.

3. The details of the symbols are as follows.

BLK: Number of blocks (in 1024-byte units)

N: Number of times Flash memory is to be accessed

Expression (Result of division in parentheses is rounded off at decimal point):

(End address/40000H) – (Start address/40000H) + 1

[Example]

Start address = 00000H & End address = 3FFFFH → N = 1

Start address = 3FC00H & End address = 403FFH → N = 2

4. The details of the symbols are as follows.

CBLK: Total number of blocks of CodeFlash

[Example] Code Flash size = 64 KB → CBLK = 64

DBLK: Total number of blocks of DataFlash

[Example] Data Flash size = 4 KB → DBLK = 4

N: Number of times Flash memory is to be accessed

Expression (Rounded off at decimal point): CBLK/256

[Example] CBLK = 256 → N = 1

CBLKK = 384 → N = 2

5.1.2 Flash memory parameter characteristics in wide-voltage mode

(1) Flash memory programming mode setting time

Parameter	Symbol	MIN.	TYP.	MAX.
TOOL0↓ to $\overline{\text{RESET}}$↑	t_{TR}	t_{SU}		
$\overline{\text{RESET}}$↑ to TOOL0↑	t_{RT}	723 μs+t_{HD} Note 2		
TOOL0↑ to Receive mode info	t_{TM}	16 μs Note 2		
Receive mode info to Receive Baud Rate Set Command	t_{MB}	62 μs Note 2		
$\overline{\text{RESET}}$↑ to Receive Baud Rate Set Command	t_{RB}			100 ms Note 1

Notes 1. The location indicated differs depending on the setting of the option byte.
Option byte (0000C3H.bit6) = 0: $\overline{\text{RESET}}$↑ to Baud Rate Set Command reception: within 100 ms
= 1: TOOL0↑ to Baud Rate Set command reception: within 100 ms
To permit both of the option byte settings, complete the reception of the Baud Rate Set command within 100 ms from $\overline{\text{RESET}}$↑ (refer to the User's Manual of each device (t_{SUINIT})).

2. The flash memory programmer needs the specified wait time before transmission.

(2) Programming characteristic

Wait	Condition		Symbol	MIN.	MAX.
Between data transmissions	Data reception[Note 5]	16 MHz≤f_{CLK}≤32 MHz	t_{DR}	0 μs[Note 3]	
		0.75 MHz≤f_{CLK}<16 MHz		136/f_{CLK} – 8 μs[Note 3]	
	Data transmission[Note 5]		t_{DT}	6/f_{CLK}[Note 1]	10/f_{CLK}[Note 2]
From status frame transmission until data frame transmission	Check Sum command		t_{SD10}	48/f_{CLK}+ 15564/f_{CLK}× BLK[Notes 2, 4]	72/f_{CLK}+ 30720/f_{CLK}× BLK[Notes 1, 4]
From status frame transmission until data frame reception (1)	Programming command		t_{SD5}	41/f_{CLK}[Note 3]	
From status frame transmission until data frame reception (2)	Verify command		t_{SD2}	41/f_{CLK}[Note 3]	
From status frame transmission until data frame reception (3)	Security Set command		t_{SD7}	32/f_{CLK}[Note 3]	
From status frame transmission until data frame reception (4)	Security Get command		t_{SD8}	139/f_{CLK}[Note 2]	212/f_{CLK}[Note 1]
From status frame transmission until data frame reception (5)	Signature command		t_{SD11}	340/f_{CLK}[Note 2]	512/f_{CLK}[Note 1]
From status frame transmission until next command frame reception	Reset command		t_{SN1}	51/f_{CLK}[Note 3]	
	Verify command		t_{SN2}	54/f_{CLK}[Note 3]	
	Block Erase command		t_{SN3}	51/f_{CLK}[Note 3]	
	Block Blank Check command		t_{SN4}	51/f_{CLK}[Note 3]	
	Programming command		t_{SN5}	51/f_{CLK}[Note 3]	
	Baud Rate Set command		t_{SN6}	67 μs[Note 3]	
	Security Set command		t_{SN7}	51/f_{CLK}[Note 3]	
	Security Release command		t_{SN9}	51/f_{CLK}[Note 3]	
From data frame transmission until next command frame reception	Security Get command		t_{DN8}	44/f_{CLK}[Note 3]	
	Checksum command		t_{DN10}	44/f_{CLK}[Note 3]	
	Signature command		t_{DN11}	44/f_{CLK}[Note 3]	

Notes 1. This is as a guide of the time-out time.

2. The Flash memory programmer must be ready for receiving communication data within the specified time.

3. The Flash memory programmer needs the specified time before transmission.

4. The detail of the symbol is as follows.
BLK: Number of blocks (in 1024-byte units)

5. The device operates at either 0.75 MHz or 1 MHz since reset release until reception of the Baud Rate Set command. Calculate the time on the assumption that fclk = 0.75 MHz so that communication can be executed during this period.

(3) Command characteristics

Command	Symbol	Condition	MIN.	MAX.
Reset	t_{CS1}	–	$58/f_{CLK}$ Note 2	$255/f_{CLK}$ Note 1
Verify	t_{CS2}	Code flash	$58/f_{CLK}$ Note 2	$335/f_{CLK}$ Note 1
		Data flash	$58/f_{CLK}$ Note 2	$351/f_{CLK}$ Note 1
	t_{DS2}	Code flash	$64/f_{CLK}$ Note 2	$11981/f_{CLK}$ Note 1
		Data flash	$64/f_{CLK}$ Note 2	$11980/f_{CLK}$ Note 1
Block Erase	t_{CS3}	Code flash	$58/f_{CLK}$ Note 2	$59455/f_{CLK}$+265331 μs Note 1
		Data flash	$58/f_{CLK}$ Note 2	$248862/f_{CLK}$+299307 μs Note 1
Block Blank Check	t_{CS4}	Code flash	$58/f_{CLK}$ Note 2	$3799/f_{CLK}$+134 μs+ (1259/f_{CLK}+278 μs)×BLK+ (199/f_{CLK}+57 μs)×N Notes 1, 3
		Data flash	$58/f_{CLK}$ Note 2	$2494/f_{CLK}$+168 μs+ (5035/f_{CLK}+1110 μs)×BLK Notes 1, 3
Programming	t_{CS5}	Code flash	$58/f_{CLK}$ Note 2	$1432/f_{CLK}$ Note 1
		Data flash	$58/f_{CLK}$ Note 2	$346/f_{CLK}$ Note 1
	t_{DS5}	Code flash	$64/f_{CLK}$ Note 2	$107803/f_{CLK}$+138891 μs Note 1
		Data flash	$64/f_{CLK}$ Note 2	$287076/f_{CLK}$+488315 μs Note 1
	t_{SS5}	Code flash	$1287/f_{CLK}$+72 μs Note 2	$1732/f_{CLK}$+36 μs+ (4351/f_{CLK}+7324 μs)×BLK+ (184/f_{CLK}+44 μs)×N Notes 1, 3
		Data flash	$276/f_{CLK}$+57 μs Note 2	$398/f_{CLK}$+58 μs+ (17403/f_{CLK}+29293 μs)×BLK Notes 1, 3
Baud Rate Set	t_{CS6}	–	58 μs Note 2	4735 μs Note 1
Security Set	t_{CS7}	–	$58/f_{CLK}$ Note 2	$168/f_{CLK}$ Note 1
	t_{DS7}	–	$60/f_{CLK}$ Note 2	$242909/f_{CLK}$+1075967 μs Note 1
Security Get	t_{CS8}	–	$58/f_{CLK}$ Note 2	$154/f_{CLK}$ Note 1
Security Release	t_{CS9}	Model with data flash	$58/f_{CLK}$ Note 2	$128408/f_{CLK}$+534723 μs+ (1259/f_{CLK}+278 μs)×CBLK+ (5035/f_{CLK}+1110 μs)×DBLK+ (199/f_{CLK}+57 μs)×N Notes 1, 4
		Model without data flash	$58/f_{CLK}$ Note 2	$128084/f_{CLK}$+534653 μs+ (1259/f_{CLK}+278 μs)×CBLK+ (199/f_{CLK}+57 μs)×N Notes 1, 4
Checksum	t_{CS10}	Code flash	$58/f_{CLK}$ Note 2	$203/f_{CLK}$ Note 1
		Data flash	$58/f_{CLK}$ Note 2	$219/f_{CLK}$ Note 1
Signature Get	t_{CS11}	–	$58/f_{CLK}$ Note 2	$111/f_{CLK}$ Note 1

Notes 1. This is as a guide of the time-out time.

2. The Flash memory programmer must be ready for receiving communication data within the specified time.

3. The details of the symbols are as follows.

BLK: Number of blocks (in 1024-byte units)

N: Number of times Flash memory is to be accessed

Expression (Result of division in parentheses is rounded off at decimal point):

(End address/40000H) – (Start address/40000H) + 1

[Example]

Start address = 00000H & End address = 3FFFFH → N = 1

Start address = 3FC00H & End address = 403FFH → N = 2

4. The details of the symbols are as follows.

CBLK: Total number of blocks of CodeFlash
[Example] Code Flash size = 64 KB → CBLK = 64

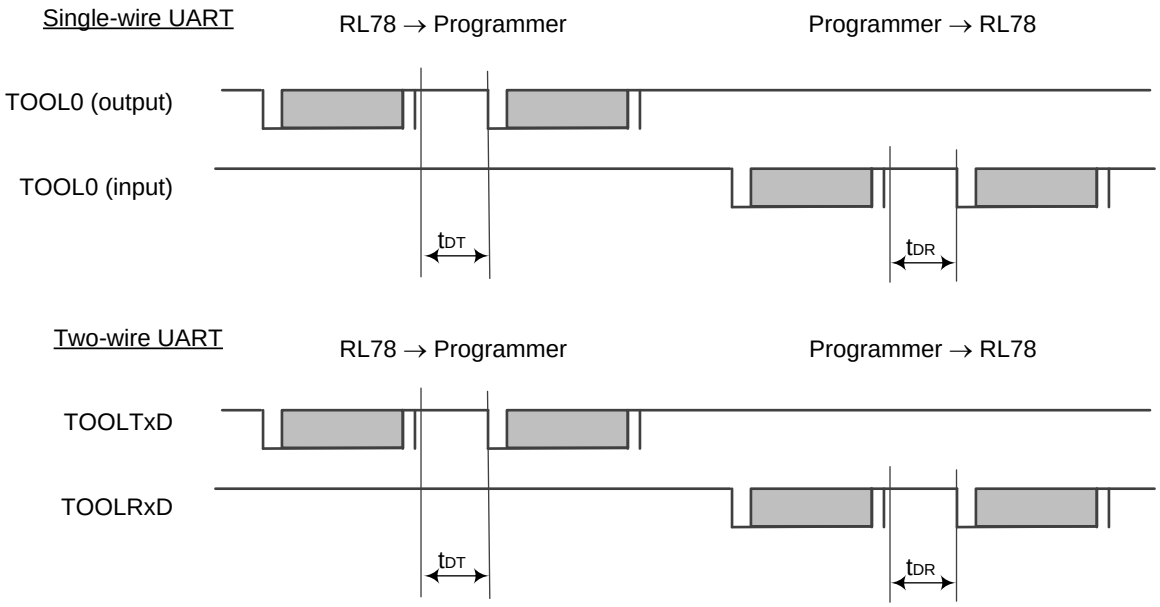
DBLK: Total number of blocks of DataFlash
[Example] Data Flash size = 4 KB → DBLK = 4

N: Number of times Flash memory is to be accessed
Expression (Rounded off at decimal point): CBLK/256
[Example] CBLK = 256 → N = 1
CBLKK = 384 → N = 2

5.2 UART Communication Mode

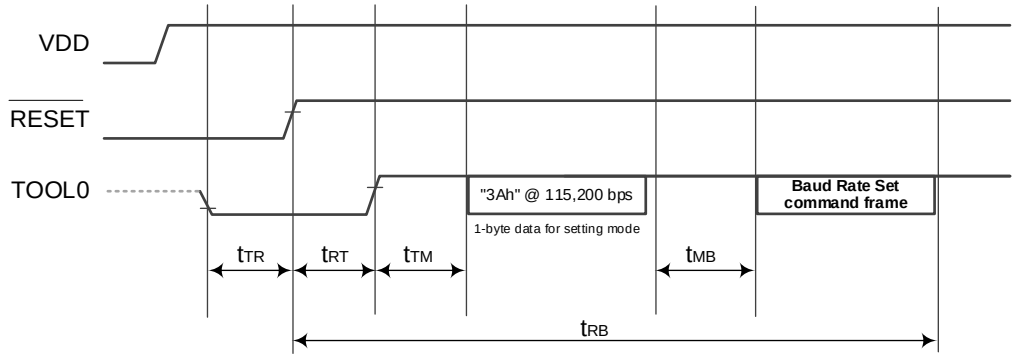
In the figure below, TOOL0 is illustrated as two separate lines for the sake of description, but it is actually a single line. The VDD level of TOOL0 can be achieved by using a pull-up resistor (the pin is Hi-Z).

(a) Data frame

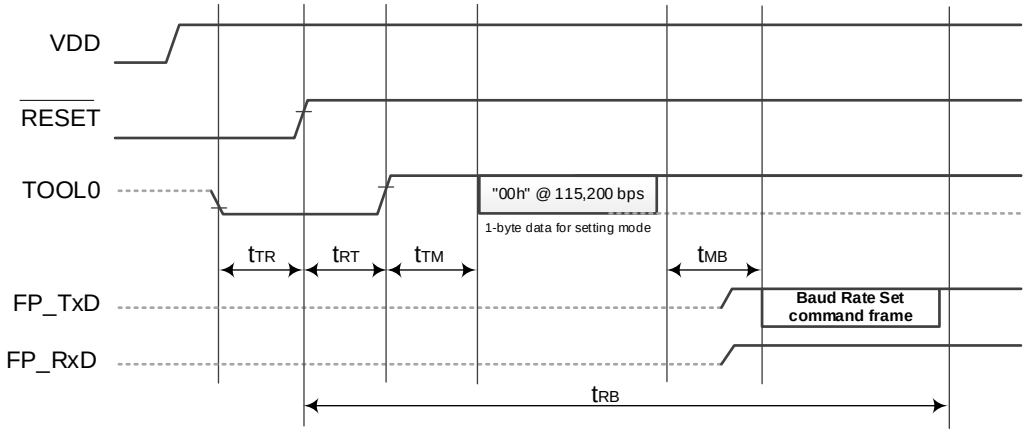


(b) Programming mode setting

Single-wire UART

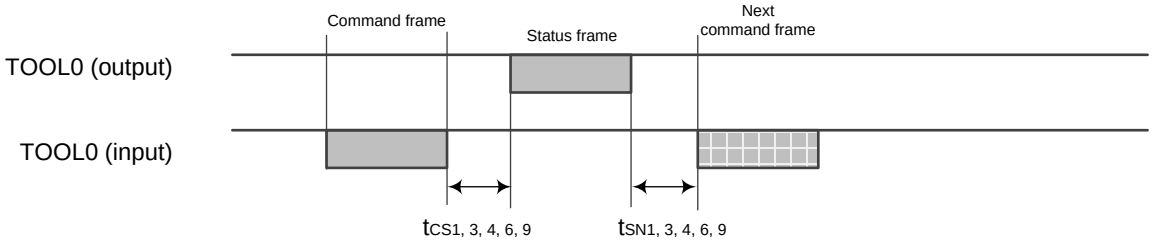


Two-wire UART

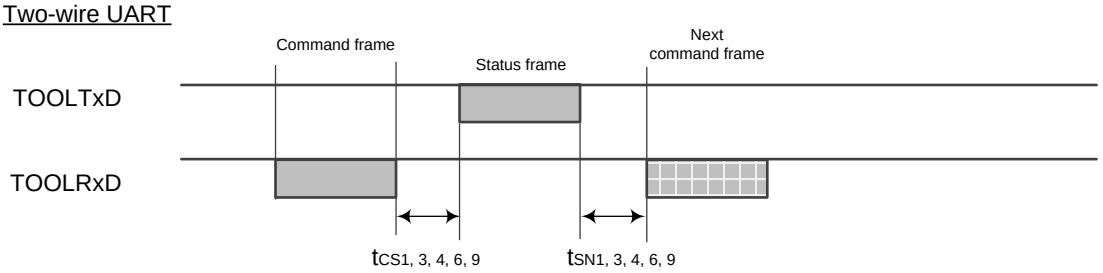


(c) Reset command/Block Erase command/Block Blank Check command/Baud Rate Set command/Security Release command

Single-wire UART

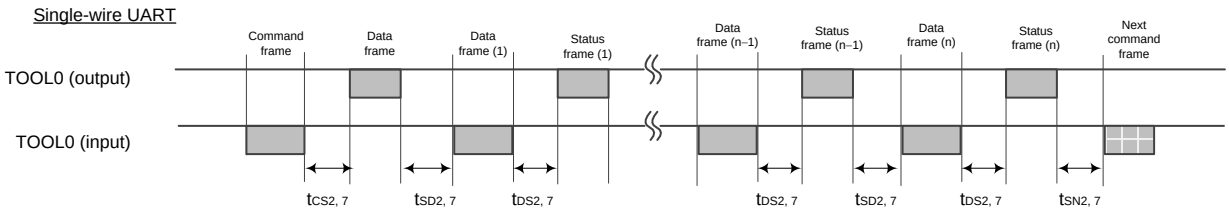


Two-wire UART

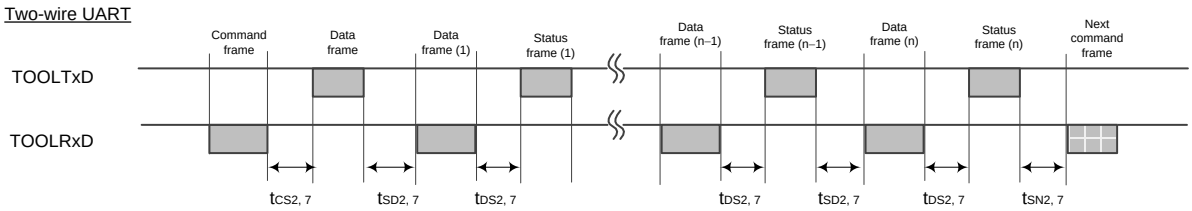


(d) Verify command/Security Set command

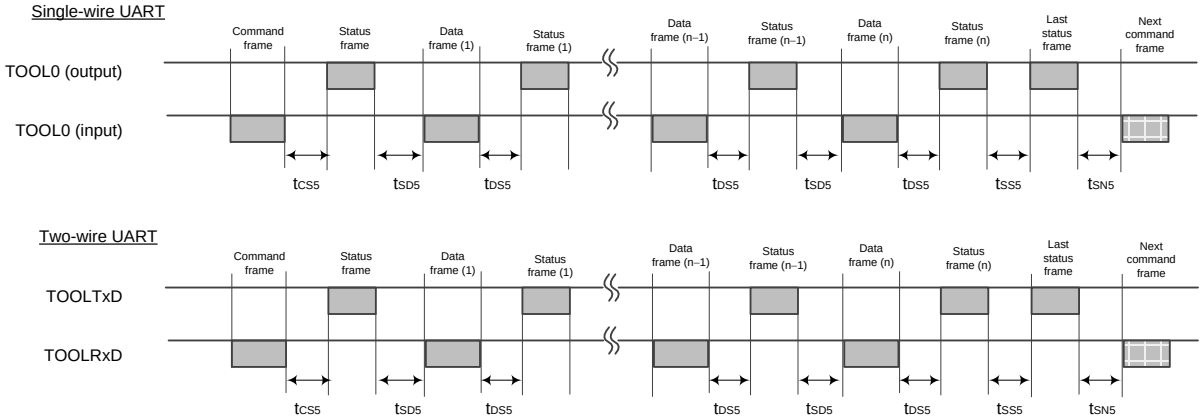
Single-wire UART



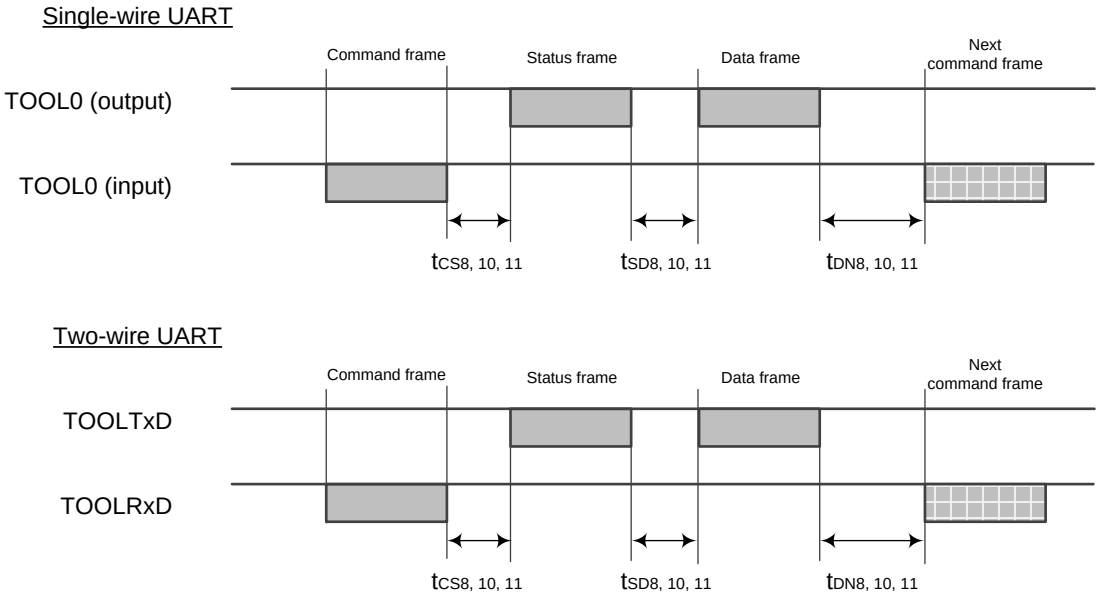
Two-wire UART



(e) Programming command



(f) Security Get command/Check Sum command/Signature command



Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Nov. 7, 2011	–	First edition issued
1.10	Nov. 20, 2025		Rev1.1 edition issued
		Page.1	Target device item added
		Page.21	Figure 3-4. Status Frame for Baud Rate Set Command (from RL78 to Programmer) D01 example error correction Incorrect) 20 MHz: 18H Correct) 20 MHz: 14H
		Page32 and Page 35	Figure 3-31. & Figure 3-35. Security Data Frame (from RL78 to Programmer) error correction RES value: FFFFH Incorrect) Invalid data Correct) (Reserve)
		Page75 and Page 79	(1) Flash memory programming mode setting time $\overline{\text{RESET}}$ ↑ to Receive Baud Rate Set Command Incorrect) Min. 100ms Correct) Max. 100ms

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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