R8C/35A Group

Power Control Using Wait Mode

R01AN0077EJ0100
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1. Abstract

This document describes a setting method and application examples for power control using wait mode.

2. Introduction

The application example described in this document applies to the following microcomputer (MCU) and parameters:

- MCU: R8C/35A Group
- Oscillation frequencies: 20 MHz (XIN clock), 32.768 kHz (XCIN clock)

This application note can be used with other R8C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Application Examples

This application note describes application examples of the following two sample programs:

- Sample program 1: Exit using the CPU clock immediately before entering wait mode
- Sample program 2: Exit using the XIN clock

3.1 Sample Program 1 Outline

Operating modes are switched and the MCU enters and exits wait mode according to the procedure shown below. The timer RA interrupt and $\overline{\text{INT0}}$ interrupt are used to exit wait mode. Entering and exiting wait mode are controlled using a variable (mode).

(1) After reset is deasserted, oscillate the XIN clock and then the XCIN clock by a program.
(2) After waiting for the XIN clock and XCIN clock oscillation to stabilize, switch the system clock to the XIN clock and change the operating mode to high-speed clock mode (no division). Then stop the low-speed on-chip oscillator clock. Set the VCA20 bit in the VCA2 register to 0 (internal power low consumption disabled).
(3) When entering wait mode, switch the system clock to the XCIN clock and change the operating mode to low-speed clock mode (divide-by-8 mode), and stop the XIN clock. Then set the following:
  - Set the variable (mode) to 1.
  - Set the CM35 bit in the CM3 register to 0 (settings of the CM06 bit in the CM0 register, and bits CM16 and CM17 in the CM1 register are enabled).
  - Set bits CM37 and CM36 to 00b (the MCU exits using the CPU clock immediately before entering wait mode or stop mode).
  - Set the VCA20 bit to 1 (internal power low consumption enabled).
(4) Execute the WAIT instruction to enter wait mode. At this point, an interrupt used for exiting wait mode is enabled and an interrupt for the interrupt enable flag (I flag) is enabled.
(5) Set the VCA20 bit to 0 using the timer RA interrupt (every 1 second) or $\overline{\text{INT0}}$ interrupt (falling edge signal) and the MCU exits wait mode. When the MCU exits wait mode, XCIN keeps operating at the system clock. If the MCU exits wait mode using the timer RA interrupt, a clock update is performed and the MCU enters wait mode again after returning to the main process. If the MCU exits wait mode using the $\overline{\text{INT0}}$ interrupt, it does not enter wait mode after setting 0 to the variable (mode) and returning to the main process.
(6) After oscillating the XIN clock and waiting until the XIN clock oscillation stabilizes when the variable (mode) is 0, switch to use the XIN clock as the system clock, and set the operating mode to high-speed clock mode (no division).
(7) Repeat steps (3) to (6).

Refer to r01an0077_src_sample1 for the sample program.

Figure 3.1 shows a Wait Mode Operating Example.

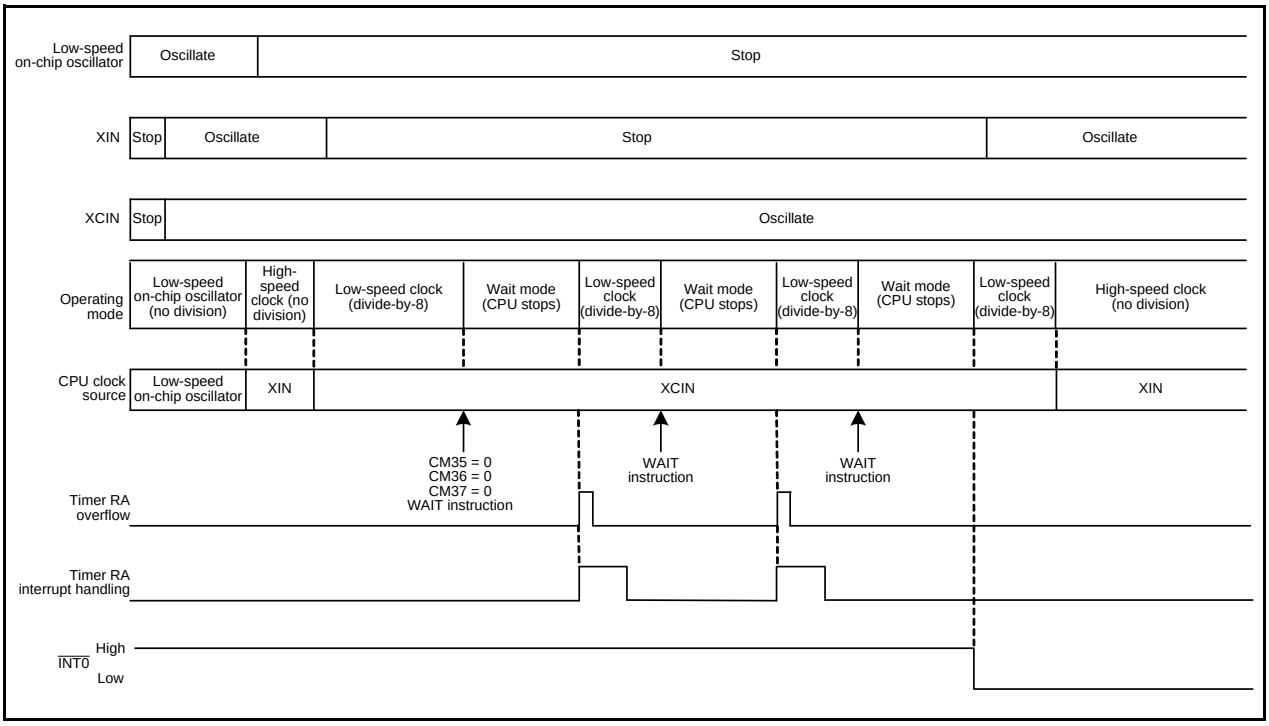


Figure 3.1 Wait Mode Operating Example

Table 3.1 Pin Used and Its Function

Pin Name	I/O	Function
P4_5/$\overline{\text{INT0}}$	Input	Wait mode exit signal

3.2 Sample Program 2 Outline

Operating modes are switched and the MCU enters and exits wait mode according to the procedure shown below. The timer RA interrupt is used to exit wait mode.

(1) After reset is deasserted, the MCU enters low-speed on-chip oscillator mode (divide-by-8 mode) by a program. Set the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled) and the VCA20 bit in the VCA2 register to 0 (internal power low consumption disabled).

(2) When entering wait mode, set the following:
- Set the CM35 bit in the CM3 register to 0 (settings of the CM06 bit in the CM0 register, and bits CM16 and CM17 in the CM1 register are enabled).
- Set bits CM37 and CM36 in the CM3 register to 11b (select the XIN clock as the system clock when exiting wait mode or stop mode).
- Set the FMR27 bit to 0 (low-current-consumption read mode disabled).

(3) Execute the WAIT instruction to enter wait mode. At this point, an interrupt used for exiting wait mode is enabled and an interrupt for the interrupt enable flag (I flag) is enabled.

(4) After entering wait mode, a timer RA interrupt is generated and the MCU exits wait mode. There is no handling for the timer RA interrupt. When the MCU exits wait mode, the XIN clock automatically becomes the system clock, and the operating mode is changed to high-speed clock mode (divide-by-8 mode). After waiting for the XIN clock oscillation to stabilize, change the operating mode to high-speed clock mode (no division) by a program.

Refer to r01an0077_src_sample2 for the sample program.

Figure 3.2 shows Wait Mode Operating Example.

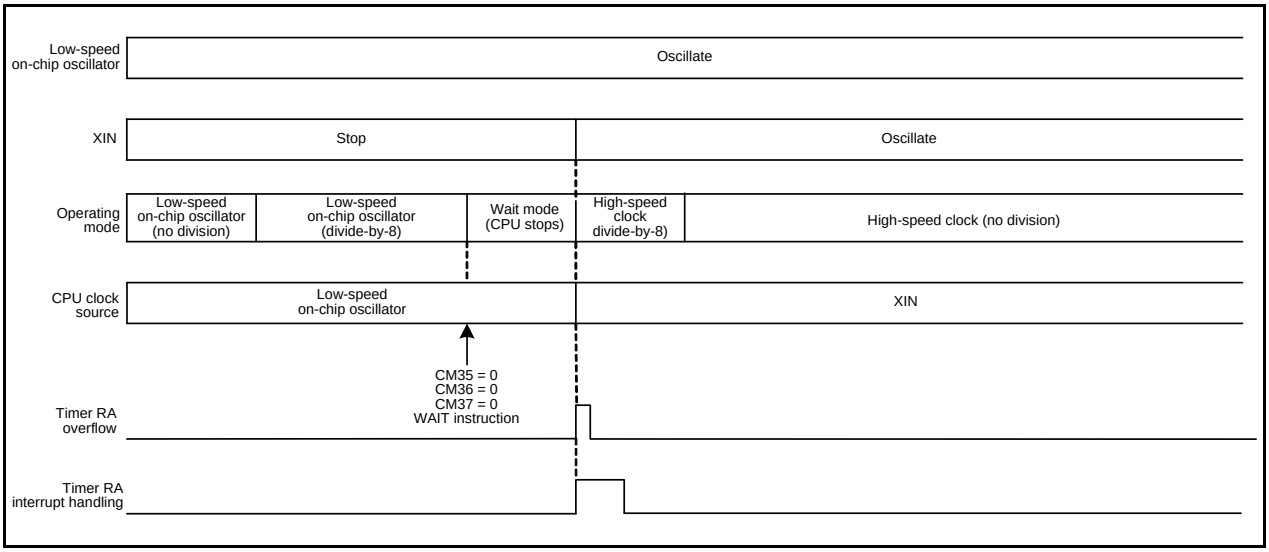


Figure 3.2 Wait Mode Operating Example

3.3 Memory

Table 3.2 Memory for Sample Program 1

Memory	Size	Remarks
ROM	451 bytes	In the r01an0077_src_sample1.c module
RAM	4 bytes	In the r01an0077_src_sample1.c module
Maximum user stack	10 bytes	
Maximum interrupt stack	18 bytes	

Table 3.3 Memory for Sample Program 2

Memory	Size	Remarks
ROM	213 bytes	In the r01an0077_sample2.c module
RAM	0 bytes	In the r01an0077_sample2.c module
Maximum user stack	10 bytes	
Maximum interrupt stack	18 bytes	

Memory size varies depending on the C compiler version and compile options.
The above apply to the following conditions:
C compiler: M16C Series, R8C Family C Compiler V.5.45 Release 01
Compile options: -c -finfo -dir “$(CONFIGDIR)” -R8C

4. Software

This section shows the initial setting procedures and values to set the example described in section **3. Application Examples**. Refer to the latest **R8C/35A Group** hardware user's manual for details on individual registers.

The × in the register's Setting Value represents bits not used in this application, blank spaces represent bits that do not change, and the dash represents reserved bits or bits that have nothing assigned.

4.1 Function Tables

Declaration	void mcu_init (void)		
Outline	System clock setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Oscillate the XIN clock and then XCIN clock. Set the system clock (XIN clock). Stop the low-speed on-chip oscillator.		

Declaration	void sfr_init (void)		
Outline	Initial setting of SFRs		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Perform initial setting for the SFRs to use the wait mode exit signal (P4_5/$\overline{\text{INT0}}$) as an input port. Perform initial setting for the SFR to use timer RA in timer mode.		

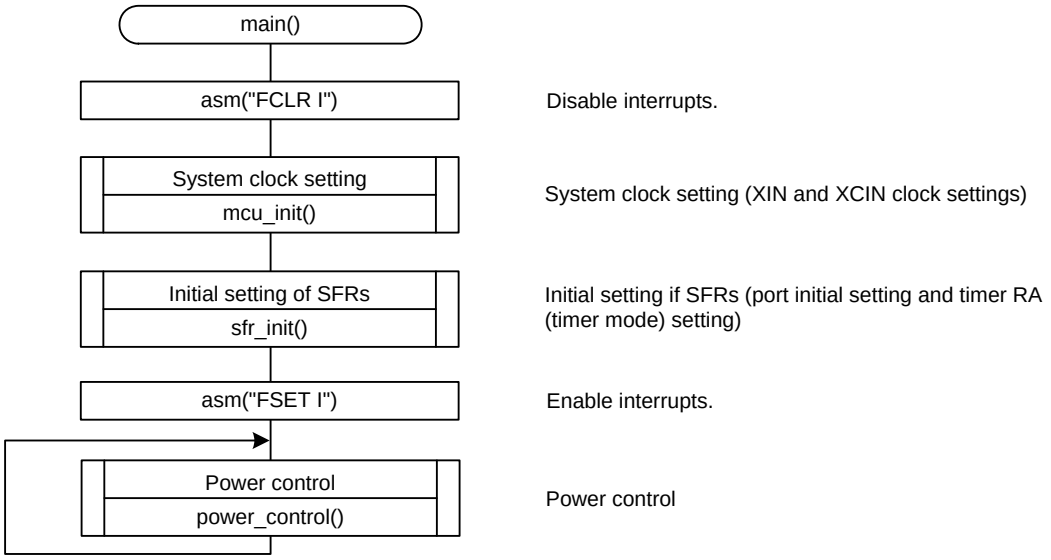
Declaration	void_power_control (void)		
Outline	Power control processing		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	unsigned char mode		Mode control
Returned value	Type	Value	Meaning
	None	—	—
Function	Perform wait mode enter processing and wait mode exit processing.		

Declaration	void _int0 (void)		
Outline	$\overline{\text{INT0}}$ interrupt handling		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	unsigned char mode		Mode control
Returned value	Type	Value	Meaning
	None	—	—
Function	Disable internal power low consumption in the $\overline{\text{INT0}}$ interrupt handling (VCA20 is 0). Exit wait mode (mode is 0)		

Declaration	void _timer_ra (void)		
Outline	Timer RA interrupt handling		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	unsigned char sec_cnt		Second counter
	unsigned char min_cnt		Minute counter
	unsigned char hour_cnt		Hour counter
Returned value	Type	Value	Meaning
	None	—	—
Function	Disable internal power low consumption (VCA20 is 0) and perform the clock update in the timer RA interrupt handling.		

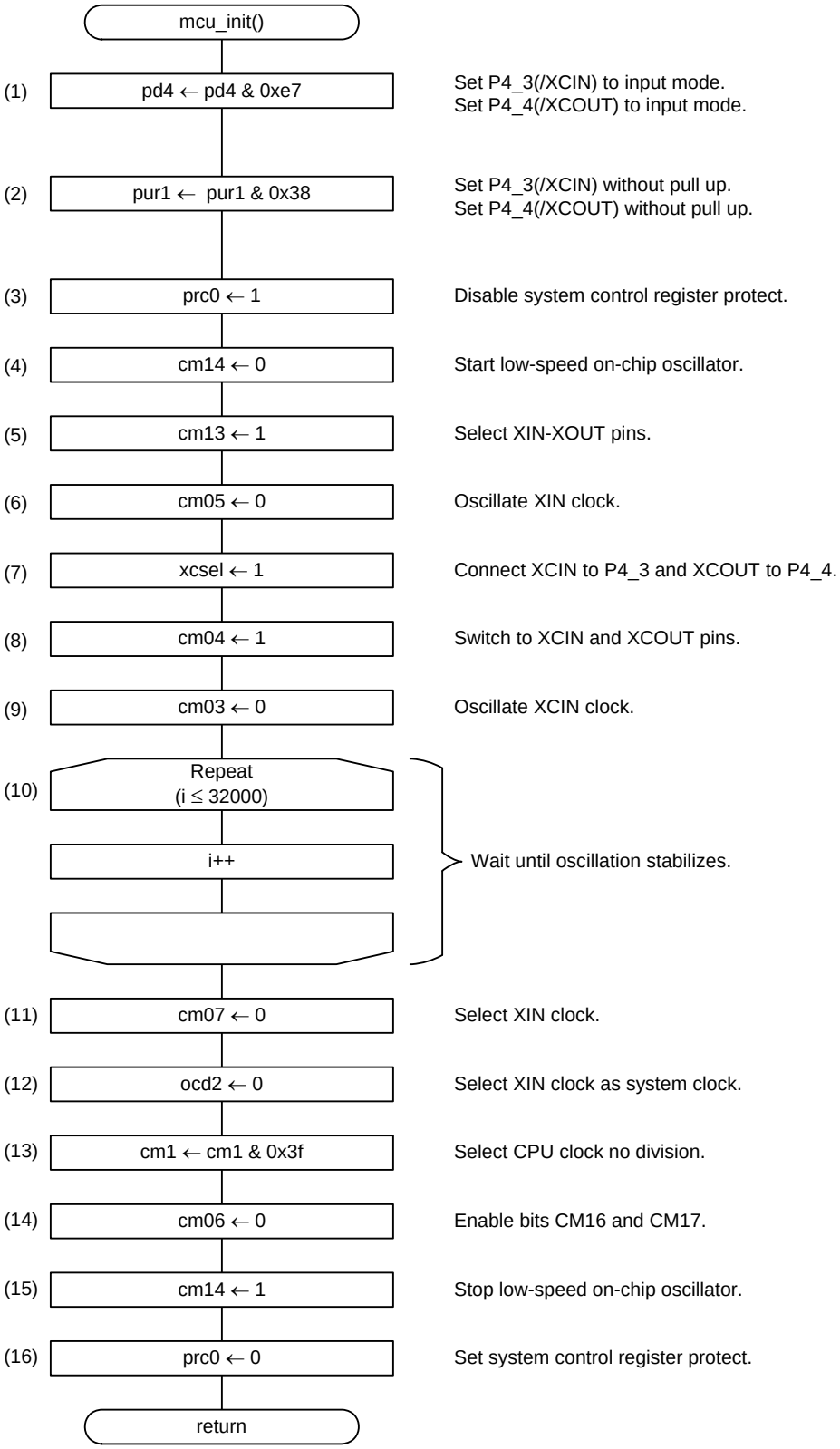
4.2 Main Function

• Flowchart



4.3 System Clock Setting

• Flowchart



• Register settings

(1) Set P4_3(/XCIN) and P4_4(/XCOUT) to input mode.

Port P4 Direction Register (PD4)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x		0	0	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b3	PD4_3	Port P4_3 direction bit	0: Input mode (functions as an input port)	R/W
b4	PD4_4	Port P4_4 direction bit	0: Input mode (functions as an input port)	R/W

(2) Set P4_3(/XCIN) and P4_4(/XCOUT) without pull-up.

Pull-Up Control Register 1 (PUR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	x	x	x	—	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PU10	P4_3 pull-up	0: Not pulled up	R/W
b1	PU11	P4_4 to P4_7 pull-up	0: Not pulled up	R/W

(3) Enable writing to registers CM0, CM1, CM3, and OCD.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—		x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, and OCD 1: Write enabled	R/W

(4) Start the low-speed on-chip oscillator.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			—	0		x	x	x

Bit	Symbol	Bit Name	Function	R/W
b4	CM14	Low-speed on-chip oscillator stop bit	0: Low-speed on-chip oscillator on	R/W

(5) Switch P4_6 and P4_7 to XIN-XOUT pins.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			—		1	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b3	CM13	Port/XIN-XOUT switch bit	1: XIN-XOUT pins	R/W

(6) Oscillate the XIN clock.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			0				—	—

Bit	Symbol	Bit Name	Function	R/W
b5	CM05	XIN clock (XIN-XOUT) stop bit	0: XIN clock oscillates	R/W

(7) Connect XCIN to P4_3 and XCOUT to P4_4.

I/O Function Pin Select Register (PINSR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	x	x	—	—	1

Bit	Symbol	Bit Name	Function	R/W
b0	XCSEL	XCIN/XCOUT pin connect bit	1: XCIN connected to P4_3, XCOUT connected to P4_4	R/W

(8) Switch to XCIN-XCOUT pins.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value				1			—	—

Bit	Symbol	Bit Name	Function	R/W
b4	CM04	Port/XCIN-XCOUT switch bit	1: XCIN-XCOUT pins	R/W

(9) Oscillate the XCIN clock.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value					0		—	—

Bit	Symbol	Bit Name	Function	R/W
b3	CM03	XCIN clock stop bit	0: XCIN clock oscillates	R/W

(10) Wait until oscillation stabilizes.

(11) Select the XIN clock.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0						—	—

Bit	Symbol	Bit Name	Function	R/W
b7	CM07	XIN, XCIN clock select bit	0: XIN clock	R/W

(12) Select the XIN clock as the system clock.

Oscillation Stop Detection Register (OCD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	0	x	x

Bit	Symbol	Bit Name	Function	R/W
b2	OCD2	System clock select bit	1: XIN clock selected	R/W

(13) Set CPU clock division select bit 1.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	—			x	x	x

Bit	Symbol	Bit Name	Function	R/W
b6	CM16	CPU clock division select bit 1	b7 b6 0 0: No division mode	R/W
b7	CM17			R/W

(14) Set CPU clock division select bit 0.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		0					—	—

Bit	Symbol	Bit Name	Function	R/W
b6	CM06	CPU clock division select bit 0	0: Bits CM16 and CM17 in CM1 register enabled	R/W

(15) Stop the low-speed on-chip oscillator.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			—	1		x	x	x

Bit	Symbol	Bit Name	Function	R/W
b4	CM14	Low-speed on-chip oscillator stop bit	1: Low-speed on-chip oscillator off	R/W

(16) Disable writing to registers CM0, CM1, CM3, and OCD.

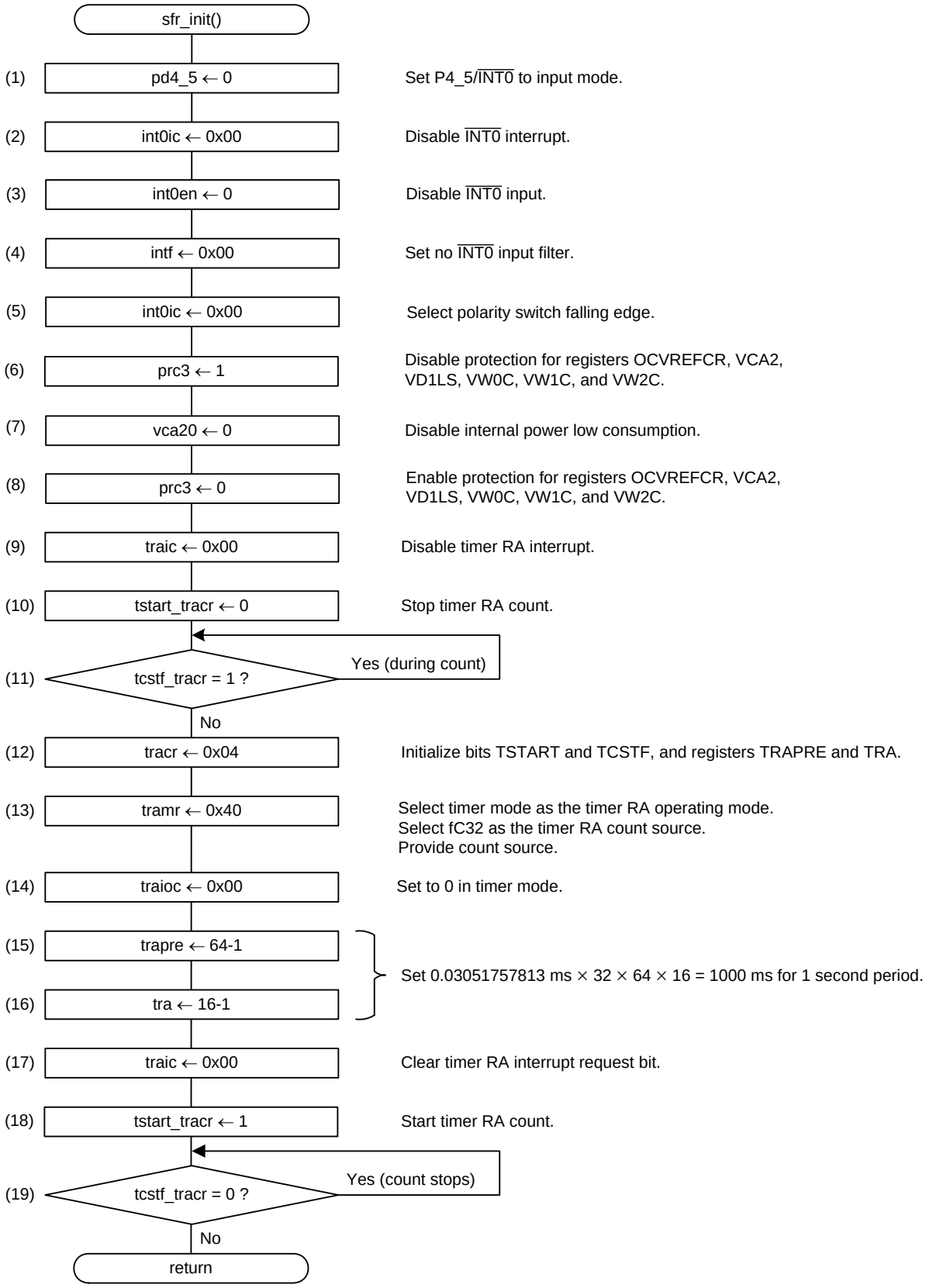
Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—		x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, and OCD. 0: Write disabled	R/W

4.4 Initial Setting of SFRs

• Flowchart



• Register Settings

(1) Set P4_5/$\overline{\text{INT0}}$ to input mode.

Port P4 Direction Register (PD4)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	0			—	—	—

Bit	Symbol	Bit Name	Function	R/W
b5	PD4_5	Port P4_5 direction bit	0: Input mode (functions as an input port)	R/W

(2) Disable the $\overline{\text{INT0}}$ interrupt.

INT0 Interrupt Control Register (INT0IC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—		0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(3) Disable $\overline{\text{INT0}}$ input.

External Input Enable Register 0 (INTEN)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	x	x	x		0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0EN	$\overline{\text{INT0}}$ input enable bit	0: Disabled	R/W

(4) Set to no $\overline{\text{INT0}}$ input filter.

INT Input Filter Select Register 0 (INTF)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	x	x	x	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0F0	$\overline{\text{INT0}}$ input filter select bit	b1 b0 0 0: No filter	R/W
b1	INT0F1			R/W

(5) Set $\overline{\text{INT0}}$ polarity switch to the falling edge.

INT0 Interrupt Control Register (INT0IC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	0				

Bit	Symbol	Bit Name	Function	R/W
b4	POL	Polarity switch bit	0: Falling edge selected	R/W

(6) Enable writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	1	x	x	

Bit	Symbol	Bit Name	Function	R/W
b3	PRC3	Protect bit 3	Enables writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C. 1: Write enabled	R/W

(7) Disable internal power low consumption.

Voltage Detect Register 2 (VCA2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value				x	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	VCA20	Internal power low consumption enable bit	0: Low power consumption disabled	R/W

(8) Disable writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	x	x	

Bit	Symbol	Bit Name	Function	R/W
b3	PRC3	Protect bit 3	Enables writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C. 0: Write disabled	R/W

(9) Disable the timer RA interrupt.

Interrupt Control Register (TRAIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(10) Stop the timer RA count.

Timer RA Control Register (TRACR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—			—			0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RA count start bit	0: Count stops	R/W

(11) Wait until the timer RA count stops.

Timer RA Control Register (TRACR)

Bit	Symbol	Bit Name	Function	R/W
b1	TCSTF	Timer RA count status flag	0: Count stops 1: During count	R

(12) Initialize bits TSTART and TCSTF, and registers TRAPRE and TRA.

Timer RA Control Register (TRACR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	0	0	—	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RA count start bit	0: Count stops	R/W
b1	TCSTF	Timer RA count status flag	0: Count stops	R
b2	TSTOP	Timer RA count forcible stop bit	When this bit is set to 1, the count is forcibly stopped. When read, its content is 0.	R/W
b4	TEDGF	Active edge judgment flag	0: Active edge not received	R/W
b5	TUNDF	Timer RA underflow flag	0: No underflow	R/W

(13)Set the timer RA mode register.

Timer RA Mode Register (TRAMR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	1	0	0	—	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RA operating mode select bit	b2 b1 b0 0 0 0: Timer mode	R/W
b1	TMOD1			R/W
b2	TMOD2			R/W
b4	TCK0	Timer RA count source select bit	b6 b5 b4 1 0 0: fC32	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	TCKCUT	Timer RA count source cutoff bit	0: Provides count source	R/W

(14) Set the timer RA I/O control register.

Timer RA I/O Control Register (TRAIOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	Set to 0 in timer mode.	R/W
b1	TOPCR	TRAIO output control bit		R/W
b2	TOENA	TRAO output enable bit		R/W
b3	TIOSEL	Hardware LIN function select bit	Set to 0. When using hardware LIN function, set to 1.	R/W
b4	TIPF0	TRAIO input filter select bit	Set to 0 in timer mode.	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIO event input control bit		R/W
b7	TIOGT1			R/W

(15) Set 64-1 (3Fh) to the timer RA prescaler register.

Timer RA Prescaler Register (TRAPRE)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	1	1	1	1	1	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts an internal count source	00h to FFh	R/W

(16) Set 16-1 (0Fh) to the timer RA register.

Timer RA Register (TRA)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	1	1	1	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts on underflow of TRAPRE register	00h to FFh	R/W

(17) Clear the timer RA interrupt request bit.

Interrupt Control Register (TRAIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(18) Start timer RA counter.

Timer RA Control Register (TRACR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—			—			1

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RA count start bit	1: Count starts	R/W

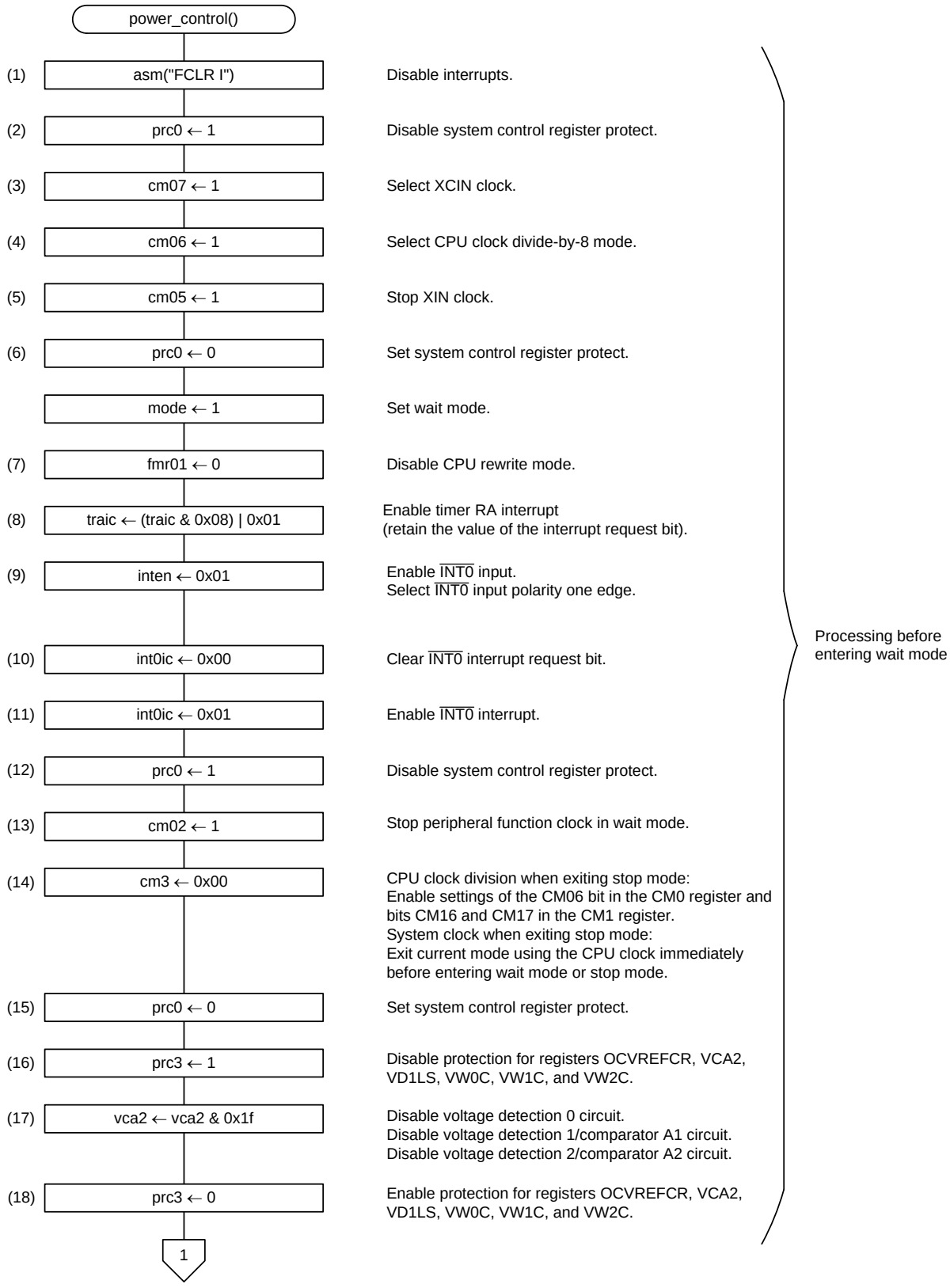
(19) Wait until the timer RA count starts.

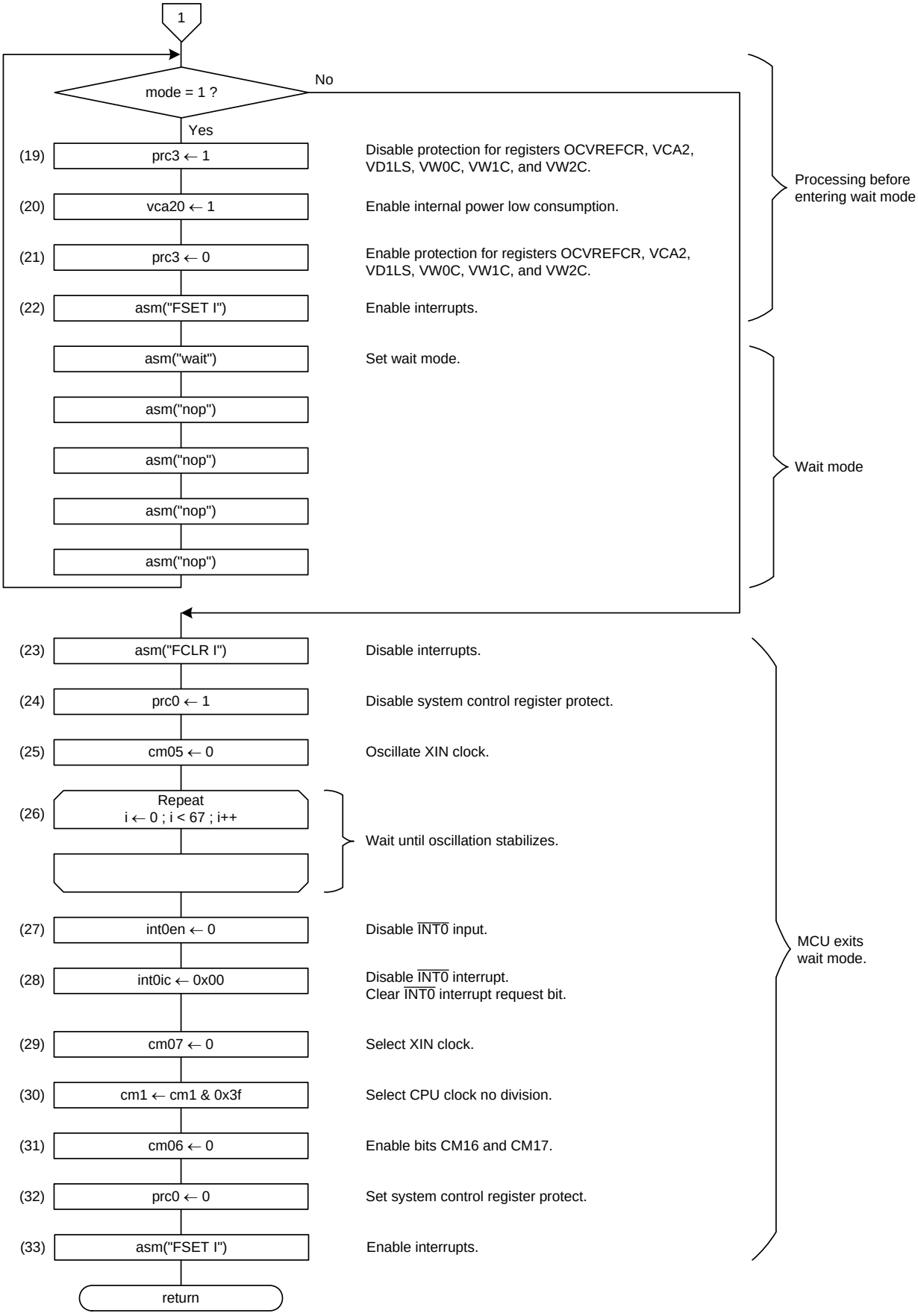
Timer RA Control Register (TRACR)

Bit	Symbol	Bit Name	Function	R/W
b1	TCSTF	Timer RA count status flag	0: Count stops 1: During count	R

4.5 Power Control Processing

• Flowchart




1
mode = 1 ?
No
Yes
(19) prc3 ← 1
Disable protection for registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C.
(20) vca20 ← 1
Enable internal power low consumption.
(21) prc3 ← 0
Enable protection for registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C.
(22) asm("FSET I")
Enable interrupts.
Processing before entering wait mode
asm("wait")
Set wait mode.
asm("nop")
asm("nop")
asm("nop")
asm("nop")
Wait mode
(23) asm("FCLR I")
Disable interrupts.
(24) prc0 ← 1
Disable system control register protect.
(25) cm05 ← 0
Oscillate XIN clock.
(26) Repeat i ← 0 ; i < 67 ; i++
Wait until oscillation stabilizes.
(27) int0en ← 0
Disable INT0 input.
(28) int0ic ← 0x00
Disable INT0 interrupt.
Clear INT0 interrupt request bit.
(29) cm07 ← 0
Select XIN clock.
(30) cm1 ← cm1 & 0x3f
Select CPU clock no division.
(31) cm06 ← 0
Enable bits CM16 and CM17.
(32) prc0 ← 0
Set system control register protect.
(33) asm("FSET I")
Enable interrupts.
MCU exits wait mode.
return

• Register settings

(1) Disable interrupts.

(2) Enable writing to registers CM0, CM1, CM3, and OCD.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—		x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, and OCD. 1: Write enabled	R/W

(3) Select the XCIN clock.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1						—	—

Bit	Symbol	Bit Name	Function	R/W
b7	CM07	XIN, XCIN clock select bit	1: XCIN clock	R/W

(4) Set CPU clock division select bit 0.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		1					—	—

Bit	Symbol	Bit Name	Function	R/W
b6	CM06	CPU clock division select bit 0	1: Divide-by-8 mode	R/W

(5) Stop the XIN clock.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			1				—	—

Bit	Symbol	Bit Name	Function	R/W
b5	CM05	XIN clock (XIN-XOUT) stop bit	1: XIN clock stops	R/W

(6) Disable writing to registers CM0, CM1, CM3, and OCD.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—		x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, and OCD. 0: Write disabled	R/W

(7) Disable CPU rewrite mode.

Flash Memory Control Register 0 (FMR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	x	x	x	0	—

Bit	Symbol	Bit Name	Function	R/W
b1	FMR01	CPU rewrite mode select bit	0: CPU rewrite mode disabled	R/W

(8) Enable the timer RA interrupt. At this point, retain the value of the interrupt request bit.

Interrupt Control Register (TRAIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—		0	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 1: Level 1	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W

(9) Set to $\overline{\text{INT0}}$ input enable and set $\overline{\text{INT0}}$ input polarity to one edge.

External Input Enable Register 0 (INTEN)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	x	x	x	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	INT0EN	$\overline{\text{INT0}}$ input enable bit	1: Enabled	R/W
b1	INT0PL	$\overline{\text{INT0}}$ input polarity select bit	0: One edge	R/W

(10) Clear the $\overline{\text{INT0}}$ interrupt request bit.

INT0 Interrupt Control Register (INT0IC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—		0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(11) Enable the $\overline{\text{INT0}}$ interrupt.

INT0 Interrupt Control Register (INT0IC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—		0	0	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 1: Level 1	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(12) Enable writing to registers CM0, CM1, CM3, and OCD.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—		x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, and OCD. 1: Write enabled	R/W

(13) Stop the peripheral function clock in wait mode.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value						1	—	—

Bit	Symbol	Bit Name	Function	R/W
b2	CM02	Wait mode peripheral function clock stop bit	1: Peripheral function clock stops in wait mode	R/W

(14) Set the CM35 bit to 0 (settings of the CM06 bit in the CM0 register, and bits CM16 and CM17 in the CM1 register are enabled). Set bits CM37 and CM36 to 0 (the MCU exits the current mode using the CPU clock immediately before entering wait or stop mode).

System Clock Control Register 3 (CM3)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	—	—	—	—	x

Bit	Symbol	Bit Name	Function	R/W
b5	CM35	CPU clock division when exiting wait mode select bit	0: Following settings are enabled: CM06 bit in CM0 register Bits CM16 and CM17 in CM1 register	R/W
b6	CM36	System clock when exiting wait mode or stop mode select bit	b7 b6 0 0: MCU exits with the CPU clock immediately before entering wait or stop mode.	R/W
b7	CM37			R/W

(15) Disable writing to registers CM0, CM1, CM3, and OCD.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—		x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, and OCD. 0: Write disabled	R/W

(16) Enable writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	1	x	x	

Bit	Symbol	Bit Name	Function	R/W
b3	PRC3	Protect bit 3	Enables writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C. 1: Write enabled	R/W

(17) Disable the voltage detection 0 circuit, voltage detection 1/comparator A1 circuit, and voltage detection 2/ comparator A2 circuit.

Voltage Detect Register 2 (VCA2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	x	x	x	x	

Bit	Symbol	Bit Name	Function	R/W
b5	VCA25	Voltage detection 0 enable bit	0: Voltage detection 0 circuit disabled	R/W
b6	VCA26	Voltage detection 1/ comparator A1 enable bit	0: Voltage detection 1/comparator A1 circuit disabled	R/W
b7	VCA27	Voltage detection 2/ comparator A2 enable bit	0: Voltage detection 2/comparator A2 circuit disabled	R/W

(18) Disable writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	x	x	

Bit	Symbol	Bit Name	Function	R/W
b3	PRC3	Protect bit 3	Enables writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C. 0: Write disabled	R/W

(19) Enable writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	1	x	x	

Bit	Symbol	Bit Name	Function	R/W
b3	PRC3	Protect bit 3	Enables writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C. 1: Write enabled	R/W

(20) Enable internal power low consumption.

Voltage Detect Register 2 (VCA2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value				x	x	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	VCA20	Internal power low consumption enable bit	1: Low consumption enabled	R/W

(21) Disable writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	x	x	

Bit	Symbol	Bit Name	Function	R/W
b3	PRC3	Protect bit 3	Enables writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C. 0: Write disabled	R/W

(22) Enable interrupts.

(23) Disable interrupts.

(24) Enable writing to registers CM0, CM1, CM3, and OCD.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—		x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, and OCD. 1: Write enabled	R/W

(25) Oscillate the XIN clock.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			0				—	—

Bit	Symbol	Bit Name	Function	R/W
b5	CM05	XIN clock (XIN-XOUT) stop bit	0: XIN clock oscillates	R/W

(26) Wait until oscillation stabilizes.

(27) Disable $\overline{\text{INT0}}$ input.

External Input Enable Register 0 (INTEN)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	x	x	x		0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0EN	$\overline{\text{INT0}}$ input enable bit	1: Disabled	R/W

(28) Disable the $\overline{\text{INT0}}$ interrupt. Clear the $\overline{\text{INT0}}$ interrupt request bit.

INT0 Interrupt Control Register (INT0IC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—		0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(29) Select the XIN clock.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0						—	—

Bit	Symbol	Bit Name	Function	R/W
b7	CM07	XIN, XCIN clock select bit	0: XIN clock	R/W

(30) Set CPU clock division select bit 1.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	—			x	x	x

Bit	Symbol	Bit Name	Function	R/W
b6	CM16	CPU clock division select bit 1	b7 b6 0 0: No division mode	R/W
b7	CM17			R/W

(31) Set CPU clock division select bit 0.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		0					—	—

Bit	Symbol	Bit Name	Function	R/W
b6	CM06	CPU clock division select bit 0	0: Bits CM16 and CM17 in CM1 register enabled	R/W

(32) Disable writing to registers CM0, CM1, CM3, and OCD.

Protect Register (PRCR)

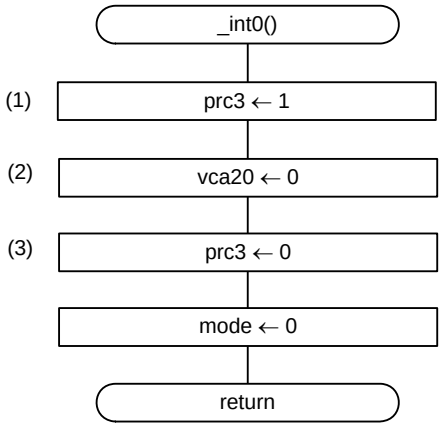
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—		x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, and OCD. 0: Write disabled	R/W

(33) Enable interrupts.

4.6 $\overline{\text{INT0}}$ Interrupt Handling

• Flowchart



Disable protection to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C.

Disable internal power low consumption.

Enable protection to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C.

Exit wait mode.

• Register settings

(1) Enable writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	1	x	x	

Bit	Symbol	Bit Name	Function	R/W
b3	PRC3	Protect bit 3	Enables writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C. 1: Write enabled	R/W

(2) Disable internal power low consumption.

Voltage Detect Register 2 (VCA2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value				x	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	VCA20	Internal power low consumption enable bit	0: Power low consumption disabled	R/W

(3) Disable writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C.

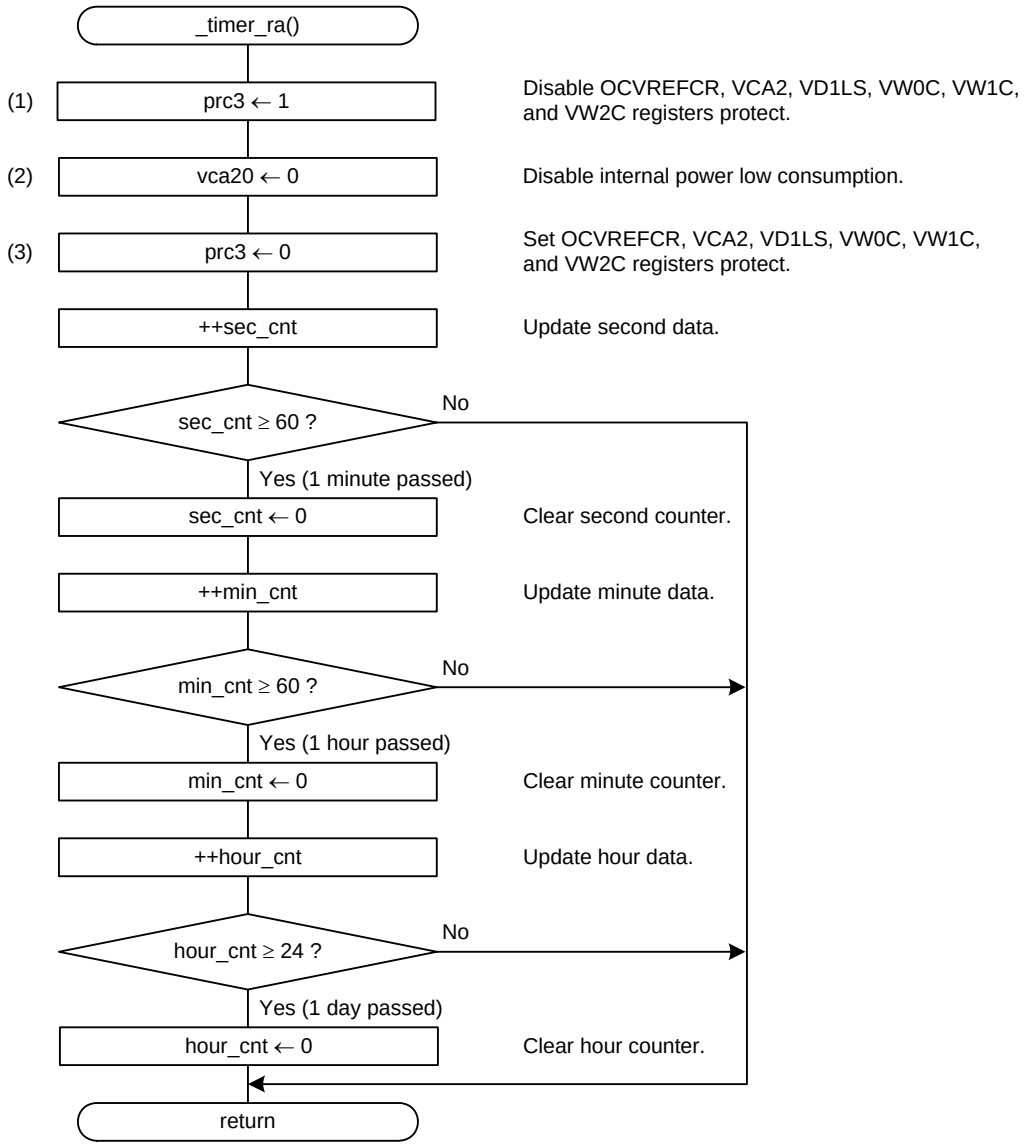
Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	x	x	

Bit	Symbol	Bit Name	Function	R/W
b3	PRC3	Protect bit 3	Enables writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C. 0: Write disabled	R/W

4.7 Timer RA Interrupt Handling

• Flowchart



• Register settings

(1) Enable writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	1	x	x	

Bit	Symbol	Bit Name	Function	R/W
b3	PRC3	Protect bit 3	Enables writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C. 1: Write enabled	R/W

(2) Disable internal power low consumption.

Voltage Detect Register 2 (VCA2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value				x	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	VCA20	Internal power low consumption enable bit	0: Power low consumption disabled	R/W

(3) Disable writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	x	x	

Bit	Symbol	Bit Name	Function	R/W
b3	PRC3	Protect bit 3	Enables writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C. 0: Write disabled	R/W

5. Sample Program

A sample program can be downloaded from the Renesas Electronics website.
To download, click “Application Notes” in the left-hand side menu of the R8C Family page.

6. Reference Documents

R8C/35A Group User’s Manual: Hardware Rev.0.40
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

Website and Support

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Revision History	R8C/35A Group Power Control Using Wait Mode

Rev.	Date	Description	
		Page	Summary
1.00	Dec. 22, 2010	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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