R8C/35A Group

Power Control Using Stop Mode

R01AN0076EJ0100
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1. Abstract

This document describes a setting method and application examples for power control using stop mode.

2. Introduction

The application example described in this document applies to the following microcomputer (MCU) and parameters:

- MCU: R8C/35A Group
- Oscillation frequencies: 20 MHz (XIN clock), 32.768 kHz (XCIN clock)

This application note can be used with other R8C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Application Examples

This application note describes application examples of the following three sample programs:

- Sample program 1
  Reset → Low-speed on-chip oscillator (no division mode) → High-speed clock mode (no division mode) → Stop mode → High-speed clock mode (divide-by-8 mode) → High-speed clock mode (no division mode)
- Sample program 2
  Reset → Low-speed on-chip oscillator (no division mode) → Low-speed on-chip oscillator (divide-by-8 mode) → Stop mode → High-speed clock mode (divide-by-8 mode) → High-speed clock mode (no division mode)
- Sample program 3
  Reset → Low-speed on-chip oscillator (no division mode) → Low-speed clock mode (divide-by-8 mode) → Stop mode → Low-speed clock mode (divide-by-8 mode) → Low-speed clock mode (no division mode)

The shared program outlines are as follows:

- Power control modes are switched by signals input from an external source. The following pins are used for signals input from an external source.
  Stop mode enter signal: Active level (low) and P1_7
  Stop mode exit signal: Active level (low) and P4_5/$\overline{\text{INT0}}$
- In this application note, operation after reset is deasserted is referred to as standard operating mode (mode = 0).
- When the stop mode enter signal is enabled in standard operating mode (mode = 0), the MCU enters stop mode (mode = 1) by a program. When the stop mode enter signal is held low three times consecutively, it is determined that the signal is enabled.
- When the falling edge (from high level to low level) is input to the stop mode exit signal in stop mode, the MCU exits stop mode by the $\overline{\text{INT0}}$ interrupt.

Table 3.1 shows the pins used and their functions.

Table 3.1 Pins Use and Their Functions

Pin Name	I/O	Function
P1_7	Input	Stop mode enter signal
P4_5/$\overline{\text{INT0}}$	Input	Stop mode exit signal

3.1 Sample Program 1 Outline

- After reset is deasserted, the MCU enters high-speed clock mode (no division mode) by a program.
- Timer RA generates a 10 ms main period.
- When entering stop mode, set the following:

(1) Set the CM35 bit in the CM3 register to 0 (settings of the CM06 bit in the CM0 register, and bits CM16 and CM17 in the CM1 register are enabled).

(2) Set bits CM37 and CM36 in the CM3 register to 00b (the MCU exits the current mode using the CPU clock immediately before entering wait mode or stop mode).

Since the CM06 bit becomes 1 (divide-by-8 mode) when entering stop mode, the operating mode changes to high-speed clock mode (divide-by-8 mode) after exiting stop mode. The MCU enters high-speed clock mode (no division mode) by a program after exiting stop mode.

Refer to r01an0076_src_sample1 for the sample program.

Figure 3.1 shows Transition between Modes and Figure 3.2 shows a Procedure for Transitioning between Various Modes.

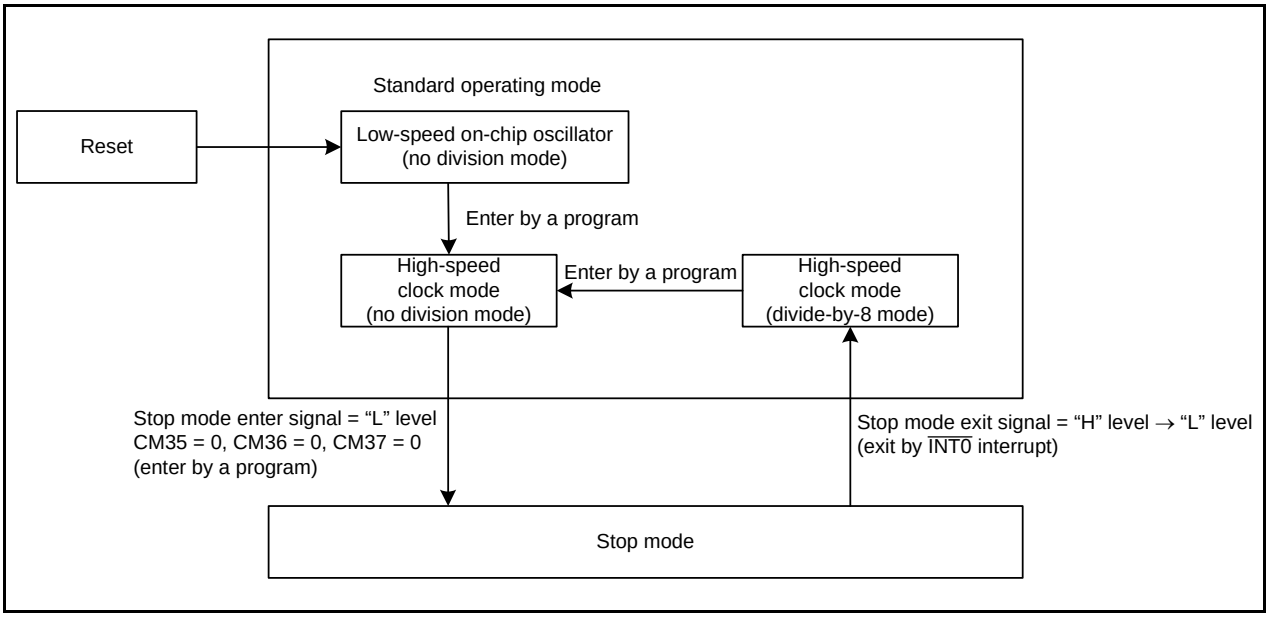


Figure 3.1 Transition between Modes

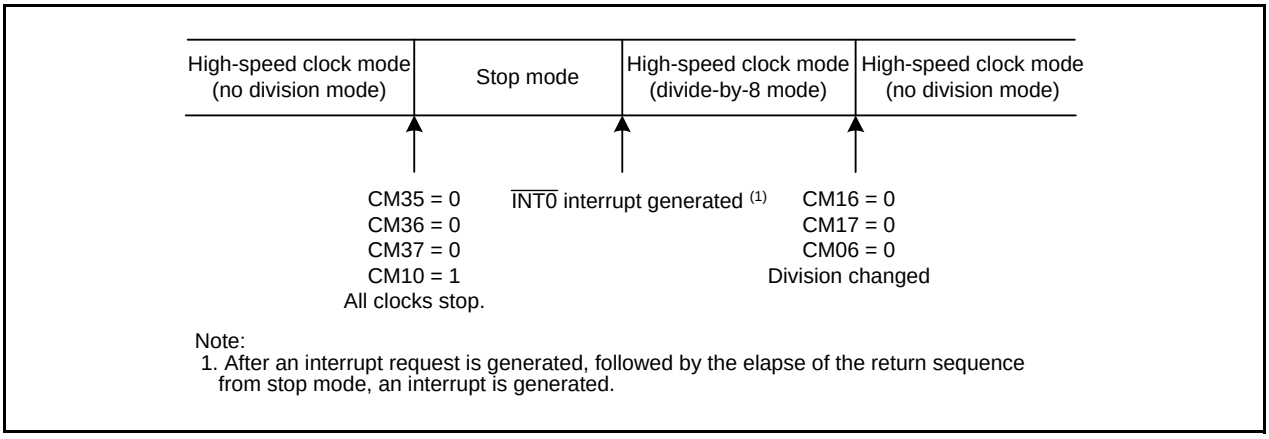


Figure 3.2 Procedure for Transitioning between Various Modes

3.2 Sample Program 2 Outline

- After reset is deasserted, the MCU enters low-speed on-chip oscillator mode (divide-by-8 mode) by a program.
- Set the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled) and the VCA20 bit in the VCA2 register to 0 (internal power low consumption disabled).
- Timer RA generates a 10 ms main period.
- When entering stop mode, set the following:

(1) Set the CM35 bit in the CM3 register to 0 (settings of the CM06 bit in the CM0 register, and bits CM16 and CM17 in the CM1 register are enabled).
(2) Set bits CM37 and CM36 in the CM3 register to 11b (select the XIN clock for the system clock when exiting wait mode or stop mode).
(3) Set the FMR27 bit to 0 (low-current-consumption read mode disabled).

Since the CM06 bit becomes 1 (divide-by-8 mode) when entering stop mode, the operating mode changes to high-speed clock mode (divide-by-8 mode) after exiting stop mode. The MCU enters high-speed clock mode (no division mode) by a program after exiting stop mode.

Refer to r01an0076_src_sample2 for the sample program.

Figure 3.3 shows Transition between Modes and Figure 3.4 shows a Procedure for Transitioning between Various Modes.

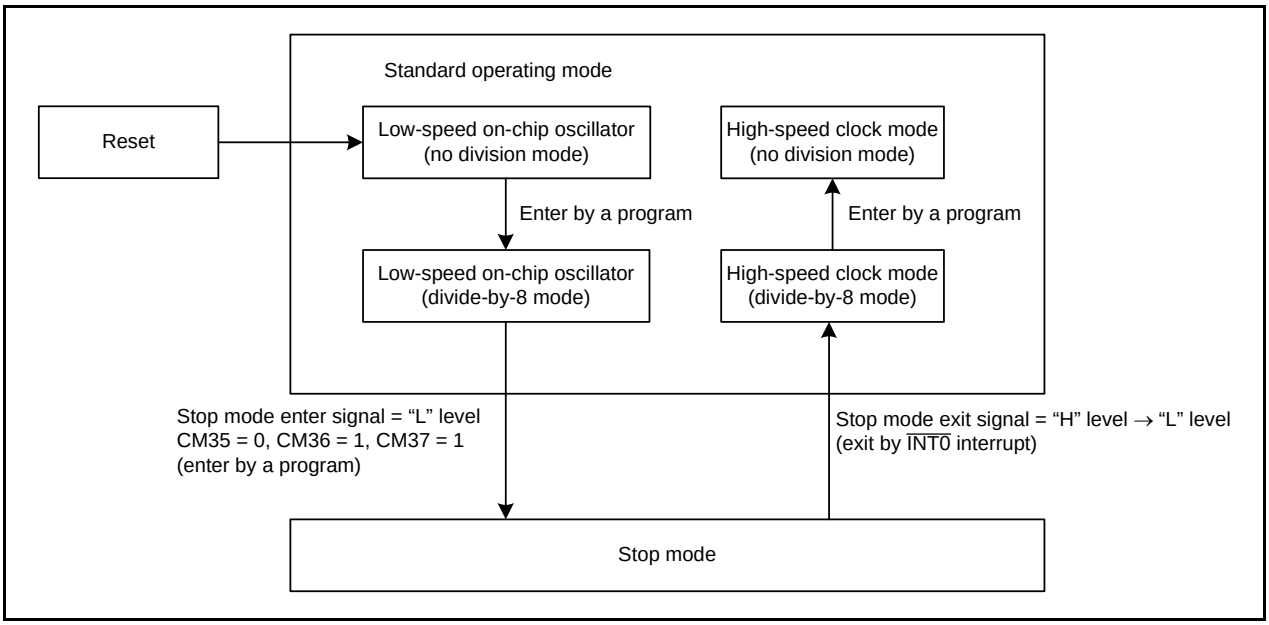


Figure 3.3 Transition between Modes

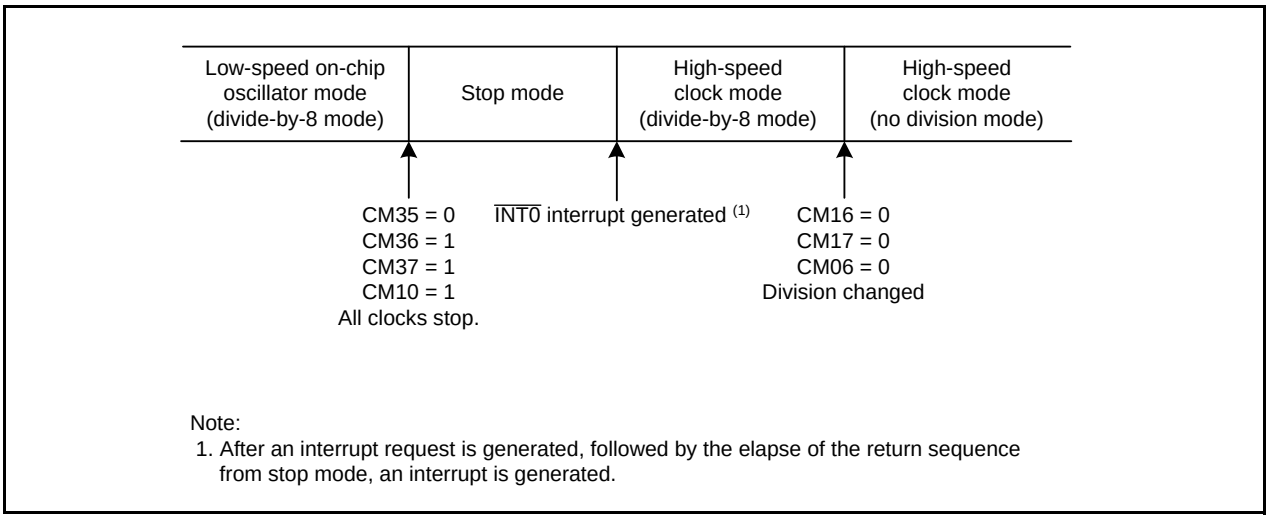


Figure 3.4 Procedure for Transitioning between Various Modes

3.3 Sample Program 3 Outline

- After reset is deasserted, the MCU enters low-speed clock mode (divide-by-8 mode) by a program.
- Timer RA generates a main period of approximately 60 ms.
- When entering stop mode, set the following:

(1) Set the CM35 bit in the CM3 register to 0 (settings of the CM06 bit in the CM0 register, and bits CM16 and CM17 in the CM1 register are enabled).

(2) Set bits CM37 and CM36 in the CM3 register to 00b (the MCU exits the current mode using the CPU clock immediately before entering wait mode or stop mode). Since the CM06 bit becomes 1 (divide-by-8 mode) when entering stop mode, the operating mode changes to low-speed clock mode (divide-by-8 mode) after exiting stop mode. Set the MCU to low-speed clock mode (no division mode) by a program after exiting stop mode.

Refer to r01an0076_src_sample3 for the sample program.

Figure 3.5 shows Transition between Modes and Figure 3.6 shows a Procedure for Transitioning between Various Modes.

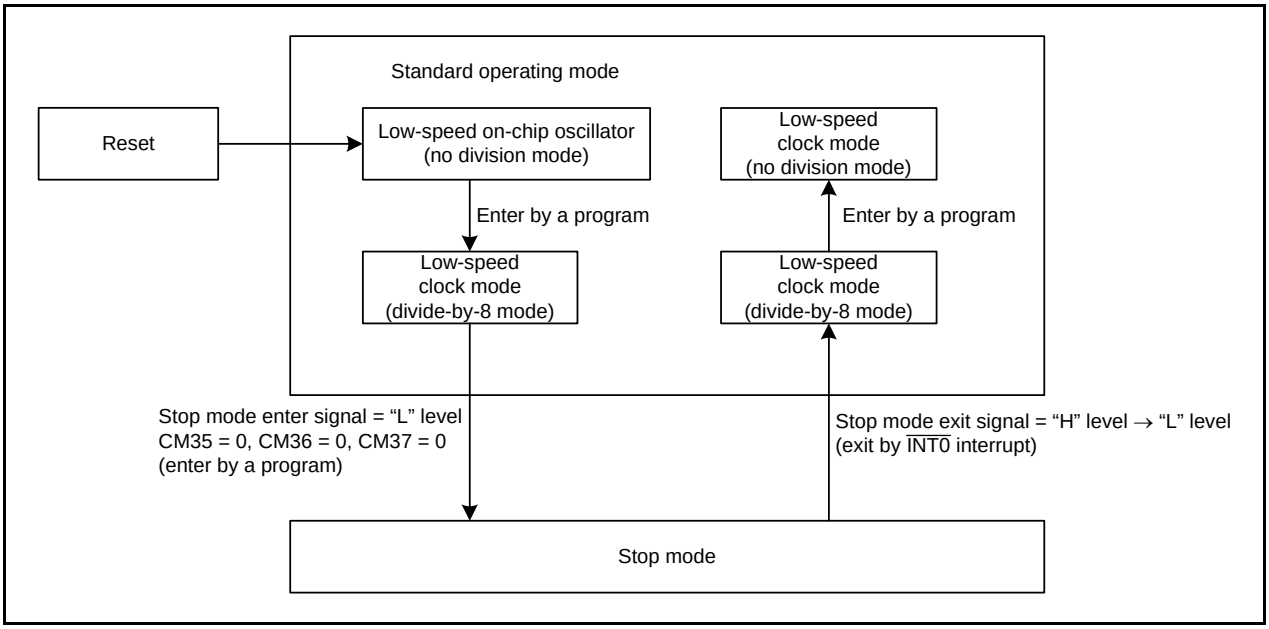


Figure 3.5 Transition between Modes

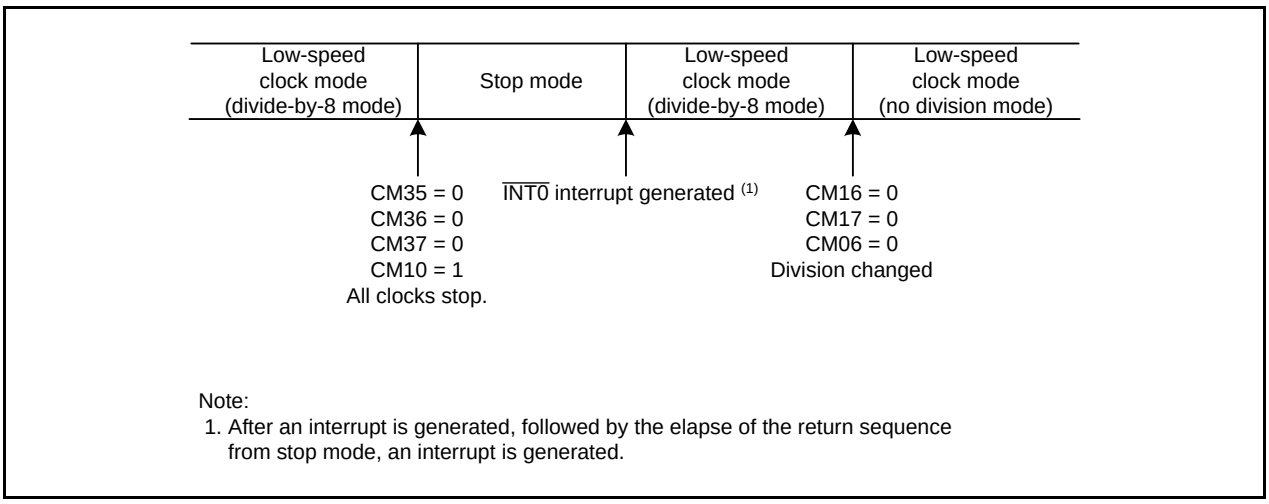


Figure 3.6 Procedure for Transitioning between Various Modes

3.4 Memory

Table 3.2 Memory for Sample Program 1

Memory	Size	Remarks
ROM	359 bytes	In the r01an0076_src_sample1.c module
RAM	2 bytes	In the r01an0076_src_sample1.c module
Maximum user stack	10 bytes	
Maximum interrupt stack	18 bytes	

Table 3.3 Memory for Sample Program 2

Memory	Size	Remarks
ROM	331 bytes	In the r01an0076_sample2.c module
RAM	2 bytes	In the r01an0076_sample2.c module
Maximum user stack	10 bytes	
Maximum interrupt stack	18 bytes	

Table 3.4 Memory for Sample Program3

Memory	Size	Remarks
ROM	335 bytes	In the r01an0076_sample3.c module
RAM	2 bytes	In the r01an0076_sample3.c module
Maximum user stack	10 bytes	
Maximum interrupt stack	18 bytes	

Memory size varies depending on the C compiler version and compile options.
The above apply to the following conditions:
C compiler: M16C Series, R8C Family C Compiler V.5.45 Release 01
Compile options: -c -finfo -dir “$(CONFIGDIR)” -R8C

4. Software

This section shows the initial setting procedures and values to set the example described in section **3. Application Examples**. Refer to the latest **R8C/35A Group** hardware user's manual for details on individual registers.

The × in the register's Setting Value represents bits not used in this application, blank spaces represent bits that do not change, and the dash represents reserved bits or bits that have nothing assigned.

4.1 Function Tables

Declaration	void mcu_init (void)		
Outline	System clock setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Set the system clock (XIN clock).		

Declaration	void sfr_init (void)		
Outline	Initial setting of SFRs		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Perform initial setting for the SFRs to use the stop mode enter signal (P1_7) and stop mode exit signal (P4_5/INT0) as input ports. Perform initial setting for the SFR to use timer RA in timer mode.		

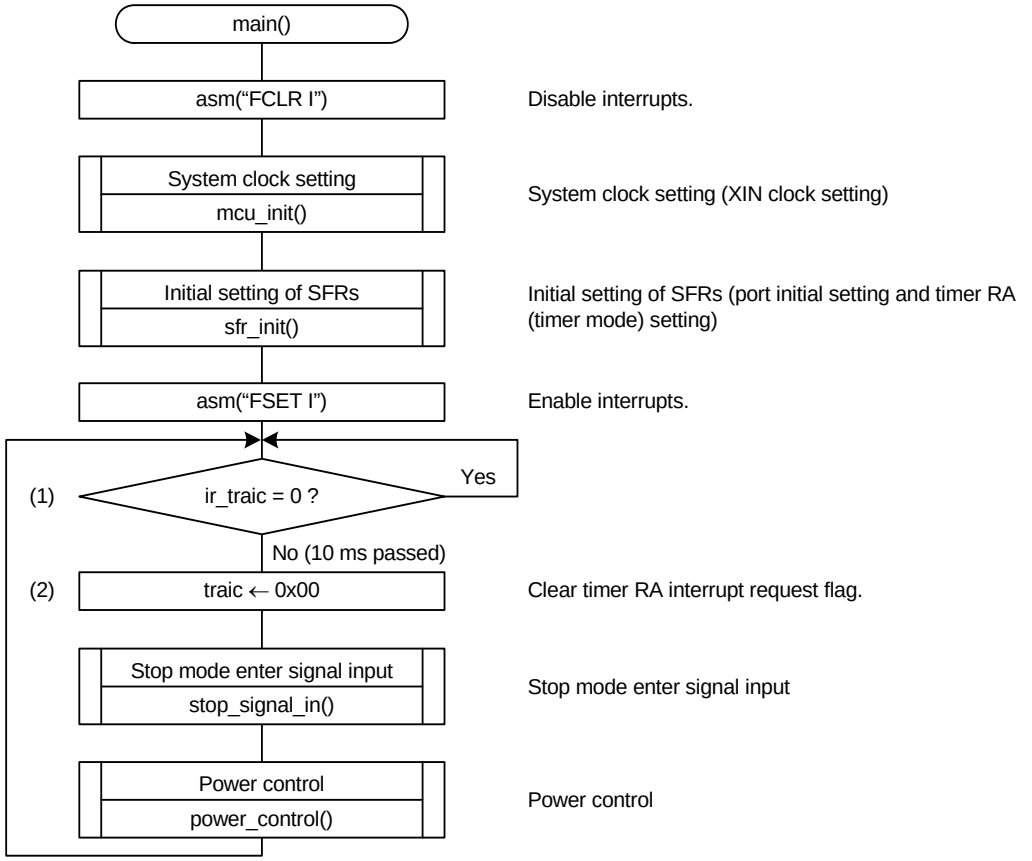
Declaration	void stop_signal_in (void)		
Outline	Stop mode enter signal input		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	unsigned char mode		Mode control
Returned value	Type	Value	Meaning
	None	—	—
Function	Determine the low-level input for the stop mode enter signal (P1_7) three times successively and set the stop mode enter request (mode = 1).		

Declaration	void power_control (void)		
Outline	Power control processing		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	unsigned char mode		Mode control
Returned value	Type	Value	Meaning
	None	—	—
Functions	Perform stop mode enter processing and stop mode exit processing. When exiting stop mode, wait until oscillation stabilizes.		

Declaration	void _int0 (void)		
Outline	$\overline{\text{INT0}}$ interrupt handling		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Protect the system control register in the $\overline{\text{INT0}}$ interrupt handling.		

4.2 Main Function

• Flowchart



• Register settings

(1) Wait until a timer RA interrupt request is generated.

Interrupt Control Register (TRAIC)

Bit	Symbol	Bit Name	Function	R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R/W

(2) Clear the timer RA interrupt request flag.

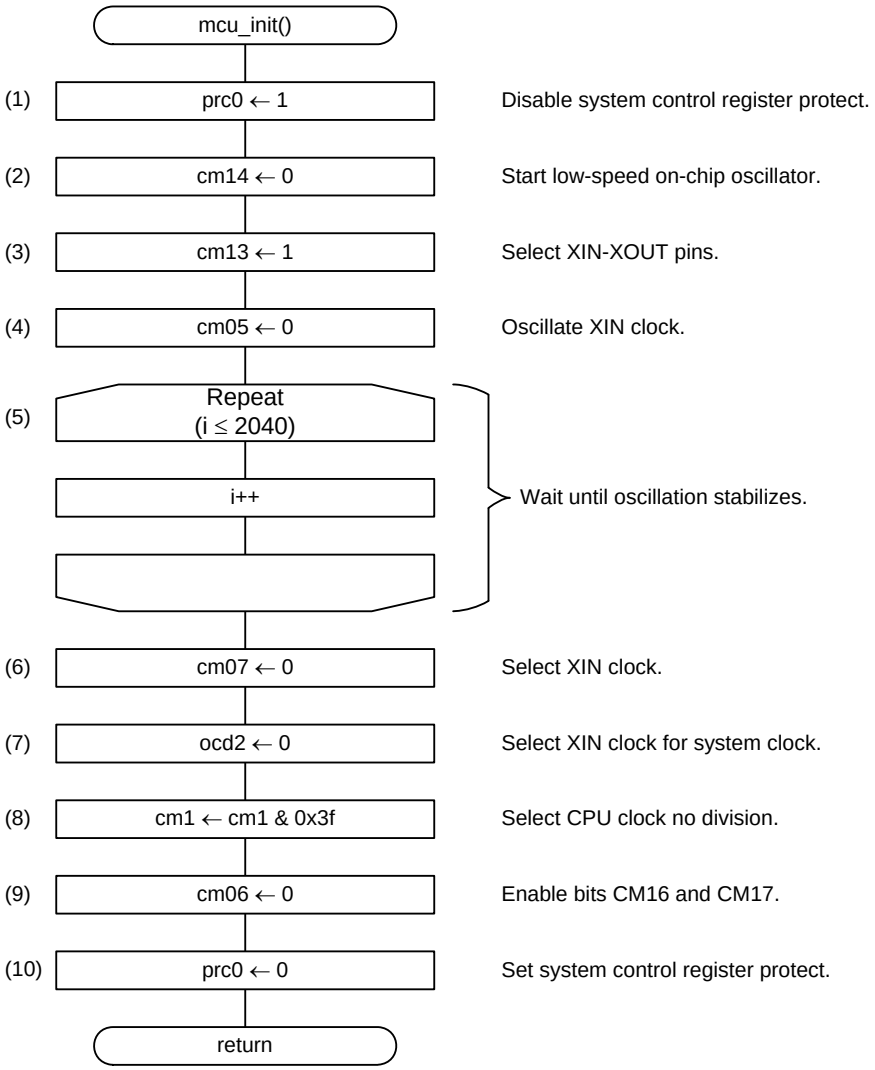
Interrupt Control Register (TRAIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

4.3 System Clock Setting

• Flowchart



• Register settings

(1) Enable writing to registers CM0, CM1, CM3, and OCD.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, and OCD. 1: Write enabled	R/W

(2) Start the low-speed on-chip oscillator.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			—	0		x	x	

Bit	Symbol	Bit Name	Function	R/W
b4	CM14	Low-speed on-chip oscillator stop bit	0: Low-speed on-chip oscillator on	R/W

(3) Switch ports P4_6 and P4_7 to XIN-XOUT pins.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			—		1	x	x	

Bit	Symbol	Bit Name	Function	R/W
b3	CM13	Port/XCIN-XCOUT switch bit	1: XIN-XOUT pins	R/W

(4) Oscillate the XIN clock.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			0	x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b5	CM05	XIN clock (XIN-XOUT) stop bit	0: XIN clock oscillates	R/W

(5) Wait until oscillation stabilizes.

(6) Select the XIN clock.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0			x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b7	CM07	XIN, XCIN clock select bit	0: XIN clock	R/W

(7) Select the XIN clock as the system clock.

Oscillation Stop Detection Register (OCD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	0	x	x

Bit	Symbol	Bit Name	Function	R/W
b2	OCD2	System clock select bit	0: XIN clock selected	R/W

(8) Set CPU clock division select bit 1.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	—			x	x	

Bit	Symbol	Bit Name	Function	R/W
b6	CM16	CPU clock division select bit 1	b7 b6 0 0: No division mode	R/W
b7	CM17			R/W

(9) Set CPU clock division select bit 0.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		0		x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	CM06	CPU clock division select bit 0	0: Bits CM16 and CM17 in CM1 register enabled	R/W

(10) Disable writing to registers CM0, CM1, CM3, and OCD.

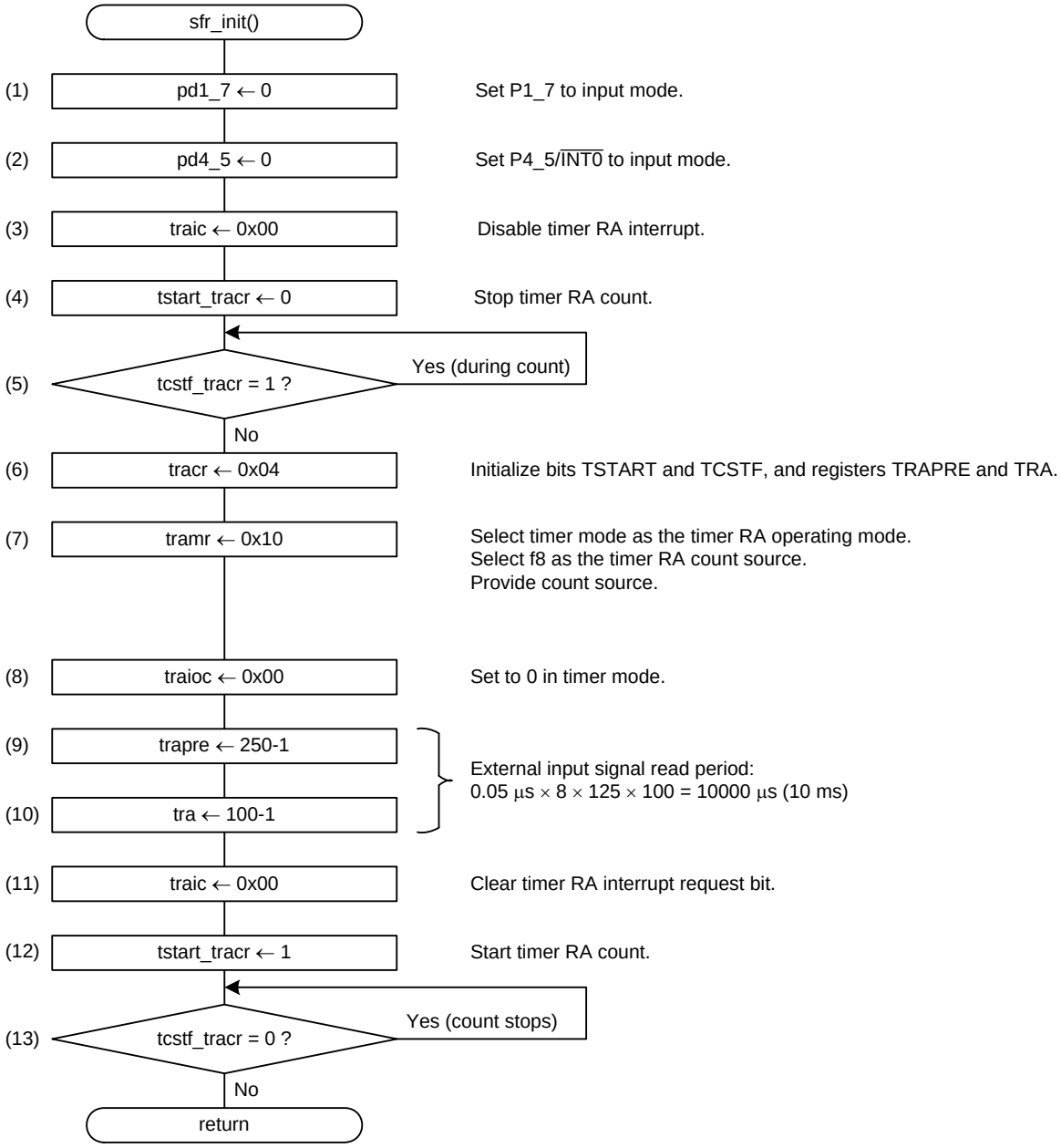
Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, and OCD. 0: Write disabled	R/W

4.4 SFR Initial Setting

• Flowchart



• Register Settings

(1) Set P1_7 to input mode.

Port P1 Direction Register (PD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	x	x	x	x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b7	PD1_7	Port P1_7 direction bit	0: Input mode (functions as an input port)	R/W

(2) Set P4_5/$\overline{\text{INT0}}$ to input mode.

Port P4 Direction Register (PD4)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	0	x	x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b5	PD4_5	Port P4_5 direction bit	0: Input mode (functions as an input port)	R/W

(3) Disable the timer RA interrupt.

Interrupt Control Register (TRAIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(4) Stop the timer RA count.

Timer RA Control Register (TRACR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—			—			0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RA count start bit	0: Count stops	R/W

(5) Wait until the timer RA count stops.

Timer RA Control Register (TRACR)

Bit	Symbol	Bit Name	Function	R/W
b1	TCSTF	Timer RA count status flag	0: Count stops 1: During count	R

(6) Initialize bits TSTART and TCSTF, and registers TRAPRE and TRA.

Timer RA Control Register (TRACR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	0	0	—	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RA count start bit	0: Count stops	R/W
b1	TCSTF	Timer RA count status flag	0: Count stops	R
b2	TSTOP	Timer RA count forcible stop bit	When this bit is set to 1, the count is forcibly stopped. When read, its content is 0.	R/W
b4	TEDGF	Active edge judgment flag	0: Active edge not received	R/W
b5	TUNDF	Timer RA underflow flag	0: No underflow	R/W

(7) Set the timer RA mode register.

Timer RA Mode Register (TRAMR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	1	—	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RA operating mode select bit	b2 b1 b0 0 0 0: Timer mode	R/W
b1	TMOD1			R/W
b2	TMOD2			R/W
b4	TCK0	Timer RA count source select bit	b6 b5 b4 0 0 1: f8	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	TCKCUT	Timer RA count source cutoff bit	0: Provides count source	R/W

(8) Set the timer RA I/O control register.

Timer RA I/O Control Register (TRAIOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	Set to 0 in timer mode.	R/W
b1	TOPCR	TRAIO output control bit		R/W
b2	TOENA	TRAO output enable bit		R/W
b3	TIOSEL	Hardware LIN function select bit	Set to 0. When using hardware LIN function, set to 1.	R/W
b4	TIPF0	TRAIO input filter select bit	Set to 0 in timer mode.	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIO event input control bit		R/W
b7	TIOGT1			R/W

(9) Set 250-1 (F9h) to the timer RA prescaler register.

Timer RA Prescaler Register (TRAPRE)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	1	1	1	1	0	0	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts an internal count source	00h to FFh	R/W

(10) Set 100-1 (63h) to the timer RA register.

Timer RA Register (TRA)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	1	1	0	0	0	1	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts on underflow of TRAPRE register	00h to FFh	R/W

(11) Clear the timer RA interrupt request bit.

Interrupt Control Register (TRAIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(12) Start the timer RA count.

Timer RA Control Register (TRACR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—			—			1

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RA count start bit	1: Count starts	R/W

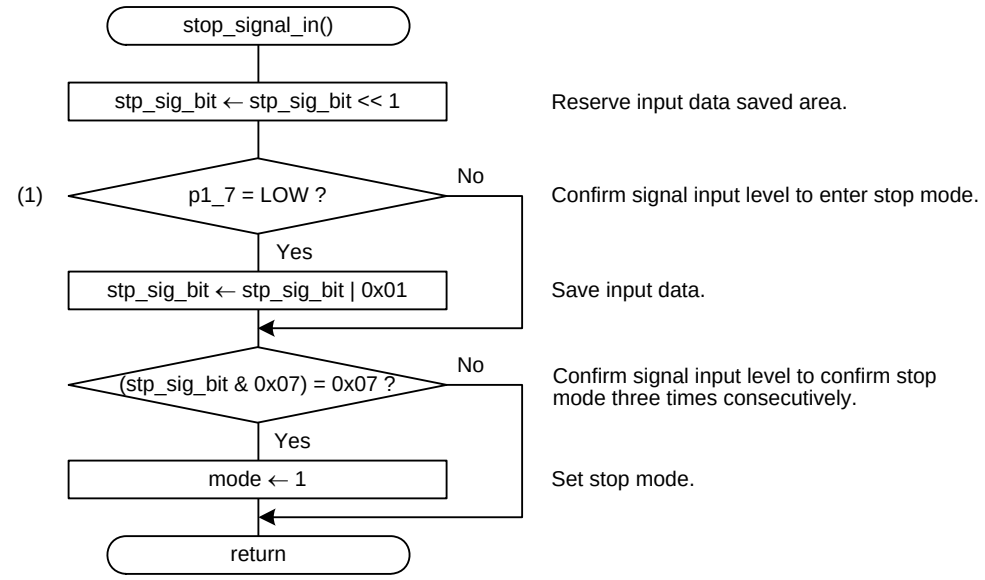
(13) Wait until the timer RA count starts.

Timer RA Control Register (TRACR)

Bit	Symbol	Bit Name	Function	R/W
b1	TCSTF	Timer RA count status flag	0: Count stops 1: During count	R

4.5 Signal Input to Enter Stop Mode

• Flowchart



• Register settings

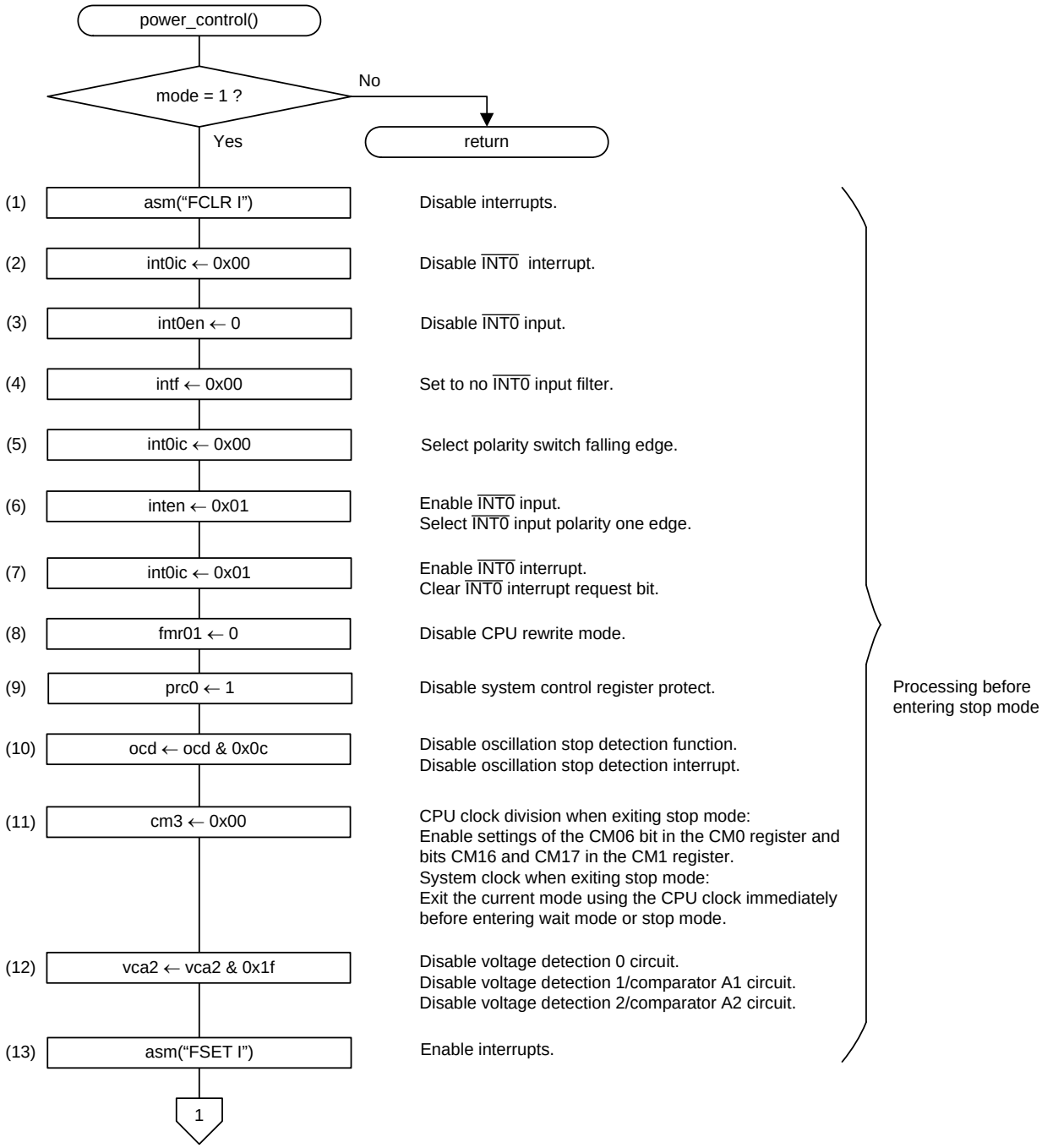
(1) Confirm P1_7 is low.

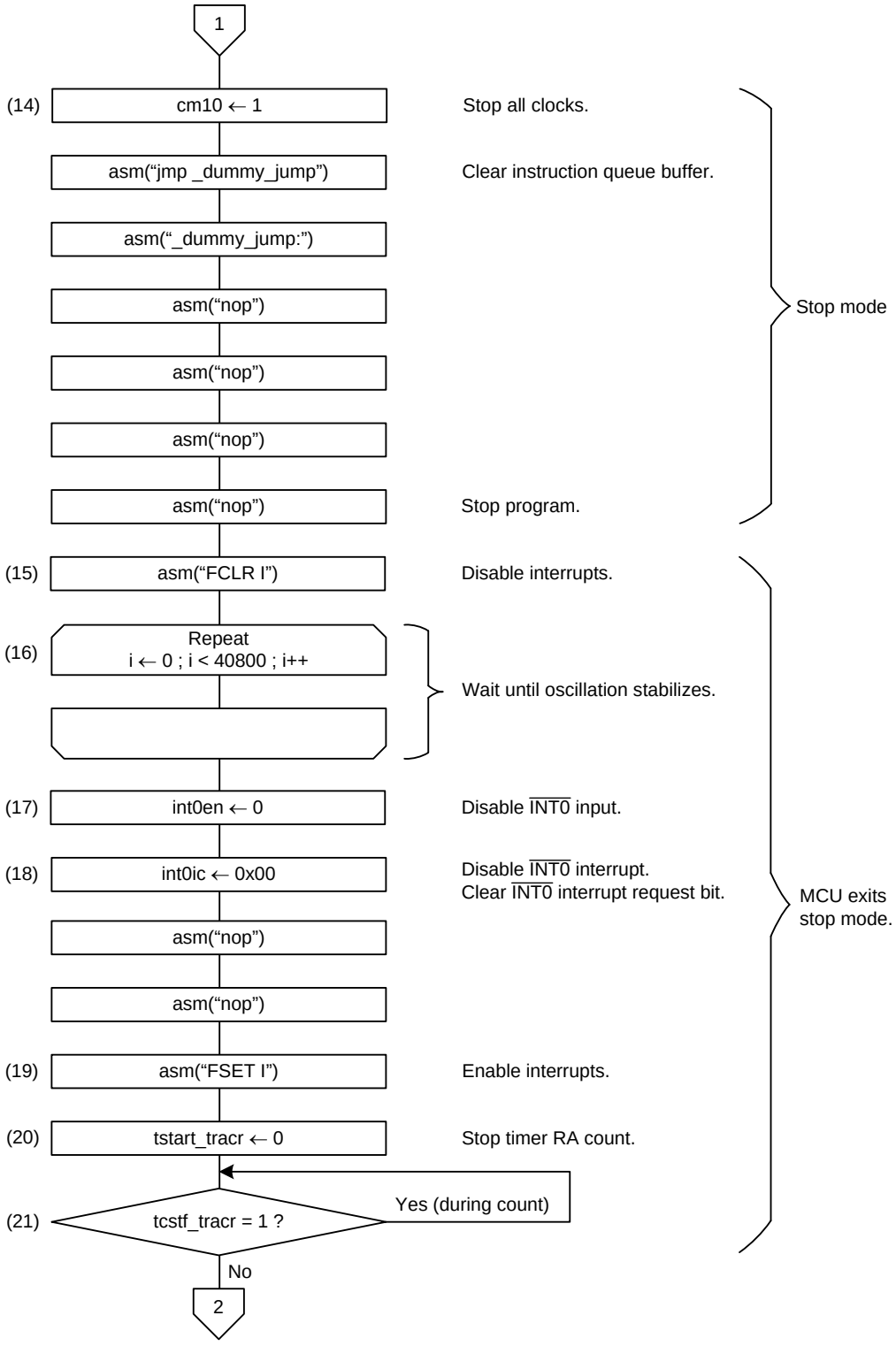
Port P1 Register (P1)

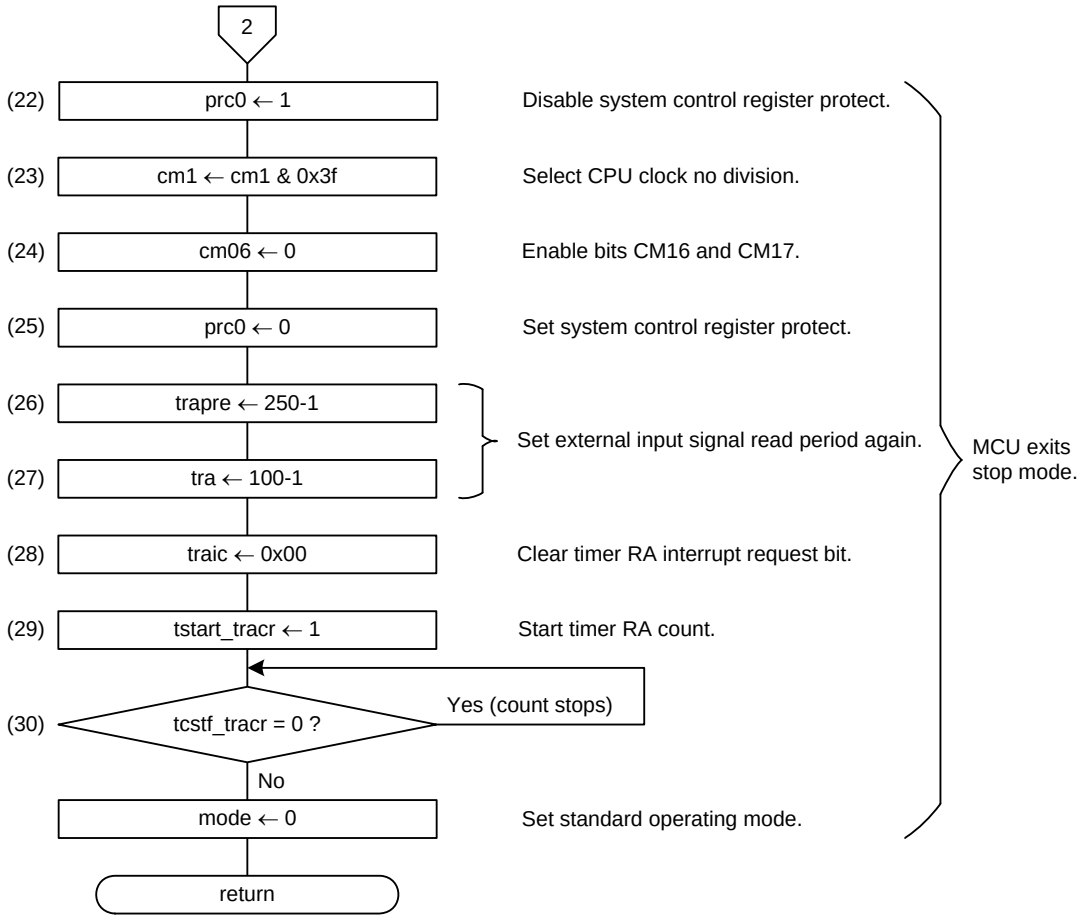
Bit	Symbol	Bit Name	Function	R/W
b7	P1_7	Port P1_7 bit	0: “L” level 1: “H” level	R/W

4.6 Power Control Processing

• Flowchart




1
(14)
cm10 ← 1
Stop all clocks.
asm(“jmp _dummy_jump”)
Clear instruction queue buffer.
asm(“_dummy_jump:”)
asm(“nop”)
asm(“nop”)
asm(“nop”)
asm(“nop”)
Stop program.
Stop mode
(15)
asm(“FCLR I”)
Disable interrupts.
(16)
Repeat
i ← 0 ; i < 40800 ; i++
Wait until oscillation stabilizes.
(17)
int0en ← 0
Disable INT0 input.
(18)
int0ic ← 0x00
Disable INT0 interrupt.
Clear INT0 interrupt request bit.
asm(“nop”)
asm(“nop”)
(19)
asm(“FSET I”)
Enable interrupts.
(20)
tstart_tracr ← 0
Stop timer RA count.
(21)
tcstf_tracr = 1 ?
Yes (during count)
No
2
MCU exits
stop mode.


2
(22)
prc0 ← 1
Disable system control register protect.
(23)
cm1 ← cm1 & 0x3f
Select CPU clock no division.
(24)
cm06 ← 0
Enable bits CM16 and CM17.
(25)
prc0 ← 0
Set system control register protect.
(26)
trapre ← 250-1
Set external input signal read period again.
(27)
tra ← 100-1
(28)
traic ← 0x00
Clear timer RA interrupt request bit.
(29)
tstart_tracr ← 1
Start timer RA count.
(30)
tcstf_tracr = 0 ?
Yes (count stops)
No
mode ← 0
Set standard operating mode.
return
MCU exits stop mode.

• Register settings

(1) Disable interrupts.

(2) Disable the $\overline{\text{INT0}}$ interrupt.

INT0 Interrupt Control Register (INT0IC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—		0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(3) Disable the $\overline{\text{INT0}}$ input.

External Input Enable Register 0 (INTEN)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	x	x	x		0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0EN	$\overline{\text{INT0}}$ input enable bit	0: Disabled	R/W

(4) Set to no $\overline{\text{INT0}}$ input filter.

INT Input Filter Select Register 0 (INTF)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	x	x	x	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0F0	$\overline{\text{INT0}}$ input filter select bit	b1 b0 0 0: No filter	R/W
b1	INT0F1			R/W

(5) Set the $\overline{\text{INT0}}$ polarity switch to the falling edge.

INT0 Interrupt Control Register (INT0IC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	0				

Bit	Symbol	Bit Name	Function	R/W
b4	POL	Polarity switch bit	0: Falling edge selected	R/W

(6) Enable the $\overline{\text{INT0}}$ input and set the $\overline{\text{INT0}}$ input polarity to one edge.

External Input Enable Register 0 (INTEN)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	x	x	x	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	INT0EN	$\overline{\text{INT0}}$ input enable bit	1: Enabled	R/W
b1	INT0PL	$\overline{\text{INT0}}$ input polarity select bit	0: One edge	R/W

(7) Enable the $\overline{\text{INT0}}$ interrupt and clear the $\overline{\text{INT0}}$ interrupt request bit.

INT0 Interrupt Control Register (INT0IC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—		0	0	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 1: Level 1	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(8) Disable CPU rewrite mode.

Flash Memory Control Register 0 (FMR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	x	x	x	0	—

Bit	Symbol	Bit Name	Function	R/W
b1	FMR01	CPU rewrite mode select bit	0: CPU rewrite mode disabled	R/W

(9) Enable writing to registers CM0, CM1, CM3, and OCD.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, and OCD 1: Write enabled	R/W

(10) Disable oscillation stop detection and the oscillation stop detection interrupt.

Oscillation Stop Detection Register (OCD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x		0	0

Bit	Symbol	Bit Name	Function	R/W
b0	OCD0	Oscillation stop detection enable bit	0: Oscillation stop detection function disabled	R/W
b1	OCD1	Oscillation stop detection interrupt enable bit	0: Disabled	R/W

(11) Set the CM35 bit to 0 (settings of the CM06 bit in the CM0 register, and bits CM16 and CM17 in the CM1 register are enabled). Set bits CM37 and CM36 to 0 (the MCU exits the current mode using the CPU clock immediately before entering wait or stop mode).

System Clock Control Register 3 (CM3)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	—	—	—	—	x

Bit	Symbol	Bit Name	Function	R/W
b5	CM35	CPU clock division when exiting wait mode select bit	0: Following settings are enabled: CM06 bit in CM0 register Bits CM16 and CM17 in CM1 register	R/W
b6	CM36	System clock when exiting wait mode or stop mode select bit	b7 b6 0 0: MCU exits with the CPU clock immediately before entering wait or stop mode.	R/W
b7	CM37			R/W

(12) Disable the voltage detection 0 circuit, voltage detection 1/comparator A1 circuit, and voltage detection 2/comparator A2 circuit.

Voltage Detect Register 2 (VCA2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	x	x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b5	VCA25	Voltage detection 0 enable bit	0: Voltage detection 0 circuit disabled	R/W
b6	VCA26	Voltage detection 1/ comparator A1 enable bit	0: Voltage detection 1/comparator A1 circuit disabled	R/W
b7	VCA27	Voltage detection 2/ comparator A2 enable bit	0: Voltage detection 2/comparator A2 circuit disabled	R/W

(13) Enable interrupts.

(14) Stop all clocks (stop mode).

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			—			x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	CM10	All clock stop control bit	1: All clocks stop (stop mode)	R/W

(15) Disable interrupts.

(16) Wait until oscillation stabilizes.

(17) Disable $\overline{\text{INT0}}$ input.

External Input Enable Register 0 (INTEN)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	x	x	x		0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0EN	$\overline{\text{INT0}}$ input enable bit	1: Disabled	R/W

(18) Disable the $\overline{\text{INT0}}$ interrupt. Clear the interrupt request bit.

INT0 Interrupt Control Register (INT0IC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—		0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(19) Enable interrupts.

(20) Stop the timer RA count.

Timer RA Control Register (TRACR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—			—			0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RA count start bit	0: Count stops	R/W

(21) Wait until the timer RA count stops.

Timer RA Control Register (TRACR)

Bit	Symbol	Bit Name	Function	R/W
b1	TCSTF	Timer RA count status flag	0: Count stops 1: During count	R

(22) Enable writing to registers CM0, CM1, CM3, and OCD.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, and OCD 1: Write enabled	R/W

(23) Set CPU clock division select bit 1.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	—			x	x	

Bit	Symbol	Bit Name	Function	R/W
b6	CM16	CPU clock division select bit 1	b7 b6 0 0: No division mode	R/W
b7	CM17			R/W

(24) Set CPU clock division select bit 0.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	0		x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	CM06	CPU clock division select bit 0	0: Bits CM16 and CM17 in CM1 register enabled	R/W

(25) Disable writing to registers CM0, CM1, CM3, and OCD.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, and OCD. 0: Write disabled	R/W

(26) Set 250-1 (F9h) to the timer RA prescaler register.

Timer RA Prescaler Register (TRAPRE)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	1	1	1	1	0	0	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts an internal count source	00h to FFh	R/W

(27) Set 100-1 (63h) to the timer RA register.

Timer RA Register (TRA)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	1	1	0	0	0	1	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts on underflow of TRAPRE register	00h to FFh	R/W

(28) Clear the timer RA interrupt request bit.

Interrupt Control Register (TRAIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(29) Start the timer RA count.

Timer RA Control Register (TRACR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—			—			1

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RA count start bit	1: Count starts	R/W

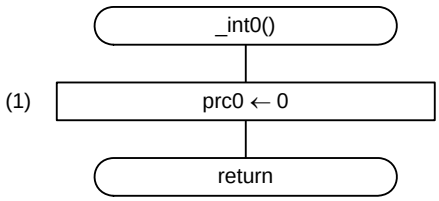
(30) Wait until the timer RA count starts.

Timer RA Control Register (TRACR)

Bit	Symbol	Bit Name	Function	R/W
b1	TCSTF	Timer RA count status flag	0: Count stops 1: During count	R

4.7 $\overline{\text{INT0}}$ Interrupt Handling

• Flowchart



Set system control register protect.

• Register setting

(1) Disable writing to registers CM0, CM1, CM3, and OCD.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, and OCD. 0: Write disabled	R/W

5. Sample Program

A sample program can be downloaded from the Renesas Electronics website.
To download, click “Application Notes” in the left-hand side menu of the R8C Family page.

6. Reference Documents

R8C/35A Group User’s Manual: Hardware Rev.0.40
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

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http://www.renesas.com/

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Revision History	R8C/35A Group Power Control Using Stop Mode

Rev.	Date	Description	
		Page	Summary
1.00	Dec. 17, 2010	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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