FAQs: Low-Voltage Operational Amplifiers

This application note addresses some frequently asked questions about the low-voltage operational amplifiers.

Contents

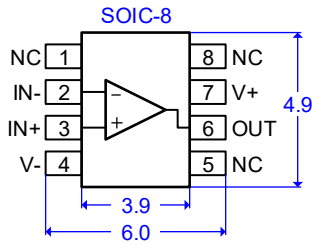
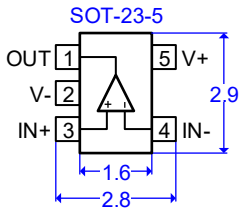
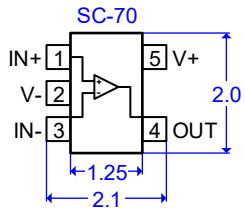
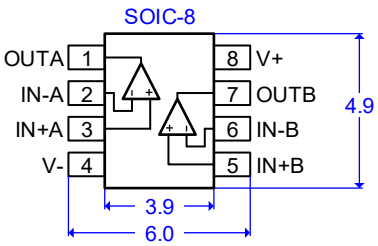
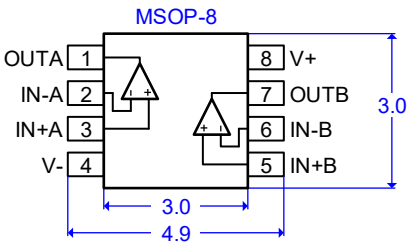
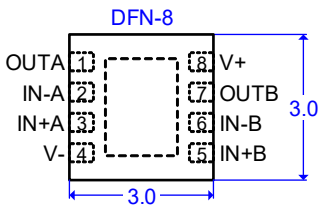
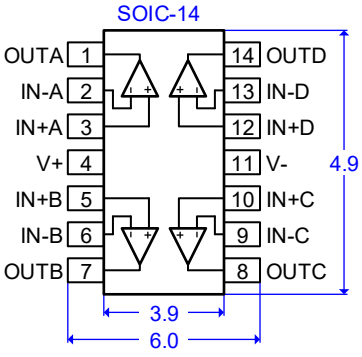
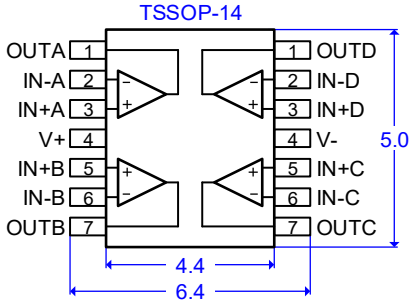
1. What is so special about Renesas low-voltage precision op-amps?

The ISL28134, ISL28x30, and ISL28x33 families of precision low-voltage op amps have ultra-low input offset voltages. These op amps have an automatic offset-zeroing mechanism on-chip and are available in a variety of small packages, making them ideal for precise sensor signal conditioning in space constraint applications.

Table 1. Key Performance Parameters of Auto-Zeroing Amplifiers

Part Number	Ch. (#)	V_{CC} (V)	V_{OS} (µV)	I_B (pA)	I_Q (µA)	GBW (MHz)	SR (V/µs)	R-R	A_{OL} (dB)	CMRR (dB)	PSRR (dB)	Package
ISL28134	1	2.25 to 6	2.5	120	675	3.5	1.5	I/O	174	135	135	SOIC-8, SOT23-5
ISL28133	1	1.8 to 5.5	6	30	18	0.4	0.2	I/O	174	125	138	SOT23-5, SC-70
ISL28233	2											SOIC-8, MSOP-8, DFN-8
ISL28433	4											SOIC-14, TSSOP-14
ISL28130	1	1.8 to 5.5	40	250	20	0.4	0.2	I/O	150	125	138	SOIC-8, SOT23-5, SC-70
ISL28230	2											SOIC-8, MSOP-8, DFN-8
ISL28430	4											SOIC-14, TSSOP-14

Table 2. Package Line-up of Auto-Zeroing Amplifiers

Single Channel			
Dual Channels			
Quad Channels			

2. How can I get the best circuit performance when using ultra-low offset auto-zero amplifiers?

The most important advantage of Renesas' ISL28x3x families of auto-zero amplifiers is their extremely low offset voltage.

Despite having the highest precision amplifier in your circuit, you may not get the highest precision from your application. By using an auto-zero amplifier, the upper limit of precision quickly becomes limited by the circuit design itself and the layout of the printed circuit board (PCB).

A major source of offset voltage errors are thermoelectric voltages on the PCB. This error voltage, also known as Thermocouple- or Seebeck voltages, is created at the junction of two dissimilar metals and is proportional to the temperature of the junction. The Seebeck voltage varies greatly depending on the two metals used and can range from microvolts up to millivolts. Temperature drifts of this voltage can range from a few microvolts to tens of tens of microvolts per degree Celsius.

Typical metallic junctions on a PCB are solder-to-board traces and solder-to-component leads. If the temperature of the PCB at one end of a component is different from the temperature of the other end, the Seebeck voltages are not equal; therefore, resulting in a thermal voltage error. Figure 1 shows an example.

In a high-gain configuration, R_F is much greater than R_G, with the closed-loop gain being simply $A_{CL} = 1 + R_F/R_G$.

A Seebeck difference across R_G appears as an offset voltage directly at the inverting input of the amplifier. This offset error gets amplified by the closed-loop gain, resulting in a substantially larger voltage error at the output.

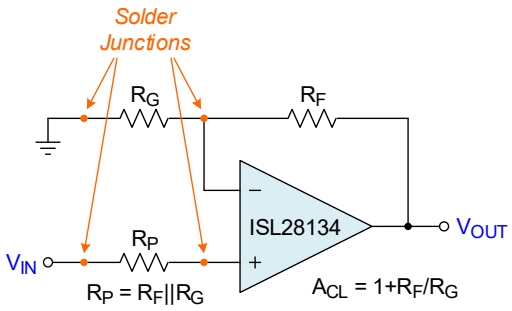


Figure 1. Using a Dummy Resistor Minimizes Offset Errors Because of Seebeck Voltages and Bias Currents

This thermocouple error can be reduced by using a dummy component to match the thermoelectric error source. For example, adding a resistance, R_P, in series with the non-inverting input does not affect the AC performance of the amplifier. However, placing it physically close to R_G ensures their Seebeck potentials are near equal, minimizing the thermocouple error. Furthermore, by matching the value of R_P with the value of the parallel combination of R_G and R_F, ($R_P = R_G \parallel R_F$), the offset error because of input bias currents is also minimized.

The Seebeck voltage difference across the feedback resistor (R_F) is not as critical as this voltage error appears at the output and is not amplified by the closed-loop gain.

Another method for minimizing offset errors because of Seebeck voltages is to maintain a constant ambient temperature throughout the circuit board. Here, using a ground plane in the PCB design helps distribute heat throughout the board and has the added benefit of reducing EMI noise pickup.

The PC board surface should remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board reduces surface moisture and provides a humidity barrier, reducing parasitic resistance on the board.

Using guard rings around the amplifier inputs can further reduce leakage currents. Figure 2 shows an example layout using the surface mount dual amplifier ISL28233.

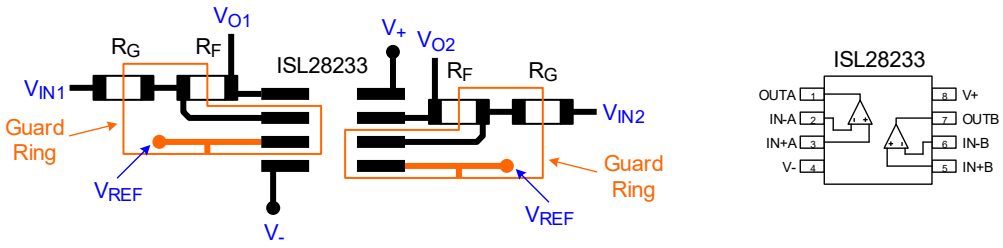


Figure 2. Using Guard Rings Minimizes Leakage Current

While the guard rings do not need to be of a specific width, each guard ring should form a continuous loop around the inverting and non-inverting op-amp inputs. By setting the guard ring voltage equal to the voltage at the non-inverting input, both parasitic resistance and capacitance are reduced.

3. Can I use the ISL28134 for precision high-side current sensing?

Yes. Figure 3 shows the classic circuit for positive supply rail current sensing. Here, negative feedback ensures that the voltage at the inverting input equals that at the non-inverting input, making $I_L \times R_S = I_O \times R_{IN}$. Then, substituting I_O with V_O/R_O and solving for I_L gives:

(EQ. 1) $$I_L = \frac{V_O}{R_O} \times \frac{R_{IN}}{R_S}$$

For precision measurements use p-channel MOSFETs instead of PNP bipolar junction transistors (BJTs) to eliminate the error because of the current gain of the PNP.

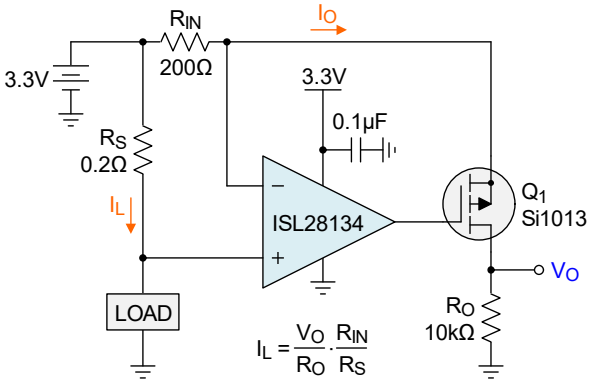


Figure 3. High-Side Current Sensing at Low-Voltage

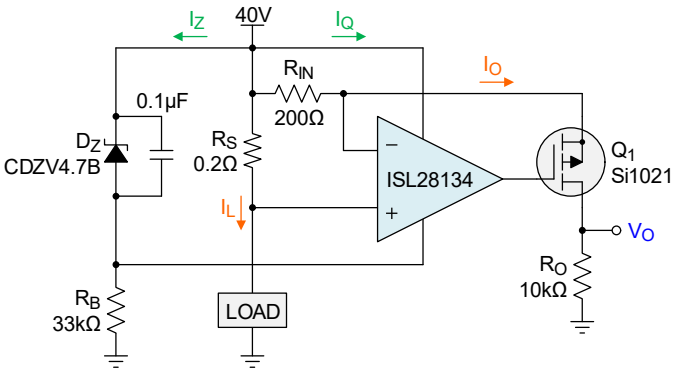


Figure 4. High-Side Current Sensing at High-Voltage

Making V_{Omax} = 2V, results in a maximum load current of $I_{L\text{-}max}$ = 0.2A, and a sensitivity of 1V/100mA.

For high-voltage application, the same circuit can be applied, although with a minor change in the supply voltage arrangement (Figure 4). As the ISL28134 is a low-voltage device, its supply rails must be level shifted to the 40V supply rail. This is accomplished with a Zener diode (D_Z) and a biasing resistor, R_B. The Zener voltage must cover the supply range of the op amp, therefore, a 3.3V to 5.1V Zener diode is recommended.

While the positive supply terminal of the op amp is connected to the 40V system supply, the op-amp ground or negative supply terminal is connected to the anode of the Zener diode. Because both the Zener diode current (I_Z) and the op-amp quiescent current (I_Q) flow through R_B, its value is calculated using Equation 2:

(EQ. 2) $$R_B = \frac{V_S - V_Z}{I_Z + I_Q}$$

Note: For the previous component values, both circuits have a sensitivity of V_O/I_L = 1V/100mA (Figure 5).

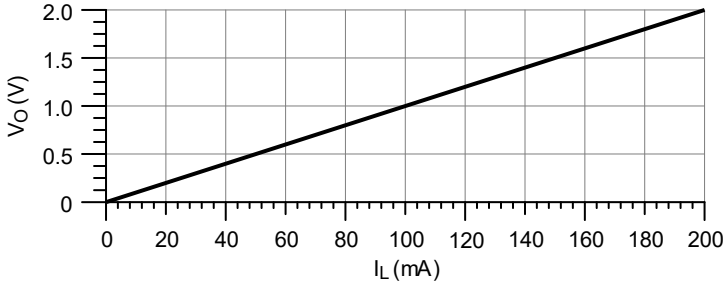


Figure 5. High-Side Current Sensing at High-Voltage

4. How can I increase op-amp output current?

The ISL28x3x precision op amps may only drive a few milli-amps of output current before becoming non-linear. For applications with higher current demand, add an NPN transistor as current booster to the output (Figure 6). Practically, the NPN becomes a part of the op-amp output stage.

To prevent the op-amp output from saturating (even at high temperature), reserve a 1V range for the base-emitter voltage. In a 3.3V application, this gives you a maximum output voltage of about V_{Omax} = 2V. As V_O is attenuated by the feedback voltage divider down to V_{IN}, the maximum input voltage becomes $V_{INmax} = V_{Omax} \times R_G/(R_G+R_F)$, or 0.2V in this case.

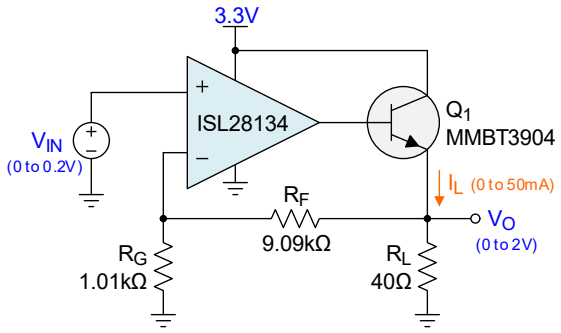


Figure 6. Output Current Boost Circuit

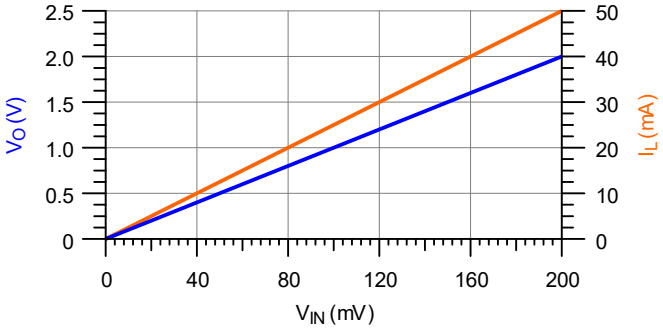


Figure 7. V_O, I_L vs V_{IN} Characteristics

For more detailed information consult application note *R13AN0008: Boosting Op-Amp Output Current*.

5. What is the maximum output loading of the precision op amp?

To obtain the best performance out of your op-amp circuit, use the R_L value specified in the test conditions of the datasheet. This value is typically 10kΩ for most op amps but can be up to 100kΩ for others.

Low-voltage precision op amps are designed to drive only small output currents up to 1mA or less, without deviating from their specified performance. Driving higher loads (lower R_L value) without modifying the amplifier circuit distorts the output signal. (Figure 9).

During amplifier design, minimize output loading because of the feedback path by making $R_G + R_F \geq 10R_L$.

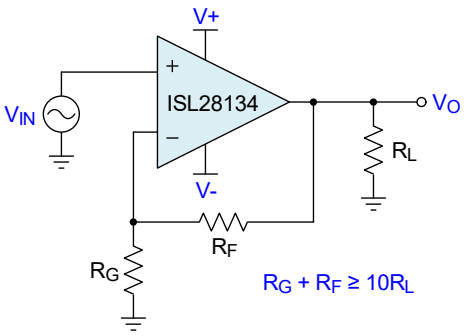


Figure 8. Non-inverting Amplifier with R_L

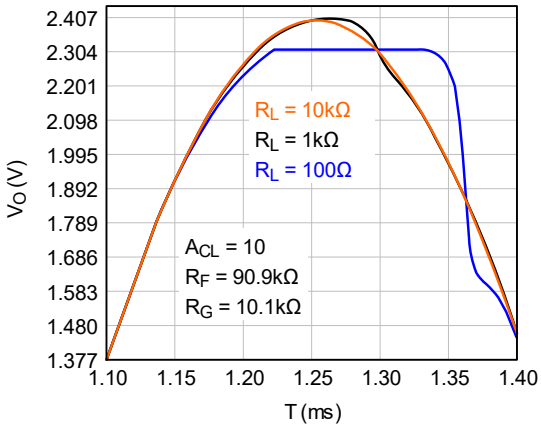


Figure 9. 1kHz Sinewave Distortions because of Overloading

However, if you were to drive a higher load than 10kΩ, such as 333Ω for the example below, consult the V_O-I_L characteristic in the datasheet. Draw a load resistance line, in this case for 333Ω, into the output characteristic (Figure 10). The point where the R_L line crosses the V_{OH} line, gives you the maximum output voltage (V_{Omax} = 2V) and the resulting output current (I_O = 6mA), the op amp can support.

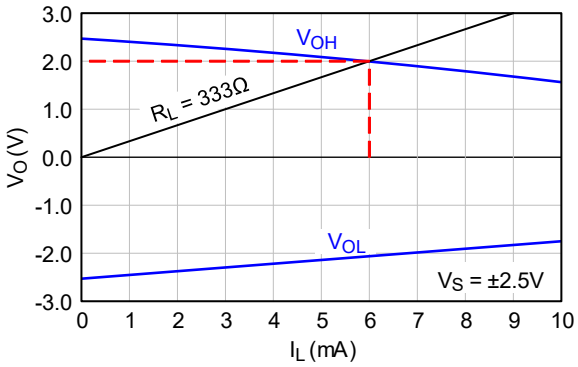


Figure 10. Determine V_O and I_L for a given R_L

To avoid exceeding the newfound V_O maximum, you need to either lower the input signal range, the gain setting, or both. As a higher output load also reduces the op-amp slew rate, you need to determine the new, reduced slew rate value, which might force you to reduce the input signal bandwidth too.

Conclusion: The maximum output load (or minimum load resistance) of the ISL28x3x family of low-voltage precision op amps is 10kΩ. For driving higher loads (lower load resistance), use op amps with higher output drive capability, such as READ2304 (dual) and READ4304 (quad).

6. How do I compensate for parasitic capacitance at the inverting input?

Every op amp has parasitic input capacitances, C_P, by default. Bad PCB layout, however, can further increase this capacitance. As the feedback path connects to the inverting input, parasitic capacitance at this input can degrade amplifier stability. Here, the combination of C_P and high-value feedback and gain resistors, R_F and R_G, forms a low-pass filter whose cutoff frequency, f_c, might fall within the gain bandwidth of the op amp: $f_c < f_{GBW}$. If this happens, overshoot, ringing, and gain peaking occur.

To compensate for C_P, connect a compensation capacitor, C_C, parallel to R_F. This removes the gain peak, therefore, restoring circuit stability. The value of C_C is calculated using Equation 3:

(EQ. 3) $$C_F = \frac{1}{2\pi} \times \frac{GBW \times R_G}{(f_{pk} R_F)^2}$$

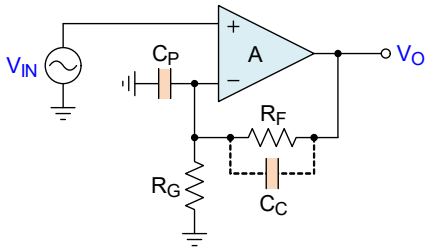


Figure 11. Input Capacitance Compensation with C_C

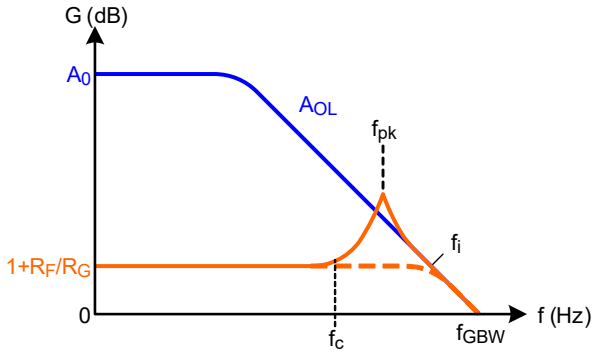


Figure 12. C_C removes Gain Peak and restores Stability

Note: For narrow-bandwidth amplifiers, such as the ISL28134, ISL28x33, and ISL28x30, this phenomenon is usually not observed. However, with wideband amplifiers, such as the READx304, instability because of C_P might be a possibility.

7. How do I compensate for capacitive loading at the output?

While there are numerous phase compensation methods for a variety of applications with capacitive loading, the following is the most commonly applied one: the op amp as a voltage reference buffer (Figure 13).

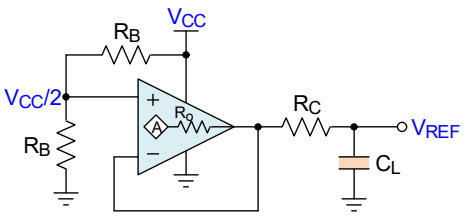


Figure 13. R_C isolates C_L from R_O

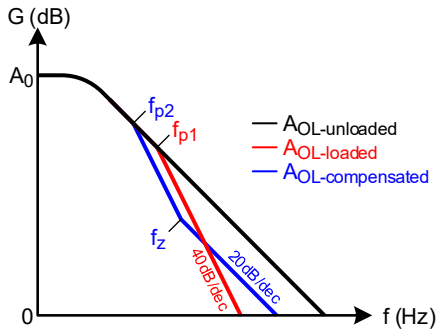


Figure 14. R_C restores Circuit Stability by reducing A_{OL} Slope from -40dB/decade to -20dB/decade

In the previous voltage reference buffer, the output voltage $V_{REF} = V_{CC}/2$, is buffered with a large capacitance, C_L. Without a compensation resistor, R_C, C_L loads the open-loop gain by forming a low-pass filter with the op-amp output resistance, R_O. The cutoff or pole frequency, f_{p1}, of this low-pass is:

(EQ. 4) $$f_{p1} = \frac{1}{2\pi \times R_O C_L}$$

This pole adds phase lag to the original A_{OL} phase of the op amp, therefore, reducing phase margin and causing the circuit to become unstable.

However, inserting a small compensation resistor, R_C, creates a slightly lower pole frequency, f_{p2}, and a zero frequency, f_z, at the op-amp output. Their values are calculated with:

(EQ. 5) $$f_{p2} = \frac{1}{2\pi \times (R_O + R_C) C_L}$$

(EQ. 6) $$f_z = \frac{1}{2\pi \times R_C C_L}$$

The zero creates a phase lead that counteracts the phase lag of the pole, therefore, reducing the A_{OL} slope from -40dB/decade to -20dB/decade, and restoring circuit stability.

While Equation 7 helps you approximate the value of R_C, (only if you know R_O), you still need to perform several frequency response measurements to ensure the circuit remains stable across the capacitor tolerance and temperature.

(EQ. 7) $$R_C = \frac{2.5(1 + \sqrt{1 + 0.8 R_O \times \pi f_T C_L})}{\pi f_T C_L}$$

Determining the open-loop output resistance, R_O, is an undertaking on its own, and therefore discussed in a separate section.

8. How can I measure the op-amp open-loop output impedance?

Load the output of a non-inverting amplifier with a large capacitance, such as 1µF, and measure the frequency of the gain peak, f_{pk} (Figure 15).

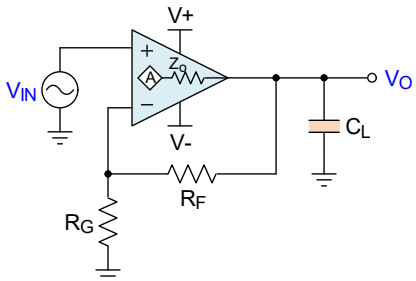


Figure 15. Loading the Output Capacitively Causes Gain Peak

Then calculate the open-loop output impedance with Equation 8:

(EQ. 8) $$Z_O = \frac{GBW \times \beta}{2\pi f_{pk}^{2} C_L} \quad \text{with} \quad \beta = \frac{R_G}{R_G + R_F}$$

For detailed information on how to derive Equation 8, consult application note: *How to determine an Op-amp's Open-Loop Output Impedance for a given capacitive Load*.

9. How do I bias an AC-coupled amplifier with single-supply?

To ensure symmetric input and output dynamic signal ranges, both op-amp inputs must be biased with a reference potential that equals half the supply voltage: $V_{REF} = V_S/2$ (Figure 16). The reference potential can be generated either with an integrated voltage reference IC (recommended for best PSRR), or with a voltage divider, also known as ratio-metric biasing.

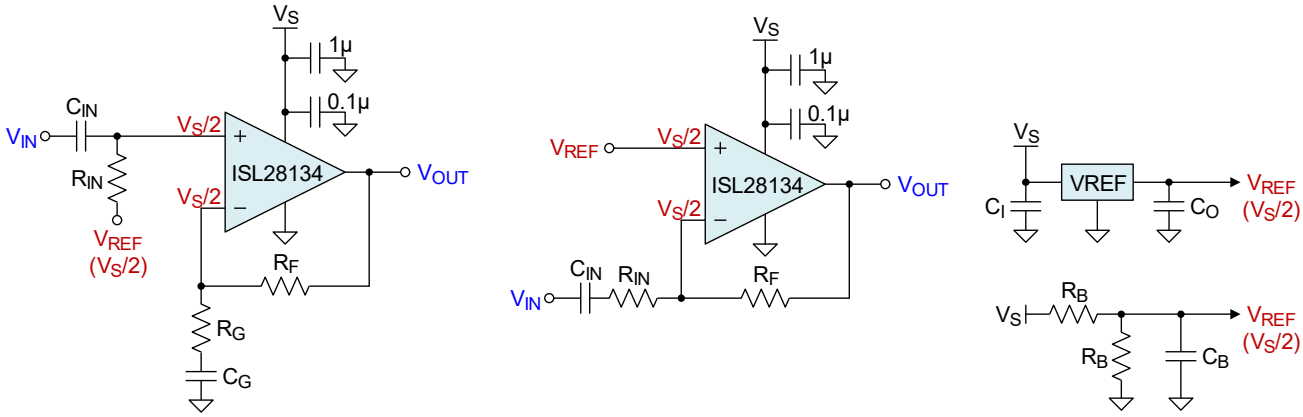


Figure 16. Biasing the Op-Amp Inputs of a Non-Inverting (Left) and an Inverting Amplifier (Right) with $V_S/2$ Potential for Symmetric Input and Output Dynamic Range

Figure 17. Methods of generating Bias Potentials

For detailed information on how to calculate the individual component values, consult application note *R13AN0003: How to Bias Op-Amps Correctly*.

10. Op Amp Limitations Causing Output Errors

All op-amp parameters represent limitations because of their finite values. With the exception of slew rate, these parameters can be represented as input errors that are amplified by the noise gain, or non-inverting closed-loop gain (1/β) and appear at the output. Figure 18 depicts the op-amp input-error model and its equations.

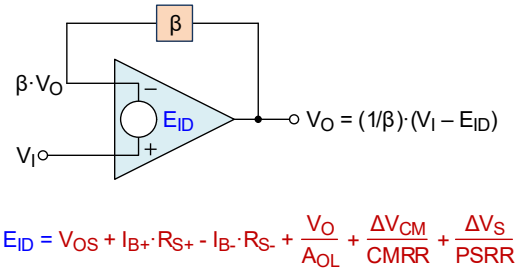


Figure 18. Op-Amp Input Error Sources

To minimize the total output error, each error is discussed, and a solution or caution provided to reduce the error.

10.1 How do I reduce gain-error because of finite open-loop gain, A_{OL}?

Gain error is the difference between the actual closed-loop gain magnitude over frequency, $|A_{CL}(f)|$, and its ideal value at DC, commonly denoted as 1/β or A_{CLi}.

The only region where this difference becomes visible in a Bode plot is around the -3dB frequency of $|A_{CL}|$, where $|A_{CLi}|$ crosses $|A_{OL}|$. There, $|A_{CL}|$ drops to $1/\sqrt{2}$ or about 70% of $|A_{CLi}|$, resulting in a gain error of ~30%.

For the majority of the frequency range, where this difference is not obvious, the gain error can be estimated using the loop-gain, T, using:

(EQ. 9) $$\text{Gain Error (\%)} \approx \frac{100}{T(V/V)}$$

On a Bode plot, the loop gain, T, in dB, is the difference between the open-loop gain and the ideal closed loop gain:

(EQ. 10) $$T(dB) = A_{OL}(dB) - A_{CLi}(dB)$$

Also, converting the dB value into linear values gives T in V/V.

$$T(V/V) = 10^{T(dB)/20}$$

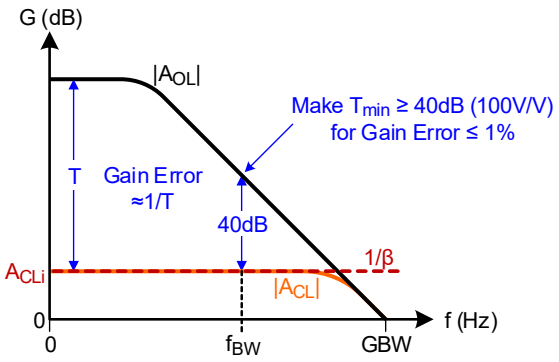


Figure 19. Limit Bandwidth where Gain Error = 1%

It is common practice to limit the signal bandwidth to a frequency where T ≥ 40dB (or 100V/V), to limit the gain error to ≤ 1% (Equation 9).

An even faster method to calculate the signal bandwidth for a specified gain error is given with Equation 11:

(EQ. 11) $$f_{BW} = \frac{GBW}{A_{CLi} \times 10^{T/20}}$$

With:

- f_{BW} = Maximum signal bandwidth (Hz)
- GBW = Gain-bandwidth of the op amp
- A_{CLi} = Ideal closed-loop gain (V/V)
- T = Desired minimum loop-gain (dB)

Conclusion: The higher A_{OL}, the lower the gain error. Therefore, for high-precision applications requiring minimum gain error, use precision op amps, such as ISL28134, ISL28x33, and ISL28x30, which possess open-loop gains of A_{OL} = 174dB and A_{OL} = 150dB, respectively.

10.2 How do I reduce the output error because of input offset, V_{OS}?

The best solution is using one of our precision op amps with offset voltages down to 0.2µV (ISL28134).

However, when using a wideband op amp, such as READ2304 with an input offset of 6mV input offset, offset reduction is only possible through circuit design techniques.

One commonly used method is the implementation of a low-pass characteristic in the feedback path (Figure 20). This method does not reduce the initial offset but prevents it from being amplified by the passband gain.

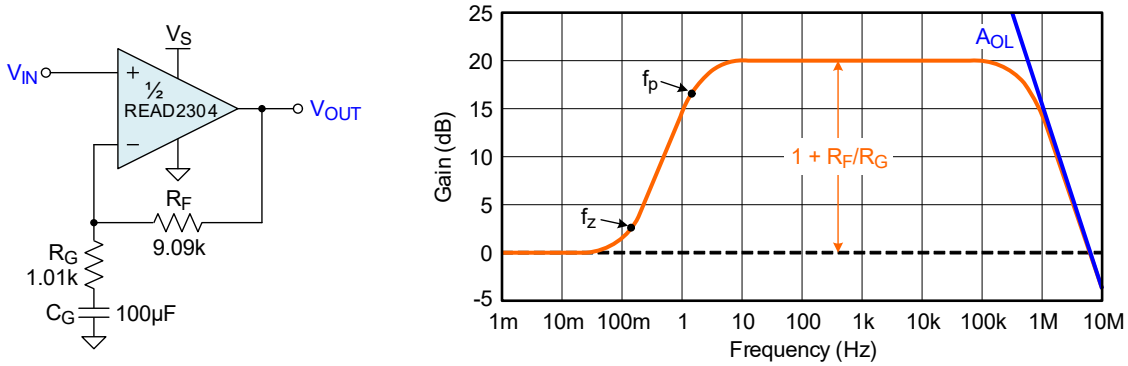


Figure 20. Because of C_G, only Frequencies above f_p are amplified by $1+R_F/R_G$. V_{OS} passes through at Unity-Gain

The pole and zero frequencies occur at: $f_p = 1/(2\pi C_G R_G) = 1.6Hz$ and $f_z = 1/[2\pi C_G(R_G+R_F)] = 0.16Hz$

The gain response shows that the DC offset and frequencies below 0.1Hz are not amplified but pass to the output at unity gain. Frequencies above f_p are amplified by the passband gain, which is $1+R_F/R_G$ = 10V/V (20dB).

Another option of actual offset reduction in a wideband amplifier is achieved with one of the many composite amplifier designs (Figure 21).

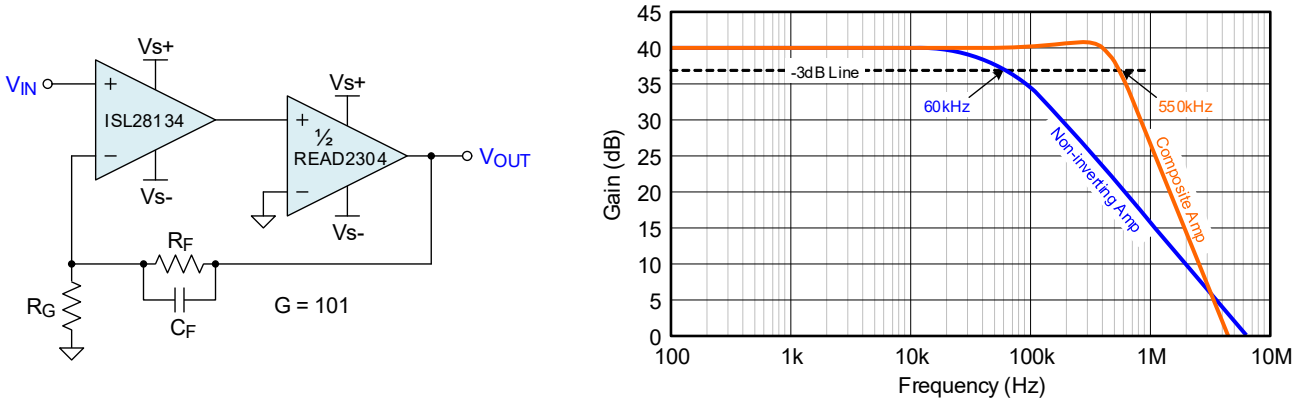


Figure 21. A Composite Amplifier Design increases Signal Bandwidth and reduces Input Offset and Gain Error

In this design, the offset of the READ2304 is reduced by the DC open-loop gain of the ISL28134. Therefore, the total offset referred to the input, $V_{OS(RTI)}$, is:

$$V_{OS(RTI)} = V_{OS1} + \frac{V_{OS2}}{A_{01}} = 5\mu V + \frac{6mV}{5 \times 10^8} = 5.000012\mu V$$

For detailed information on the calculation of the capacitance value of C_F, consult application note *R13AN0002: Composite Amplifier Design for High Gain Applications*.

10.3 How do I reduce the output error because of CMRR?

The common-mode rejection ratio (CMRR) of an op amp quantifies the ability of the device to reject common-mode signals, such as those that appear simultaneously and in-phase at both inputs. Figure 22 shows that the CMRR is high at low frequencies and drops with -20dB/decade at higher frequencies.

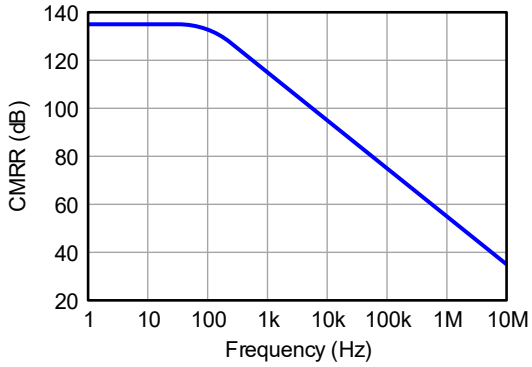


Figure 22. CMRR over Frequency

The impact of CMRR can be modeled as an input error, $E_I = \Delta V_{CM}/CMRR$, which is amplified by the closed-loop gain of the circuit to result in an output error of $E_O = A_{CL} \times \Delta V_{CM}/CMRR$.

In the case of a non-inverting amplifier, the signal input voltage is the common-mode voltage, $\Delta V_I = \Delta V_{CM}$. Depending on the signal amplitude, the input error, E_I can therefore be rather large, yielding an output error voltage of $V_O = \Delta V_I/CMRR \times (1+R_F/R_G)$ (Figure 23).

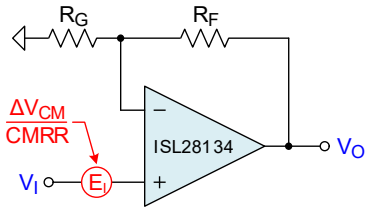


Figure 23. Non-inverting Amplifier with Common-Mode Error

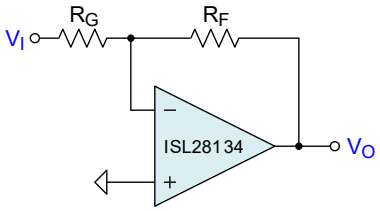


Figure 24. Inverting Amplifier without Common-Mode Error

$$V_O = \left(1 + \frac{R_F}{R_G}\right) \times \left(V_I + \frac{\Delta V_{IN}}{CMRR}\right)$$

$$V_O = -\frac{R_F}{R_G} \times V_I$$

To eliminate common-mode error, use an inverting amplifier (Figure 24), or two in series if V_O must be in phase with V_I. Here, the non-inverting input is tied to a stable reference potential, and through negative feedback, also present at the inverting input. This makes $\Delta V_{CM} = 0$ and eliminates the associated output error without affecting the swing of V_I.

10.4 How do I reduce the output error because of PSRR?

The power supply rejection ratio (PSRR) of an op amp quantifies the ability of the device to reject changes in the power supply of the device. Analogous to the CMRR, the PSRR can be modeled as an input error $E_I = \Delta V_S/PSRR$ that is assigned to the non-inverting input and therefore amplified by the non-inverting closed-loop gain (Figure 25).

Note: Errors because of PSRR affect non-inverting and inverting amplifiers equally.

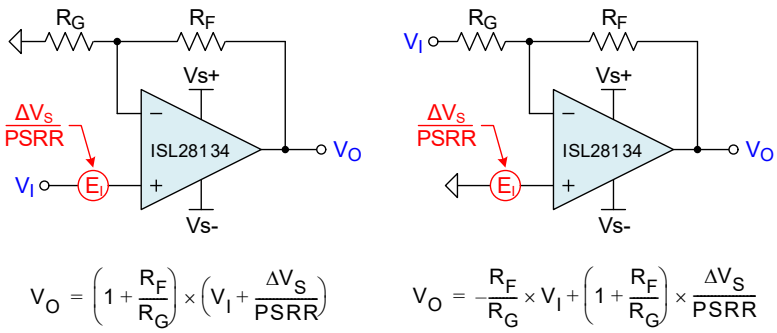


Figure 25. PSRR Error in Inverting and Non-inverting Amplifier

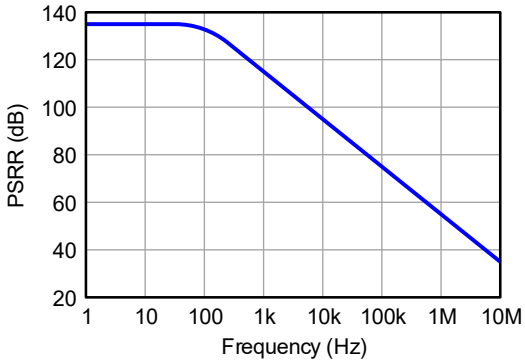


Figure 26. PSRR over Frequency

Figure 26 shows that PSRR is high at low frequencies and drops with -20dB/decade at higher frequencies. Because PSRR is frequency dependent, op-amp power supplies must be well decoupled. Figure 27 shows a typical decoupling method.

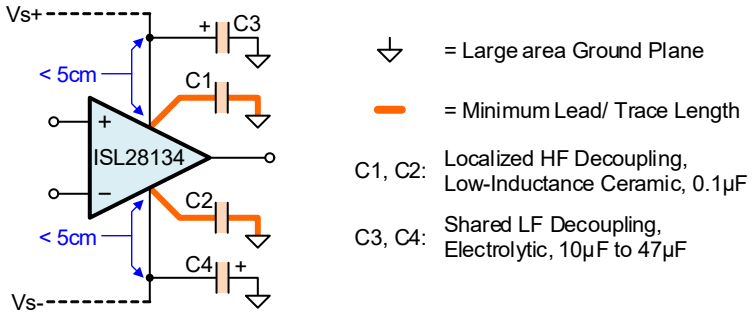


Figure 27. Proper Low and High-Frequency Decoupling Techniques for Op Amps

At low frequencies, several devices may share a 10µF to 47µF capacitor on each supply, provided it is no more than 5cm (PC track distance) from any device. At high frequencies, the supply leads should be decoupled by a low-inductance 0.1µF capacitor with short leads/PC tracks. These capacitors must also provide a return path for HF currents in the op amp load.

10.5 How do I reduce the output error because of finite slew rate, SR?

Slew rate (SR) is the speed limit of an op amp, typically measured in V/µs. It is defined as the maximum rate of change of op-amp output voltage over a specified time without causing signal distortion.

(EQ. 12) $SR = V_{pk}2\pi f_s$

Slew rate is the constant product of output voltage change and signal frequency. This means that for higher signal frequencies, the voltage amplitude must be lower to remain within the slew rate limit. Also, vice versa, for high voltage amplitude, the signal frequency must be lowered.

Another parameter related to slew rate is the full power bandwidth, FPBW, of an op amp. It describes the maximum possible signal frequency as a function of slew rate and the maximum output voltage swing of the op-amp. For any other output amplitudes less than full swing, the maximum frequency is calculated using:

(EQ. 13) $$f_{s\_max} = \frac{SR}{2\pi V_{pk}}$$

FPBW is a special case of Figure 13, as V_{pk} is replaced by $V_{Omax}/2$:

(EQ. 14) $$FPBW = \frac{SR}{2\pi V_{Omax}/2} = \frac{SR}{\pi \times V_{Omax}}$$

For example, the precision op amp, ISL28133, with a 400kHz bandwidth and rail-rail output range, has a specified slew rate of 0.2V/µs. Therefore, operating the device from a ±2.5V dual supply makes its full-power bandwidth:

$$FPBW = \frac{0.2V/\mu s}{2\pi \times 2.5V} = 12.7kHz$$

Figure 1 depicts the device undistorted output voltage for a signal frequency of 12.5kHz, slightly below its FPBW.

In strong contrast, Figure 2 shows a heavily distorted output signal inform of a triangle waveform that occurs when doubling the frequency to 25kHz. Here, the op amp is simply overburdened. Its finite slew rate does not allow the output signal to follow the input signal at the same pace. The result is a heavily distorted output signal that represents a massive output error.

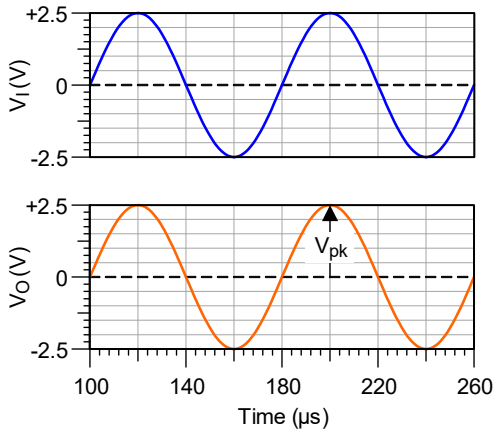


Figure 28. f_{IN} = 12.5kHz

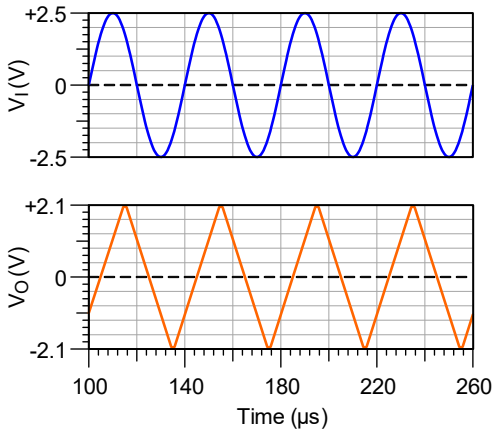


Figure 29. f_{IN} = 25kHz

To eliminate output error because of slew rate, you must reduce the output amplitude of frequency to remain within the slew rate limit, or simply choose a device with higher slew rate.

11. Do you have more op-amp application collateral?

Table 3. List of Application Notes

File Number	Title
AN519	*Operational Amplifier Noise Prediction*
AN551	*Recommended Test Procedures for Operational Amplifiers*
AN1111	*Doubling the Output Current to a Load with a Dual Op Amp*
AN1213	*VFA, CFA, Bipolar or CMOS - Which High-Speed Amplifier Is Best for Your Low-Noise Application*
AN1827	*High-Side, High Current Sensing Techniques*
AN1993	*Voltage Feedback versus Current Feedback Operational Amplifiers*
AN1306	*Avoid Instability in Rail to Rail CMOS Amplifiers*
AN1560	*Making Accurate Voltage Noise and Current Noise Measurements on Op-Amps Down to 0.1Hz*
AN1685	*Development of a Voltage Feedback Spice Op-Amp Macro Model*
AN1686	*Development of a Spice Op-Amp Macro Model for Current-Feedback Amplifiers*
AN1694	*The Four Basic Building Blocks of an Op Amp*
AN9415	*Feedback, Op Amps and Compensation*
AN9420	*Current Feedback Amplifier Theory and Applications*
AN9523	*Evaluation Programs for SPICE Op Amp Models*
AN9663	*Converting From Voltage-Feedback to Current-Feedback Amplifiers*
AN9756	*Properly Terminating Video Op Amps*
AN9757	*A Cookbook Approach to Single Supply DC-Coupled Op Amp Design*
AN9787	*An Intuitive Approach To Understanding Current Feedback Amplifiers*
R13AN0003	*How to Bias Op-Amps Correctly*
R13AN0004	*ISL2853x and ISL2863x High-Precision Instrumentation Amplifiers*
R13AN0005	*Cascading Instrumentation Amplifiers for High Gain at High Bandwidth*
R13AN0006	*How to Bias the ISL2853x and ISL2863x High-Precision Instrumentation Amplifiers*
R13AN0007	*Deriving the V_{CM} versus V_{OUT} Plot for the ISL2853x Instrumentation Amplifier*
R13AN0008	*Boosting Op-Amp Output Current*
R13AN0009	*Load Cancellation Enables Precision Op-Amps to Drive Heavy Loads*
R13AN0010	*Noise Calculations of Op-Amp Circuits*

Table 4. List of White Papers

Title
How to Monitor Sensor Health with Instrumentation Amplifiers
Sensing Elements for Current Measurements

12. Revision History

Revision	Date	Description
1.00	May 16, 2022	Initial release.

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