RX65N/RX651 Group RX630 Group

Points of Difference Between RX65N Group and RX630 Group

Introduction

This application note is intended as a reference for confirming the points of difference between the overview of functions, the I/O registers, the pin functions of the RX65N Group and RX630 Group, and notes on migration.

To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the user's manuals of the products in question.

Target Devices

RX65N Group and RX630 Group

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1. Comparison of Functions of RX65N Group and RX630 Group

A comparison of the functions of the RX65N Group and RX630 Group is provided below. For details of the functions, see section 2, Comparative Overview of Functions and section 5, Reference Documents.

Table 1.1 is a Comparison of Functions of RX65N and RX630.

Table 1.1 Comparison of Functions of RX65N and RX630

Function	RX630	RX65N Code flash 1.0MB or less	RX65N Code flash more than 1.5 MB
CPU	△		
Operating Modes	△		
Address Space	△		
Reset	○		
Option-Setting Memory	△		
Voltage Detection Circuit (LVDA)	△		
Clock Generation Circuit	△		
Frequency Measurement Circuit (MCK)	○	x	
Clock Frequency Accuracy Measurement Circuit (CAC)	x	○	
Low Power Consumption	△		
Battery Backup Function	○		
Register Write Protection Function	△		
Exception Handling	△		
Interrupt Controller (ICUb):RX630, (ICUB):RX65N	△		
Buses	△		
Memory-Protection Unit (MPU)	△		
DMA Controller (DMACA):RX630, (DMACAa):RX65N	△		
EXDMA Controller (EXDMACa)	x	○	
Data Transfer Controller (DTCa):RX630, (DTCb):RX65N	△		
Event Link Controller (ELC)	x	○	
I/O Ports	△		
Multi-Function Pin Controller (MPC)	△		
Multi-Function Timer Pulse Unit 2 (MTU2a)	○	x	
Multi-Function Timer Pulse Unit (MTU3a)	x	○	
Port Output Enable 2 (POE2a)	○	x	
Port Output Enable 3 (POE3a)	x	○	
16-Bit Timer Pulse Unit (TPUa)	△		
Programmable Pulse Generator (PPG)	○		
8-Bit Timer (TMR)	△		
Compare Match Timer (CMT)	△		
Compare Match Timer W (CMTW)	x	○	
Realtime Clock (RTCa):RX630, (RTCd):RX65N	△		
Watchdog Timer (WDTA)	△		
Independent Watchdog Timer (IWDTa)	△		
Ethernet Controller (ETHERC)	x	○	
DMA Controller for the Ethernet Controller (EDMACa)	x	○	
USB 2.0 Function Module (USBa):RX630 USB 2.0 FS Host/Function Module (USBb):RX65N	△		

Function	RX630	RX65N Code flash 1.0MB or less	RX65N Code flash more than 1.5 MB
Serial Communications Interface (SCIc, SCId):RX630 Serial Communications Interface (SCIg, SCIi, SCIh):RX65N	△		
I²C-bus Interface (RIIC):RX630, (RIICa)RX65N	△		
CAN Module (CAN)	△		
Serial Peripheral Interface (RSPI):RX630, (RSPIc):RX65N	△		
Quad Serial Peripheral Interface (QSPI)	x	○	
IEBus Controller (IEB)	○	x	
CRC Calculator (CRC):RX630, (CRCA):RX65N	△		
SD Host Interface (SDHI)	x	○	
SD Slave Interface (SDSI)	x	○	
MultiMediaCard Interface (MMCIF)	x	○	
Parallel Data Capture Unit (PDC)	x	○	
Boundary Scan	○		
AESa	x	○	○*
RNGa	x	○	○*
12-Bit A/D Converter (S12ADa):RX630, (S12ADFa):RX65N	△		
10-Bit A/D Converter (ADb)	○	x	
D/A Converter (DAa):RX630 12-Bit D/A Converter (R12DA):RX65N	△		
Temperature Sensor	△		
Data Operation Circuit (DOC)	x	○	
RAM	△		
Standby RAM	x	○	
Flash Memory (Code Flash)	△		
Flash Memory (Data Flash)	△	x	△
Trusted Secure IP (TSIP)	x		○
Graphic LCD Controller (GLCDC)	x		○
2D Drawing Engine (DRW2D)	x		○
Package (LQFP100/144 only)	△		

Note: ○: Function implemented, x: Function not implemented, △: Differences exist between implementation of function on RX630 and RX65N.

*: Implementation in Trusted Secure IP

2. Comparative Overview of Functions

2.1 CPU

Table 2.1 shows a Comparative Listing of CPU Specifications, and Table 2.2 shows a Comparative Listing of CPU Registers.

Table 2.1 Comparative Listing of CPU Specifications

Item	RX630	RX65N
CPU	• Maximum operating frequency: 100 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register set of the CPU General purpose: Sixteen 32-bit registers Control: Nine 32-bit registers Accumulator: One 64-bit register • Basic instructions: 73 • Floating-point operation instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 x 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory protection unit (MPU)	• Maximum operating frequency: 120 MHz • 32-bit RX CPU (RXv2) • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register set of the CPU General purpose: Sixteen 32-bit registers Control: Ten 32-bit registers Accumulator: Two 72-bit registers • Basic instructions: 75 • Floating-point instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 x 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory protection unit (MPU)
FPU	• Single precision floating point (32 bits) • Data types and floating-point exceptions in conformance with the IEEE754 standard	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard

Table 2.2 Comparative Listing of CPU Registers

Register	Bit	RX630	RX65N
EXTB	-	-	Exception Table Register
ACC	-	ACC: 64-bits (DSP, multiply and multiply-and-accumulate)	ACC0: 72-bits (DSP, multiply and multiply-and-accumulate) ACC1: 72-bits (DSP)

2.2 Operating Modes

Table 2.3 shows a Comparative Listing of Operating Modes Specifications, and Table 2.4 shows a Comparative Listing of Operating Modes Registers.

Table 2.3 Comparative Listing of Operating Modes Specifications

Item	RX630	RX65N
Operating modes specified by mode setting pins	Single-chip mode	Single-chip mode
	Boot mode (SCI interface)	Boot mode (SCI interface)
	Boot mode (USB interface)	Boot mode (USB interface)
	User boot mode	-
	-	Boot mode (FINE interface)
Operating modes specified by register settings	Single-chip mode	Single-chip mode
	User boot mode	-
	On-chip ROM disabled extended mode	On-chip ROM disabled extended mode
	On-chip ROM enabled extended mode	On-chip ROM enabled extended mode

Table 2.4 Comparative Listing of Operating Modes Registers

Register	Bit	RX630	RX65N
MDSR	-	Mode Status Register	-
SYSCR1	SBYRAME	-	Standby RAM Enable

2.3 Address Space

Figure 2.1 to Figure 2.3 shows the memory maps in the respective operating modes.

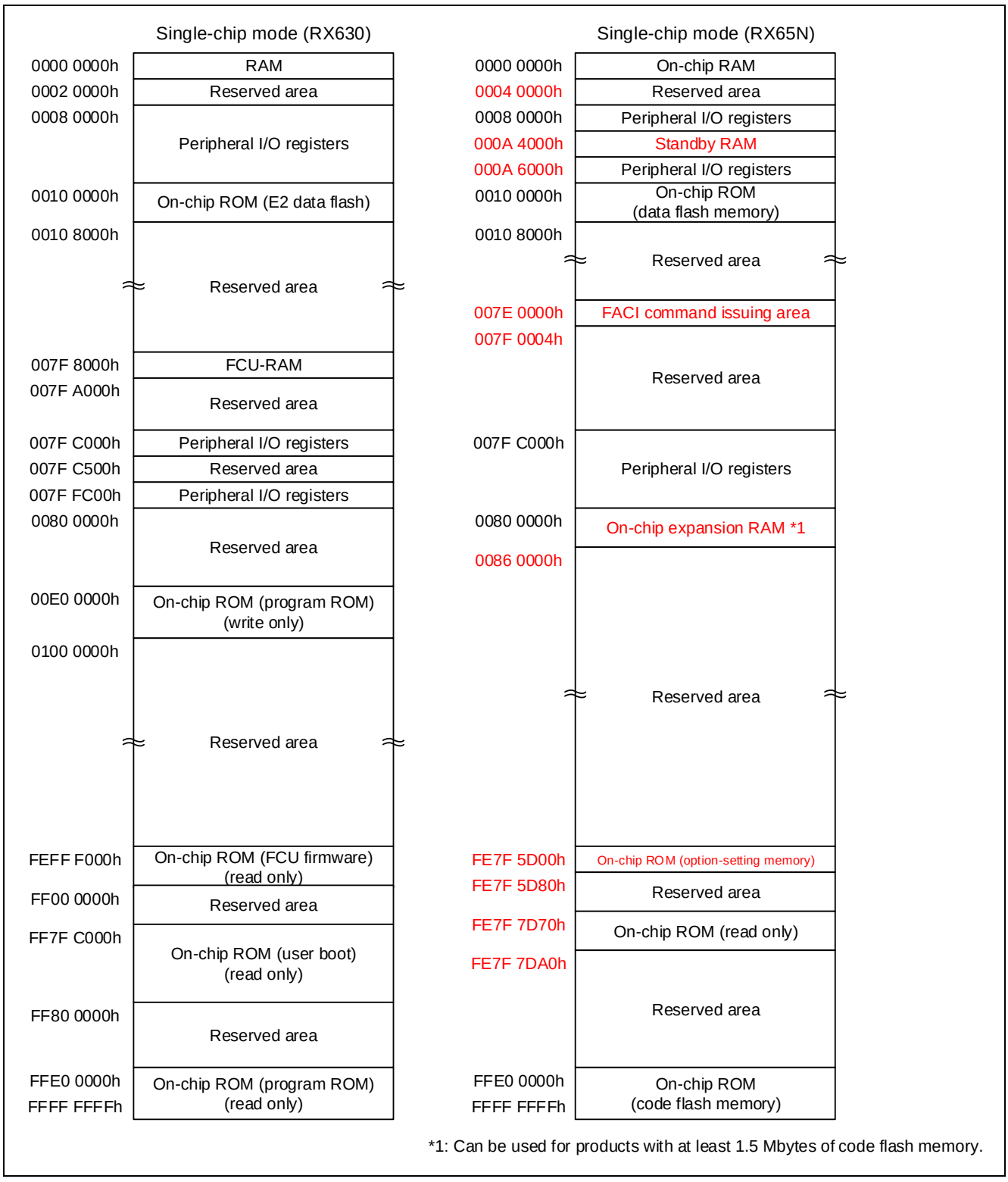

Figure 2.1 Memory Map in Each Operating Mode (Single-chip mode)

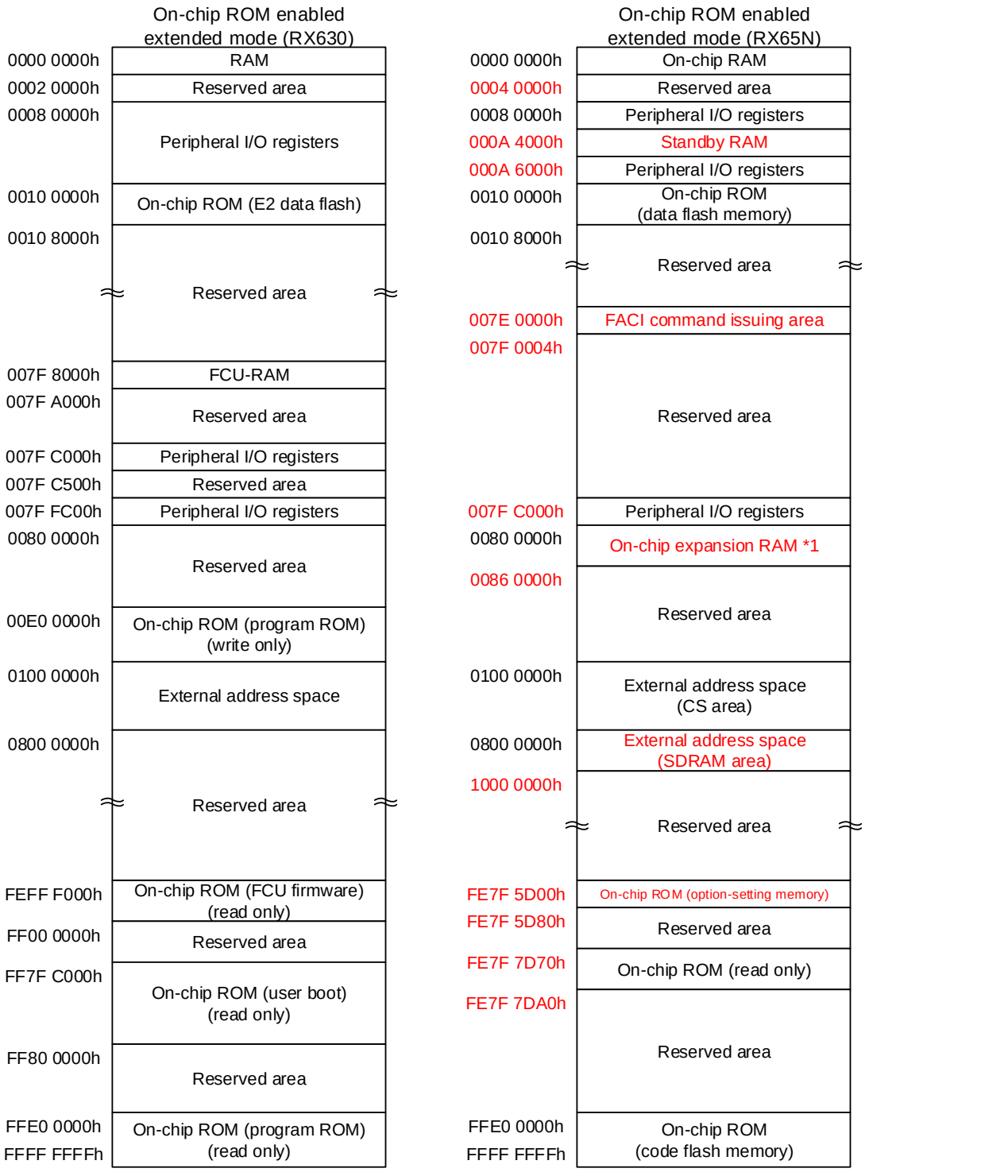

Figure 2.2 Memory Map in Each Operating Mode (On-chip ROM enabled extended mode)

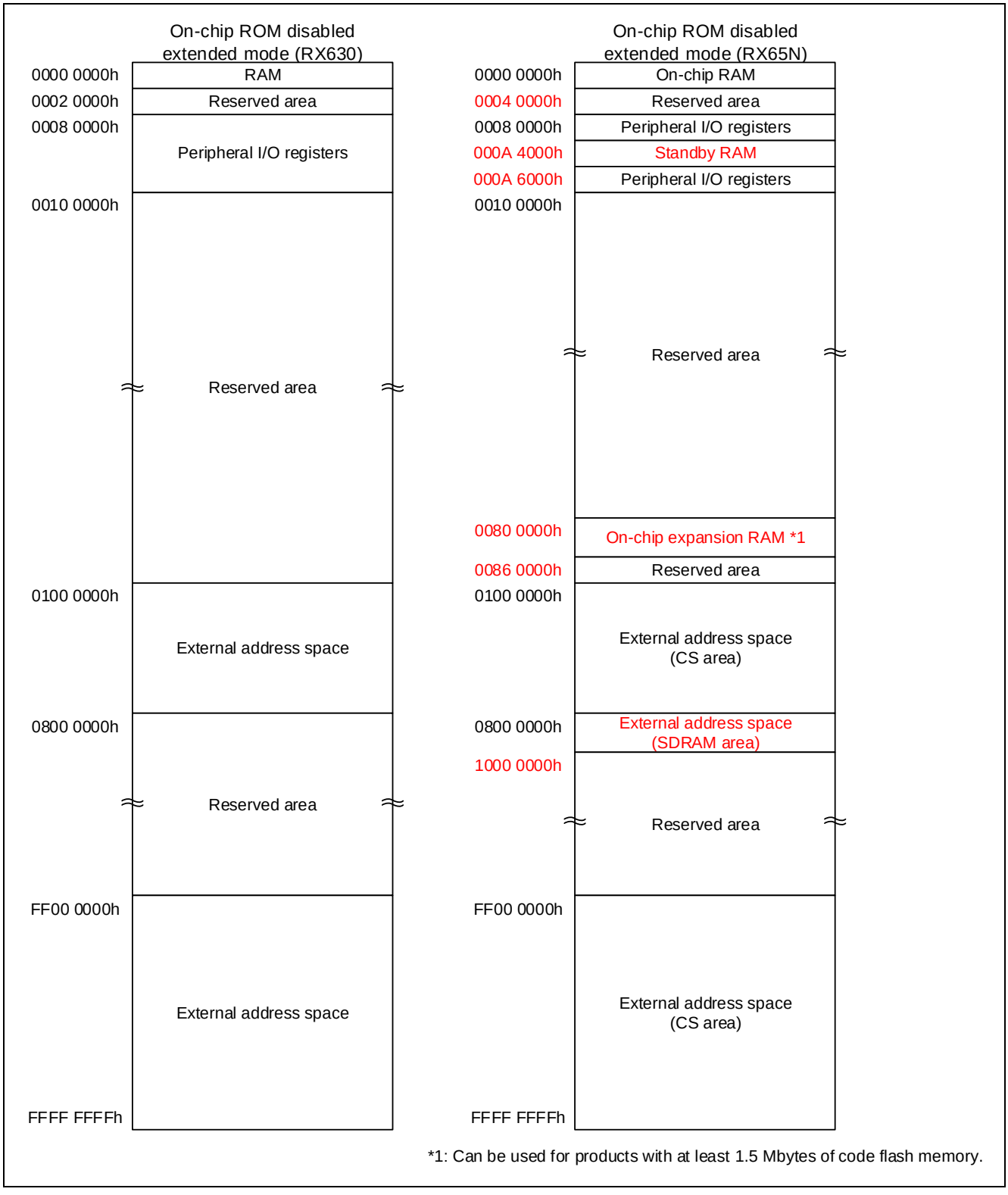

Figure 2.3 Memory Map in Each Operating Mode (On-chip ROM disabled extended mode)

2.4 Option-Setting Memory

Table 2.5 shows a Comparative Listing of Option-Setting Memory Registers , and Figure 2.4 shows a comparative of the option-setting memory.

Table 2.5 Comparative Listing of Option-Setting Memory Registers

Register	Bit	RX630	RX65N
SPCC	-	-	Serial Programmer Command Control Register
OSIS	-	-	OCD/Serial Programmer ID Setting Register
OFS0	IWDTRSTIRQS	IWDT Reset Interrupt Request Select 0: Non-maskable interrupt request is enabled 1: Reset is enabled	IWDT Reset Interrupt Request Select 0: Non-maskable interrupt request or plain interrupt request is enabled 1: Reset is enabled
	WDTRSTIRQS	WDT Reset Interrupt Request Select 0: Non-maskable interrupt request is enabled 1: Reset is enabled	WDT Reset Interrupt Request Select 0: Non-maskable interrupt request or plain interrupt request is enabled 1: Reset is enabled
OFS1	VDSEL[1:0]	-	Voltage Detection 0 Level Select
MDEB	-	Endian Select Register B	-
MDES	-	Endian Select Register S	-
MDE	TMEF[2:0]	-	Endian Select
	TMEFDB[2:0]	-	Bank Mode Select*1
TMEF	TMEF[2:0]	-	TM Enable
	TMEFDB[2:0]	-	Dual-Bank TM Enable*1
TMINF	-	-	TM Identification Data Register
BANKSEL	-	-	Bank Select Register*1
FAW	-	-	Flash Access Window Setting Register
ROMCODE	-	-	ROM Code Protection Register

*1: Can be used for products with at least 1.5 Mbytes of code flash memory.

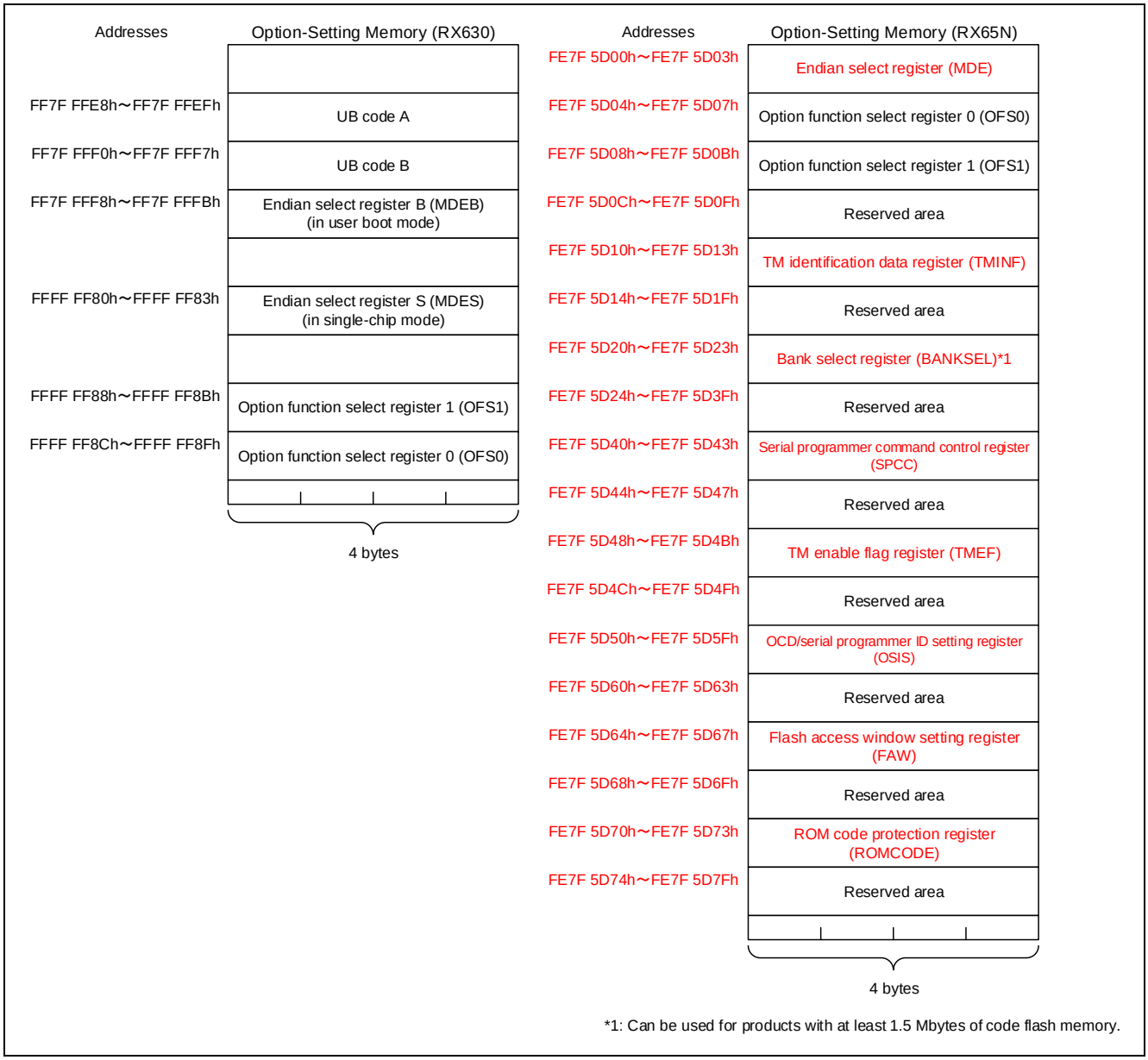

Figure 2.4 Comparative of Option-Setting Memory

2.5 Voltage Detection Circuit

Table 2.6 shows a Comparative Listing of Voltage Detection Circuit Specifications, and Table 2.7 shows a Comparative Listing of Voltage Detection Circuit Registers.

Table 2.6 Comparative Listing of Voltage Detection Circuit Specifications

Item		RX630 (LVDA)			RX65N (LVDA)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	Voltage drops past Vdet0	Voltage rises or drops past Vdet1	Voltage rises or drops past Vdet2	Voltage drops past Vdet0	Voltage rises or drops past Vdet1	Voltage rises or drops past Vdet2
	Detection voltage	One level fixed	Specify voltage using LVDLVLR.LVD1 LVLR[3:0] bits	Specify voltage using LVDLVLR.LVD2 LVLR[3:0] bits	Selectable from among three different levels by using OFS1.VDSEL[1:0] bits	Selectable from among three different levels by using LVDLVLR.LVD1 LVL[3:0] bits	Selectable from among three different levels by using LVDLVLR.LVD2 LVL[3:0] bits
	Monitor flag	-	LVD1SR.LVD1 MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2 MON flag: Monitors whether voltage is higher or lower than Vdet2	-	LVD1SR.LVD1 MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2 MON flag: Monitors whether voltage is higher or lower than Vdet2
			LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2DET flag: Vdet2 passage detection		LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2DET flag: Vdet2 passage detection
Voltage detection processing	Reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet0 > VCC CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC CPU restart timing selectable: after specified time with VCC > Vdet2 or Vdet2 > VCC	Reset when Vdet0 > VCC CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC CPU restart timing selectable: after specified time with VCC > Vdet2 or Vdet2 > VCC
	Interrupt	-	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	-	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
			Non-maskable interrupt	Non-maskable interrupt		Non-maskable interrupt or maskable interrupt selectable	Non-maskable interrupt or maskable interrupt selectable
			Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either	Interrupt request issued when Vdet2 > VCC and VCC > Vdet2 or either		Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either	Interrupt request issued when Vdet2 > VCC and VCC > Vdet2 or either

Item		RX630 (LVDA)			RX65N (LVDA)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
Digital filter	Enable/ disable switching	-	Available	Available	-	Available	Available
	Sampling time	-	1/n LOCO frequency x 2 (n: 1, 2, 4, 8)	1/n LOCO frequency x 2 (n: 1, 2, 4, 8)	-	1/n LOCO frequency x 2 (n: 2, 4, 8, 16)	1/n LOCO frequency x 2 (n: 2, 4, 8, 16)
Event link function		-	-	-	-	Available Output of event signals on detection of Vdet1 crossings	Available Output of event signals on detection of Vdet2 crossings

Table 2.7 Comparative Listing of Voltage Detection Circuit Registers

Register	Bit	RX630 (LVDA)	RX65N (LVDA)
LVD1CR1	LVD1IRQSEL	-	Voltage Monitoring 1 Interrupt Type Select
LVD2CR1	LVD2IRQSEL	-	Voltage Monitoring 2 Interrupt Type Select
LVDLVLR	LVD1LVL[3:0]	Voltage Detection 1 Level Select (Standard voltage during drop in voltage) b3 b0 1 0 1 0: 2.95 V Do not set otherwise.	Voltage Detection 1 Level Select (Standard voltage during drop in voltage) b3 b0 1 0 0 1: 2.99 V (Vdet1_1) 1 0 1 0: 2.92 V (Vdet1_2) 1 0 1 1: 2.85 V (Vdet1_3) Settings other than above are prohibited.
		The Value after reset is different.	
	LVD2LVL[3:0]	Voltage Detection 2 Level Select (Standard voltage during drop in voltage) b7 b4 1 0 1 0: 2.95 V Do not set otherwise.	Voltage Detection 2 Level Select (Standard voltage during drop in voltage) b7 b4 1 0 0 1: 2.99 V (Vdet2_1) 1 0 1 0: 2.92 V (Vdet2_2) 1 0 1 1: 2.85 V (Vdet2_3) Settings other than above are prohibited.
		The Value after reset is different.	
LVD1CR0	LVD1FSAMP[1:0]	Sampling Clock Select b5b4 0 0: 1/1 LOCO frequency 0 1: 1/2 LOCO frequency 1 0: 1/4 LOCO frequency 1 1: 1/8 LOCO frequency	Sampling Clock Select b5b4 0 0: 1/2 LOCO frequency 0 1: 1/4 LOCO frequency 1 0: 1/8 LOCO frequency 1 1: 1/16 LOCO frequency

Register	Bit	RX630 (LVDA)	RX65N (LVDA)
LVD2CR0	LVD2FSAMP[1:0]	Sampling Clock Select b5b4 0 0: 1/1 LOCO frequency 0 1: 1/2 LOCO frequency 1 0: 1/4 LOCO frequency 1 1: 1/8 LOCO frequency	Sampling Clock Select b5b4 0 0: 1/2 LOCO frequency 0 1: 1/4 LOCO frequency 1 0: 1/8 LOCO frequency 1 1: 1/16 LOCO frequency

2.6 Clock Generation Circuit

Table 2.8 shows a Comparative Listing of Clock Generation Circuit Specifications, and Table 2.9 shows a Comparative Listing of Clock Generation Circuit Registers.

Table 2.8 Comparative Listing of Clock Generation Circuit Specifications

Item	RX630	RX65N
Uses	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, ROM, and RAM. • Generates the peripheral module clock (PCLKB) to be supplied to peripheral modules. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the USB clock (UCLK) to be supplied to the USB. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the IEBUS clock (IECLK) to be supplied to the IEBUS. • Generates the RTC-dedicated sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the RTC-dedicated main clock (RTCMCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the JTAG-dedicated clock (JTAGTCK) to be supplied to the JTAG.	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the ETHERC, EDMAC, RSPI, SCIi, MTU3, AES*1, GLCDC*2 and DRW2D*2. (Note 1) • Generates the peripheral module clock (PCLKB) to be supplied to peripheral modules. • Generates the peripheral module clocks (for analog conversion) (PCLKC: unit 0; PCLKD: unit 1) to be supplied to S12AD. • Generates the flash-IF clock (FCLK) to be supplied to the flash interface. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the SDRAM clock (SDCLK) to be supplied to the SDRAM. • Generates the USB clock (UCLK) to be supplied to the USBb. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the RTC sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the RTC main clock (RTCMCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the JTAG clock (JTAGTCK) to be supplied to the JTAG.
Operating frequencies	• ICLK: 100 MHz (max) • PCLKB: 50 MHz (max)	• ICLK: 120 MHz (max) (Note 2) • PCLKA: 120 MHz (max) • PCLKB: 60 MHz (max) • PCLKC: 60 MHz (max) • PCLKD: 60 MHz (max)

Item	RX630	RX65N
	• FCLK: 4 MHz to 50 MHz (for programming and erasing the ROM and E2 DataFlash) 50 MHz (max) (for reading from the E2 DataFlash) • BCLK: 50 MHz (max) • BCLK pin output: 25 MHz (max) • UCLK: 48 MHz (max) • CANMCLK: 20 MHz (max) • IECLK: 50 MHz (max) • RTCSCLK: 32.768 kHz • RTCMCLK: 4 MHz to 16 MHz • IWDTCLK: 125 kHz • JTAGTCK: 10 MHz (max)	• FCLK: 4 MHz to 60 MHz (for programming and erasing the code flash memory and data flash memory*2) 60 MHz (max) (for reading from the data flash memory)*2 • BCLK: 120 MHz (max) • BCLK pin output: 60 MHz (max) • SDCLK pin output: 60 MHz (max) • UCLK: 48 MHz (max) • CACCLK: Same as the clock from respective oscillators • CANMCLK: 24 MHz (max) • RTCSCLK: 32.768 kHz • RTCMCLK: 8 MHz to 16 MHz • IWDTCLK: 120 kHz • JTAGTCK: 10 MHz (max)
Main clock oscillator	• Resonator frequency: 4 MHz to 16 MHz • External clock input frequency: 20 MHz (max) • Connectable resonator or additional circuit: ceramic resonator, crystal resonator • Connection pin: EXTAL, XTAL • Oscillation stop detection function: When an oscillation stop is detected with the main clock, the system clock source is switched to LOCO, and MTU output can be forcedly driven to the high-impedance.	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max) • Connectable resonator or additional circuit: ceramic resonator, crystal resonator • Connection pin: EXTAL, XTAL • Oscillation stop detection function: When an oscillation stop is detected with the main clock, the system clock source is switched to LOCO, and MTU3 output can be forcedly driven to the high-impedance.
Sub-clock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pin: XCIN, XCOUT	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pin: XCIN, XCOUT
PLL frequency synthesizer	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 16 MHz • Frequency multiplication ratio: Selectable from 8, 10, 12, 16, 20, 24, 25, and 50 • VCO oscillation frequency: 104 MHz to 200 MHz	• Input clock source: Main clock, HOCO • Input pulse frequency division ratio: Selectable from 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable from 10 to 30 • Output clock frequency of the PLL frequency synthesizer: 120 MHz to 240 MHz
High-speed on-chip oscillator (HOCO)	• Oscillation frequency: 50 MHz • HOCO power supply control	• Selectable from 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 125 MHz	Oscillation frequency: 240 kHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 125 kHz	Oscillation frequency: 120 kHz

Item	RX630	RX65N
JTAG external clock input (TCK)	Input clock frequency: 10 MHz (max)	Input clock frequency: 10 MHz (max)
Control of output on BCLK pin	• BCLK clock output or high output is selectable • BCLK or BCLK/2 is selectable	• BCLK clock output or high output is selectable • BCLK or BCLK/2 is selectable
Control of output on SDCLK pin	-	SDCLK clock output or high output is selectable
Event link function (output)	-	Detection of stopping of the main clock oscillator
Event link function (input)	-	Switching of the clock source to the low-speed on-chip oscillator

*1: Can be used for products with code flash memory less than 1 megabyte.
*2: Can be used for products with at least 1.5 Mbytes of code flash memory.
Note 1: Restrictions in relation to the clock when ETHERC is in use are as follows.
12.5 MHz ≤ PCLKA ≤ 120 MHz, PCLKA frequency = ICLK frequency
Note 2: When the frequency of ICLK is set to faster than 50 MHz, the value of the ROMWT register needs to be modified.

Table 2.9 Comparative Listing of Clock Generation Circuit Registers

Register	Bit	RX630	RX65N
SCKCR	PCKD[3:0]	-	Peripheral Module Clock D (PCLKD) Select
	PCKC[3:0]	-	Peripheral Module Clock C (PCLKC) Select
	PCKA[3:0]	-	Peripheral Module Clock A (PCLKA) Select
	PSTOP0	-	SDCLK Pin Output Control
ROMWT	-	-	ROM Wait Cycle Setting Register
SCKCR2	IEBCK[3:0]	IEBUS Clock (IECLK) Select	-
	UCK[3:0]	USB Clock (UCLK) Select b7 b4 0 0 1 0: x1/3 0 0 1 1: x1/4 Settings other than above are prohibited when USB is in use. When USB is not in use, these bits are read as 0001b. The write value should be 0001b.	USB Clock (UCLK) Select b7 b4 0 0 0 1: x1/2 0 0 1 0: x1/3 0 0 1 1: x1/4 0 1 0 0: x1/5 Settings other than above are prohibited when USB is in use. When USB is not in use, these bits are read as 0001b. The write value should be 0001b.

Register	Bit	RX630	RX65N
PLLCR	PLIDIV[1:0]	PLL Input Frequency Division Ratio Select b1 b0 0 0: x1 0 1: x1/2 1 0: x1/4 1 1: Setting prohibited	PLL Input Frequency Division Ratio Select b1 b0 0 0: x1 0 1: x1/2 1 0: x1/3 1 1: Setting prohibited
	PLLSRCSEL	-	PLL Clock Source Select
	STC[5:0]	Frequency Multiplication Factor Select b13 b8 0 0 0 1 1 1: x8 0 0 1 0 0 1: x10 0 0 1 0 1 1: x12 0 0 1 1 1 1: x16 0 1 0 0 1 1: x20 0 1 0 1 1 1: x24 0 1 1 0 0 0: x25 1 1 0 0 0 1: x50 Settings other than above are prohibited.	Frequency Multiplication Factor Select b13 b8 0 1 0 0 1 1: x10.0 0 1 0 1 0 0: x10.5 0 1 0 1 0 1: x11.0 0 1 0 1 1 0: x11.5 0 1 0 1 1 1: x12.0 0 1 1 0 0 0: x12.5 : : 1 1 0 0 0 1: x25.0 : : 1 1 1 0 0 1: x29.0 1 1 1 0 1 0: x29.5 1 1 1 0 1 1: x30.0 Settings other than above are prohibited.
		The Value after reset is different.	
HOCOCR2	-	-	High-Speed On-Chip Oscillator Control Register 2
OSCOVFSR	-	-	Oscillation Stabilization Flag Register
MOSCWTCR*	MSTS[4:0]:RX630 MSTS[7:0]:RX65N	Main Clock Oscillator Waiting Time (b4 to b0)	Main Clock Oscillator Waiting Time (b7 to b0)
		The Value after reset is different.	
SOSCWTCR*	SSTS[4:0]:RX630 SSTS[7:0]:RX65N	Sub-Clock Oscillator Waiting Time (b4 to b0)	Sub-Clock Oscillator Waiting Time (b7 to b0)
		The Value after reset is different.	
MOFCR	MODRV2[1:0]	-	Main Clock Oscillator Driving Ability 2 Switching
	MOSEL	-	Main Clock Oscillator Switching

Note: * In the User's Manual: Hardware of the RX630 Group, MOSCWTCR and SOSCWTCR are described in section 11, Low Power Consumption.

2.7 Low Power Consumption

Table 2.10 shows a Comparative Listing of Low Power Consumption Specifications, Table 2.11 to Table 2.14shows a Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode, and Table 2.15 shows a Comparative Listing of Low Power Consumption Registers.

Table 2.10 Comparative Listing of Low Power Consumption Specifications

Item	RX630	RX65N
Reducing power consumption by switching clock signals	The frequency division ratio is settable independently for the system clock (ICLK), peripheral module clock (PCLKB), external bus clock (BCLK), and flash interface clock (FCLK).	The frequency division ratio is settable independently for the system clock (ICLK), peripheral module clock (PCLKA, PCLKB, PCLKC, PCLKD), external bus clock (BCLK), and flash interface clock (FCLK).
BCLK output control function	BCLK output or high-level output can be selected.	BCLK output or high-level output can be selected.
SDCLK output control function	-	SDCLK output or high-level output can be selected.
Module-stop function	Functions can be stopped independently for each peripheral module.	Functions can be stopped independently for each peripheral module.
Function for transition to low power consumption mode	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.
Low power consumption modes	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode
Function for lower operating power consumption	• Power consumption can be reduced in normal operation, sleep mode, and all-module clock stop mode by selecting an appropriate operating power consumption control mode according to the operating frequency and operating voltage. • Three operating power control modes — High-speed operating mode — Low-speed operating mode 1 — Low-speed operating mode 2	• Power consumption can be reduced in normal operation, sleep mode, and all-module clock stop mode by selecting an appropriate operating power consumption control mode according to the operating frequency and operating voltage range. • Three operating power control modes — High-speed operating mode — Low-speed operating mode 1 — Low-speed operating mode 2 There is no difference in power consumption when the same conditions (frequency and voltage) are set in low-speed operating modes 1 and 2.

Table 2.11 Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode (Sleep Mode)

Entering and Exiting Low Power Consumption Modes and Operating States	RX630 Sleep Mode	RX65N Sleep Mode
Transition condition	Control register + instruction	Control register + instruction
Method of release other than reset	Interrupt	Interrupt
State after release	Program execution state (interrupt processing)	Program execution state (interrupt processing)
Main clock oscillator	Operating possible	Operating possible
Sub-clock oscillator	Operating possible	Operating possible
High-speed on-chip oscillator	Operating possible	Operating possible
Low-speed on-chip oscillator	Operating possible	Operating possible
IWDT-dedicated on-chip oscillator	Operating possible	Operating possible
PLL	Operating possible	Operating possible
CPU	Stopped (Retained)	Stopped (Retained)
RAM1 (0001 0000h to 0001 FFFFh)	Operating possible (Retained)	-
RAM0 (0000 0000h to 0000 FFFFh)	Operating possible (Retained)	-
RAM and expansion RAM	-	Operating possible (Retained)
Standby RAM	-	Operating possible (Retained)
Flash memory	Operating	Operating
USB 2.0 function module (USB)	Operating possible	-
USBFS host/function module (USBb)	-	Operating possible
Watchdog timer (WDT)	Stopped (Retained)	-
Watchdog timer (WDTA)	-	Stopped (Retained)
Independent watchdog timer (IWDT)	Operating possible	Operating possible
Realtime clock (RTC)	Operating possible	Operating possible
8-bit timer (unit 0, unit 1) (TMR)	Operating possible	Operating possible
Voltage detection circuit (LVD)	Operating possible	-
Voltage detection circuit (LVDA)	-	Operating possible
Power-on reset circuit	Operating	Operating
Peripheral modules	Operating possible	Operating possible
I/O ports	Operating	Operating

Table 2.12 Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode (All-Module Clock Stop Mode)

Entering and Exiting Low Power Consumption Modes and Operating States	RX630 All-Module Clock Stop Mode	RX65N All-Module Clock Stop Mode
Transition condition	Control register + instruction	Control register + Instruction
Method of release other than reset	Interrupt	Interrupt
State after release	Program execution state (interrupt processing)	Program execution state (interrupt processing)
Main clock oscillator	Operating possible	Operating possible
Sub-clock oscillator	Operating possible	Operating possible
High-speed on-chip oscillator	Operating possible	Operating possible
Low-speed on-chip oscillator	Operating possible	Operating possible
IWDT-dedicated on-chip oscillator	Operating possible	Operating possible
PLL	Operating possible	Operating possible
CPU	Stopped (Retained)	Stopped (Retained)
RAM1 (0001 0000h to 0001 FFFFh)	Stopped (Retained)	-
RAM0 (0000 0000h to 0000 FFFFh)	Stopped (Retained)	-
RAM and expansion RAM	-	Stopped (Retained)
Standby RAM	-	Stopped (Retained)
Flash memory	Stopped (Retained)	Stopped (Retained)
USB 2.0 function module (USB)	Stopped	-
USBFS host/function module (USBb)	-	Stopped
Watchdog timer (WDT)	Stopped (Retained)	-
Watchdog timer (WDTA)	-	Stopped (Retained)
Independent watchdog timer (IWDT)	Operating possible	Operating possible
Realtime clock (RTC)	Operating possible	Operating possible
8-bit timer (unit 0, unit 1) (TMR)	Operating possible	Operating possible
Voltage detection circuit (LVD)	Operating possible	-
Voltage detection circuit (LVDA)	-	Operating possible
Power-on reset circuit	Operating	Operating
Peripheral modules	Stopped (Retained)	Stopped (Retained)
I/O ports	Retained	Retained

Table 2.13 Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode (Software Standby Mode)

Entering and Exiting Low Power Consumption Modes and Operating States	RX630 Software Standby Mode	RX65N Software Standby Mode
Transition condition	Control register + instruction	Control register + instruction
Method of release other than reset	Interrupt	Interrupt
State after release	Program execution state (interrupt processing)	Program execution state (interrupt processing)
Main clock oscillator	Operating possible	Operating possible
Sub-clock oscillator	Operating possible	Operating possible
High-speed on-chip oscillator	Stopped	Stopped
Low-speed on-chip oscillator	Stopped	Stopped
IWDT-dedicated on-chip oscillator	Operating possible	Operating possible
PLL	Stopped	Stopped
CPU	Stopped (Retained)	Stopped (Retained)
RAM1 (0001 0000h to 0001 FFFFh)	Stopped (Retained)	-
RAM0 (0000 0000h to 0000 FFFFh)	Stopped (Retained)	-
RAM and expansion RAM	-	Stopped (Retained)
Standby RAM	-	Stopped (Retained)
Flash memory	Stopped (Retained)	Stopped (Retained)
USB 2.0 function module (USB)	Stopped	-
USBFS host/function module (USBb)	-	Stopped
Watchdog timer (WDT)	Stopped (Retained)	-
Watchdog timer (WDTA)	-	Stopped (Retained)
Independent watchdog timer (IWDT)	Operating possible	Operating possible
Realtime clock (RTC)	Operating possible	Operating possible
8-bit timer (unit 0, unit 1) (TMR)	Stopped (Retained)	Stopped (Retained)
Voltage detection circuit (LVD)	Operating possible	-
Voltage detection circuit (LVDA)	-	Operating possible
Power-on reset circuit	Operating	Operating
Peripheral modules	Stopped (Retained)	Stopped (Retained)
I/O ports	Retained	Retained

Table 2.14 Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode (Deep Software Standby Mode)

Entering and Exiting Low Power Consumption Modes and Operating States	RX630 Deep Software Standby Mode	RX65N Deep Software Standby Mode
Transition condition	Control register + instruction	Control register + instruction
Method of release other than reset	Interrupt	Interrupt
State after release	Program execution state (reset processing)	Program execution state (reset processing)
Main clock oscillator	Operating possible	Operating possible
Sub-clock oscillator	Operating possible	Operating possible
High-speed on-chip oscillator	Stopped	Stopped
Low-speed on-chip oscillator	Stopped	Stopped
IWDT-dedicated on-chip oscillator	Stopped (Undefined)	Stopped (Undefined)
PLL	Stopped	Stopped
CPU	Stopped (Undefined)	Stopped (Undefined)
RAM1 (0001 0000h to 0001 FFFFh)	Stopped (Undefined)	-
RAM0 (0000 0000h to 0000 FFFFh)	Stopped (Retained/Undefined)	-
RAM and expansion RAM	-	Stopped (Undefined)
Standby RAM	-	Stopped (Retained/Undefined)
Flash memory	Stopped (Retained)	Stopped (Retained)
USB 2.0 function module (USB)	Stopped (Retained/Undefined)	-
USBFS host/function module (USBb)	-	Stopped (Retained/Undefined)
Watchdog timer (WDT)	Stopped (Undefined)	-
Watchdog timer (WDTA)	-	Stopped (Undefined)
Independent watchdog timer (IWDT)	Stopped (Undefined)	Stopped (Undefined)
Realtime clock (RTC)	Operating possible	Operating possible
8-bit timer (unit 0, unit 1) (TMR)	Stopped (Undefined)	Stopped (Undefined)
Voltage detection circuit (LVD)	Operating possible	-
Voltage detection circuit (LVDA)	-	Operating possible
Power-on reset circuit	Operating	Operating
Peripheral modules	Stopped (Undefined)	Stopped (Undefined)
I/O ports	Retained	Retained

Table 2.15 Comparative Listing of Low Power Consumption Registers

Register	Bit	RX630	RX65N
MSTPCRA	MSTPA0	-	Compare Match Timer W (Unit 1) Module Stop
	MSTPA1	-	Compare Match Timer W (Unit 0) Module Stop
	MSTPA9	Multifunction Timer Pulse Unit 2 Module Stop Target module: MTU (MTU0 to MTU5)	Multifunction Timer Pulse Unit 3 Module Stop Target module: MTU3
	MSTPA12	16-Bit Timer Pulse Unit 1 (Unit 1) Module Stop	-
	MSTPA16	-	12-bit A/D Converter (Unit 1) Module Stop
	MSTPA17	12-bit A/D Converter (Unit 1) Module Stop	12-bit A/D Converter (Unit 0) Module Stop
	MSTPA19	D/A Converter Module Stop Target module: 10-bit D/A	12-bit D/A Converter Module Stop Target module: 12-bit D/A
	MSTPA23	10-bit A/D Converter Module Stop	-
	MSTPA29	Module Stop A29	EXDMA Controller Module Stop Target module: EXDMAC
MSTPCRB	MSTPB2	CAN Module 2 Module Stop	-
	MSTPB4	Serial Communication Interface SCId Module Stop Target module: SCId (SCI12)	Serial Communication Interface SCIh Module Stop Target module: SCIh (SCI12)
	MSTPB6	-	Data Operation Circuit Module Stop
	MSTPB9	-	Event Link Controller Module Stop
	MSTPB15	-	Ethernet Controller and Ethernet Controller DMA Controller (Channel 0) Modules Stop
	MSTPB19	Universal Serial Bus Interface (Port 0) Module Stop	Universal Serial Bus 2.0 FS Interface Module Stop
	MSTPB20	I^2C Bus Interface 1 Module Stop	I2C Bus Interface 1 Module Stop*1
	MSTPB22	-	Parallel Data Capture Unit Module Stop
MSTPCRC	MSTPC1	RAM1 Module Stop	-
	MSTPC2	-	Expansion RAM Module Stop*1
	MSTPC7	-	Standby RAM Module Stop
	MSTPC16	I^2C Bus Interface 3 Module Stop	-
	MSTPC18	IEBUS Module Stop	-
	MSTPC19	Frequency Measurement Circuit Module Stop Target module: MCK	CAC Module Stop Target module: CAC
	MSTPC23	-	Quad Serial Peripheral Interface Module Stop
	MSTPC28	-	2D drawing engine Module Stop*1
	MSTPC29	-	Graphic-LCD controller Module Stop*1
MSTPCRD	-	-	Module Stop Control Register D
MOSCWTCR*	MSTS[4:0]:RX630 MSTS[7:0]:RX65N	Main Clock Oscillator Waiting Time (b4 to b0)	Main Clock Oscillator Waiting Time (b7 to b0)
		The Value after reset is different.	

Register	Bit	RX630	RX65N
SOSCWTCR*	SSTS[4:0]:RX630 SSTS[7:0]:RX65N	Sub-Clock Oscillator Waiting Time (b4 to b0)	Sub-Clock Oscillator Waiting Time (b7 to b0)
		The Value after reset is different.	
PLLWTCR	-	PLL Wait Control Register	-

Note: * In the User's Manual: Hardware of the RX65N Group, MOSCWTCR and SOSCWTCR are described in section 9, Clock Generation Circuit

*1: Can be used for products with at least 1.5 Mbytes of code flash memory.

2.8 Register Write Protection Function

Table 2.16 shows a Comparative Listing of Register Write Protection Function Specifications.

Table 2.16 Comparative Listing of Register Write Protection Function Specifications

Item	RX630	RX65N
PRC0 bit	Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR	Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR,MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, OSTDCR, OSTDSR
PRC1 bit	• Registers related to the operating modes: SYSCR0, SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR, RSTCKCR, MOSCWTCR, SOSCWTCR, PLLWTCR, DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, DPSIEGR0 to DPSIEGR3 • Registers related to clock generation circuit: MOFCR, HOCOPCR • Software reset register: SWRR	• Registers related to the operating modes: SYSCR0, SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, DPSIEGR0 to DPSIEGR3 • Registers related to clock generation circuit: MOSCWTCR, SOSCWTCR, MOFCR, HOCOPCR • Software reset register: SWRR
PRC3 bit	Registers related to the LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1,LVD2SR	Registers related to the LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

2.9 Exception Handling

Table 2.17shows a Comparative Listing of Vector, and Table 2.18 shows a Comparative Listing of Return from Exception Handling Routine.

Table 2.17 Comparative Listing of Vector

Exception (Event)		RX630	RX65N
Undefined instruction exception		Fixed vector table	Exception vector table (EXTB)
Privileged instruction exception		Fixed vector table	Exception vector table (EXTB)
Access exception		Fixed vector table	Exception vector table (EXTB)
Floating-point exception		Fixed vector table	Exception vector table (EXTB)
Reset		Fixed vector table	Exception vector table (EXTB)
Non-maskable interrupt		Fixed vector table	Exception vector table (EXTB)
Interrupt	Fast interrupt	FINTV	FINTV
	Other than above	Relocatable vector table (INTB)	Interrupt vector table (INTB)
Unconditional trap		Relocatable vector table (INTB)	Interrupt vector table (INTB)

Table 2.18 Comparative Listing of Return from Exception Handling Routine

Exception		RX230	RX65N
Undefined instruction exception		RTE	RTE
Privileged instruction exception		RTE	RTE
Access exception		RTE	RTE
Floating-point exception		RTE	RTE
Reset		Return is impossible	Return is impossible
Non-maskable interrupt		Prohibited	Prohibited
Interrupt	Fast interrupt	RTFI	RTFI
	Other than above	RTE	RTE
Unconditional trap		RTE	RTE

2.10 Interrupt Controller

Table 2.19 shows a Comparative Listing of Interrupt Controller Specifications, and Table 2.20 shows a Comparative Listing of Interrupt Controller Registers.

Table 2.19 Comparative Listing of Interrupt Controller Specifications

Item		RX630 (ICUb)	RX65N (ICUB)
Interrupt	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection Edge detection or level detection is fixed for each source of connected peripheral modules. • Interrupt grouping: Multiple interrupt requests can be allocated to a single interrupt vector. — Number of groups for edge detection interrupts: 7 (groups 0 to 6) — Number of groups for level detection interrupts: 1 (group 12)	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection (detection method is fixed for each interrupt source) • Group interrupt: Multiple interrupt sources are grouped together and treated as an interrupt source. — Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) — Group BL0/BL1/BL2 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) — Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt B: Any of the interrupt sources for peripheral modules that use PCLKB as the operating clock can be assigned to interrupt vector numbers 128 to 207. • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.
Interrupt	Peripheral function interrupts	• Interrupt unit selection: One of the two interrupt request units can be selected as an interrupt request source. Number of interrupts per unit: 6.	

Item		RX630 (ICUb)	RX65N (ICUB)
	External pin interrupts	• Interrupts from pins IRQ0 to IRQ15 • Number of sources: 16 • Interrupt detection: Low level/falling edge/rising edge/rising and falling edges One of these detection methods can be set for each source. • Digital filter function: supported	• Interrupts from signals input to IRQi pins (i = 0 to 15) • Number of sources: 16 • Interrupt detection method: Detection of low level, falling edge, rising edge, rising and falling edges. One of these detection methods can be set for each source. • Digital filter can be used to remove noise.
	Software interrupt	• Interrupt generated by writing to a register • One interrupt source	• Interrupt request can be generated by writing to a register. • Two interrupt sources
	Interrupt priority level	Specified by registers.	Priority level can be set with interrupt source priority register r (IPRr) (r = 000 to 255).
	Fast interrupt function	Faster interrupt processing of the CPU can be set only for a single interrupt source.	CPU interrupt response time can be reduced. This function can be used for only one interrupt source.
	DTC and DMAC control	The DTC and DMAC can be activated by interrupt sources.	Interrupt sources can be used to start the DTC and DMAC.
	EXDMAC control	-	• Interrupt selected by software configurable interrupt B source select register 144 or software configurable interrupt A source select register 208 can be used to start EXDMAC0. • Interrupt selected by software configurable interrupt B source select register 145 or software configurable interrupt A source select register 209 can be used to start EXDMAC1.
Non-maskable interrupts	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter function: supported	• Interrupt by the input signal to the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter can be used to remove noise.
Non-maskable interrupts	Oscillation stop detection interrupt	Interrupt on detection of oscillation having stopped	This interrupt occurs when the main clock oscillator stop is detected.
	WDT underflow/refresh error interrupt	Interrupt on an underflow of the down counter or occurrence of a refresh error	This interrupt occurs when the watchdog timer (WDT) underflows or a refresh error occurs.
	IWDT underflow/refresh error interrupt	Interrupt on an underflow of the down counter or occurrence of a refresh error	This interrupt occurs when the independent watchdog timer (IWDT) underflows or a refresh error occurs.
	Voltage monitoring 1 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)	Interrupt from voltage detection circuit 1 (LVD1)

Item		RX630 (ICUb)	RX65N (ICUB)
	Voltage monitoring 2 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)	Interrupt from voltage detection circuit 2 (LVD2)
	RAM error interrupt	-	This interrupt occurs when a parity check error is detected in the RAM (including the expanded RAM*1).
Return from low power consumption modes	Sleep mode	Return is initiated by non-maskable interrupts or any other interrupt source.	Exit sleep mode by any interrupt source.
	All-module clock stop mode	Return is initiated by non-maskable interrupts, IRQ0 to IRQ15 interrupts, TMR, USB resume, RTC alarm/periodic, IWDT, voltage monitoring 1, voltage monitoring 2, and oscillator-stopped detection interrupts.	Exit all-module clock stop mode by the NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection interrupt, USB resume, RTC alarm, RTC period, IWDT, software configurable interrupt 146 to 157).
	Software standby mode	Return is initiated by non-maskable interrupts, IRQ0 to IRQ15 interrupts, USB resume, RTC alarm/periodic interrupts.	Exit all-module clock stop mode by the NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, RTC period, IWDT).
	Deep software standby mode	A certain external pin interrupt source pin, any of peripheral interrupts (the RTC alarm, RTC interval, USB resume, voltage monitoring 1, and voltage monitoring 2 interrupts).	Exit all-module clock stop mode by the NMI pin interrupt, specific external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, RTC period).

*1: Can be used for products with at least 1.5 Mbytes of code flash memory.

Table 2.20 Comparative Listing of Interrupt Controller Registers

Register	Bit	RX630 (ICUb)	RX65N (ICUB)
IPRn	-	n = 000-253	n = 000-255
SWINT2R	-	-	Software Interrupt 2 Generation Register
DTCERn	DTCE	DTC Activation Enable 0: DTC activation is disabled 1: DTC activation is enabled	DTC Transfer Request Enable 0: The corresponding interrupt source is not selected as the DTC trigger. 1: The corresponding interrupt source is selected as the DTC trigger.
NMISR	RAMST	-	RAM Error Interrupt Status Flag
NMIER	RAMEN	-	RAM Error Interrupt Enable
GRPm	-	Group m Interrupt Source Register (m: group number)	-
GRPBE0	-	-	Group BE0 Interrupt Request Register
GRPBL0	-	-	Group BL0 Interrupt Request Register
GRPBL1	-	-	Group BL1 Interrupt Request Register
GRPBL2	-	-	Group BL2 Interrupt Request Register
GRPAL0	-	-	Group AL0 Interrupt Request Register
GRPAL1	-	-	Group AL1 Interrupt Request Register
GENm	-	Group m Interrupt Enable Register (m = group number)	-
GENBE0	-	-	Group BE0 Interrupt Request Enable Register
GENBL0	-	-	Group BL0 Interrupt Request Enable Register
GENBL1	-	-	Group BL1 Interrupt Request Enable Register
GENBL2	-	-	Group BL2 Interrupt Request Enable Register
GENAL0	-	-	Group AL0 Interrupt Request Enable Register
GENAL1	-	-	Group AL1 Interrupt Request Enable Register
GCRm	-	Group m Interrupt Clear Register (m = group number)	-
GCRBE0	-	-	Group BE0 Interrupt Clear Register
SEL	-	Unit Selecting Register	-
PIBRk	-	-	Software Configurable Interrupt B Request Register k (k = 0h to Bh)
PIARk	-	-	Software Configurable Interrupt A Request Register k (k = 0h to 5h, Bh)

Register	Bit	RX630 (ICUb)	RX65N (ICUB)
SLIBXRn	-	-	Software Configurable Interrupt B Source Select Register Xn (n = 128 to 143)
SLIBRn	-	-	Software Configurable Interrupt B Source Select Register n (n = 144 to 207)
SLIARn	-	-	Software Configurable Interrupt A Source Select Register n (n = 208 to 255)
SELEXDR	-	-	EXDMAC Trigger Select Register
SLIPRCR	-	-	Software Configurable Interrupt Source Select Register Write Protect Register

2.11 Buses

Table 2.21 shows a Comparative Listing of Bus Specifications, Table 2.22 shows a Comparative Listing of External Bus Specifications, and Table 2.23 shows a Comparative Listing of Bus Registers.

Table 2.21 Comparative Listing of Bus Specifications

Bus Type		RX630	RX65N
CPU bus	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, expansion RAM*1, code flash memory) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, expansion RAM*1, code flash memory) • Operates in synchronization with the system clock (ICLK)
Memory bus	Memory bus 1	Connected to RAM	Connected to RAM
	Memory bus 2	Connected to ROM	Connected to code flash memory
	Memory bus 3	None	Connected to expansion RAM*1
Internal main bus	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DMAC, DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the DMAC, DTC, extended bus master • Connected to on-chip memory (RAM, expansion RAM*1, code flash memory) • Operates in synchronization with the system clock (ICLK)
Internal peripheral bus	Internal peripheral bus 1	• Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (DTC, DMAC, EXDMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK) (EDMAC operates in synchronization with the BCLK)
	Internal peripheral bus 2	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, 4 and 5) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral-module clock (PCLKB)

Bus Type		RX630	RX65N
	Internal peripheral bus 3	• Connected to peripheral modules (USB) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (USBb, PDC, and standby RAM) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 4	Reserved area	• Connected to peripheral modules (EDMAC, ETHERC, MTU3, SCIi, RSPI, and AES*2) • Operates in synchronization with the peripheral-module clock (PCLKA)
	Internal peripheral bus 5	Reserved area	• Connected to peripheral modules (GLCDC, DRW2D)*1 • Operates in synchronization with the peripheral-module clock (PCLKA)*1
	Internal peripheral bus 6	• Connected to ROM (P/E) and E2 DataFlash memory • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to code flash (in P/E) and data flash memory*1 • Operates in synchronization with the FlashIF clock (FCLK)
External bus CS area	CS area	• Connected to the external devices • Operates in synchronization with the external-bus clock (BCLK)	• Connected to the external devices • Operates in synchronization with the external-bus clock (BCLK)
	SDRAM area	-	• Connected to the SDRAM • Operates in synchronization with the SDRAM clock (SDCLK)

*1: Can be used for products with at least 1.5 Mbytes of code flash memory.
*2: Can be used for products with code flash memory less than 1 megabyte.

Table 2.22 Comparative Listing of External Bus Specifications

Item	RX630	RX65N
External address space	• An external address space is divided into eight CS areas (CS0 to CS7) for management. • Chip select signals can be output for each area. • Bus width can be set for each area. — Separate bus: An 8, 16 or 32-bit bus space is selectable. — Address/data multiplexed bus: An 8 or 16-bit bus space is selectable. • An endian mode can be specified for each area.	• An external address space is divided into eight CS areas (CS0 to CS7) and the SDRAM area (SDCS) for management. • Chip select signals can be output for each area. • Bus width can be set for each area. — Separate bus: An 8, 16, or 32-bit*1 bus space is selectable. — Address/data multiplexed bus: An 8 or 16-bit bus space is selectable. • An endian mode can be specified for each area.
CS area controller	• Recovery cycles can be inserted. — Read recovery: Up to 15 cycles — Write recovery: Up to 15 cycles • Cycle wait function: Wait for up to 31 cycles (page access: up to 7 cycles) • Wait control can be used to set up the following. — Timing of assertion and negation for chip-select signals (CS0# to CS7#) — The timing of assertion of the read signal (RD#) and write signals (WR0#/WR# to WR3#) — The timing with which data output starts and ends • Write access mode: Single write strobe mode/byte strobe mode • Separate bus or address/data multiplexed bus can be set for each area.	• Recovery cycles can be inserted. — Read recovery: Up to 15 cycles — Write recovery: Up to 15 cycles • Cycle wait function: Wait for up to 31 cycles (page access: up to 7 cycles) • Wait control can be used to set up the following. — Timing of assertion and negation for chip-select signals (CS0# to CS7#) — The timing of assertion of the read signal (RD#) and write signals (WR0#/WR#, and WR1# to WR3#*1) — The timing with which data output starts and ends • Write access mode: Single write strobe mode/byte strobe mode • Separate bus or address/data multiplexed bus can be set for each area.
SDRAM area controller	-	• Multiplexing output of row address/column address (8, 9, 10, or 11 bits) • Self-refresh and auto-Refresh selectable • CAS latency can be specified from one to three cycles
Write buffer function	When write data from the bus master has been written to the write buffer, write access by the bus master is completed.	When write data from the bus master has been written to the write buffer, write access by the bus master is completed.

Item	RX630	RX65N
Frequency	The CS area controller (CSC) operates in synchronization with the external-bus clock (BCLK).	• The CS area controller (CSC) operates in synchronization with the external-bus clock (BCLK).* • The SDRAM area controller (SDRAMC) operates in synchronization with the SDRAM clock (SDCLK).

Note:* The BCLK and the SDCLK should be operated with the same frequency when the SDRAM is in use.
*1: Can be used for products with at least 1.5 Mbytes of code flash memory.

Table 2.23 Comparative Listing of Bus Registers

Register	Bit	RX630	RX65N
CSnCR	BSIZE[1:0]	External Bus Width Select b5 b4 0 0: A 16-bit bus space is selected 0 1: A 32-bit bus space is selected 1 0: An 8-bit bus space is selected 1 1: Setting prohibited	External Bus Width Select b5 b4 0 0: A 16-bit bus space is selected 0 1: A 32-bit bus space is selected*1 1 0: An 8-bit bus space is selected 1 1: Setting prohibited
SDCCR	-	-	SDC Control Register
SDCMOD	-	-	SDC Mode Register
SDAMOD	-	-	SDRAM Access Mode Register
SDSELF	-	-	SDRAM Self-Refresh Control Register
SDRFCR	-	-	SDRAM Refresh Control Register
SDRFEN	-	-	SDRAM Auto-Refresh Control Register
SDICR	-	-	SDRAM Initialization Sequence Control Register
SDIR	-	-	SDRAM Initialization Register
SDADR	-	-	SDRAM Address Register
SDTR	-	-	SDRAM Timing Register
SDMOD	-	-	SDRAM Mode Register
SDSR	-	-	SDRAM Status Register
BERSR1	MST[2:0]	Bus Master Code b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved	Bus Master Code b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Extended bus master 1 1 1: EXDMAC
BUSPRI	BPHA[1:0]	Internal Peripheral Bus 1 (RAM) Priority Control	Internal Peripheral Bus 1 and 3*1 (RAM / expansion RAM*1) Priority Control
	BPHB[1:0]	-	Internal Peripheral Bus 4 and 5*1 Priority Control
EBMAPCR	-	-	Extended Bus Master Priority Control Register*1

*1: Can be used for products with at least 1.5 Mbytes of code flash memory.

2.12 Memory-Protection Unit

Table 2.24 shows a Comparative Listing of Memory-Protection Unit Registers.

Table 2.24 Comparative Listing of Memory-Protection Unit Registers

Register	Bit	RX630 (MPU)	RX65N (MPU)
MPECLR	CLR	Error Status-Clearing [Reading] 0: Fixed value for reading [Writing] 0: Nothing is done. 1: The DRW, DA and IA bits in MPESTS are set to 0.	Error Status-Clearing [Reading] 0: Fixed value for reading [Writing] 0: Nothing is done. 1: The DRW, DMPER and IMPER bits in MPESTS are set to 0.
MPESTS	IA	Instruction Memory-Protection Error Generated Bit	-
	DA	Data Memory-Protection Error Generated Bit	-
	IMPER	-	Instruction Memory-Protection Error Generation
	DMPER	-	Data Memory-Protection Error Generation

2.13 DMA Controller

Table 2.25 shows a Comparative Listing of DMA Controller Specifications, and Table 2.26 shows a Comparative Listing of DMA Controller Registers.

Table 2.25 Comparative Listing of DMA Controller Specifications

Item		RX630 (DMACA)	RX65N (DMACAa)
Number of channels		4 (DMACm (m = 0 to 3))	8 (DMACm (m = 0 to 7))
Transfer space		512 Mbytes (0000 0000h to 0FFF FFFFh and F000 0000h to FFFF FFFFh, excluding reserved areas)	512 Mbytes (0000 0000h to 0FFF FFFFh and F000 0000h to FFFF FFFFh, excluding reserved areas)
Maximum transfer data count		1Mbyte (Maximum number of transfers in block transfer mode: 1,024 data x 1,024 blocks)	64 Mbytes (Maximum number of transfers in block transfer mode: 1,024 data x 65,536 blocks)
DMAC request sources		Activation source selectable for each channel • Software trigger • Interrupt requests from peripheral modules or trigger input to external interrupt input pins	Request source selectable for each channel • Software trigger • Interrupt requests from peripheral modules or trigger input to external interrupt input pins
Channel priority		Channel 0 > Channel 1 > Channel 2 > Channel 3 (Channel 0: highest)	Channel 0 > Channel 1 > Channel 2 > Channel 3 ... > Channel 7 (Channel 0: highest)
Transfer data	1 data unit	Bit length: 8, 16, 32 bits	Bit length: 8, 16, 32 bits
	Block size	Number of data: 1 to 1,024	Number of data: 1 to 1,024
Transfer modes	Normal transfer mode	• One data transfer by one DMA transfer request • Free running mode (setting in which total number of data transfers is not specified) settable	• One data transfer by one DMA transfer request • Free running mode (setting in which total number of data transfers is not specified) settable
	Repeat transfer mode	• One data transfer by one DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination • Maximum settable repeat size: 1,024	• One data transfer by one DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination • Maximum settable repeat size: 1,024
	Block transfer mode	• One block data transfer by one DMA transfer request • Maximum settable block size: 1,024 data	• One block data transfer by one DMA transfer request • Maximum settable block size: 1,024 data
Selective functions	Extended repeat area function	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed • Area of 2 bytes to 128 Mbytes separately settable as extended repeat area for transfer source and destination	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed • Area of 2 bytes to 128 Mbytes separately settable as extended repeat area for transfer source and destination

Item		RX630 (DMACA)	RX65N (DMACAa)
Interrupt request	Transfer end interrupt	Generated on completion of transferring data volume specified by the transfer counter.	Generated when the specified number of transfers is completed in normal transfer mode Generated when the specified repeat count of transfers is completed in repeat transfer mode Generated when the specified block count of transfers is completed in block transfer mode
	Transfer escape end interrupt	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.
Event link function		-	An event link request is generated after each data transfer (for block transfer, after each block is transferred).
Power consumption reduction function		Module-stop state can be set.	Module-stop state can be set.

Table 2.26 Comparative Listing of DMA Controller Registers

Register	Bit	RX630 (DMACA)	RX65N (DMACAa)
DMCRB	-	DMA Block Transfer Count Register (b9 to b0)	DMA Block Transfer Count Register (b15 to b0)
DMIST	-	-	DMAC74 Interrupt Status Monitor Register

2.14 Data Transfer Controller

Table 2.27 shows a Comparative Listing of Data Transfer Controller Specifications, and Table 2.28 shows a Comparative Listing of Data Transfer Controller Registers.

Table 2.27 Comparative Listing of Data Transfer Controller Specifications

Item	RX630 (DTCa)	RX65N (DTCb)
Transfer modes	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address is returned to the transfer start address after the number of data transfers corresponding to “repeat size”. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 x 32 bits, 1024 bytes. • Block transfer mode — A single activation leads to the transfer of a single block. — The maximum block size is 256 x 32 bits = 1024 bytes.	• Normal transfer mode A single transfer request leads to a single data transfer. • Repeat transfer mode — A single transfer request leads to a single data transfer. — The transfer address is returned to the transfer start address after the number of data transfers corresponding to “repeat size”. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 x 32 bits, 1024 bytes. • Block transfer mode — A single transfer request leads to the transfer of a single block. — The maximum block size is 256 x 32 bits = 1024 bytes.
Transfer channels	• Channel transfer corresponding to the interrupt source is possible (transferred by the DTC activation request from the ICU). • Data of multiple channels can be transferred on a single activation source (chain transfer). • Either “executed when the counter is 0” or “always executed” can be selected for chain transfer.	• Channel transfer corresponding to the interrupt source is possible (transferred by the DTC activation request from the ICU). • Multiple data can be transferred on a single activation source (chain transfer). • Either “executed when the counter is 0” or “always executed” can be selected for chain transfer.
Transfer space	• In short-address mode: 16 Mbytes (Areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh except reserved areas) • In full-address mode: 4 Gbytes (Area from 0000 0000h to FFFF FFFFh except reserved areas)	• In short-address mode: 16 Mbytes (Areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh except reserved areas) • In full-address mode: 4 Gbytes (Area from 0000 0000h to FFFF FFFFh except reserved areas)
Data transfer units	• Length of a single data: 8, 16, or 32 bits • Number of data for a single block: 1 to 256 data	• Single data: 1 byte (8 bits), 1 word (16 bits), 1 longword (32 bits) • Single block size: 1 to 256 data
CPU interrupt requests	• An interrupt request can be generated to the CPU on a DTC activation interrupt. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of specified volume.	• An interrupt request can be generated to the CPU on a request source for a data transfer. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of specified volume.

Item	RX630 (DTCa)	RX65N (DTCb)
Event link activation	-	An event link request is generated after one data transfer (for block, after one block transfer).
Read skip	Transfer data read skip can be specified.	Reading of the transfer information can be skipped when the same transfer is repeated.
Write-back skip	When “fixed” is selected for transfer source address or transfer destination address, write-back skip execution is provided.	Write-back of the transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.
Write-back disable	-	Allows disabling the write-back of transfer information.
Sequence transfer	-	A series of complicated transfers can be registered as a sequence. Any sequence can be selected by the transfer data and executed. • Only one trigger source can be set at a time. • Up to 256 sequences for a single trigger source • The data that is initially transferred in response to a transfer request determines a sequence • The whole sequence can be executed on a single request, or be suspended in the middle of the sequence and resumed on the next transfer request (division of sequence).
Displacement addition	-	The displacement value can be added to the transfer source address (for each transfer information)
Low power consumption function	Module stop state can be specified.	Module stop state can be set.

Table 2.28 Comparative Listing of Data Transfer Controller Registers

Register	Bit	RX630 (DTCa)	RX65N (DTCb)
MRA	WBDIS	-	Write-back Disable
MRB	SQEND	-	Sequence Transfer End
	INDX	-	Index Table Reference
MRC	-	-	DTC Mode Register C
DTCVBR	-	DTC Vector Base Register The lower 12 bits: These bits are read as 0. The write value should be 0. The upper 20 bits: The upper 4 bits (b31 to b28) are ignored, and the address of this register is extended by the value specified by b27. It can be set in the range of 0000 0000h to 07FF F000h and F800 0000h to FFFF F000h in 4K-byte units.	DTC Vector Base Register Writing to the upper 4 bits (b31 to b28) is ignored, and the address of this register is extended by the value specified by b27. The lower 10 bits are reserved and the values are fixed to 0. Write 0 to the lower 10 bits if necessary. It can be set in the range of 0000 0000h to 07FF FC00h and F800 0000h to FFFF FC00h in 1K-byte units.
DTCIBR	-	-	DTC Index Table Base Register
DTCOR	-	-	DTC Operation Register
DTCSQE	-	-	DTC Sequence Transfer Enable Register
DTCDISP	-	-	DTC Address Displacement Register

2.15 I/O Ports

Table 2.29 and Table 2.30 shows a Comparative Listing of I/O Ports Specifications, and Table 2.31 and Table 2.32 shows a comparative listing of I/O port functions, and Table 2.33 shows a Comparative Listing of I/O Port Registers.

Table 2.29 Comparative Listing of I/O Ports Specifications

Port	RX630	RX65N
	177 or 176 Pins	**177 or 176 Pins**
PORT0	P00 to P03, P05, P07	P00 to P03, P05, P07
PORT1	P10 to P17	P10 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P57	P50 to P57
PORT6	P60 to P67	P60 to P67
PORT7	P70 to P77	P70 to P77
PORT8	P80 to P87	P80 to P87
PORT9	P90 to P97	P90 to P97
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7
PORTF	PF0 to PF5	PF0 to PF5
PORTG	PG0 to PG7	PG0 to PG7
PORTH	PH4, PH5	-
PORTJ	PJ3, PJ5	PJ0 to PJ3, PJ5
PORTK	PK0 to PK7	-
PORTL	PL0 to PL4	-

Table 2.30 Comparative Listing of I/O Ports Specifications

Port	RX630		RX65N	
	145 or 144 Pins	100pins	145 or 144 Pins	100pins
PORT0	P00 to P03, P05, P07	P05, P07	P00 to P03, P05, P07	P05, P07
PORT1	P12 to P17	P12 to P17	P12 to P17	P12 to P17
PORT2	P20 to P27	P20 to P27	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47	P40 to P47	P40 to P47
PORT5	P50 to P56	P50 to P55	P50 to P56	P50 to P55
PORT6	P60 to P67	-	P60 to P67	-
PORT7	P70 to P77	-	P70 to P77	-
PORT8	P80 to P83, P86, P87	-	P80 to P83, P86, P87	-
PORT9	P90 to P93	-	P90 to P93	-
PORTA	PA0 to PA7	PA0 to PA7	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7	PE0 to PE7	PE0 to PE7
PORTF	PF5	-	PF5	-
PORTJ	PJ3, PJ5	PJ3	PJ3, PJ5	PJ3
PORTK	PK2 to PK5	-	-	-
PORTL	PL0, PL1	-	-	-

Table 2.31 Comparative Listing of I/O Port Functions (Products with 1 Mbyte of code flash memory or less (RX65N))

Item	Port Symbol	RX63	RX65N
Input pull-up function	PORT0	P00～P07	P00～P07
	PORT1	P10～P17	P12～P17
	PORT2	P20～P27	P20～P27
	PORT3	P30～P34、P36、P37	P30～P34、P36、P37
	PORT4	P40～P47	P40～P47
	PORT5	P50～P57	P50～P56
	PORT6	P60～P67	P60～P67
	PORT7	P70～P77	P70～P77
	PORT8	P80～P87	P80～P83、P86、P87
	PORT9	P90～P97	P90～P93
	PORTA	PA0～PA7	PA0～PA7
	PORTB	PB0～PB7	PB0～PB7
	PORTC	PC0～PC7	PC0～PC7
	PORTD	PD0～PD7	PD0～PD7
	PORTE	PE0～PE7	PE0～PE7
	PORTF	PF0～PF5	PF5
	PORTG	PG0～PG7	—
	PORTH	PH4、PH5	—
	PORTJ	PJ3、PJ5	PJ3、PJ5

Item	Port Symbol	RX63	RX65N
	PORTK	PK0～PK7	—
	PORTL	PL0～PL4	—
Open-drain output	PORT0	P00～P07	P00～P07
	PORT1	P10～P17	P12～P17
	PORT2	P20～P27	P20～P27
	PORT3	P30～P34、P36、P37	P30～P34、P36、P37
	PORT4	P40～P47	P40～P47
	PORT5	P50～P57	P50～P56
	PORT6	P60～P67	P60～P67
	PORT7	P70～P77	P70～P77
	PORT8	P80～P87	P80～P83、P86、P87
	PORT9	P90～P97	P90～P93
	PORTA	PA0～PA7	PA0～PA7
	PORTB	PB0～PB7	PB0～PB7
	PORTC	PC0～PC7	PC0～PC7
	PORTD	PD0～PD7	PD0～PD7
	PORTE	PE0～PE7	PE0～PE7
	PORTF	PF0～PF5	PF5
	PORTG	PG0～PG7	—
	PORTH	PH4、PH5	—
	PORTJ	PJ3、PJ5	PJ3、PJ5
	PORTK	PK0～PK7	—
	PORTL	PL0～PL4	—
Drive capacity switching function	PORT0	P00～P07	P00～P07
	PORT1	P10～P17	P12～P17
	PORT2	P20～P27	P20～P27
	PORT3	P30～P34、P36、P37	P30～P34、P36、P37
	PORT4	P40～P47	P40～P47
	PORT5	P50～P57	P50～P56
	PORT6	P60～P67	P60～P67
	PORT7	P70～P77	P70～P77
	PORT8	P80～P87	P80～P83、P86、P87
	PORT9	P90～P97	P90～P93
	PORTA	PA0～PA7	PA0～PA7
	PORTB	PB0～PB7	PB0～PB7
	PORTC	PC0～PC7	PC0～PC7
	PORTD	PD0～PD7	PD0～PD7
	PORTE	PE0～PE7	PE0～PE7
	PORTF	PF0～PF5	PF5
	PORTG	PG0～PG7	—
	PORTH	PH4、PH5	—
	PORTJ	PJ3、PJ5	PJ3、PJ5
	PORTK	PK0～PK7	—
	PORTL	PL0～PL4	—
5 V tolerant	PORT0	P07	P07
	PORT1	P10～P17	P12～P17
	PORT2	P20～P27	P20～P27
	PORT3	P30～P34、P36、P37	P30～P34、P36、P37

Item	Port Symbol	RX63	RX65N
	PORT4	P40～P47	P40～P47
	PORT5	P50～P57	P50～P56
5 V tolerant	PORT6	P60～P67	P60～P67
	PORT7	P70～P77	P70～P77
	PORT8	P80～P87	P80～P83、P86、P87
	PORT9	P90～P97	P90～P93
	PORTA	PA0～PA7	PA0～PA7
	PORTB	PB0～PB7	PB0～PB7
	PORTC	PC0～PC7	PC0～PC7
	PORTD	PD0～PD7	PD0～PD7
	PORTE	PE0～PE7	PE0～PE7
	PORTF	PF0～PF5	PF5
	PORTG	PG0～PG7	—
	PORTH	PH4、PH5	—
	PORTJ	PJ3、PJ5	PJ3、PJ5
	PORTK	PK0～PK7	—
	PORTL	PL0～PL4	—

Table 2.32 Comparative Listing of I/O Port Functions (Products with at least 1.5 Mbytes of code flash memory (RX65N))

Item	Port Symbol	RX63	RX65N
Input pull-up function	PORT0	P00～P07	P00～P07
	PORT1	P10～P17	P12～P17
	PORT2	P20～P27	P20～P27
	PORT3	P30～P34、P36、P37	P30～P34、P36、P37
	PORT4	P40～P47	P40～P47
	PORT5	P50～P57	P50～P56
	PORT6	P60～P67	P60～P67
	PORT7	P70～P77	P70～P77
	PORT8	P80～P87	P80～P83、P86、P87
	PORT9	P90～P97	P90～P93
	PORTA	PA0～PA7	PA0～PA7
	PORTB	PB0～PB7	PB0～PB7
	PORTC	PC0～PC7	PC0～PC7
	PORTD	PD0～PD7	PD0～PD7
	PORTE	PE0～PE7	PE0～PE7
	PORTF	PF0～PF5	PF5
	PORTG	PG0～PG7	—
	PORTH	PH4、PH5	—
	PORTJ	PJ3、PJ5	PJ3、PJ5
	PORTK	PK0～PK7	—
	PORTL	PL0～PL4	—
Open-drain output	PORT0	P00～P07	P00～P07
	PORT1	P10～P17	P12～P17
	PORT2	P20～P27	P20～P27
	PORT3	P30～P34、P36、P37	P30～P34、P36、P37

Item	Port Symbol	RX63	RX65N
	PORT4	P40～P47	P40～P47
	PORT5	P50～P57	P50～P56
	PORT6	P60～P67	P60～P67
	PORT7	P70～P77	P70～P77
	PORT8	P80～P87	P80～P83、P86、P87
	PORT9	P90～P97	P90～P93
	PORTA	PA0～PA7	PA0～PA7
	PORTB	PB0～PB7	PB0～PB7
	PORTC	PC0～PC7	PC0～PC7
	PORTD	PD0～PD7	PD0～PD7
	PORTE	PE0～PE7	PE0～PE7
	PORTF	PF0～PF5	PF5
	PORTG	PG0～PG7	—
	PORTH	PH4、PH5	—
	PORTJ	PJ3、PJ5	PJ3、PJ5
	PORTK	PK0～PK7	—
	PORTL	PL0～PL4	—
Drive capacity switching function	PORT0	P00～P07	P00～P07
	PORT1	P10～P17	P12～P17
	PORT2	P20～P27	P20～P27
	PORT3	P30～P34、P36、P37	P30～P34、P36、P37
	PORT4	P40～P47	P40～P47
	PORT5	P50～P57	P50～P56
	PORT6	P60～P67	P60～P67
	PORT7	P70～P77	P70～P77
	PORT8	P80～P87	P80～P83、P86、P87
	PORT9	P90～P97	P90～P93
	PORTA	PA0～PA7	PA0～PA7
	PORTB	PB0～PB7	PB0～PB7
	PORTC	PC0～PC7	PC0～PC7
	PORTD	PD0～PD7	PD0～PD7
	PORTE	PE0～PE7	PE0～PE7
	PORTF	PF0～PF5	PF5
	PORTG	PG0～PG7	—
	PORTH	PH4、PH5	—
	PORTJ	PJ3、PJ5	PJ3、PJ5
	PORTK	PK0～PK7	—
	PORTL	PL0～PL4	—
5 V tolerant	PORT0	P07	P07
	PORT1	P10～P17	P12～P17
	PORT2	P20～P27	P20～P27
	PORT3	P30～P34、P36、P37	P30～P34、P36、P37
	PORT4	P40～P47	P40～P47
	PORT5	P50～P57	P50～P56
5 V tolerant	PORT6	P60～P67	P60～P67
	PORT7	P70～P77	P70～P77
	PORT8	P80～P87	P80～P83、P86、P87
	PORT9	P90～P97	P90～P93

Item	Port Symbol	RX63	RX65N
	PORTA	PA0～PA7	PA0～PA7
	PORTB	PB0～PB7	PB0～PB7
	PORTC	PC0～PC7	PC0～PC7
	PORTD	PD0～PD7	PD0～PD7
	PORTE	PE0～PE7	PE0～PE7
	PORTF	PF0～PF5	PF5
	PORTG	PG0～PG7	—
	PORTH	PH4、PH5	—
	PORTJ	PJ3、PJ5	PJ3、PJ5
	PORTK	PK0～PK7	—
	PORTL	PL0～PL4	—

Table 2.33 Comparative Listing of I/O Port Registers

Register	Bit	RX630	RX65N
DSCR2	-	-	Drive Capacity Control Register 2

2.16 Multi-Function Pin Controller

Table 2.34 shows a comparative listing of functions assigned to each multiplexed pin, and Table 2.35 shows a Comparative Listing of Multi-Function Pin Controller Registers.

Blue characters exist only in the RX65N, and orange characters exist only in the RX630. "√" indicates pin implemented, "×" indicates pin not implemented, "-" indicates no assignment pin for function, Grey hatching indicates pin function not implemented.

Table 2.34 Comparative Listing of Functions Assigned to Each Multiplexed Pin

Module/Function	Pin Functions	Allocation Port	RX630			RX65N		
			177 / 176 pin	145 / 144 pin	100 pin	177 / 176 pin	145 / 144 pin	100 pin
Interrupt	NMI (input)	P35	√	√	√	√	√	√
EXDMA controller	EDREQ0 (input)	P22				√	√	√
		P55				√	√	√
		P80				√	√	×
	EDACK0 (output)	P23				√	√	√
		P54				√	√	√
		P81				√	√	×
	EDREQ1 (input)	P24				√	√	√
		P33				√	√	√
		P82				√	√	×
	EDACK1 (output)	P25				√	√	√
		P56				√	√	×
		P83				√	√	×
		PJ3				√	√	√
Interrupt	IRQ0-DS (input)	P30	√	√	√	√	√	√
	IRQ0 (input)	P10	√	×	×	√	×	×
		PD0	√	√	√	√	√	√
	IRQ1-DS (input)	P31	√	√	√	√	√	√
	IRQ1 (input)	P11	√	×	×	√	×	×
		PD1	√	√	√	√	√	√
	IRQ2-DS (input)	P32	√	√	√	√	√	√
	IRQ2 (input)	P12	√	√	√	√	√	√
		PD2	√	√	√	√	√	√
	IRQ3-DS (input)	P33	√	√	√	√	√	√
	IRQ3 (input)	P13	√	√	√	√	√	√
		PD3	√	√	√	√	√	√
	IRQ4-DS (input)	PB1	√	√	√	√	√	√
	IRQ4 (input)	P14	√	√	√	√	√	√
		P34	√	√	√	√	√	√
		PD4	√	√	√	√	√	√
		PF5	√	√	×	√	√	×
	IRQ5-DS (input)	PA4	√	√	√	√	√	√
	IRQ5 (input)	P15	√	√	√	√	√	√
		PD5	√	√	√	√	√	√
		PE5	√	√	√	√	√	√
	IRQ6-DS (input)	PA3	√	√	√	√	√	√
	IRQ6 (input)	P16	√	√	√	√	√	√
		PD6	√	√	√	√	√	√
		PE6	√	√	√	√	√	√

Module/Function	Pin Functions	Allocation Port	RX630			RX65N		
			177 / 176 pin	145 / 144 pin	100 pin	177 / 176 pin	145 / 144 pin	100 pin
Interrupt	IRQ7-DS (input)	PE2	√	√	√	√	√	√
	IRQ7 (input)	P17	√	√	√	√	√	√
		PD7	√	√	√	√	√	√
		PE7	√	√	√	√	√	√
	IRQ8-DS (input)	P40	√	√	√	√	√	√
	IRQ8 (input)	P00	√	√	×	√	√	×
		P20	√	√	√	√	√	√
	IRQ9-DS (input)	P41	√	√	√	√	√	√
	IRQ9 (input)	P01	√	√	×	√	√	×
		P21	√	√	√	√	√	√
	IRQ10-DS (input)	P42	√	√	√	√	√	√
	IRQ10 (input)	P02	√	√	×	√	√	×
		P55	√	√	√	√	√	√
	IRQ11-DS (input)	P43	√	√	√	√	√	√
	IRQ11 (input)	P03	√	√	×	√	√	×
		PA1	√	√	√	√	√	√
	IRQ12-DS (input)	P44	√	√	√	√	√	√
	IRQ12 (input)	PB0	√	√	√	√	√	√
		PC1	√	√	√	√	√	√
	IRQ13-DS (input)	P45	√	√	√	√	√	√
	IRQ13 (input)	P05	√	√	√	√	√	√
		PC6	√	√	√	√	√	√
	IRQ14-DS (input)	P46	√	√	√	√	√	√
	IRQ14 (input)	PC0	√	√	√	√	√	√
		PC7	√	√	√	√	√	√
	IRQ15-DS (input)	P47	√	√	√	√	√	√
	IRQ15 (input)	P07	√	√	√	√	√	√
		P67	√	√	×	√	√	×
RX630: Multi-function timer unit 2 RX65N: Multi-function timer unit 3	MTIOC0A (input/output)	P34	√	√	√	√	√	√
		PB3	√	√	√	√	√	√
	MTIOC0B (input/output)	P13	√	√	√	√	√	√
		P15	√	√	√	√	√	√
		PA1	√	√	√	√	√	√
	MTIOC0C (input/output)	P32	√	√	√	√	√	√
		PB1	√	√	√	√	√	√
	MTIOC0D (input/output)	P33	√	√	√	√	√	√
		PA3	√	√	√	√	√	√
	MTIOC1A (input/output)	P20	√	√	√	√	√	√
		PE4	√	√	√	√	√	√
	MTIOC1B (input/output)	P21	√	√	√	√	√	√
		PB5	√	√	√	√	√	√
	MTIOC2A (input/output)	P26	√	√	√	√	√	√
		PB5	√	√	√	√	√	√
	MTIOC2B (input/output)	P27	√	√	√	√	√	√
		PE5	√	√	√	√	√	√

Module/Function	Pin Functions	Allocation Port	RX630			RX65N		
			177 / 176 pin	145 / 144 pin	100 pin	177 / 176 pin	145 / 144 pin	100 pin
RX630: Multi-function timer unit 2 RX65N: Multi-function timer unit 3	MTIOC3A (input/output)	P14	√	√	√	√	√	√
		P17	√	√	√	√	√	√
		PC1	√	√	√	√	√	√
		PC7	√	√	√	√	√	√
	MTIOC3B (input/output)	P17	√	√	√	√	√	√
		P22	√	√	√	√	√	√
		P80	√	√	×	√	√	×
		PB7	√	√	√	√	√	√
		PC5	√	√	√	√	√	√
		PE1	-	-	-	√	√	√
	MTIOC3C (input/output)	P16	√	√	√	√	√	√
		P56	√	√	×	√	√	×
		PC0	√	√	√	√	√	√
		PC6	√	√	√	√	√	√
		PJ3	√	√	√	√	√	√
	MTIOC3D (input/output)	P16	√	√	√	√	√	√
		P23	√	√	√	√	√	√
		P81	√	√	×	√	√	×
		PB6	√	√	√	√	√	√
		PC4	√	√	√	√	√	√
		PE0	-	-	-	√	√	√
	MTIOC4A (input/output)	P21	-	-	-	√	√	√
		P24	√	√	√	√	√	√
		P82	√	√	×	√	√	×
		PA0	√	√	√	√	√	√
		PB3	√	√	√	√	√	√
		PE2	√	√	√	√	√	√
	MTIOC4B (input/output)	P17	-	-	-	√	√	√
		P30	√	√	√	√	√	√
		P54	√	√	√	√	√	√
		PC2	√	√	√	√	√	√
		PD1	√	√	√	√	√	√
		PE3	√	√	√	√	√	√
	MTIOC4C (input/output)	P25	√	√	√	√	√	√
		P83	√	√	×	√	√	×
		P87	-	-	-	√	√	×
		PB1	√	√	√	√	√	√
		PE1	√	√	√	√	√	√
		PE5	√	√	√	√	√	√
	MTIOC4D (input/output)	P31	√	√	√	√	√	√
		P55	√	√	√	√	√	√
		P86	-	-	-	√	√	×
		PC3	√	√	√	√	√	√
		PD2	√	√	√	√	√	√
		PE4	√	√	√	√	√	√

Module/Function	Pin Functions	Allocation Port	RX630			RX65N		
			177 / 176 pin	145 / 144 pin	100 pin	177 / 176 pin	145 / 144 pin	100 pin
RX630: Multi-function timer unit 2 RX65N: Multi-function timer unit 3	MTIC5U (input)	P12	√	×	×	√	×	×
		PA4	√	√	√	√	√	√
		PD7	√	√	√	√	√	√
	MTIC5V (input)	P11	√	×	×	√	×	×
		PA6	√	√	√	√	√	√
		PD6	√	√	√	√	√	√
	MTIC5W (input)	P10	√	×	×	√	×	×
		PB0	√	√	√	√	√	√
		PD5	√	√	√	√	√	√
	MTIOC6A (input/output)	PE7				√	√	√
		PJ1				√	×	×
	MTIOC6B (input/output)	PA5				√	√	√
		PJ0				√	×	×
	MTIOC6C (input/output)	PE6				√	√	√
		P85				√	×	×
	MTIOC6D (input/output)	PA0				√	√	√
		P84				√	×	×
	MTIOC7A (input/output)	PA2				√	√	√
	MTIOC7B (input/output)	PA1				√	√	√
	MTIOC7C (input/output)	P67				√	√	×
	MTIOC7D (input/output)	P66				√	√	×
	MTIOC8A (input/output)	PD6				√	√	√
	MTIOC8B (input/output)	PD4				√	√	√
	MTIOC8C (input/output)	PD5				√	√	√
	MTIOC8D (input/output)	PD3				√	√	√
	MTCLKA (input)	P14	√	√	√	√	√	√
		P24	√	√	√	√	√	√
		PA4	√	√	√	√	√	√
		PC6	√	√	√	√	√	√
	MTCLKB (input)	P15	√	√	√	√	√	√
		P25	√	√	√	√	√	√
		PA6	√	√	√	√	√	√
		PC7	√	√	√	√	√	√
	MTCLKC (input)	P22	√	√	√	√	√	√
		PA1	√	√	√	√	√	√
		PC4	√	√	√	√	√	√
	MTCLKD (input)	P23	√	√	√	√	√	√
		PA3	√	√	√	√	√	√
		PC5	√	√	√	√	√	√

Module/Function	Pin Functions	Allocation Port	RX630			RX65N		
			177 / 176 pin	145 / 144 pin	100 pin	177 / 176 pin	145 / 144 pin	100 pin
RX630: Port output enable 2 RX65N: Port output enable 3	POE0# (input)	P32	-	-	-	√	√	√
		P93	-	-	-	√	√	×
		PC4	√	√	√	√	√	√
		PD1	-	-	-	√	√	√
		PD7	√	√	√	√	√	√
	POE1# (input)	PB5	√	√	√			
		PD6	√	√	√			
	POE2# (input)	P34	√	√	√			
		PA6	√	√	√			
		PD5	√	√	√			
	POE3# (input)	P33	√	√	√			
		PB3	√	√	√			
		PD4	√	√	√			
	POE4# (input)	P33				√	√	√
		P92				√	√	×
		PB5				√	√	√
		PD0				√	√	√
		PD6				√	√	√
	POE8# (input)	P17	√	√	√	√	√	√
		P30	√	√	√	√	√	√
		PD3	√	√	√	√	√	√
		PE3	√	√	√	√	√	√
		PJ5	-	-	-	√	√	×
	POE10# (input)	P32				√	√	√
		P34				√	√	√
		PA6				√	√	√
		PD5				√	√	√
	POE11# (input)	P33				√	√	√
		PB3				√	√	√
		PD4				√	√	√
16-bit timer pulse unit	TIOCA0 (input/output)	P86	√	√	×	√	√	×
		PA0	√	√	√	√	√	√
	TIOCB0 (input/output)	P17	√	√	√	√	√	√
		PA1	√	√	√	√	√	√
	TIOCC0 (input/output)	P32	√	√	√	√	√	√
		P85	-	-	-	√	×	×
	TIOCD0 (input/output)	P33	√	√	√	√	√	√
		PA3	√	√	√	√	√	√
	TIOCA1 (input/output)	P56	√	√	×	√	√	×
		PA4	√	√	√	√	√	√
	TIOCB1 (input/output)	P16	√	√	√	√	√	√
		PA5	√	√	√	√	√	√
	TIOCA2 (input/output)	P87	√	√	×	√	√	×
		PA6	√	√	√	√	√	√
	TIOCB2 (input/output)	P15	√	√	√	√	√	√
		PA7	√	√	√	√	√	√

Module/Function	Pin Functions	Allocation Port	RX630			RX65N		
			177 / 176 pin	145 / 144 pin	100 pin	177 / 176 pin	145 / 144 pin	100 pin
16-bit timer pulse unit	TIOCA3 (input/output)	P21	√	√	√	√	√	√
		PB0	√	√	√	√	√	√
	TIOCB3 (input/output)	P20	√	√	√	√	√	√
		PB1	√	√	√	√	√	√
	TIOCC3 (input/output)	P22	√	√	√	√	√	√
		PB2	√	√	√	√	√	√
	TIOCD3 (input/output)	P23	√	√	√	√	√	√
		PB3	√	√	√	√	√	√
	TIOCA4 (input/output)	P25	√	√	√	√	√	√
		PB4	√	√	√	√	√	√
	TIOCB4 (input/output)	P24	√	√	√	√	√	√
		PB5	√	√	√	√	√	√
	TIOCA5 (input/output)	P13	√	√	√	√	√	√
		PB6	√	√	√	√	√	√
	TIOCB5 (input/output)	P14	√	√	√	√	√	√
		PB7	√	√	√	√	√	√
	TCLKA (input)	P14	√	√	√	√	√	√
		PC2	√	√	√	√	√	√
	TCLKB (input)	P15	√	√	√	√	√	√
		PA3	√	√	√	√	√	√
		PC3	√	√	√	√	√	√
	TCLKC (input)	P16	√	√	√	√	√	√
		PB2	√	√	√	√	√	√
		PC0	√	√	√	√	√	√
	TCLKD (input)	P17	√	√	√	√	√	√
		PB3	√	√	√	√	√	√
		PC1	√	√	√	√	√	√
	TIOCA6 (input/output)	PC6	√	√	×			
	TIOCB6 (input/output)	PC7	√	√	×			
	TIOCC6 (input/output)	PC4	√	√	×			
	TIOCD6 (input/output)	PC5	√	√	×			
	TIOCA7 (input/output)	PD0	√	√	×			
	TIOCB7 (input/output)	PD1	√	√	×			
	TIOCA8 (input/output)	PD2	√	√	×			
	TIOCB8 (input/output)	PD3	√	√	×			
	TIOCA9 (input/output)	PE2	√	√	×			
	TIOCB9 (input/output)	PE3	√	√	×			

Module/Function	Pin Functions	Allocation Port	RX630			RX65N		
			177 / 176 pin	145 / 144 pin	100 pin	177 / 176 pin	145 / 144 pin	100 pin
16-bit timer pulse unit	TIOCC9 (input/output)	PE0	√	√	×			
	TIOCD9 (input/output)	PE1	√	√	×			
	TIOCA10 (input/output)	PE4	√	√	×			
	TIOCB10 (input/output)	PE5	√	√	×			
	TIOCA11 (input/output)	PE6	√	√	×			
	TIOCB11 (input/output)	PE7	√	√	×			
	TCLKE (input)	PC4	√	√	×			
	TCLKF (input)	PC5	√	√	×			
	TCLKG (input)	PD1	√	√	×			
	TCLKH (input)	PD3	√	√	×			
Programmable pulse generator	PO0 (output)	P20	√	√	√	√	√	√
	PO1 (output)	P21	√	√	√	√	√	√
	PO2 (output)	P22	√	√	√	√	√	√
	PO3 (output)	P23	√	√	√	√	√	√
	PO4 (output)	P24	√	√	√	√	√	√
	PO5 (output)	P25	√	√	√	√	√	√
	PO6 (output)	P26	√	√	√	√	√	√
	PO7 (output)	P27	√	√	√	√	√	√
	PO8 (output)	P30	√	√	√	√	√	√
	PO9 (output)	P31	√	√	√	√	√	√
	PO10 (output)	P32	√	√	√	√	√	√
	PO11 (output)	P33	√	√	√	√	√	√
	PO12 (output)	P34	√	√	√	√	√	√
	PO13 (output)	P13	√	√	√	√	√	√
		P15	√	√	√	√	√	√
	PO14 (output)	P16	√	√	√	√	√	√
	PO15 (output)	P14	√	√	√	√	√	√
		P17	√	√	√	√	√	√
	PO16 (output)	P73	√	√	×	√	√	×
		PA0	√	√	√	√	√	√
	PO17 (output)	PA1	√	√	√	√	√	√
		PC0	√	√	√	√	√	√
	PO18 (output)	PA2	√	√	√	√	√	√
		PC1	√	√	√	√	√	√
		PE1	√	√	√	√	√	√
	PO19 (output)	P74	√	√	×	√	√	×
		PA3	√	√	√	√	√	√
	PO20 (output)	P75	√	√	×	√	√	×
		PA4	√	√	√	√	√	√
	PO21 (output)	PA5	√	√	√	√	√	√
		PC2	√	√	√	√	√	√

Module/Function	Pin Functions	Allocation Port	RX630			RX65N		
			177 / 176 pin	145 / 144 pin	100 pin	177 / 176 pin	145 / 144 pin	100 pin
Programmable pulse generator	PO22 (output)	P76	√	√	×	√	√	×
		PA6	√	√	√	√	√	√
	PO23 (output)	P77	√	√	×	√	√	×
		PA7	√	√	√	√	√	√
		PE2	√	√	√	√	√	√
	PO24 (output)	PB0	√	√	√	√	√	√
		PC3	√	√	√	√	√	√
	PO25 (output)	PB1	√	√	√	√	√	√
		PC4	√	√	√	√	√	√
	PO26 (output)	P80	√	√	×	√	√	×
		PB2	√	√	√	√	√	√
		PE3	√	√	√	√	√	√
	PO27 (output)	P81	√	√	×	√	√	×
		PB3	√	√	√	√	√	√
	PO28 (output)	P82	√	√	×	√	√	×
		PB4	√	√	√	√	√	√
		PE4	√	√	√	√	√	√
	PO29 (output)	PB5	√	√	√	√	√	√
		PC5	√	√	√	√	√	√
	PO30 (output)	PB6	√	√	√	√	√	√
		PC6	√	√	√	√	√	√
	PO31 (output)	PB7	√	√	√	√	√	√
		PC7	√	√	√	√	√	√
8-bit timer	TMO0 (output)	P22	√	√	√	√	√	√
		PB3	√	√	√	√	√	√
	TMCI0 (input)	P01	√	√	×	√	√	×
		P21	√	√	√	√	√	√
		PB1	√	√	√	√	√	√
	TMRI0 (input)	P00	√	√	×	√	√	×
		P20	√	√	√	√	√	√
		PA4	√	√	√	√	√	√
	TMO1 (output)	P17	√	√	√	√	√	√
		P26	√	√	√	√	√	√
	TMCI1 (input)	P02	√	√	×	√	√	×
		P12	√	√	√	√	√	√
		P54	√	√	√	√	√	√
		PC4	√	√	√	√	√	√
	TMRI1 (input)	P24	√	√	√	√	√	√
		PB5	√	√	√	√	√	√
	TMO2 (output)	P16	√	√	√	√	√	√
		PC7	√	√	√	√	√	√
	TMCI2 (input)	P15	√	√	√	√	√	√
		P31	√	√	√	√	√	√
		PC6	√	√	√	√	√	√
	TMRI2 (input)	P14	√	√	√	√	√	√
		PC5	√	√	√	√	√	√

Module/Function	Pin Functions	Allocation Port	RX630			RX65N		
			177 / 176 pin	145 / 144 pin	100 pin	177 / 176 pin	145 / 144 pin	100 pin
8-bit timer	TMO3 (output)	P13	√	√	√	√	√	√
		P32	√	√	√	√	√	√
		P55	√	√	√	√	√	√
	TMCI3 (input)	P11	√	×	×	√	×	×
		P27	√	√	√	√	√	√
		P34	√	√	√	√	√	√
		PA6	√	√	√	√	√	√
	TMRI3 (input)	P10	√	×	×	√	×	×
		P30	√	√	√	√	√	√
		P33	√	√	√	√	√	√
Compare match timer W	TOC0 (output)	PC7				√	√	√
	TIC0 (input)	PC6				√	√	√
	TOC1 (output)	PE7				√	√	√
	TIC1 (input)	PE6				√	√	√
	TOC2 (output)	PD3				√	√	√
	TIC2 (input)	PD2				√	√	√
	TOC3 (output)	PE3				√	√	√
	TIC3 (input)	PE2				√	√	√
Ethernet controller	REF50CK0 (input)	P76				√	√	×
		PB2				√	√	√
		PE5				√	√	√
	RMII0_CRS_DV (input)	P83				√	√	×
		PB7				√	√	√
	RMII0_TXD0 (output)	P81				√	√	×
		PB5				√	√	√
	RMII0_TXD1 (output)	P82				√	√	×
		PB6				√	√	√
	RMII0_RXD0 (input)	P75				√	√	×
		PB1				√	√	√
	RMII0_RXD1 (input)	P74				√	√	×
		PB0				√	√	√
	RMII0_TXD_EN (output)	P80				√	√	×
		PA0				√	√	√
		PB4				√	√	√
	RMII0_RX_ER (input)	P77				√	√	×
		PB3				√	√	√
	ET0_CRS (input)	P83				√	√	×
		PB7				√	√	√
	ET0_RX_DV (input)	PC2				√	√	√
	ET0_EXOUT (output)	P55				√	√	√
		PA6				√	√	√
		PJ3				√	√	√
	ET0_LINKSTA (input)	P34				√	√	√
		P54				√	√	√
		PA5				√	√	√

Module/Function	Pin Functions	Allocation Port	RX630			RX65N		
			177 / 176 pin	145 / 144 pin	100 pin	177 / 176 pin	145 / 144 pin	100 pin
Ethernet controller	ET0_ETXD0 (output)	P81				√	√	×
		PB5				√	√	√
	ET0_ETXD1 (output)	P82				√	√	×
		PB6				√	√	√
	ET0_ETXD2 (output)	PC5				√	√	√
	ET0_ETXD3 (output)	PC6				√	√	√
	ET0_ERXD0 (input)	P75				√	√	×
		PB1				√	√	√
	ET0_ERXD1 (input)	P74				√	√	×
		PB0				√	√	√
	ET0_ERXD2 (input)	PC1				√	√	√
		PE4				√	√	√
	ET0_ERXD3 (input)	PC0				√	√	√
		PE3				√	√	√
	ET0_TX_EN (output)	P80				√	√	×
		PA0				√	√	√
		PB4				√	√	√
	ET0_TX_ER (output)	PC3				√	√	√
	ET0_RX_ER (input)	P77				√	√	×
		PB3				√	√	√
	ET0_TX_CLK (input)	PC4				√	√	√
	ET0_RX_CLK (input)	P76				√	√	×
		PB2				√	√	√
		PE5				√	√	√
	ET0_COL (input)	PC7				√	√	√
	ET0_WOL (output)	P73				√	√	×
		PA1				√	√	√
		PA7				√	√	√
	ET0_MDC (output)	P72				√	√	×
		PA4				√	√	√
	ET0_MDIO (input/output)	P71				√	√	×
		PA3				√	√	√
Serial communications interface	RXD0 (input)/ SMISO0 (input/output)/ SSCL0 (input/output)	P21	√	√	√	√	√	√
		P33	√	√	√	√	√	√
	TXD0 (output)/ SMOSI0 (input/output)/ SSDA0 (input/output)	P20	√	√	√	√	√	√
		P32	√	√	√	√	√	√
	SCK0 (input/output)	P22	√	√	√	√	√	√
		P34	√	√	√	√	√	√

Module/Function	Pin Functions	Allocation Port	RX630			RX65N		
			177 / 176 pin	145 / 144 pin	100 pin	177 / 176 pin	145 / 144 pin	100 pin
Serial communications interface	CTS0# (input)/ RTS0# (output)/ SS0# (input)	P23	√	√	√	√	√	√
		PJ3	√	√	√	√	√	√
	RXD1 (input)/ SMISO1 (input/output)/ SSCL1 (input/output)	P15	√	√	√	√	√	√
		P30	√	√	√	√	√	√
		PF2	√	×	×	√	×	×
	TXD1 (output)/ SMOSI1 (input/output)/ SSDA1 (input/output)	P16	√	√	√	√	√	√
		P26	√	√	√	√	√	√
		PF0	√	×	×	√	×	×
	SCK1 (input/output)	P17	√	√	√	√	√	√
		P27	√	√	√	√	√	√
		PF1	√	×	×	√	×	×
	CTS1# (input)/ RTS1# (output)/ SS1# (input)	P14	√	√	√	√	√	√
		P31	√	√	√	√	√	√
	RXD2 (input)/ SMISO2 (input/output)/ SSCL2 (input/output)	P12	√	√	√	√	√	√
		P52	√	√	√	√	√	√
	TXD2 (output)/ SMOSI2 (input/output)/ SSDA2 (input/output)	P13	√	√	√	√	√	√
		P50	√	√	√	√	√	√
	SCK2 (input/output)	P11	√	×	×	√	×	×
		P51	√	√	√	√	√	√
	CTS2# (input)/ RTS2# (output)/ SS2# (input)	P54	√	√	√	√	√	√
		PJ5	-	-	-	√	√	×
	RXD3 (input)/ SMISO3 (input/output)/ SSCL3 (input/output)	P16	√	√	√	√	√	√
		P25	√	√	√	√	√	√
	TXD3 (output)/ SMOSI3 (input/output)/ SSDA3 (input/output)	P17	√	√	√	√	√	√
		P23	√	√	√	√	√	√
	SCK3 (input/output)	P15	√	√	√	√	√	√
		P24	√	√	√	√	√	√
	CTS3# (input)/ RTS3# (output)/ SS3# (input)	P26	√	√	√	√	√	√

Module/Function	Pin Functions	Allocation Port	RX630			RX65N		
			177 / 176 pin	145 / 144 pin	100 pin	177 / 176 pin	145 / 144 pin	100 pin
Serial communications interface	RXD4 (input)/ SMISO4 (input/output)/ SSCL4 (input/output)	PB0	√	√	×	√	√	×
		PK4	√	√	×	-	-	-
	TXD4 (output)/ SMOSI4 (input/output)/ SSDA4 (input/output)	PB1	√	√	×	√	√	×
		PK5	√	√	×	-	-	-
	SCK4 (input/output)	P70	√	√	×	-	-	-
		PB3	√	√	×	√	√	×
	CTS4# (input)/ RTS4# (output)/ SS4# (input)	PB2	√	√	×	√	√	×
		PE6	√	√	×	-	-	-
	RXD5 (input)/ SMISO5 (input/output)/ SSCL5 (input/output)	PA2	√	√	√	√	√	√
		PA3	√	√	√	√	√	√
		PC2	√	√	√	√	√	√
	TXD5 (output)/ SMOSI5 (input/output)/ SSDA5 (input/output)	PA4	√	√	√	√	√	√
		PC3	√	√	√	√	√	√
	SCK5 (input/output)	PA1	√	√	√	√	√	√
		PC1	√	√	√	√	√	√
		PC4	√	√	√	√	√	√
	CTS5# (input)/ RTS5# (output)/ SS5# (input)	PA6	√	√	√	√	√	√
		PC0	√	√	√	√	√	√
	RXD6 (input)/ SMISO6 (input/output)/ SSCL6 (input/output)	P01	√	√	×	√	√	×
		P33	√	√	√	√	√	√
		PB0	√	√	√	√	√	√
	TXD6 (output)/ SMOSI6 (input/output)/ SSDA6 (input/output)	P00	√	√	×	√	√	×
		P32	√	√	√	√	√	√
		PB1	√	√	√	√	√	√
	SCK6 (input/output)	P02	√	√	×	√	√	×
		P34	√	√	√	√	√	√
		PB3	√	√	√	√	√	√
	CTS6# (input)/ RTS6# (output)/ SS6# (input)	PB2	√	√	√	√	√	√
		PJ3	√	√	√	√	√	√

Module/Function	Pin Functions	Allocation Port	RX630			RX65N		
			177 / 176 pin	145 / 144 pin	100 pin	177 / 176 pin	145 / 144 pin	100 pin
Serial communications interface	RXD7 (input)/ SMISO7 (input/output)/ SSCL7 (input/output)	P57	-	-	-	√	×	×
		P92	√	√	×	√	√	×
	TXD7 (output)/ SMOSI7 (input/output)/ SSDA7 (input/output)	P55	-	-	-	√	√	×
		P90	√	√	×	√	√	×
	SCK7 (input/output)	P56	-	-	-	√	√	×
		P91	√	√	×	√	√	×
	CTS7# (input)/ RTS7# (output)/ SS7# (input)	P93	√	√	×	√	√	×
	RXD8 (input)/ SMISO8 (input/output)/ SSCL8 (input/output)	PC6	√	√	√	√	√	√
		PJ1	-	-	-	√	×	×
	TXD8 (output)/ SMOSI8 (input/output)/ SSDA8 (input/output)	PC7	√	√	√	√	√	√
		PJ2	-	-	-	√	×	×
	SCK8 (input/output)	PC5	√	√	√	√	√	√
		PJ0	-	-	-	√	×	×
	CTS8# (input)/ RTS8# (output)/ SS8# (input)	PC4	√	√	√	√	√	√
	RXD9 (input)/ SMISO9 (input/output)/ SSCL9 (input/output)	PB6	√	√	√	√	√	√
		PK3	√	√	×	-	-	-
	TXD9 (output)/ SMOSI9 (input/output)/ SSDA9 (input/output)	PB7	√	√	√	√	√	√
		PK2	√	√	×	-	-	-
	SCK9 (input/output)	P60	√	√	×	-	-	-
		PB5	√	√	√	√	√	√
	CTS9# (input)/ RTS9# (output)/ SS9# (input)	P61	√	√	×	-	-	-
		PB4	√	√	√	√	√	√

Module/Function	Pin Functions	Allocation Port	RX630			RX65N		
			177 / 176 pin	145 / 144 pin	100 pin	177 / 176 pin	145 / 144 pin	100 pin
Serial communications interface	RXD10 (input)/ SMISO10 (input/output)/ SSCL10 (input/output)	P81	√	√	×	√	√	×
		P86	-	-	-	√	√	×
		PC6	-		-	√	√	√
	TXD10 (output)/ SMOSI10 (input/output)/ SSDA10 (input/output)	P82	√	√	×	√	√	×
		P87	-	-	-	√	√	×
		PC7	-	-	-	√	√	√
	SCK10 (input/output)	P80	√	√	×	√	√	×
		P83	-	-	-	√	√	×
		PC5	-	-	-	√	√	√
	RTS10# (output)	P80				√	√	×
	CTS10# (input)/ SS10# (input)	P83				√	√	×
	CTS10# (input)/ RTS10# (output)/ SS10# (input)	P83	√	√	×	-	-	-
		PC4	-	-	-	√	√	√
	RXD11 (input)/ SMISO11 (input/output)/ SSCL11 (input/output)	P76	√	√	×	√	√	×
		PB6	-	-	-	√	√	√
	TXD11 (output)/ SMOSI11 (input/output)/ SSDA11 (input/output)	P77	√	√	×	√	√	×
		PB7	-	-	-	√	√	√
	SCK11 (input/output)	P75	√	√	×	√	√	×
		PB5	-	-	-	√	√	√
	RTS11# (output)	P75				√	√	×
	CTS11# (input)/ SS11# (input)	P74				√	√	×
	CTS11# (input)/ RTS11# (output)/ SS11# (input)	P74	√	√	×	-	-	-
		PB4	-	-	-	√	√	√
	RXD12 (input)/ SMISO12 (input/output)/ SSCL12 (input/output)/ RXDX12 (input)	PE2	√	√	√	√	√	√

Module/Function	Pin Functions	Allocation Port	RX630			RX65N		
			177 / 176 pin	145 / 144 pin	100 pin	177 / 176 pin	145 / 144 pin	100 pin
Serial communications interface	TXD12 (output)/ SMOSI12 (input/output)/ SSDA12 (input/output)/ TXDX12 (output)/ SIOX12 (input/output)	PE1	√	√	√	√	√	√
	SCK12 (input/output)	PE0	√	√	√	√	√	√
	CTS12# (input)/ RTS12# (output)/ SS12# (input)	PE3	√	√	√	√	√	√
I2C bus interface	SCL0[FM+] (input/output)	P12	√	√	√	√	√	√
	SDA0[FM+] (input/output)	P13	√	√	√	√	√	√
	SCL1 (input/output)	P21	√	√	×	√	√	×
	SDA1 (input/output)	P20	√	√	×	√	√	×
	SCL2-DS (input/output)	P16	√	√	√	√	√	√
	SDA2-DS (input/output)	P17	√	√	√	√	√	√
	SCL3 (input/output)	PC0	√	√	×			
	SDA3 (input/output)	PC1	√	√	×			
RX630: USB 2.0 Function RX65N: USB 2.0FS host/function module	USB0_DPUPE (output)	P14	√	√	√			
	USB0_VBUS (input)	P16	√	√	√	√	√	√
	USB0_EXICEN (output)	P21				√	√	√
	USB0_VBUSEN (output)	P16				√	√	√
		P24				√	√	√
		P32				√	√	√
	USB0_OVRCURA (input)	P14				√	√	√
	USB0_OVRCURB (input)	P16				√	√	√
		P22				√	√	√
	USB0_ID (input)	P20				√	√	√
CAN module	CRX0 (input)	P33	√	√	√	√	√	√
		PD2	√	√	√	√	√	√
	CTX0 (output)	P32	√	√	√	√	√	√
		PD1	√	√	√	√	√	√
	CRX1-DS (input)	P15	√	√	√	√	√	√
	CRX1 (input)	P55	√	√	√	√	√	√
	CTX1 (output)	P14	√	√	√	√	√	√
		P54	√	√	√	√	√	√
	CRX2 (input)	P67	√	√	×			
	CTX2 (output)	P66	√	√	×			

Module/Function	Pin Functions	Allocation Port	RX630			RX65N		
			177 / 176 pin	145 / 144 pin	100 pin	177 / 176 pin	145 / 144 pin	100 pin
Serial peripheral interface	RSPCKA (input/output)	PA5	√	√	√	√	√	√
		PB0	√	√	√	-	-	-
		PC5	√	√	√	√	√	√
	MOSIA (input/output)	P16	√	√	√	-	-	-
		PA6	√	√	√	√	√	√
		PC6	√	√	√	√	√	√
	MISOA (input/output)	P17	√	√	√	-	-	-
		PA7	√	√	√	√	√	√
		PC7	√	√	√	√	√	√
	SSLA0 (input/output)	PA4	√	√	√	√	√	√
		PC4	√	√	√	√	√	√
	SSLA1 (output)	PA0	√	√	√	√	√	√
		PC0	√	√	√	√	√	√
	SSLA2 (output)	PA1	√	√	√	√	√	√
		PC1	√	√	√	√	√	√
	SSLA3 (output)	PA2	√	√	√	√	√	√
		PC2	√	√	√	√	√	√
	RSPCKB (input/output)	P27	√	√	√	√	√	√
		PE1	√	√	√	-	-	-
		PE5	√	√	√	√	√	√
	MOSIB (input/output)	P26	√	√	√	√	√	√
		PE2	√	√	√	-	-	-
		PE6	√	√	√	√	√	√
	MISOB (input/output)	P30	√	√	√	√	√	√
		PE3	√	√	√	-	-	-
		PE7	√	√	√	√	√	√
	SSLB0 (input/output)	P31	√	√	√	√	√	√
		PE4	√	√	√	√	√	√
	SSLB1 (output)	P50	√	√	√	√	√	√
		PE0	√	√	√	√	√	√
	SSLB2 (output)	P51	√	√	√	√	√	√
		PE1	√	√	√	√	√	√
	SSLB3 (output)	P52	√	√	√	√	√	√
		PE2	√	√	√	√	√	√
	RSPCKC (input/output)	P56	-	-	-	√	×	×
		PD3	√	√	×	√	√	√
	MOSIC (input/output)	P54	-	-	-	√	×	×
		PD1	√	√	×	√	√	√
	MISOC (input/output)	P55	-	-	-	√	×	×
		PD2	√	√	×	√	√	√
	SSLC0 (input/output)	P57	-	-	-	√	×	×
		PD4	√	√	×	√	√	√
	SSLC1 (output)	PD5	√	√	×	√	√	√
		PJ0	-	-	-	√	×	×
	SSLC2 (output)	PD6	√	√	×	√	√	√
		PJ1	-	-	-	√	×	×

Module/Function	Pin Functions	Allocation Port	RX630			RX65N		
			177 / 176 pin	145 / 144 pin	100 pin	177 / 176 pin	145 / 144 pin	100 pin
Serial peripheral interface	SSLC3 (output)	PD7	√	√	×	√	√	√
		PJ2	-	-	-	√	×	×
IEBus controller	IERXD (input)	P16	√	√	√			
		PC2	√	√	√			
	IETXD (output)	P17	√	√	√			
		PC3	√	√	√			
Realtime clock	RTCOUT (output)	P16	√	√	√	√	√	√
		P32	√	√	√	√	√	√
	RTCIC0 (input)	P30	√	√	√	√	√	√
	RTCIC1 (input)	P31	√	√	√	√	√	√
	RTCIC2 (input)	P32	√	√	√	√	√	√
12-bit A/D converter	AN000 (input)	P40	√	√	√	√	√	√
	AN001 (input)	P41	√	√	√	√	√	√
	AN002 (input)	P42	√	√	√	√	√	√
	AN003 (input)	P43	√	√	√	√	√	√
	AN004 (input)	P44	√	√	√	√	√	√
	AN005 (input)	P45	√	√	√	√	√	√
	AN006 (input)	P46	√	√	√	√	√	√
	AN007 (input)	P47	√	√	√	√	√	√
	AN008 (input)	PD0	√	√	√			
	AN009 (input)	PD1	√	√	√			
	AN010 (input)	PD2	√	√	√			
	AN011 (input)	PD3	√	√	√			
	AN012 (input)	PD4	√	√	√			
	AN013 (input)	PD5	√	√	√			
	AN014 (input)	P90	√	√	×			
	AN015 (input)	P91	√	√	×			
	AN016 (input)	P92	√	√	×			
	AN017 (input)	P93	√	√	×			
	AN018 (input)	P00	√	√	×			
	AN019 (input)	P01	√	√	×			
	AN020 (input)	P02	√	√	×			
	ADTRG0# (input)	P07	√	√	√	√	√	√
		P16	√	√	√	√	√	√
		P25	√	√	√	√	√	√
	AN100 (input)	PE2				√	√	√
	AN101 (input)	PE3				√	√	√
	AN102 (input)	PE4				√	√	√
	AN103 (input)	PE5				√	√	√
	AN104 (input)	PE6				√	√	√
	AN105 (input)	PE7				√	√	√
	AN106 (input)	PD6				√	√	√
	AN107 (input)	PD7				√	√	√
	AN108 (input)	PD0				√	√	√
	AN109 (input)	PD1				√	√	√
	AN110 (input)	PD2				√	√	√

Module/Function	Pin Functions	Allocation Port	RX630			RX65N		
			177 / 176 pin	145 / 144 pin	100 pin	177 / 176 pin	145 / 144 pin	100 pin
12-bit A/D converter	AN111 (input)	PD3				√	√	√
	AN112 (input)	PD4				√	√	√
	AN113 (input)	PD5				√	√	√
	AN114 (input)	P90				√	√	×
	AN115 (input)	P91				√	√	×
	AN116 (input)	P92				√	√	×
	AN117 (input)	P93				√	√	×
	AN118 (input)	P00				√	√	×
	AN119 (input)	P01				√	√	×
	AN120 (input)	P02				√	√	×
	ADTRG1# (input)	P13				√	√	√
		P17				√	√	√
10-bit A/D converter	AN0 (input)	PE2	√	√	√			
	AN1 (input)	PE3	√	√	√			
	AN2 (input)	PE4	√	√	√			
	AN3 (input)	PE5	√	√	√			
	AN4 (input)	PE6	√	√	√			
	AN5 (input)	PE7	√	√	√			
	AN6 (input)	PD6	√	√	√			
	AN7 (input)	PD7	√	√	√			
	ADTRG# (input)	P13	√	√	√			
		P17	√	√	√			
RX630: 12-bit A/D converter RX65N: 10-bit A/D converter	ANEX0 (output)	PE0	√	√	√	√	√	√
	ANEX1 (input)	PE1	√	√	√	√	√	√
RX630: 12-bit D/A converter RX65N: 10-bit D/A converter	DA0 (output)	P03	√	√	×	√	√	×
	DA1 (output)	P05	√	√	√	√	√	√
Parallel data capture unit	PIXCLK (input)	P24				√	√	×
	VSYNC (input)	P32				√	√	×
	HSYNC (input)	P25				√	√	×
	PIXD0 (input)	P15				√	√	×
	PIXD1 (input)	P86				√	√	×
	PIXD2 (input)	P87				√	√	×
	PIXD3 (input)	P17				√	√	×
	PIXD4 (input)	P20				√	√	×
	PIXD5 (input)	P21				√	√	×
	PIXD6 (input)	P22				√	√	×
	PIXD7 (input)	P23				√	√	×
	PCKO (output)	P33				√	√	×
MMC host interface	MMC_RES# (output)	P75				√	√	×
		PE7				√	√	√
	MMC_CLK (output)	P77				√	√	×
		PD5				√	√	√

Module/Function	Pin Functions	Allocation Port	RX630			RX65N		
			177 / 176 pin	145 / 144 pin	100 pin	177 / 176 pin	145 / 144 pin	100 pin
MMC host interface	MMC_CD (input)	PC2				√	√	×
		PE6				√	√	√
	MMC_CMD (input/output)	P76				√	√	×
		PD4				√	√	√
	MMC_D0 (input/output)	PC3				√	√	×
		PD6				√	√	√
	MMC_D1 (input/output)	PC4				√	√	×
		PD7				√	√	√
	MMC_D2 (input/output)	P80				√	√	×
		PD2				√	√	√
	MMC_D3 (input/output)	P81				√	√	×
		PD3				√	√	√
	MMC_D4 (input/output)	P82				√	√	×
		PE0				√	√	√
	MMC_D5 (input/output)	PC5				√	√	×
		PE1				√	√	√
	MMC_D6 (input/output)	PC6				√	√	×
		PE2				√	√	√
	MMC_D7 (input/output)	PC7				√	√	×
		PE3				√	√	√
SD host interface	SDHI_CLK (output)	P21				√	√	×
		P77				√	√	×
		PD5				√	√	√
	SDHI_CMD (input/output)	P20				√	√	×
		P76				√	√	×
		PD4				√	√	√
	SDHI_CD (input)	P25				√	√	×
		P81				√	√	×
		PE6				√	√	√
	SDHI_WP (input)	P24				√	√	×
		P80				√	√	×
		PE7				√	√	√
	SDHI_D0 (input/output)	P22				√	√	×
		PC3				√	√	×
		PD6				√	√	√
	SDHI_D1 (input/output)	P23				√	√	×
		PC4				√	√	×
		PD7				√	√	√
	SDHI_D2 (input/output)	P75				√	√	×
		P87				√	√	×
		PD2				√	√	√
	SDHI_D3 (input/output)	P17				√	√	×
		PC2				√	√	×
		PD3				√	√	√
SD slave interface	SDSI_CLK (input)	P77				√	√	×
		PB5				√	√	√

Module/Function	Pin Functions	Allocation Port	RX630			RX65N		
			177 / 176 pin	145 / 144 pin	100 pin	177 / 176 pin	145 / 144 pin	100 pin
SD slave interface	SDSI_CMD (input/output)	P76				√	√	×
		PB4				√	√	√
	SDSI_D0 (input/output)	PC3				√	√	×
		PB6				√	√	√
	SDSI_D1 (input/output)	PC4				√	√	×
		PB7				√	√	√
	SDSI_D2 (input/output)	P75				√	√	×
		PB2				√	√	√
	SDSI_D3 (input/output)	PC2				√	√	×
		PB3				√	√	√
Clock frequency accuracy measurement circuit	CACREF (input)	PC7				√	√	√
		PA0				√	√	√
Quad serial peripheral interface	QSPCLK (input/output)	P77				√	√	×
		PD5				√	√	√
	QSSL (input/output)	P76				√	√	×
		PD4				√	√	√
	QMO/QIO0 (input/output)	PC3				√	√	×
		PD6				√	√	√
	QMI/QIO1 (input/output)	PC4				√	√	×
		PD7				√	√	√
	QIO2 (input/output)	P80				√	√	×
		PD2				√	√	√
	QIO3 (input/output)	P81				√	√	×
		PD3				√	√	√
LCD control	LCD_EXTCLK (input)*1	P73				√	×	×
		PD0				√	√	√
	LCD_CLK (output) *1	P14				√	×	×
		PB5				√	√	√
	LCD_TCON0 (output) *1	P13				√	×	×
		PB4				√	√	√
	LCD_TCON1 (output) *1	P12				√	×	×
		PB3				√	√	√
	LCD_TCON2 (output) *1	PB2				√	√	√
		PJ2				√	×	×
	LCD_TCON3 (output) *1	PB1				√	√	√
		PJ1				√	×	×
	LCD_DATA0 (output) *1	PB0				√	√	√
		PJ0				√	×	×
	LCD_DATA1 (output) *1	P85				√	×	×
		PA7				√	√	√
	LCD_DATA2 (output) *1	P84				√	×	×
		PA6				√	√	√
	LCD_DATA3 (output) *1	P57				√	×	×
		PA5				√	√	√
	LCD_DATA4 (output) *1	P56				√	×	×
		PA4				√	√	√

Module/Function	Pin Functions	Allocation Port	RX630			RX65N		
			177 / 176 pin	145 / 144 pin	100 pin	177 / 176 pin	145 / 144 pin	100 pin
LCD control	LCD_DATA5 (output) *1	P55				√	×	×
		PA3				√	√	√
	LCD_DATA6 (output) *1	P54				√	×	×
		PA2				√	√	√
	LCD_DATA7 (output) *1	P11				√	×	×
		PA1				√	√	√
	LCD_DATA8 (output) *1	P83				√	×	×
		PA0				√	√	√
	LCD_DATA9 (output) *1	PC7				√	×	×
		PE7				√	√	√
	LCD_DATA10 (output) *1	PC6				√	×	×
		PE6				√	√	√
	LCD_DATA11 (output) *1	PC5				√	×	×
		PE5				√	√	√
	LCD_DATA12 (output) *1	P82				√	×	×
		PE4				√	√	√
	LCD_DATA13 (output) *1	P81				√	×	×
		PE3				√	√	√
	LCD_DATA14 (output) *1	P80				√	×	×
		PE2				√	√	√
	LCD_DATA15 (output) *1	PC4				√	×	×
		PE1				√	√	√
	LCD_DATA16 (output) *1	PC3				√	×	×
		PE0				√	√	√
	LCD_DATA17 (output) *1	P77				√	×	×
		PD7				√	√	√
	LCD_DATA18 (output) *1	P76				√	×	×
		PD6				√	√	√
	LCD_DATA19 (output) *1	PC2				√	×	×
		PD5				√	√	√
	LCD_DATA20 (output) *1	P75				√	×	×
		PD4				√	√	√
	LCD_DATA21 (output) *1	P74				√	×	×
		PD3				√	√	√
	LCD_DATA22 (output) *1	PC1				√	×	×
		PD2				√	√	√
	LCD_DATA23 (output) *1	P72				√	×	×
		PD1				√	√	√

*1: Can be used for products with at least 1.5 Mbytes of code flash memory.

Table 2.35 Comparative Listing of Multi-Function Pin Controller Registers

Register	Bit	RX630 (MPC)	RX65N (MPC)
P0nPFS	PSEL	Pin Function Select (PSEL[4:0]) b4-b0	Pin Function Select (PSEL[5:0]) b5-b0
	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P00: IRQ8 (177/176/145/144 pin) P01: IRQ9 (177/176/145/144 pin) P02: IRQ10 (177/176/145/144 pin) P03: IRQ11 (177/176/145/144 pin) P05: IRQ13 (177/176/145/144/100/80 pin) P07: IRQ15 (177/176/145/144/100/80 pin)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P00: IRQ8 (177/176/145/144 pin) P01: IRQ9 (177/176/145/144 pin) P02: IRQ10 (177/176/145/144 pin) P03: IRQ11 (177/176/145/144 pin) P05: IRQ13 (177/176/145/144/100 pin) P07: IRQ15 (177/176/145/144/100 pin)
	ASEL	Analog Input Function Select 0: Used other than as analog pin. 1: Used as analog pin. P00: AN018 (177/176/145/144 pin) P01: AN019 (177/176/145/144 pin) P02: AN020 (177/176/145/144 pin) P03: DA0 (177/176/145/144 pin) P05: DA1 (177/176/145/144/100/80 pin)	Analog Function Select 0: Used other than as analog pin. 1: Used as analog pin. P00: AN118 (177/176/145/144 pin) P01: AN119 (177/176/145/144 pin) P02: AN120 (177/176/145/144 pin) P03: DA0 (177/176/145/144 pin) P05: DA1 (177/176/145/144/100 pin)
P1nPFS	PSEL	Pin Function Select (PSEL[4:0]) b4-b0	Pin Function Select (PSEL[5:0]) b5-b0
	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P10: IRQ0 (177/176 pin) P11: IRQ1 (177/176 pin) P12: IRQ2 (177/176/145/144/100/80 pin) P13: IRQ3 (177/176/145/144/100/80 pin) P14: IRQ4 (177/176/145/144/100/80 pin) P15: IRQ5 (177/176/145/144/100/80 pin) P16: IRQ6 (177/176/145/144/100/80 pin) P17: IRQ7 (177/176/145/144/100/80 pin)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P10: IRQ0 (177/176 pin) P11: IRQ1 (177/176 pin) P12: IRQ2 (177/176/145/144/100 pin) P13: IRQ3 (177/176/145/144/100 pin) P14: IRQ4 (177/176/145/144/100 pin) P15: IRQ5 (177/176/145/144/100 pin) P16: IRQ6 (177/176/145/144/100 pin) P17: IRQ7 (177/176/145/144/100 pin)
P2nPFS	PSEL	Pin Function Select (PSEL[4:0]) b4-b0	Pin Function Select (PSEL[5:0]) b5-b0

Register	Bit	RX630 (MPC)	RX65N (MPC)
P2nPFS	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P20: IRQ8 (177/176/145/144/100/80 pin) P21: IRQ9 (177/176/145/144/100/80 pin)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P20: IRQ8 (177/176/145/144/100 pin) P21: IRQ9 (177/176/145/144/100 pin)
P3nPFS	PSEL	Pin Function Select (PSEL[4:0]) b4-b0	Pin Function Select (PSEL[5:0]) b5-b0
	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0-DS (177/176/145/144/100/80 pin) P31: IRQ1-DS (177/176/145/144/100/80 pin) P32: IRQ2-DS (177/176/145/144/100/80 pin) P33: IRQ3-DS (177/176/145/144/100 pin) P34: IRQ4 (177/176/145/144/100/80 pin)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0-DS (177/176/145/144/100 pin) P31: IRQ1-DS (177/176/145/144/100 pin) P32: IRQ2-DS (177/176/145/144/100 pin) P33: IRQ3-DS (177/176/145/144/100 pin) P34: IRQ4 (177/176/145/144/100 pin)
P4nPFS	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P40: IRQ8-DS (177/176/145/144/100/80 pin) P41: IRQ9-DS (177/176/145/144/100/80 pin) P42: IRQ10-DS (177/176/145/144/100/80 pin) P43: IRQ11-DS (177/176/145/144/100/80 pin) P44: IRQ12-DS (177/176/145/144/100/80 pin) P45: IRQ13-DS (177/176/145/144/100/80 pin) P46: IRQ14-DS (177/176/145/144/100/80 pin) P47: IRQ15-DS (177/176/145/144/100/80 pin)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P40: IRQ8-DS (177/176/145/144/100 pin) P41: IRQ9-DS (177/176/145/144/100 pin) P42: IRQ10-DS (177/176/145/144/100 pin) P43: IRQ11-DS (177/176/145/144/100 pin) P44: IRQ12-DS (177/176/145/144/100 pin) P45: IRQ13-DS (177/176/145/144/100 pin) P46: IRQ14-DS (177/176/145/144/100 pin) P47: IRQ15-DS (177/176/145/144/100 pin)

Register	Bit	RX630 (MPC)	RX65N (MPC)
P4nPFS	ASEL	Analog Input Function Select 0: Used other than as analog pin. 1: Used as analog pin. P40: AN000 (177/176/145/144/100/80 pin) P41: AN001 (177/176/145/144/100/80 pin) P42: AN002 (177/176/145/144/100/80 pin) P43: AN003 (177/176/145/144/100/80 pin) P44: AN004 (177/176/145/144/100/80 pin) P45: AN005 (177/176/145/144/100/80 pin) P46: AN006 (177/176/145/144/100/80 pin) P47: AN007 (177/176/145/144/100/80 pin)	Analog Input Function Select 0: Used other than as analog pin. 1: Used as analog pin. P40: AN000 (177/176/145/144/100 pin) P41: AN001 (177/176/145/144/100 pin) P42: AN002 (177/176/145/144/100 pin) P43: AN003 (177/176/145/144/100 pin) P44: AN004 (177/176/145/144/100 pin) P45: AN005 (177/176/145/144/100 pin) P46: AN006 (177/176/145/144/100 pin) P47: AN007 (177/176/145/144/100 pin)
P5nPFS	PSEL	Pin Function Select (PSEL[4:0]) b4-b0	Pin Function Select (PSEL[5:0]) b5-b0
	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P55: IRQ10 (177/176/145/144/100/80 pin)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P55: IRQ10 (177/176/145/144/100 pin)
P6nPFS	PSEL	Pin Function Select (PSEL[4:0]) b4-b0	Pin Function Select (PSEL[5:0]) b5-b0
	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P67: IRQ15 (177/176/145/144 pin)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P67: IRQ15 (177/176/145/144 pin)
P7nPFS	PSEL	Pin Function Select (PSEL[4:0]) b4-b0	Pin Function Select (PSEL[5:0]) b5-b0
P8nPFS	PSEL	Pin Function Select (PSEL[4:0]) b4-b0	Pin Function Select (PSEL[5:0]) b5-b0
P9nPFS	PSEL	Pin Function Select (PSEL[4:0]) b4-b0	Pin Function Select (PSEL[5:0]) b5-b0
	ASEL	Analog Input Function Select 0: Used other than as analog pin. 1: Used as analog pin. P90: AN014 (177/176/145/144 pin) P91: AN015 (177/176/145/144 pin) P92: AN016 (177/176/145/144 pin) P93: AN017 (177/176/145/144 pin)	Analog Input Function Select 0: Used other than as analog pin. 1: Used as analog pin. P90: AN114 (177/176/145/144 pin) P91: AN115 (177/176/145/144 pin) P92: AN116 (177/176/145/144 pin) P93: AN117 (177/176/145/144 pin)
PAnPFS	PSEL	Pin Function Select (PSEL[4:0]) b4-b0	Pin Function Select (PSEL[5:0]) b5-b0

Register	Bit	RX630 (MPC)	RX65N (MPC)
PAnPFS	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PA1: IRQ11 (177/176/145/144/100/80 pin) PA3: IRQ6-DS (177/176/145/144/100/80 pin) PA4: IRQ5-DS (177/176/145/144/100/80 pin)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PA1: IRQ11 (177/176/145/144/100 pin) PA3: IRQ6-DS (177/176/145/144/100 pin) PA4: IRQ5-DS (177/176/145/144/100 pin)
PBnPFS	PSEL	Pin Function Select (PSEL[4:0]) b4-b0	Pin Function Select (PSEL[5:0]) b5-b0
	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PB0: IRQ12 (177/176/145/144/100/80 pin) PB1: IRQ4-DS (177/176/145/144/100/80 pin)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PB0: IRQ12 (177/176/145/144/100 pin) PB1: IRQ4-DS (177/176/145/144/100 pin)
PCnPFS	PSEL	Pin Function Select (PSEL[4:0]) b4-b0	Pin Function Select (PSEL[5:0]) b5-b0
	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PC0: IRQ14 (177/176/145/144/100 pin) PC1: IRQ12 (177/176/145/144/100 pin) PC6: IRQ13 (177/176/145/144/100/80 pin) PC7: IRQ14 (177/176/145/144/100/80 pin)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PC0: IRQ14 (177/176/145/144/100 pin) PC1: IRQ12 (177/176/145/144/100 pin) PC6: IRQ13 (177/176/145/144/100 pin) PC7: IRQ14 (177/176/145/144/100 pin)
PDnPFS	PSEL	Pin Function Select (PSEL[4:0]) b4-b0	Pin Function Select (PSEL[5:0]) b5-b0
	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PD0: IRQ0 (177/176/145/144/100/80 pin) PD1: IRQ1 (177/176/145/144/100/80 pin) PD2: IRQ2 (177/176/145/144/100/80 pin) PD3: IRQ3 (177/176/145/144/100 pin) PD4: IRQ4 (177/176/145/144/100 pin) PD5: IRQ5 (177/176/145/144/100 pin) PD6: IRQ6 (177/176/145/144/100 pin) PD7: IRQ7 (177/176/145/144/100 pin)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PD0: IRQ0 (177/176/145/144/100 pin) PD1: IRQ1 (177/176/145/144/100 pin) PD2: IRQ2 (177/176/145/144/100 pin) PD3: IRQ3 (177/176/145/144/100 pin) PD4: IRQ4 (177/176/145/144/100 pin) PD5: IRQ5 (177/176/145/144/100 pin) PD6: IRQ6 (177/176/145/144/100 pin) PD7: IRQ7 (177/176/145/144/100 pin)

Register	Bit	RX630 (MPC)	RX65N (MPC)
PDnPFS	ASEL	Analog Input Function Select 0: Used other than as analog pin. 1: Used as analog pin. PD0：AN008 (177/176/145/144/100/80 pin) PD1：AN009 (177/176/145/144/100/80 pin) PD2：AN010 （177/176/145/144/100/80 pin） PD3：AN011 （177/176/145/144/100 pin） PD4：AN012 （177/176/145/144/100 pin） PD5：AN013 （177/176/145/144/100 pin） PD6：AN6 （177/176/145/144/100 pin） PD7：AN7 （177/176/145/144/100 pin）	Analog Input Function Select 0: Used other than as analog pin. 1: Used as analog pin. PD0: AN108 (177/176/145/144/100 pin) PD1: AN109 (177/176/145/144/100 pin) PD2: AN110 (177/176/145/144/100 pin) PD3: AN111 (177/176/145/144/100 pin) PD4: AN112 (177/176/145/144/100 pin) PD5: AN113 (177/176/145/144/100 pin) PD6: AN106 (177/176/145/144/100 pin) PD7: AN107 (177/176/145/144/100 pin)
PEnPFS	PSEL	Pin Function Select (PSEL[4:0]) b4-b0	Pin Function Select (PSEL[5:0]) b5-b0
	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PE2: IRQ7-DS (177/176/145/144/100/80 pin) PE5: IRQ5 (177/176/145/144/100/80 pin) PE6: IRQ6 (177/176/145/144/100 pin) PE7: IRQ7 (177/176/145/144/100 pin)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PE2: IRQ7-DS (177/176/145/144/100 pin) PE5: IRQ5 (177/176/145/144/100 pin) PE6: IRQ6 (177/176/145/144/100 pin) PE7: IRQ7 (177/176/145/144/100 pin)
	ASEL	Analog Input Function Select 0: Used other than as analog pin. 1: Used as analog pin. PE0：ANEX0 (177/176/145/144/100/80 pin) PE1：ANEX1 (177/176/145/144/100/80 pin) PE2：AN0 (177/176/145/144/100/80 pin) PE3：AN1 (177/176/145/144/100/80 pin) PE4：AN2 (177/176/145/144/100/80 pin) PE5：AN3 (177/176/145/144/100/80 pin) PE6：AN4 (177/176/145/144/100 pin) PE7：AN5 (177/176/145/144/100 pin)	Analog Input Function Select 0: Used other than as analog pin. 1: Used as analog pin. PE0: ANEX0 (177/176/145/144/100 pin) PE1: ANEX1 (177/176/145/144/100 pin) PE2: AN100 (177/176/145/144/100 pin) PE3: AN101 (177/176/145/144/100 pin) PE4: AN102 (177/176/145/144/100 pin) PE5: AN103 (177/176/145/144/100 pin) PE6: AN104 (177/176/145/144/100 pin) PE7: AN105 (177/176/145/144/100 pin)

Register	Bit	RX630 (MPC)	RX65N (MPC)
PFnPFS	PSEL	Pin Function Select (PSEL[4:0]) b4-b0	Pin Function Select (PSEL[5:0]) b5-b0
	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PF5：IRQ4 (177/176/145/144 pin)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PF5: IRQ4 (177/176/145/144 pin)
PJnPFS	PSEL	Pin Function Select (PSEL[4:0]) b4-b0	Pin Function Select (PSEL[5:0]) b5-b0
PKnPFS	-	PKn Pin Function Control Register	-
PFCSS0	CS0S	CS0# Output Pin Select 0: Set P60 as CS0# output pin 1: Set PC7 as CS0# output pin	CS0# Output Pin Select 0: Set P60 as CS0# output pin 1: Set PC7 as CS0# output pin Note. P60 is not present in 100-pin products. When CS0# output is used, set this bit to 1.
	CS1S[1:0]	CS1# Output Pin Select b3 b2 0 0: Set P61 as CS1# output pin 0 1: Set P71 as CS1# output pin 1 x: Set PC6 as CS1# output pin	CS1# Output Pin Select b3 b2 0 0: Set P61 as CS1# output pin 0 1: Set P71 as CS1# output pin 1 X: Set PC6 as CS1# output pin Note. P61 and P71 are not present in 100-pin products. When CS1# output is used, set these bits to 1xb.
	CS2S[1:0]	CS2# Output Pin Select b5 b4 0 0: Set P62 as CS2# output pin 0 1: Set P72 as CS2# output pin 1 x: Set PC5 as CS2# output pin	CS2# Output Pin Select b5 b4 0 0: Set P62 as CS2# output pin 0 1: Set P72 as CS2# output pin 1 X: Set PC5 as CS2# output pin Note. P62 and P72 are not present in 100-pin products. When CS2# output is used, set these bits to 1xb.
	CS3S[1:0]	CS3# Output Pin Select b7 b6 0 0: Set P63 as CS3# output pin 0 1: Set P73 as CS3# output pin 1 x: Set PC4 as CS3# output pin	CS3# Output Pin Select b7 b6 0 0: Set P63 as CS3# output pin 0 1: Set P73 as CS3# output pin 1 X: Set PC4 as CS3# output pin Note. P63 and P73 are not present in 100-pin products. When CS3# output is used, set these bits to 1xb.

Register	Bit	RX630 (MPC)	RX65N (MPC)
PFCSS1	CS4S[1:0]	CS4# Output Pin Select b1 b0 0 0: Set P64 as CS4# output pin 0 1: Set P74 as CS4# output pin 1 x: Set P24 as CS4# output pin	CS4# Output Pin Select b1 b0 0 0: Set P64 as CS4# output pin 0 1: Set P74 as CS4# output pin 1 X: Set P24 as CS4# output pin Note. P64 and P74 are not present in 100-pin products. When CS4# output is used, set these bits to 1xb.
	CS5S[1:0]	CS5# Output Pin Select b3 b2 0 0: Set P65 as CS5# output pin 0 1: Set P75 as CS5# output pin 1 x: Set P25 as CS5# output pin	CS5# Output Pin Select b3 b2 0 0: Set P65 as CS5# output pin 0 1: Set P75 as CS5# output pin 1 X: Set P25 as CS5# output pin Note. P65 and P75 are not present in 100-pin products. When CS5# output is used, set these bits to 1xb.
	CS6S[1:0]	CS6# Output Pin Select b5 b4 0 0: Set P66 as CS6# output pin 0 1: Set P76 as CS6# output pin 1 x: Set P26 as CS6# output pin	CS6# Output Pin Select b5 b4 0 0: Set P66 as CS6# output pin 0 1: Set P76 as CS6# output pin 1 X: Set P26 as CS6# output pin Note. P66 and P76 are not present in 100-pin products. When CS6# output is used, set these bits to 1xb.
	CS7S[1:0]	CS7# Output Pin Select b7 b6 0 0: Set P67 as CS7# output pin 0 1: Set P77 as CS7# output pin 1 x: Set P27 as CS7# output pin	CS7# Output Pin Select b7 b6 0 0: Set P67 as CS7# output pin 0 1: Set P77 as CS7# output pin 1 X: Set P27 as CS7# output pin Note. P67 and P77 are not present in 100-pin products. When CS7# output is used, set these bits to 1xb.
PFBCR0	ADRHMS2	-	A16 to A23 Output Enable
	BCLKO	-	BCLK Forced Output
	DH32E	D16 to D31 Output Enable	D16 to D31 Output Enable*1
	WR32BC32E	WR3#/BC3# Output Enable WR2#/BC2# Output Enable	WR3#/BC3# and WR2#/BC2# Output Enable*1

Register	Bit	RX630 (MPC)	RX65N (MPC)
PFBCR1	WAITS[1:0]	WAIT Select b1b0 0 0: Configures P57 as the WAIT# input pin. 0 1: Configures P55 as the WAIT# input pin. 1 0: Configures PC5 as the WAIT# input pin. 1 1: Configures P51 as the WAIT# input pin.	WAIT Select b1b0 0 0: Setting invalid 0 1: Configures P55 as the WAIT# input pin. 1 0: Configures PC5 as the WAIT# input pin. 1 1: Configures P51 as the WAIT# input pin.
	ALES	-	ALE Select*1
	MDSDE	-	SDRAM Pin Enable
	DQM1E	-	DQM1 Enable
	SDCLKE	-	SDCLK Enable
PFBCR2	-	-	External Bus Control Register 2*1
PFBCR3	-	-	External Bus Control Register 3*1
PFENET	-	-	Ethernet Control Register
PFUSB0	-	USB0 Control Register	-

*1: Can be used for products with at least 1.5 Mbytes of code flash memory.

2.17 16-Bit Timer Pulse Unit

Table 2.36 shows a Comparative Listing of 16-Bit Timer Pulse Unit Specifications.

Table 2.36 Comparative Listing of 16-Bit Timer Pulse Unit Specifications

Item	RX630 (TPUa)	RX65N (TPUa)
Pulse input/output	Maximum 32 (for unit 0: 16, for unit 1: 16)	Maximum 16 (1 unit only)
Count clocks	Seven or eight types are provided for each channel.	Seven or eight types are provided for each channel.
Available operations	• Waveform output at compare match • Input capture function (noise filters can be set) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match and input capture • Synchronous input/output for registers by counter synchronous operation • Maximum of 15-phase PWM output by combination with synchronous operation • Cascaded operation	• Waveform output at compare match • Input capture function (noise filters can be set) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match and input capture • Synchronous input/output for registers by counter synchronous operation • Maximum of 15-phase PWM output by combination with synchronous operation • Cascaded operation
Buffer operation	• Channels 0, 3, 6, and 9 • Automatic transfer of register data	• Channels 0 and 3 • Automatic transfer of register data
Phase coefficient mode	Channels 1, 2, 4, 5, 7, 8, 10, and 11	Channels 1, 2, 4, and 5
Interrupt sources	52 sources (for unit 0: 26, for unit 1: 26)	26 sources
Generation of trigger	Programmable pulse generator (PPG) output trigger can be generated.	Programmable pulse generator (PPG) output trigger can be generated.
	Conversion start trigger for the A/D converter can be generated.	Conversion start trigger for the A/D converter can be generated.
Event link function (output)	-	Six types of event signal can be output to the ELC. • Compare match A (TPU0 to TPU3) • Compare match B (TPU0 to TPU3) • Compare match C (TPU0, TPU3) • Compare match D (TPU0, TPU3) • Overflow (TPU0 to TPU3) • Underflow (TPU1, TPU2)
Event link function (input)	-	Any of the three operations in response to event input is possible. • Starting counts (TPU0 to TPU3) • Restarting counts (TPU0 to TPU3) • Input capture operation (TPU0 to TPU3)

2.18 8-Bit Timer

Table 2.37 shows a Comparative Listing of 8-Bit Timer Specifications, and Table 2.38 shows a Comparative Listing of 8-Bit Timer Registers.

Table 2.37 Comparative Listing of 8-Bit Timer Specifications

Item	RX630 (TMR)	RX65N (TMR)
Count clocks	• Frequency divided clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock	• Frequency-divided clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock
Number of channels	(8 bits x 2 channels) x 2 units	(8 bits x 2 channels) x 2 units
Compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selected by compare match A or B, or an external reset signal.	Selected by compare match A or B, or an external reset signal.
Timer output	Output pulses with a desired duty cycle or PWM output	Output pulses with a desired duty cycle or PWM output
Cascading of two channels	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
Event link function (output)	-	Compare match A, compare match B, and overflow (TMR0 to TMR3)
Event link function (input)	-	One of the following three operations proceeds in response to an event reception: (1) Counting start operation (TMR0 to TMR3) (2) Event counting operation (TMR0 to TMR3) (3) Counting restart operation (TMR0 to TMR3)
DTC activation	DTC can be activated by compare match A interrupts or compare match B interrupts.	DTC can be activated by compare match A interrupts or compare match B interrupts.
A/D conversion start trigger of the A/D converter	Compare match A of TMR0 and TMR2	Compare match A of TMR0 or TMR2

Item	RX630 (TMR)	RX65N (TMR)
Capable of generating baud rate clock for SCI	Generates baud rate clock for SCI	Generation of baud rate clock for SCI
Low power consumption function	Each unit can be placed in a module stop state	Each unit can be placed in a module stop state

Table 2.38 Comparative Listing of 8-Bit Timer Registers

Register	Bit	RX630 (TMR)	RX65N (TMR)
TCSTR	-	-	Timer Counter Start Register

2.19 Compare Match Timer

Table 2.39 shows a Comparative Listing of Compare Match Timer Specifications.

Table 2.39 Comparative Listing of Compare Match Timer Specifications

Item	RX630 (CMT)	RX65N (CMT)
Count clocks	Four frequency dividing clocks One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected individually for each channel.	Four frequency dividing clocks One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.
Interrupt	A compare match interrupt can be requested individually for each channel.	A compare match interrupt can be requested for each channel.
Event link function (output)	-	An event signal is output upon a CMT1 compare match.
Event link function (input)	-	• Linking to the specified module is possible. • CMT1 count start, event counter, or count restart operation is possible.
Low power consumption function	Each unit can be placed in a module-stop state.	Each unit can be placed in a module stop state.

2.20 Realtime Clock

Table 2.40 shows a Comparative Listing of Realtime Clock Specifications, and Table 2.41 shows a Comparative Listing of Realtime Clock Registers.

Table 2.40 Comparative Listing of Realtime Clock Specifications

Item	RX630 (RTCa)	RX65N (RTCd)
Count modes	Calendar count mode	Calendar count mode/binary count mode
Count source	Sub-clock (XCIN) or main clock (EXTAL)	Sub-clock (XCIN) or main clock (EXTAL)
Clock and calendar functions	• Calendar count mode — Year, month, date, day of the week, hours, minutes, and seconds are counted and represented in BCD — Selection of 12- or 24-hour mode — 30-second adjustment (30 seconds or less are rounded down to 00 second, and 30 seconds or more are rounded up to one minute) — Automatic leap year adjustment — Start/stop function — Indicates the state of 1, 2, 4, 8, 16, 32, or 64 Hz in binary. — Time error adjustment function — Output a 1-Hz clock	• Calendar count mode — Year, month, date, day-of-week, hour, minute, second are counted, BCD display — 12 hours/24 hours mode switching function — 30 seconds adjustment function (a number less than 30 is rounded down to 00 seconds, and 30 seconds or more are rounded up to one minute) — Automatic adjustment function for leap years • Binary count mode — Count seconds in 32 bits, binary display • Common to both modes — Start/stop function — The sub-second digit is displayed in binary units (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, or 64 Hz). — Clock error correction function — Clock (1 Hz/64 Hz) output

Item	RX630 (RTCa)	RX65N (RTCd)
Interrupt	• Alarm interrupt (ALM) Year, month, date, day of the week, hours, minutes, and seconds can be selected as conditions for the alarm interrupt • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second can be selected as an interrupt period. • Carry interrupt (CUP) Indicates occurrence of a carry to the seconds counter or a carry to the 64-Hz counter during reading of the 64-Hz counter • Recovery from software standby mode or deep software standby mode can be performed by an alarm interrupt or periodic interrupt	• Alarm interrupt (ALM) As an alarm interrupt condition, selectable which of the below is compared with: — Calendar count mode: Year, month, date, day-of-week, hour, minute, or second can be selected — Binary count mode: Each bit of the 32-bit binary counter • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, or 1/256 second can be selected as an interrupt period. • Carry interrupt (CUP) An interrupt is generated at either of the following timings: — When a carry from the 64-Hz counter to the second counter is generated. — When the 64-Hz counter is changed and the R64CNT register is read at the same time. • Recovery from software standby mode or deep software standby mode can be performed by an alarm interrupt or periodic interrupt
Time-capture function	Times when any of three event signals are input can be captured The month, date, hour, minute, and second are captured for each event	Times can be captured when the edge of the time capture event input pin is detected. For every event input, month, date, hour, minute, and second are captured or 32-bit binary counter value is captured.
Event link function	-	Periodic event output

Table 2.41 Comparative Listing of Realtime Clock Registers

Register	Bit	RX630 (RTCa)	RX65N (RTCd)
BCNT0*1	-	-	Binary Counter 0
BCNT1*1	-	-	Binary Counter 1
BCNT2*1	-	-	Binary Counter 2
BCNT3*1	-	-	Binary Counter 3
BCNT0AR*1	-	-	Binary Counter 0 Alarm Register
BCNT1AR*1	-	-	Binary Counter 1 Alarm Register
BCNT2AR*1	-	-	Binary Counter 2 Alarm Register
BCNT3AR*1	-	-	Binary Counter 3 Alarm Register
BCNT0AER*1	-	-	Binary Counter 0 Alarm Enable Register
BCNT1AER*1	-	-	Binary Counter 1 Alarm Enable Register
BCNT2AER*1	-	-	Binary Counter 2 Alarm Enable Register
BCNT3AER*1	-	-	Binary Counter 3 Alarm Enable Register
RCR1	RTCOS	-	RTCOUT Output Select
RCR2	CNTMD	-	Count Mode Select
RCR3	RTCDV[2:0]	-	Sub-Clock Oscillator Drive Capacity Control
BCNT0CPy*1	-	-	BCNT0 Capture Register y (y = 0 to 2)
BCNT1CPy*1	-	-	BCNT1 Capture Register y (y = 0 to 2)
BCNT2CPy*1	-	-	BCNT2 Capture Register y (y = 0 to 2)
BCNT3CPy*1	-	-	BCNT3 Capture Register y (y = 0 to 2)

Note 1. In binary count mode

2.21 Watchdog Timer

Table 2.42 shows a Comparative Listing of Watchdog Timer Specifications, and Table 2.43 shows a Comparative Listing of Watchdog Timer Registers.

Table 2.42 Comparative Listing of Watchdog Timer Specifications

Item	RX630 (WDTA)	RX65N (WDTA)
Count source	Peripheral clock (PCLK)	Peripheral module clock (PCLK)
Clock division ratio	Divide by 4, 64, 128, 512, 2,048, or 8,192	Divide by 4, 64, 128, 512, 2,048, or 8,192
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Counting automatically starts after a reset (auto-start mode) • Counting is started by refreshing the WDTRR register (writing 00h and then FFh) (register start mode)	• Auto-start mode: Counting automatically starts after a reset or after an underflow or refresh error occurs • Register start mode: Counting is started by refresh operation (writing to the WDTRR register)
Conditions for stopping the counter	• Pin reset (the down-counter and registers return to their initial values) • A counter underflows or a refresh error is generated Count restarts automatically in auto-start mode, or by refreshing the counter in register start mode.	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error is generated
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Watchdog timer Reset sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Interrupt sources	Non-maskable interrupt sources • A non-maskable interrupt (WUNI) is generated by an underflow of the down-counter • Refreshing outside the refresh-permitted period (refresh error)	Non-maskable interrupt/interrupt sources • Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read by the WDTSR register.	The down-counter value can be read by the WDTSR register.

Table 2.43 Comparative Listing of Watchdog Timer Registers

Register	Bit	RX630 (WDTA)	RX65N (WDTA)
WDTRCR	RSTIRQS	Reset Interrupt Request Selection 0: Non-maskable interrupt request output is enabled 1: Reset output is enabled	Reset Interrupt Request Selection 0: Non-maskable interrupt request or interrupt request output is enabled 1: Reset output is enabled

2.22 Independent Watchdog Timer

Table 2.44 shows a Comparative Listing of Independent Watchdog Timer Specifications, and Table 2.45 shows a Comparative Listing of Independent Watchdog Timer Registers.

Table 2.44 Comparative Listing of Independent Watchdog Timer Specifications

Item	RX630 (IWDTa)	RX65N (IWDTa)
Count source	IWDT-dedicated clock (IWDTCLK)	IWDT-dedicated clock (IWDTCLK)
Clock division ratio	Divide by1, 16, 32, 64, 128, or 256	Divide by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Counting automatically starts after a reset (auto-start mode) • Counting is started by refreshing the IWDTRR register (writing 00h and then FFh) (register start mode)	• Counting automatically starts after a reset (auto-start mode) • Counting is started (register start mode) by refreshing the counter (writing 00h and then FFh to the IWDTRR register).
Conditions for stopping the counter	• Pin reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error is generated Count restarts automatically in auto-start mode, or by refreshing the counter in register start mode	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error occurs Counting restarts (In auto-start mode, counting automatically restarts after a reset or after a non-maskable interrupt request/interrupt request is output. In register start mode, counting restarts after refreshing.)
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Watchdog timer Reset sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Interrupt sources	Non-maskable interrupt sources • A non-maskable interrupt (WUNI) is generated by an underflow of the down-counter • When refreshing is done outside the refresh-permitted period (refresh error)	Non-maskable interrupt/interrupt sources • Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read by the IWDTSR register.	The down-counter value can be read by the IWDTSR register.
Event link function (output)	-	• Down-counter underflow event output • Refresh error event output

Item	RX630 (IWDTa)	RX65N (IWDTa)
Auto-start mode (controlled by option function select register 0 (OFS0))	• Selecting the clock frequency divide ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)	• Selecting the clock frequency divide ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)
Register start mode (controlled by the IWDT registers)	• Selecting the clock frequency divide ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)	• Selecting the clock frequency divide ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)

Table 2.45 Comparative Listing of Independent Watchdog Timer Registers

Register	Bit	RX630 (IWDTa)	RX65N (IWDTa)
IWDTRCR	RSTIRQS	Reset Interrupt Request Selection 0: Non-maskable interrupt request output is enabled. 1: Reset output is enabled.	Reset Interrupt Request Select 0: Non-maskable interrupt request or interrupt request output is enabled. 1: Reset output is enabled.

2.23 USB 2.0 Function Module

Table 2.46 shows a Comparative Listing of USB 2.0 Function Module Specifications, and Table 2.47 shows a Comparative Listing of USB 2.0 Function Module Registers.

Table 2.46 Comparative Listing of USB 2.0 Function Module Specifications

Item	RX630 (USBa)	RX65N (USBb)
Features	• USB Device Controller (UDC) and transceiver for USB 2.0 are incorporated.	• USB Device Controller (UDC) and transceiver for USB 2.0 are incorporated. Host controller, function controller, and On-The-Go (OTG) are supported (one channel) • The host controller and the function controller can be switched by software.
	• One port is provided. • Self-power mode or bus-power mode can be selected.	• One port is provided. • Self-power mode or bus power mode can be selected.
		When the host controller is selected: • Full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) are supported • Automatic scheduling for SOF and packet transmissions • Programmable intervals for isochronous and interrupt transfers • Multiple peripheral devices can be connected for communication via a one-stage hub.
	• Programmable intervals for isochronous and interrupt transfers • Full-speed transfer (12 Mbps) is supported*1 • Control transfer stage control function • Device state control function • Auto response function for SET_ADDRESS request • SOF interpolation function	When the function controller is selected: • Full-speed transfer (12 Mbps) is supported*1 • Control transfer stage control function • Device state control function • Auto response function for SET_ADDRESS request • SOF interpolation function
Communication data transfer types	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer
Pipe configuration	• Buffer memory for USB communications is provided. • Up to ten pipes can be selected (including the default control pipe). • Endpoint numbers can be assigned flexibly to PIPE1 to PIPE9.	• Buffer memory for USB communication is provided. • Up to 10 pipes can be selected (including the default control pipe). • PIPE1 to PIPE9 can be assigned any endpoint number.

Item	RX630 (USBa)	RX65N (USBb)
Pipe configuration	Transfer conditions that can be set for each pipe: • PIPE0: Control transfer, 64-byte single buffer • PIPE1 and PIPE2: 64-byte double buffer can be specified for bulk transfer 256-byte double buffer for isochronous transfer • PIPE3 to PIPE5: Bulk transfer, 64-byte double buffer • PIPE6 to PIPE9: Interrupt transfer, 64-byte single buffer	Transfer conditions that can be set for each pipe: • PIPE0: Control transfer, 64-byte single buffer • PIPE1 and PIPE2: 64-byte double buffer can be specified for bulk transfer 256-byte double buffer for isochronous transfer • PIPE3 to PIPE5: Bulk transfer, 64-byte double buffer • PIPE6 to PIPE9: Interrupt transfer, 64-byte single buffer
Other functions	• Reception ending function using transaction count • Function that changes the BRDY interrupt event notification timing (BFRE) • Function that automatically clears the buffer memory after the data for the pipe specified at the DnFIFO (n = 0 or 1) port has been read (DCLRM) • NAK setting function for response PID generated by end of transfer (SHTNAK)	• Reception ending function using transaction count • Function that changes the BRDY interrupt event notification timing (BFRE) • Function that automatically clears the buffer memory after the data for the pipe specified at the DnFIFO (n = 0, 1) port has been read (DCLRM) • NAK setting function for response PID generated by end of transfer (SHTNAK) • On-chip pull-up and pull-down resistors of D+/DM-
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Note 1. Low-speed transfer (1.5Mbps) is not supported when function controller operation is selected.

Table 2.47 Comparative Listing of USB 2.0 Function Module Registers

Register	Bit	RX630 (USBa)	RX65N (USBb)
SYSCFG	DRPD	-	D+/D- Line Resistor Control
	DCFM	-	Controller Function Select
SYSSTS0	LNST[1:0]	USB Data Line Status Monitor b1b0 0 0: SE0 0 1: J-state 1 0: K-state 1 1: SE1	USB Data Line Status Monitor Flag • During Low-Speed Operation (Only in Host Controller Operation) b1 b0 0 0: SE0 0 1: K-state 1 0: J-state 1 1: SE1 • During Full-Speed Operation b1 b0 0 0: SE0 0 1: J-state 1 0: K-state 1 1: SE1
	IDMON	-	External ID0 Input Pin Monitor Flag

Register	Bit	RX630 (USBa)	RX65N (USBb)
	SOFEA	-	SOF Active Monitor Flag When the Host Controller is Selected
	HTACT	-	USB Host Sequencer Status Monitor Flag
	OVCMON[1:0]	-	External USB0_OVRCURA/ USB0_OVRCURB Input Pin Monitor Flag
DVSTCTR0	RHST[2:0]	USB Bus Reset Status b2 b0 0 0 0: Communication speed not determined 1 0 0: USB bus reset in progress 0 1 0: Full-speed connection	USB Bus Reset Status Flag • When the host controller is selected b2 b0 0 0 0: Communication speed not determined (powered state or no connection) 1 x x: USB bus reset in progress 0 0 1: Low-speed connection 0 1 0: Full-speed connection • When the function controller is selected b2 b0 0 0 0: Communication speed not determined 0 0 1: USB bus reset in progress 0 1 0: USB bus reset in progress or full-speed connection
DVSTCTR0	UACT	-	USB Bus Enable
	RESUME	-	Resume Output
	USBRST	-	USB Bus Reset Output
	RWUPE	-	Wakeup Detection Enable
	VBUSEN	-	USB0_VBUSEN Output Pin Control
	EXICEN	-	USB0_EXICEN Output Pin Control
	HNPBTOA	-	Host Negotiation Protocol (HNP) Control
D0FIFOSEL, D1FIFOSEL	DREQE	DMA Transfer Request Enable 0: DMA transfer request is disabled. 1: DMA transfer request is enabled.	DMA/DTC Transfer Request Enable 0: DMA/DTC transfer request is disabled. 1: DMA/DTC transfer request is enabled.
INTENB1	-	-	Interrupt Enable Register 1
SOFCFG	TRNENSEL	-	Transaction-Enabled Time Select
INTSTS1	-	-	Interrupt Status Register 1

Register	Bit	RX630 (USBa)	RX65N (USBb)
USBADDR	STSRECOV [3:0]	Status Recovery b11 b8 1 0 0 1: Recovery is to the full-speed state (DVSTCTR0.RHST[2:0] = 010), and INSTS0.DVSQ[2:0] = 001 (default state). 1 0 1 0: Recovery is to the full-speed state (DVSTCTR0.RHST[2:0] = 010), and INSTS0.DVSQ[2:0] = 010 (address state). 1 0 1 1: Recovery is to the full-speed state (DVSTCTR0.RHST[2:0] = 010), and INSTS0.DVSQ[2:0] = 011 (configured state). Other than above: Setting prohibited	Status Recovery • Recovery when the function controller is selected b11 b8 1 0 0 1: Return to the full-speed state (bits DVSTCTR0.RHST[2:0] = 010b), bits INTSTS0.DVSQ[2:0] = 001b (Default state) 1 0 1 0: Return to the full-speed state (bits DVSTCTR0.RHST[2:0] = 010b), bits INTSTS0.DVSQ[2:0] = 010b (Address state) 1 0 1 1: Return to the full-speed state (bits DVSTCTR0.RHST[2:0] = 010b), bits INTSTS0.DVSQ[2:0] = 011b (Configured state) Settings other than above are prohibited. • Recovery when the host controller is selected b11 b8 1 0 0 0: Return to the full-speed state (bits VSTCTR0.RHST[2:0] = 010b) Settings other than above are prohibited.
USBREQ	-	USB Request Type Register R/W attribute: R	USB Request Type Register R/W attribute: R/W*
USBVAL	-	USB Request Value Register R/W attribute: R	USB Request Value Register R/W attribute: R/W*
USBINDX	-	USB Request Index Register R/W attribute: R	USB Request Index Register R/W attribute: R/W*
USBLENG	-	USB Request Length Register R/W attribute: R	USB Request Length Register R/W attribute: R/W*
DCPCFG	-	-	DCP Configuration Register
DCPMAXP	DEVSEL [3:0]	-	Device Select
DCPCTR	SUREQCLR	-	SUREQ Bit Clear
	SUREQ	-	Setup Token Transmission
PIPEMAXP	DEVSEL [3:0]	-	Device Select
DEVADDn	-	-	Device Address n Configuration Register (n = 0 to 5)
PHYSLEW	-	-	PHY Cross Point Adjustment Register

Register	Bit	RX630 (USBa)	RX65N (USBb)
DPUSR0R	RPUE0	-	D+ Pull-Up Resistor Control
	DRPD0	-	D+/D- Pull-Down Resistor Control
	DOVCA0	-	USB OVRCURA Input Flag
	DOVCB0	-	USB OVRCURB Input Flag
DPUSR1R	DMINTE0	-	USB D- Interrupt Enable/Clear
	DOVRCRAE0	-	USB OVRCURA Interrupt Enable/Clear
	DOVRCRBE0	-	USB OVRCURB Interrupt Enable/Clear
	DMINT0	-	USB D- Interrupt Source Recovery Flag
	DOVRCRA0	-	USB OVRCURA Interrupt Source Recovery Flag
	DOVRCRB0	-	USB OVRCURB Interrupt Source Recovery Flag

Note: * When the function controller is selected, these bits can only be read from, and writing to these bits is invalid. When the host controller is selected, these bits can be read from and written to.

2.24 Serial Communications Interface

The RX630 Group has 7 independent serial communications interface channels (SCIc: 6 channels, SCId: 1 channel).

The RX65N Group has 13 independent serial communications interface channels (SCIg: 10 channels, SCIi: 2 channels, SCIh: 1 channel).

Table 2.48 shows a Comparative Listing of SCIc and SCIg Specifications, Table 2.49 shows a Comparative Listing of SCIi Specifications, Table 2.50 shows a Comparative Listing of SCId and SCIh Specifications, Table 2.51 shows a Comparative Listing of Serial Communications Interface Channels Specifications, and Table 2.52 shows a Comparative Listing of Serial Communications Interface Registers.

Table 2.48 Comparative Listing of SCIc and SCIg Specifications

Item		RX630 (SCIc)	RX65N (SCIg)
Number of channels		12 channels	10 channels
Serial communication modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		• Transmitter: Enables continuous transmission by double-buffering. • Receiver: Enables continuous reception by double-buffering.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable as LSB first or MSB first transfer.	Selectable as LSB first or MSB first transfer.
Interrupt sources		Transmit-end, transmit-data-empty, receive-data-full, and receive error Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)	Transmit end, transmit data empty, receive data full, and receive error Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)
Low power consumption function		Module stop state can be set for each channel.	Module stop state can be set for each channel.
Asynchronous mode	Data length	7, or 8 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	CTSn and RTSn pins can be used in transfer control.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Start bit detection	Low level	Low level or falling edge is selectable.

Item		RX630 (SCIc)	RX65N (SCIg)
Asynchronous mode	Break detection	Break can be detected by reading RXDn pin level directly in case of a framing error	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.
	Clock source	• Selectable from internal or external clock • Enables transfer rate clock input from TMR (SCI5 and SCI6)	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5 and SCI6).
	Double-speed mode	-	Baud rate generator double-speed mode is selectable.
	Multi-processor communication function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	CTSn and RTSn pins can be used in transfer control.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
Smart card interface mode	Error processing	An error signal can be automatically transmitted on detection of a parity error during reception	An error signal can be automatically transmitted when detecting a parity error during reception
		Data can be automatically re-transmitted on receiving an error signal during transmission	Data can be automatically retransmitted when receiving an error signal during transmission
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	I^2C bus format	I^2C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer rate	Up to 384 kbps. Fast mode is supported	Fast mode is supported.
	Noise cancellation	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error
	SS input pin function	Applying the high level to the SS# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.
Bit rate modulation function		-	Correction of outputs from the on-chip baud rate generator can reduce errors.

Item	RX630 (SCIc)	RX65N (SCIg)
Event link function	-	Error (receive error, error signal detection) event output
	-	Receive data full event output
	-	Transmit data empty event output
	-	Transmit end event output

Table 2.49 Comparative Listing of SCIi Specifications

Item		RX630 (-)	RX65N (SCIi)
Number of channels		-	2 channels
Serial communication modes		-	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		-	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		-	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		-	Selectable between LSB-first or MSB-first transfer.
Interrupt sources		-	Transmit end, transmit data empty, receive data full, receive error, receive data ready, and match Completion of generation of start condition, restart condition, or stop condition (simple I²C mode)
Low power consumption function		-	Module stop state can be set for each channel.
Asynchronous mode	Data length	-	7, 8, or 9 bits
	Transmission stop bits	-	1 or 2 bits
	Parity	-	Even parity, odd parity, or no parity
	Receive error detection	-	Parity, overrun, and framing errors
	Hardware flow control	-	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Transmit/receive FIFO	-	16-stage FIFOs for transmit and receive buffers

Item		RX630 (-)	RX65N (SCIi)
Asynchronous mode	Data match detection	-	Compares receive data and comparison data, and generates interrupt when they are matched
	Start bit detection	-	Low level or falling edge is selectable.
	Break detection	-	When a framing error occurs, a break can be detected by reading the internal register.
	Clock source	-	An internal or external clock can be selected.
	Double-speed mode	-	Baud rate generator double-speed mode is selectable.
	Multi-processor communication function	-	Serial communication among multiple processors
	Noise cancellation	-	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	-	8 bits
	Receive error detection	-	Overrun error
	Hardware flow control	-	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Transmit/receive FIFO	-	16-stage FIFOs for transmit and receive buffers
Smart card interface mode	Error processing	-	An error signal can be automatically transmitted when detecting a parity error during reception
		-	Data can be automatically retransmitted when receiving an error signal during transmission
	Data type	-	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	-	I^2C bus format
	Operating mode	-	Master (single-master operation only)
	Transfer speed	-	Fast mode is supported.
	Noise canceler	-	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.
Simple SPI mode	Data length	-	8 bits
	Error detection	-	Overrun error
	SS input pin function	-	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	-	Four kinds of settings for clock phase and clock polarity are selectable.

Item	RX630 (-)	RX65N (SCIi)
Bit rate modulation function	-	Correction of outputs from the on-chip baud rate generator can reduce errors.

Table 2.50 Comparative Listing of SCId and SCIh Specifications

Item		RX630 (SCId)	RX65N (SCIh)
Number of channels		1 channel	1 channel
Serial communication modes		• Asynchronous operation • Clock synchronous operation • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C-bus • Simple SPI bus
Transfer speed		Bit rate specifiable with on-chip baud rate generator.	Bit rate specifiable with the on-chip baud rate generator.
Full-duplex communication		• Transmitter: Enables continuous transmission by double-buffering. • Receiver: Enables continuous reception by double-buffering.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable as LSB first or MSB first transfer.	Selectable as LSB first or MSB first transfer.
Interrupt sources		Transmit-end, transmit-data-empty, receive-data-full, and receive error Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)	Transmit end, transmit data empty, receive data full, and receive error Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)
Low power consumption function		Module-stop state can be set.	Module stop state can be set.
Asynchronous mode	Data length	7, or 8 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	CTSn and RTSn pins can be used in transfer control.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Start bit detection	Low level	Low level or falling edge is selectable.
	Break detection	Break can be detected by reading RXDn pin level directly in case of a framing error	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.

Item		RX630 (SCId)	RX65N (SCIh)
Asynchronous mode	Clock source	• Selectable from internal or external clock • Enables transfer rate clock input from TMR	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI12).
	Double-speed mode	-	Baud rate generator double-speed mode is selectable.
	Multi-processor communication function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	CTSn and RTSn pins can be used in transfer control.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
Smart card interface mode	Error processing	An error signal can be automatically transmitted on detection of a parity error during reception	An error signal can be automatically transmitted on detection of a parity error during reception
		Data can be automatically re-transmitted on receiving an error signal during transmission	Data can be automatically retransmitted when receiving an error signal during transmission
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	I^2C bus format	I^2C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer rate	Up to 384 kbps. Fast mode is supported	Fast mode is supported.
	Noise cancellation	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error
	SS input pin function	Applying the high level to the SS# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock sense are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.

Item		RX630 (SCId)	RX65N (SCIh)
Extended serial mode	Start Frame transmission	• Output of a low level as the Break Field over a specified width and generation of interrupts on completion • Detection of bus collisions and the generation of interrupts on detection	• Output of a low level as the Break Field over a specified width and generation of interrupts on completion • Detection of bus collisions and the generation of interrupts on detection
	Start Frame reception	• Detection of the Break Field low width and generation of an interrupt on detection • Comparison of Control Fields 0 and 1 and generation of an interrupt when the two match • Two kinds of data for comparison (primary and secondary) can be set in Control Field 1. • A priority interrupt bit can be set in Control Field 1. • Handling of Start Frames that do not include a Break Field • Handling of Start Frames that do not include a Control Field • Function for measuring bit rates	• Detection of the Break Field low width and generation of an interrupt on detection • Comparison of Control Fields 0 and 1 and generation of an interrupt when the two match • Two kinds of data for comparison (primary and secondary) can be set in Control Field 1. • A priority interrupt bit can be set in Control Field 1. • Handling of Start Frames that do not include a Break Field • Handling of Start Frames that do not include a Control Field • Function for measuring bit rates
	I/O control function	• Selectable polarity for TXDX12 and RXDX12 signals • Selection of a digital filter for RXDX12 • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Selectable timing for the sampling of data received through RXDX12 • Signals received on RXDX12 can be passed through to SCIc when the extended serial mode control section is off.	• Selectable polarity for TXDX12 and RXDX12 signals • Selection of a digital filter for the RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Selectable timing for the sampling of data received through RXDX12 • Signals received on RXDX12 can be passed through to SCIg when the extended serial mode control section is off.
	Timer function	Usable as a reloading timer	Usable as a reloading timer
Bit rate modulation function		-	Correction of outputs from the on-chip baud rate generator can reduce errors.

Table 2.51 Comparative Listing of Serial Communications Interface Channels Specifications

Item	RX630 (SCIc, SCId)	RX65N (SCIg, SCIi, SCIh)
Asynchronous mode	SCI0 to SCI12	SCI0 to SCI12
Clock synchronous mode	SCI0 to SCI12	SCI0 to SCI12
Smart card interface mode	SCI0 to SCI12	SCI0 to SCI12
Simple I²C mode	SCI0 to SCI12	SCI0 to SCI12
Simple SPI mode	SCI0 to SCI12	SCI0 to SCI12
Extended serial mode	SCI12	SCI12
TMR clock input	SCI5, SCI6, SCI12	SCI5, SCI6, SCI12
Event link function	-	SCI5
FIFO mode	-	SCI10, SCI11

Table 2.52 Comparative Listing of Serial Communications Interface Registers

Register	Bit	RX630 (SCIc, SCId)	RX65N (SCIg, SCIi, SCIh)
RDRH	-	-	Receive Data Register H
RDRL	-	-	Receive Data Register L
RDRHL	-	-	Receive Data Register HL
FRDR	-	-	Receive FIFO Data Register
TDRH	-	-	Transmit Data Register H
TDRL	-	-	Transmit Data Register L
TDRHL	-	-	Transmit Data Register HL
FTDR	-	-	Transmit FIFO Data Register
SMR	CHR	Character Length (Valid only in asynchronous mode) 0: Selects 8 bits as the data length 1: Selects 7 bits as the data length	Character Length (Valid only in asynchronous mode) Selects in combination with the SCMR.CHR1 bit. CHR1 CHR 0 0: Transmit/receive in 9-bit data length 0 1: Transmit/receive in 9-bit data length 1 0: Transmit/receive in 8-bit data length 1 1: Transmit/receive in 7-bit data length
	CM	Communications Mode 0: Asynchronous mode 1: Clock synchronous mode	Communications Mode 0: Asynchronous mode or simple I2C mode 1: Clock synchronous mode or simple SPI mode
SSR	RDRF	-	Receive Data Full Flag
	TDRE	-	Transmit Data Empty Flag
SSRFIFO	-	-	Serial Status Register
SCMR	CHR1	-	Character Length 1
MDDR	-	-	Modulation Duty Register
SEMR	BRME	-	Bit Rate Modulation Enable
	BGDM	-	Baud Rate Generator Double-Speed Mode Select
	RXDESEL	-	Asynchronous Start Bit Edge Detection Select

Register	Bit	RX630 (SCIc, SCId)	RX65N (SCIg, SCIi, SCIh)
FCR	-	-	FIFO Control Register
FDR	-	-	FIFO Data Count Register
LSR	-	-	Line Status Register
CDR	-	-	Comparison Data Register
DCCR	-	-	Data Comparison Control Register
SPTR	-	-	Serial Port Register
CR2	BCCS[1:0]	Bus Collision Detection Clock Select b5 b4 0 0: SCI base clock 0 1: SCI base clock frequency divided by 2 1 0: SCI base clock frequency divided by 4 1 1: Setting prohibited	Bus Collision Detection Clock Select • When SEMR.BGDM = 0 or SEMR.BGDM = 1 and SMR.CKS[1:0] = a value other than 00b b5 b4 0 0: SCI base clock 0 1: SCI base clock frequency divided by 2 1 0: SCI base clock frequency divided by 4 1 1: Setting prohibited • When SEMR.BGDM = 1 and SMR.CKS[1:0] = 00b b5 b4 0 0: SCI base clock frequency divided by 2 0 1: SCI base clock frequency divided by 4 1 0: Setting prohibited 1 1: Setting prohibited

2.25 I²C-bus Interface

Table 2.53 shows a Comparative Listing of I2C-bus Interface Specifications, and Table 2.54 shows a Comparative Listing of I2C-bus Interface Registers.

Table 2.53 Comparative Listing of I²C-bus Interface Specifications

Item	RX630 (RIIC)	RX65N (RIICa)
Number of channels	4 channels	2 channels / 3 channels*1
Communication format	• I²C bus format or SMBus format • Master mode or slave mode selectable • Automatic securing of the various set-up times, hold times, and bus-free times for the transfer rate	• I²C bus format or SMBus format • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate
Transfer speed	Up to 1 Mbps	Fast-mode Plus is supported (up to 1 Mbps)
SCL clock	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%.	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%.
Issuing and detection conditions	Start, restart, and stop conditions are automatically generated. Start conditions (including restart conditions) and stop conditions are detectable.	Start, restart, and stop conditions are generated automatically. Start conditions (including restart conditions) and stop conditions are detectable.
Slave addresses	• Up to three slave-address settings can be made. • Seven- and ten-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.
Acknowledgement	• For transmission, the acknowledge bit is automatically loaded. — Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. — If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.	• For transmission, the acknowledge bit is automatically loaded. — Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. — If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.

Item	RX630 (RIIC)	RX65N (RIICa)
Wait function	In reception, the following periods of waiting can be obtained by holding the clock signal (SCL) at the low level: • Waiting between the eighth and ninth clock cycles • Waiting between the ninth clock cycle and the first clock cycle of the next transfer (WAIT function)	In reception, the following periods of waiting can be obtained by holding the SCL clock at the low level: • Waiting between the eighth and ninth clock cycles • Waiting between the ninth clock cycle and the first clock cycle of the next transfer
SDA output delay function	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.
Arbitration	• For multi-master operation — Operation to synchronize the SCL (clock) signal in cases of conflict with the SCL signal from another master is possible. — When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the internal signal for the SDA line and the level on the SDA line not matching is detectable. • Loss of arbitration due to non-matching of internal and line levels for data is detectable in slave transmission.	• For multi-master operation — Operation to synchronize the SCL clock in cases of conflict with the SCL signal from another master is possible. — When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the internal signal for the SDA line and the level on the SDA line not matching is detectable. • Loss of arbitration due to non-matching of internal and line levels for data is detectable in slave transmission.
Timeout detection function	The internal time-out function is capable of detecting long-interval stop of the SCL (clock signal).	The internal timeout function is capable of detecting long-interval stop of the SCL clock.
Noise canceler	The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable by software.	The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable by software.

Item	RX630 (RIIC)	RX65N (RIICa)
Interrupt sources	Four sources • Error in transfer or occurrence of events (detection of AL, NACK, time-out, a start condition including a restart condition, or a stop condition) • Receive-data-full (including matching with a slave address) • Transmit-data-empty (including matching with a slave address) • Transmission complete	Four sources • Error in transfer or occurrence of events Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end
Low power consumption function	Module stop state can be set.	Module stop state can be set.
RIIC operating modes	Four modes Master transmit mode, master receive mode, slave transmit mode, and slave receive mode	Four modes Master transmit mode, master receive mode, slave transmit mode, and slave receive mode
Event link function	-	Four sources (RIIC0): • Error in transfer or occurrence of events Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end

*1: Can be used for products with at least 1.5 Mbytes of code flash memory.

Table 2.54 Comparative Listing of I²C-bus Interface Registers

Register	Bit	RX630 (RIIC)	RX65N (RIICa)
ICMR2	TMWE	Timeout Internal Counter Write Enable	-
TMOCNT	-	Timeout Internal Counter	-

2.26 CAN Module

Table 2.55 shows a Comparative Listing of CAN Module Specifications.

Table 2.55 Comparative Listing of CAN Module Specifications

Item	RX630 (CAN)	RX65N (CAN)
Number of channels	3 channels	2 channels
Protocol	ISO 11898-1 compliant (standard and extended frames)	ISO 11898-1 compliant (standard and extended frames)
Bit rate	Programmable bit rate up to 1 Mbps (fCAN ≥ 8 MHz) fCAN: CAN clock source	Programmable bit rate up to 1 Mbps (fCAN ≥ 8 MHz) fCAN: CAN clock source
Message box	32 mailboxes: Two selectable mailbox modes • Normal mailbox mode: 32 mailboxes can be configured for either transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for either transmission or reception. Of the other mailboxes, four FIFO stages can be configured for transmission and four FIFO stages for reception.	32 mailboxes: Two selectable mailbox modes • Normal mailbox mode: 32 mailboxes can be configured for either transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for either transmission or reception. Of the other mailboxes, four FIFO stages can be configured for transmission and four FIFO stages for reception.
Reception	• Data frame and remote frame can be received. • Selectable receiving ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot reception function • Selectable from overwrite mode (message overwritten) and overrun mode (message discarded) • The reception complete interrupt can be individually enabled or disabled for each mailbox.	• Data frame and remote frame can be received. • Selectable receiving ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot reception function • Selectable from overwrite mode (message overwritten) and overrun mode (message discarded) • The reception complete interrupt can be individually enabled or disabled for each mailbox.
Acceptance filter	• Eight acceptance masks (one mask for every four mailboxes) • The mask can be individually enabled or disabled for each mailbox.	• Eight acceptance masks (one mask for every four mailboxes) • The mask can be individually enabled or disabled for each mailbox.

Item	RX630 (CAN)	RX65N (CAN)
Transmission	• Data frame and remote frame can be transmitted. • Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot transmission function • Selectable from ID priority mode and mailbox number priority mode • Transmission request can be aborted (the completion of abort can be confirmed with a flag) • The transmission complete interrupt can be individually enabled or disabled for each mailbox.	• Data frame and remote frame can be transmitted. • Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot transmission function • Selectable from ID priority mode and mailbox number priority mode • Transmission request can be aborted (the completion of abort can be confirmed with a flag) • The transmission complete interrupt can be individually enabled or disabled for each mailbox.
Mode transition for bus-off recovery	Mode transition for the recovery from the bus-off state can be selected: • ISO 11898-1 Specifications compliant • Automatic entry to CAN halt mode at bus-off entry • Automatic entry to CAN halt mode at bus-off end • Entry to CAN halt mode by a program • Transition into error-active state by a program	Mode transition for the recovery from the bus-off state can be selected: • ISO 11898-1 Standards compliant • Automatic entry to CAN halt mode at bus-off entry • Automatic entry to CAN halt mode at bus-off end • Entry to CAN halt mode by a program • Transition into error-active state by a program
Error status monitoring	• CAN bus errors (stuff error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored. • Transition to error states can be detected (error-warning, error-passive, bus-off entry, and bus-off recovery). • The error counters can be read.	• CAN bus errors (stuff error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored. • Transition to error states can be detected (error-warning, error-passive, bus-off entry, and bus-off recovery). • The error counters can be read.
Time stamp function	• Time stamp function using a 16-bit counter • The reference clock can be selected from 1-, 2-, 4- and 8-bit time periods.	• Time stamp function using a 16-bit counter • The reference clock can be selected from 1-, 2-, 4- and 8-bit time periods.
Interrupt function	Five types of interrupt sources (reception complete, transmission complete, receive FIFO, transmit FIFO, and error interrupts)	Five types of interrupt sources (reception complete, transmission complete, receive FIFO, transmit FIFO, and error interrupts)
CAN sleep mode	Supply current can be reduced by stopping the CAN clock.	Current consumption can be reduced by stopping the CAN clock.
Software support unit	Three software support units: • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support	Three software support units: • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support
CAN clock source	Peripheral module clock (PCLK) or CANMCLK	Peripheral module clock (PCLKB) or CANMCLK

Item	RX630 (CAN)	RX65N (CAN)
Test mode	Three test modes available for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback)	Three test modes available for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback)
Power consumption reducing function	Module stop state can be set.	Module stop state can be set.

2.27 Serial Peripheral Interface

Table 2.56 shows a Comparative Listing of Serial Peripheral Interface Specifications, and Table 2.57 shows a Comparative Listing of Serial Peripheral Interface Registers.

Table 2.56 Comparative Listing of Serial Peripheral Interface Specifications

Item	RX630 (RSPI)	RX65N (RSPIc)
Number of channels	3 channels	3 channels
RSPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (four-wire method) or clock synchronous operation (three-wire method). • Transmit-only operation is available. • Capable of serial communications in master/slave mode • Switching of the polarity of the serial transfer clock • Switching of the phase of the serial transfer clock	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK
Data format	• MSB-first/LSB-first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits).	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits). • Byte swapping of transmit and receive data is selectable
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the divisor is 2 to 4096). • In slave mode, the externally input clock is used as the serial clock (the maximum frequency is that of PCLK divided by 8). Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4). Width at high level: 2 cycles of PCLK; width at low level: 2 cycles of PCLK

Item	RX630 (RSPI)	RX65N (RSPIc)
Buffer configuration	Double buffer configuration for the transmit/receive buffers	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection* • Parity error detection • Underrun error detection
SSL control function	• Four SSL signals (SSLn0 to SSLn3) for each channel • In single-master mode, SSLn0 to SSLn3 signals are output. • In multi-master mode: SSLn0 signal for input, and SSLn1 to SSLn3 signals for either output or unused. • In slave mode: SSLn0 signal for input, and SSLn1 to SSLn3 signals for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity	• Four SSL pins (SSLn0 to SSLn3) for each channel • In single-master mode, SSLn0 to SSLn3 pins are output. • In multi-master mode: SSLn0 pin for input, and SSLn1 to SSLn3 pins for either output or unused. • In slave mode: SSLn0 pin for input, and SSLn1 to SSLn3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity
Control in master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function

Item	RX630 (RSPI)	RX65N (RSPIc)
Interrupt sources	Maskable interrupt sources • RSPI receive interrupt (receive buffer full) • RSPI transmit interrupt (transmit buffer empty) • RSPI error interrupt (mode fault, overrun, parity error) • RSPI idle interrupt (RSPI idle)	Interrupt sources • Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, underrun, or parity error) • RSPI idle interrupt (RSPI idle)
Event link function (output)	-	The following events can be output to the event link controller. (RSPI0) • Receive buffer full signal • Transmit buffer empty signal • Mode fault, overrun, underrun, or parity error signal • RSPI idle signal • Transmission-completed signal
Other functions	• Function for initializing the RSPI • Loopback mode	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Note: * In master reception and when the RSPCK auto-stop function is enabled, an overrun error does not occur because the transfer clock is stopped at the timing of overrun error detection.

Table 2.57 Comparative Listing of Serial Peripheral Interface Registers

Register	Bit	RX630 (RSPI)	RX65N (RSPIc)
SPSR	MODF	Mode Fault Error Flag 0: No mode fault error occurs 1: A mode fault error occurs	Mode Fault Error Flag 0: Neither a mode fault error nor an underrun error occurs 1: A mode fault error or an underrun error occurs
	UDRF	-	Underrun Error Flag
	SPTEF		Transmit Buffer Empty Flag
	SPRF		Receive Buffer Full Flag
SPDR	-	RSPI Data Register Accessible size • Longwords access (the SPLW bit is 1) • Words access (the SPLW bit is 0)	RSPI Data Register Accessible size • Longwords access (the SPLW bit is 1 and the SPBYT bit is 0) • Words access (the SPLW bit is 0 and the SPBYT bit is 0) • Bytes access (the SPBYT bit is 1)
SPDCR	SPBYT	-	RSPI Byte Access Specification
SPCR2	SCKASE	-	RSPCK Auto-Stop Function Enable
SPDCR2	-	-	RSPI Data Control Register 2

2.28 CRC Calculator

Table 2.58 shows a Comparative Listing of CRC Calculator Specifications, and Table 2.59 shows a Comparative Listing of CRC Calculator Registers.

Table 2.58 Comparative Listing of CRC Calculator Specifications

Item	RX630 (CRC)	RX65N (CRCA)	
Data size	8 bits	8 bits	32 bits
Data for CRC calculation	CRC code generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 32n-bit units (where n is a whole number)
CRC processor unit	Operation executed on 8 bits in parallel	8-bit parallel processing	32-bit parallel processing
CRC generating polynomial	One of three generating polynomials selectable: • 8-bit CRC — $X^8 + X^2 + X + 1$ • 16-bit CRC — $X^{16} + X^{15} + X^2 + 1$ — $X^{16} + X^{12} + X^5 + 1$	One of five generating polynomials selectable: • 8-bit CRC — $X^8 + X^2 + X + 1$ • 16-bit CRC — $X^{16} + X^{15} + X^2 + 1$ — $X^{16} + X^{12} + X^5 + 1$	One of five generating polynomials selectable: • 32-bit CRC — $X^{32} + X^{26} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ — $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$
CRC calculation switching	CRC code generation for LSB-first or MSB-first communication selectable	The order of the bits produced by CRC calculation can be switched for LSB first or MSB first communication	
Low power consumption function	Module stop state can be set.	Module stop state can be set.	

Table 2.59 Comparative Listing of CRC Calculator Registers

Register	Bit	RX630 (CRC)	RX65N (CRCA)
CRCCR	GPS[1:0]:RX630 GPS[2:0]:RX65N	CRC Generating Polynomial Switching b1 b0 0 0: No calculation is executed. 0 1: $X^8 + X^2 + X + 1$ 1 0: $X^{16} + X^{15} + X^2 + 1$ 1 1: $X^{16} + X^{12} + X^5 + 1$	CRC Generating Polynomial Switching b2 b0 0 0 0: No calculation is executed. 0 0 1: 8-bit CRC ($X^8 + X^2 + X + 1$) 0 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$) 0 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$) 1 0 0: 32-bit CRC ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1 : 32-bit CRC ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) 1 1 0: No calculation is executed. 1 1 1: No calculation is executed.
	LMS	CRC Calculation Switching (b2)	CRC Calculation Switching (b6)
CRCDIR	-	CRC Data Input Register Accessible size • Bytes access	CRC Data Input Register Accessible size • Longwords access (When 32-bit CRC is selected) • Bytes access (When 16-bit or 8-bit CRC is selected)
CRCDOR	-	CRC Data Output Register Accessible size • Words access When an 8-bit CRC is in use, the valid CRC code is obtained in the low-order byte (b7 to b0).	CRC Data Output Register Accessible size • Longwords access (When 32-bit CRC is selected) • Words access (When 16-bit CRC is selected) • Bytes access (When 8-bit CRC is selected)

2.29 12-Bit A/D Converter

Table 2.60 shows a Comparative Listing of 12-Bit A/D Converter Specifications, and Table 2.61 shows a Comparative Listing of 12-Bit A/D Converter Registers.

Table 2.60 Comparative Listing of 12-Bit A/D Converter Specifications

Item	RX630 (S12ADa)	RX65N (S12ADFa)
Number of units	1 unit	2 units
Input channels	Up to 21 channels	Unit 0: 8 channels Unit 1: 21 channels + one extended channel
Extended analog function	Temperature sensor output, internal reference voltage	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	1.0 μs per channel (when A/D conversion clock ADCLK = 50 MHz)	0.48 μs per channel (12-bit conversion mode) 0.45 μs per channel (10-bit conversion mode) 0.42 μs per channel (8-bit conversion mode) (A/D conversion clock: when ADCLK operates at 60 MHz)
A/D conversion clock (ADCLK)	4 types: PCLK, PCLK/2, PCLK/4, PCLK/8	Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. PCLK to ADCLK frequency ratio = 1:1, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.

Item	RX630 (S12ADa)	RX65N (S12ADFa)
Data register	• For analog input: 21 data registers • For temperature sensor: One data register • For internal reference voltage: One data register • The A/D conversion result is held in a 12-bit A/D data register. • In A/D-converted value addition mode, A/D conversion results are stored in a 14-bit A/D data register.	• 29 registers for analog input (eight for Unit0 and 21 for Unit1), 1 for A/D-converted data duplication in double trigger mode per unit, and 2 for A/D-converted data duplication during extended operation in double trigger mode per unit. • One register for temperature sensor (Unit1) • One register for internal reference (Unit1) • One register for self-diagnosis per unit • The results of A/D conversion are stored in 12-bit A/D data registers. • 8-, 10-, and 12-bit accuracy output for the results of A/D conversion • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.

Item	RX630 (S12ADa)	RX65N (S12ADFa)
Operating modes	• Single scan mode: — A/D conversion is to be performed for only once on the analog inputs of up to 21 arbitrarily selected channels. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: — A/D conversion is to be performed sequentially on the analog inputs of up to 21 arbitrarily selected channels. (Do not use continuous scan mode when temperature sensor output or A/D internal reference voltage is selected.)	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 8 channels (Unit0) / 21 channels (Unit1) arbitrarily selected. — A/D conversion is performed only once on the temperature sensor output (Unit1). — A/D conversion is performed only once on the internal reference voltage (Unit1). — A/D conversion is performed only once on the extended analog input (Unit1). • Continuous scan mode: — A/D conversion is performed repeatedly on the analog input of up to 8 channels (Unit0) / 21 channels (Unit1) arbitrarily selected, temperature sensor output (Unit1), and internal reference voltage (Unit1) of the arbitrarily selected channel. — A/D conversion is performed repeatedly on the extended analog input (Unit1). • Group scan mode: — Two (groups A and B) or three (groups A, B, and C) can be selected as the number of the groups to be used. Only the combination of groups A and B can be selected when the number of the groups is two. — Analog inputs, temperature sensor output (Unit1), and internal reference voltage (Unit1) that are arbitrarily selected are divided into two groups (group A and B) or three groups (group A, B, and C), and A/D conversion of the analog input selected on a group basis is performed only once. — The conditions for scanning start of groups A, B, and C (synchronous trigger) can be independently selected, thus allowing A/D conversion of each group to be started independently.

Item	RX630 (S12ADa)	RX65N (S12ADFa)
Operating modes	-	• Group scan mode (when group priority control selected): — If a priority-group trigger is input during scanning of the low-priority group, scan of the low-priority group is stopped and scan of the priority group is started. The priority order is group A (highest) > group B > group C (lowest). — Whether or not to restart scanning of the low-priority group after processing for the high-priority group completes, is selectable. Rescan can also be set to start either from the beginning of the selected channel or the channel on which A/D conversion is not completed.
Conditions for A/D conversion start	• Software trigger • Synchronous trigger Trigger by MTU, TPU, or TMR • Asynchronous trigger A/D conversion can be started by the ADTRG0# pin.	• Software trigger • Synchronous trigger Trigger by the multi-function timer pulse unit (MTU), 8-bit timer (TMR), 16-bit timer pulse unit (TPU), or event link controller (ELC). • Asynchronous trigger A/D conversion can be triggered by the external trigger ADTRG0# (Unit0) or ADTRG1# (Unit1) pin (independently for two units).
Functions	• Sample-and-hold function • Number of sampling states is adjustable. • A/D-converted value addition mode	• Sample-and-hold function • Channel-dedicated sample-and-hold function (three channels for Unit0 only) • Variable sampling state count (settable for each channel) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection assist function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • 12-/10-/8-bit conversion switching • Automatic clear function of A/D data registers • Extended analog input • Comparison function (windows A and B)

Item	RX630 (S12ADa)	RX65N (S12ADFa)
Interrupt sources	• A scan end interrupt (S12ADI0) request can be generated on completion of A/D conversion. • An S12ADI0 interrupt can activate the DMAC or DTC.	• In the modes except double trigger mode and group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of single scan. (independently for two units). • In double trigger mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of double scan. (independently for two units). • In group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of group A scan, whereas a scan end interrupt request (GBADI or GBADI1) for group B can be generated on completion of group B scan, and a group C scan end interrupt request (GCADI or GCADI1) can be generated on completion of group C scan. • When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of double scan of group A, and the corresponding scan end interrupt request (GBADI/GCADI or GBADI1/GCADI1) can be generated on completion of group B and group C scan. • A compare interrupt request (S12CMPAI, S12CMPAI1, S12CMPBI, or S12CMPBI1) can be generated upon a match with the comparison condition for the digital compare function. • The S12ADI/S12ADI1, GBADI/GBADI1, and GCADI/GCADI1 interrupts can activate the DMA controller (DMAC) and data transfer controller (DTC).
Event link function	-	• An ELC event is generated upon completion of all scans • Able to start scanning by a trigger from the ELC
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Table 2.61 Comparative Listing of 12-Bit A/D Converter Registers

Register	Bit	RX630 (S12ADa)	RX65N (S12ADFa)
ADDBLDR	-	-	A/D Data Duplication Register
ADDBLDRA	-	-	A/D Data Duplication Register A
ADDBLDRB	-	-	A/D Data Duplication Register B
ADRD	-	-	A/D Self-Diagnosis Data Register
ADCSR	DBLANS[4:0]	-	Double Trigger Channel Select
	GBADIE	-	Group B Scan End Interrupt Enable
	DBLE	-	Double Trigger Mode Select
	EXTRG	Trigger Select (b0)	Trigger Select (b8)
	TRGE	Trigger Start Enable (b1)	Trigger Start Enable (b9)
	CKS[1:0]	A/D Conversion Clock Select	-
	ADIE	Scan End Interrupt Enable (b4)	Scan End Interrupt Enable (b12)
	ADCS:RX630 ADCS[1:0]:RX65N	Scan Mode Select b6 0: Single scan mode 1: Continuous scan mode	Scan Mode Select b14b13 0 0: Single scan mode 0 1: Group scan mode 1 0: Continuous scan mode 1 1: Setting prohibited
	ADST	A/D Conversion Start (b7)	A/D Conversion Start (b15)
ADANS0	-	A/D Channel Select Register 0	-
ADANS1	-	A/D Channel Select Register 1	-
ADANSA0	-	-	A/D Channel Select Register A0
ADANSA1	-	-	A/D Channel Select Register A1
ADANSB0	-	-	A/D Channel Select Register B0
ADANSB1	-	-	A/D Channel Select Register B1
ADANSC0	-	-	A/D Channel Select Register C0
ADANSC1	-	-	A/D Channel Select Register C1
ADADS0	-	A/D-Converted Value Addition Mode Select Register 0	A/D-Converted Value Addition/Average Function Select Register 0
ADADS1	-	A/D-Converted Value Addition Mode Select Register 1	A/D-Converted Value Addition/Average Function Select Register 1

Register	Bit	RX630 (S12ADa)	RX65N (S12ADFa)
ADADC	-	A/D-Converted Value Addition Count Select Register	A/D-Converted Value Addition/ Average Count Select Register
	ADC[1:0]:RX630 ADC[2:0]:RX65N	Addition Count Select b1b0 0 0: 1-time conversion (no addition; same as normal conversion) 0 1: 2-time conversion (addition once) 1 0: 3-time conversion (addition twice) 1 1: 4-time conversion (addition three times)	Addition Count Select b2 b0 0 0 0: 1-time conversion (no addition; same as normal conversion) 0 0 1: 2-time conversion (addition once) 0 1 0: 3-time conversion (addition twice) 0 1 1: 4-time conversion (addition three times) 1 0 1: 16-time conversion (addition 15 times) Settings other than above are prohibited.
	AVEE	-	Average Mode Enable
ADCER	ADPRC[1:0]	-	A/D Conversion Resolution Setting
	DIAGVAL[1:0]	-	Self-Diagnosis Conversion Voltage Select
	DIAGLD	-	Self-Diagnosis Mode Select
	DIAGM	-	Self-Diagnosis Enable
ADSTRGR	ADSTRS[3:0]	A/D Conversion Start Trigger Select	-
	TRSB[5:0]	-	A/D Conversion Start Trigger Select for Group B
	TRSA[5:0]	-	A/D Conversion Start Trigger Select
ADEXICR	TSSAD	Temperature Sensor Output A/D Converted Value Addition Mode Select	Temperature Sensor Output A/D Converted Value Addition/ Averaging Mode Select
	OCSAD	A/D Internal Reference Voltage A/D Converted Value Addition Mode Select	Internal Reference Voltage A/D Converted Value Addition/ Average Mode Select
	TSS	Temperature Sensor Output A/D Conversion Select	-
	TSSA	-	Temperature Sensor Output A/D Conversion Select
	OCS	A/D Internal Reference Voltage A/D Conversion Select	-
	OCSA	-	Internal Reference Voltage A/D Conversion Select
	TSSB	-	Temperature Sensor Output A/D Conversion Select
	OCSB	-	Internal Reference Voltage A/D Conversion Select
	EXSEL[1:0]	-	Extended Analog Input Select
	EXOEN	-	Extended Analog Output Control

Register	Bit	RX630 (S12ADa)	RX65N (S12ADFa)
ADGCEXCR	-	-	A/D Group C Extended Input Control Register
ADGCTRGR	-	-	A/D Group C Trigger Select Register
ADSSTR01	-	A/D Sampling State Register 01	-
ADSSTR23	-	A/D Sampling State Register 23	-
ADSSTRn	-	-	A/D Sampling State Register n (n = 0 to 15, L, T, O)
ADSHCR	-	-	A/D Sample-and-Hold Circuit Control Register
ADSHMSR	-	-	A/D Sample-and-Hold Operating Mode Select Register
ADDISCR	-	-	A/D Disconnection Detection Control Register
ADGSPCR	-	-	A/D Group Scan Priority Control Register
ADCMPCR	-	-	A/D Comparison Function Control Register
ADCMPANSR0	-	-	A/D Comparison Function Window A Channel Select Register 0
ADCMPANSR1	-	-	A/D Comparison Function Window A Channel Select Register 1
ADCMPANSER	-	-	A/D Comparison Function Window A Extended Input Select Register
ADCMPLR0	-	-	A/D Comparison Function Window A Comparison Condition Setting Register 0
ADCMPLR1	-	-	A/D Comparison Function Window A Comparison Condition Setting Register 1
ADCMPLER	-	-	A/D Comparison Function Window A Extended Input Comparison Condition Setting Register
ADCMPDR0	-	-	A/D Comparison Function Window A Lower Level Setting Register
ADCMPDR1	-	-	A/D Comparison Function Window A Upper Level Setting Register
ADCMPSR0	-	-	A/D Comparison Function Window A Channel Status Register 0
ADCMPSR1	-	-	A/D Comparison Function Window A Channel Status Register 1
ADCMPSER	-	-	A/D Comparison Function Window A Extended Input Channel Status Register

Register	Bit	RX630 (S12ADa)	RX65N (S12ADFa)
ADWINMON	-	-	A/D Comparison Function Window A/B Status Monitoring Register
ADCMPBNSR	-	-	A/D Comparison Function Window B Channel Select Register
ADWINLLB	-	-	A/D Comparison Function Window B Lower Level Setting Register
ADWINULB	-	-	A/D Comparison Function Window B Upper Level Setting Register
ADCMPBSR	-	-	A/D Comparison Function Window B Channel Status Register
ADSAM	-	-	A/D Conversion Time Setting Register
ADSAMPR	-	-	A/D Conversion Time Setting Protection Release Register

2.30 D/A Converter

Table 2.62 shows a Comparative Listing of D/A Converter Specifications, and Table 2.63 shows a Comparative Listing of D/A Converter Registers.

Table 2.62 Comparative Listing of D/A Converter Specifications

Item	RX630 (DAa)	RX65N (R12DA)
Resolution	10 bits	12 bits
Output channel	2 channels	2 channels
Countermeasure against mutual interference between analog modules	Measure against interference between D/A and A/D conversion D/A converted data update timing is controlled by the 10-bit A/D converter synchronous D/A conversion enable input signal from the 10-bit A/D converter (degradation of A/D conversion accuracy caused by interference is reduced by controlling the D/A converter inrush current generation timing with the enable signal).	Measure against interference between D/A and A/D conversion: D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable input signal from the 12-bit A/D converter (unit 1). Therefore, the degradation of A/D conversion accuracy due to interference is reduced by controlling the timing in which the 12-bit D/A converter inrush current occurs, with the enable signal.
Low power consumption function	Module-stop state can be set for each unit.	Module stop state can be set.
Event link function (input)	-	DA0 conversion can be started when an event signal is input.
Output buffer amplifier control function	-	Buffered output (gain = 1) or unbuffered output can be selected.

Table 2.63 Comparative Listing of D/A Converter Registers

Register	Bit	RX630 (DAa)	RX65N (R12DA)
DADRm	-	D/A Data Register m (DADRm) (m = 0, 1) 10-bit data can be relocated by setting the DPSEL bit in DADPR.	D/A Data Register m (DADRm) (m = 0, 1) 12-bit data can be relocated by setting the DADPR.DPSEL bit.
DAAMPCR	-	-	D/A Output Amplifier Control Register *1
DAASWCR	-	-	D/A Output Amplifier Stabilization Wait Control Register *1
DAADUSR	-	-	D/A A/D Synchronous Unit Select Register

2.31 Temperature Sensor

Table 2.64 shows a Comparative Listing of Temperature Sensor Registers.

Table 2.64 Comparative Listing of Temperature Sensor Registers

Register	Bit	RX630	RX65N (TEMPS)
TSCDRH, TSCDRL :RX630 TSCDR :RX65N	-	Temperature Sensor Calibration Data Register TSCDRH :(b3-b0) TSCDRL :(b7-b0) The TSCDR register stores temperature sensor calibration data measured for each chip at factory shipment.	Temperature Sensor Calibration Data Register TSCDR : (b11 to b0) The TSCDR register stores temperature sensor calibration data measured for each chip at factory shipment.

2.32 RAM

Table 2.65 shows a Comparative Listing of RAM Specifications, and Table 2.66 shows a Comparative Listing of RAM Registers.

Table 2.65 Comparative Listing of RAM Specifications

Item	RX630	RX65N
RAM capacity	• 64 KB RAM0: 64 KB • 96 KB RAM0: 64 KB RAM1: 32 KB • 128 KB RAM0: 64 KB RAM1: 64 KB	256 KB RAM0: 256 KB 384 KB*1 Expansion RAM: 384 KB
RAM address	• When the RAM capacity is 64 KB RAM0: 0000 0000h to 0000 FFFFh RAM1: - • When the RAM capacity is 96 KB RAM0: 0000 0000h to 0000 FFFFh RAM1: 0001 0000h to 0001 7FFFh • When the RAM capacity is 128 KB RAM0: 0000 0000h to 0000 FFFFh RAM1: 0001 0000h to 0001 FFFFh	RAM0: 0000 0000h to 0003 FFFFh Expansion RAM: 0080 0000h to 0085 FFFFh*1
Access	• Single-cycle access is possible for both reading and writing. • RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. • Enabling or disabling of the RAM is selectable.
Data retention function	Data in RAM0 can be retained in deep software standby mode.	Not available in deep software standby mode (Data in Standby RAM can be retained)
Low power consumption function	The module-stop state is independently selectable for RAM0 and RAM1.	The module-stop state is selectable.
Error checking function	-	• Detection of 1-bit errors • A non-maskable interrupt or interrupt is generated in response to an error.

*1: Can be used for products with at least 1.5 Mbytes of code flash memory.

Table 2.66 Comparative Listing of RAM Registers

Register	Bit	RX630	RX65N
RAMMODE	-	-	RAM Operating Mode Control Register
RAMSTS	-	-	RAM Error Status Register
RAMECAD	-	-	RAM Error Address Capture Register
RAMPRCR	-	-	RAM Protection Register
EXRAMMODE	-	-	Expansion RAM Operating Mode Control Register*1
EXRAMSTS	-	-	Expansion RAM Error Status Register*1
EXRAMECAD	-	-	Expansion RAM Error Address Capture Register*1
EXRAMPRCR	-	-	Expansion RAM Protection Register*1

*1: Can be used for products with at least 1.5 Mbytes of code flash memory.

2.33 Flash Memory (Code Flash)

Table 2.67 shows a Comparative Listing of Flash Memory (Code Flash) Specifications, and Table 2.68 shows a Comparative Listing of Flash Memory Registers

Table 2.67 Comparative Listing of Flash Memory (Code Flash) Specifications

Item	RX630	RX65N
Memory space	• User area: 2 Mbytes max. • User boot area: 16 Kbytes	User area: 2 Mbytes max.*1
ROM cache	-	• Capacity: 256 Bytes • Mapping method: 8-way set associative • Replace method: LRU method • Line size: 16 bytes
Read cycle	A read operation takes one cycle of ICLK	When the cache is hit: One cycle When the cache is missed: One cycle if ICLK ≤ 50 MHz Two cycles if 50 MHz < ICLK ≤ 100 MHz Three cycles if ICLK > 100 MHz
Value after erase	FFh	FFh
Programming/erasing method	• The chip incorporates a dedicated sequencer (FCU) for programming of the ROM/E2 DataFlash. • Programming and erasing the ROM/E2 DataFlash are handled by issuing commands to the FCU. • Programming/erasure through transfer by a dedicated flash-memory programmer via a serial interface (serial programming) • Programming/erasure of flash memory by a user program (self-programming)	• The chip incorporates a dedicated sequencer (FCU) for programming and erasure of the flash memory. • Programming and erasing the code flash memory is handled by the FACI commands specified in the FACI command issuing area (007E 0000h) • Programming/erasure through transfer by a dedicated flash-memory programmer via a serial interface (serial programming) • Programming/erasure of flash memory by a user program (self-programming)
Security function	Prevents unauthorized modification or reading of data	Protects against illicit tampering with or reading out of data in flash memory
Protection function	• Software controlled protection: The registers and lock bits can be set to prevent unintentional programming. • FCU command-lock: When abnormal operations are detected during programming/erasure, this function disables any further programming/erasure.	Protects against erroneous programming of the flash memory
Dual bank function *1	-	The dual-bank structure makes a safe update possible in cases where programming is suspended. • Linear mode: the code flash memory is used as one area • Dual mode: the code flash memory is divided into two areas

Item	RX630	RX65N
Trusted Memory (TM) function	-	Protects against illicit reading of blocks 8 and 9 in the code flash memory Dual mode: blocks 8, 9 ,46, and 47*1
Background Operation (BGO)	The CPU is able to execute program code from the ROM while the E2 DataFlash memory is being programmed or erased.	• The code flash memory can be read while the code flash memory is being programmed or erased.*1 • The data flash memory can be read while the code flash memory is being programmed or erased.*1 • The code flash memory can be read while the data flash memory is being programmed or erased.*1
Suspension and resumption	• The CPU is able to execute program code from the ROM during suspension of programming or erasure. • Programming and erasure of the ROM can be restarted (resumed) after suspension.	• The CPU is able to execute program code from the Code Flash during suspension of programming or erasure. • Programming and erasure of the Code Flash can be restarted (resumed) after suspension.
Units of programming and erasure	• Units of programming for the user area or user boot area: 128 bytes • Units of erasure for the user area: In block units • Units of erasure for the user boot area: 16 Kbytes	• Units of programming for the user area: 128 bytes • Units of erasure for the user area: Block units
Other functions	Interrupts can be accepted during self-programming (When interrupt vector address are set other than ROM.)	Interrupts can be accepted during self-programming (When interrupt and exception vector addresses are set other than code flash memory.)
	In the initial settings of this MCU, an expansion area of the option-setting memory can be set	In the initial settings of this MCU, an expansion area of the option-setting memory can be set.

Item	RX630	RX65N
On-board programming	• Programming in boot mode (for the SCI interface) — The asynchronous serial interface (SCI1) is used. — The transfer rate is adjusted automatically. — The user boot area can also be programmed. • Programming in USB boot mode — USB0 is used. — Dedicated hardware is not required, so direct connection to a PC is possible. • Programming in the user boot mode — Able to create original boot programs of the user's making. • Programming by a routine for ROM programming within the user program — This allows ROM programming without resetting the system.	• Programming/erasure in boot mode (for the SCI interface) — The asynchronous serial interface (SCI1) is used. — The transfer rate is adjusted automatically. • Programming/erasure in boot mode (for the USB interface) — USBb is used — Dedicated hardware is not required, so direct connection to a PC is possible. • Programming/erasure in boot mode (for the FINE interface) — FINE is used. • Programming/erasure by a routine for code flash memory programming within the user program — This allows code flash memory programming without resetting the system
Off-board programming	A Flash programmer can be used to program the user area and user boot area	A flash programmer can be used to program or erase the user area
Unique ID	A 16-byte ID code provided for each MCU(The unique ID is only available for the G-version products.)	A 16-byte ID code provided for each MCU

*1: Can be used for products with at least 1.5 Mbytes of code flash memory.

Table 2.68 Comparative Listing of Flash Memory Registers

Register	Bit	RX630	RX65N
FWEPROR	FLWE[1:0]	Flash Programming/Erasure b1 b0 0 0: Disables programming and erasure of the ROM, programming and erasure of lock bits, reading of lock bits, and blank checking 0 1: Enables programming and erasure of the ROM, programming and erasure of lock bits, reading of lock bits, and blank checking 1 0: Disables programming and erasure of the ROM, programming and erasure of lock bits, reading of lock bits, and blank checking 1 1: Disables programming and erasure of the ROM, programming and erasure of lock bits, reading of lock bits, and blank checking	Flash Programming and Erasure Enabling b1 b0 0 0: Prohibits programming/erasure, and blank checking*1. 0 1: Permits programming/erasure, and blank checking*1. 1 0: Prohibits programming/erasure, and blank checking*1. 1 1: Prohibits programming/erasure, and blank checking*1.
FMODR	-	Flash Mode Register	-
FASTAT	DFLWPE	E2 DataFlash Programming/Erasure Protection Violation Flag	-
	DFLRPE	E2 DataFlash Read Protection Violation Flag	-
	DFLAE	E2 DataFlash Access Violation Flag	-
	ROMAE	ROM Access Violation Flag	-
	DFAE	-	Data Flash Access Error Flag*1
	CFAE	-	Code Flash Access Error Flag
FAEINT	DFLWPEIE	E2 DataFlash Programming/Erasure Protection Violation Interrupt Enable	-
	DFLRPEIE	E2 DataFlash Read Protection Violation Interrupt Enable	-
	DFLAEIE	E2 DataFlash Access Violation Interrupt Enable	-
	ROMAEIE	ROM Access Violation Interrupt Enable	-
	DFAEIE	-	Data Flash Access Error Interrupt Enable*1
	CFAEIE	-	Code Flash Access Error Interrupt Enable
DFLRE0	-	E2 DataFlash Read Enable Register 0	-
DFLRE1	-	E2 DataFlash Read Enable Register 1	-
DFLWE0	-	E2 DataFlash P/E Enable Register 0	-

Register	Bit	RX630	RX65N
DFLWE1	-	E2 DataFlash P/E Enable Register 1	-
FSADDR	-	-	FACI Command Start Address Register
FEADDR	-	-	FACI Command End Address Register
FCURAME	-	FCU RAM Enable Register	-
FSTATR0	-	Flash Status Register 0	-
FSTATR1	-	Flash Status Register 1	-
FSTATR	-	-	Flash Status Register
FENTRYR	FENTRY0	ROM P/E Mode Entry 0	-
	FENTRYC	-	Code Flash Memory P/E Mode Entry
	FENTRY1	ROM P/E Mode Entry 1	-
	FENTRY2	ROM P/E Mode Entry 2	-
	FENTRY3	ROM P/E Mode Entry 3	-
	FENTRYD	E2 DataFlash P/E Mode Entry	Data Flash Memory P/E Mode Entry*1
	FEKEY[7:0]	Key Code	-
	KEY[7:0]	-	Key Code
FPROTR	-	Flash Protection Register	-
FRESETR	-	Flash Reset Register	-
FCMDR	-	FCU Command Register	FACI Command Register
FCPSR	-	FCU Processing Switching Register	Flash Sequencer Processing Switching Register
FSUINITR	-	-	Flash Sequencer Set-Up Initialization Register
FAWMON	-	-	Flash Access Window Monitor Register
DFLBCCNT	-	E2 DataFlash Blank Check Control Register	-
FPESTAT	-	Flash P/E Status Register	-
DFLBCSTAT	-	E2 DataFlash Blank Check Status Register	-
FBCCNT	-	-	Data Flash Blank Check Control Register*1
FBCSTAT	-	-	Data Flash Blank Check Status Register*1
FPSADDR	-	-	Data Flash Programming Start Address Register*1
FPCKAR	-	-	Flash Sequencer Processing Clock Notification Register
FSUACR	-	-	Start-Up Area Control Register
PCKAR	-	Peripheral Clock Notification Register	-
ROMCE	-	-	ROM Cache Enable Register
ROMCIV	-	-	ROM Cache Invalidate Register
EEPFCLK	-	-	Data Flash Memory Access Frequency Setting Register*1

*1: Can be used for products with at least 1.5 Mbytes of code flash memory.

2.34 Flash Memory (Data Flash)

Table 2.69 shows a Comparative Listing of Flash Memory (Data Flash) Specifications.

Table 2.69 Comparative Listing of Flash Memory (Data Flash) Specifications

Item	RX630	RX65N*1
Memory capacity	32 Kbytes	32 Kbytes
Value after erasure	Undefined	Undefined
Block configuration	Block: 32 bytes	Block: 64 bytes
Number of blocks	1024	512

*1: Can be used for products with at least 1.5 Mbytes of code flash memory.

2.35 Package (LQFP100/144 only)

There are some differences in the outline drawing of the LQFP100, LQFP144 package, so please be careful when designing the board.

For details, refer to Design Guide for Migration between RX Family: Differences in Package External form (R01AN4591EJ).

Table 2.70 Comparison of package codes

Item	RX630	RX65N
100 pin LFQFP	PLQP0100KB-A	PLQP0100KB-B
144 pin LFQFP	PLQP0144KA-A	PLQP0144KA-B

3. Comparison of Pin Functions

A comparison of the pin functions, power supply, clock, system control pins is provided below.

Blue character : Items that exist only in either group.

Red character : Items that exist in both group, but they have differences.

Black character : Items that are same specification.

3.1 144/145pin Package

Table 3.1 shows a Comparative Listing of Pin Functions (144/145pin Package).

Table 3.1 Comparative Listing of Pin Functions (144/145pin Package)

144pin LFQFP	145pin TFLGA	RX630	RX65N
1	A1	AVSS0	AVSS0
2	B3	P05/IRQ13/DA1	P05/IRQ13/DA1
3	B1	VREFH	AVCC1
4	D3	P03/IRQ11/DA0	P03/IRQ11/DA0
5	C1	VREFL	AVSS1
6	C2	P02/TMCI1/SCK6/IRQ10/AN020	P02/TMCI1/SCK6/IRQ10/AN120
7	D4	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/AN019	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/AN119
8	D1	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/AN018	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/AN118
9	D2	PF5/IRQ4	PF5/IRQ4
10	E4	EMLE	EMLE
11	E3	PJ5	PJ5/POE8#/CTS2#/RTS2#/SS2#
12	A10	VSS	VSS
13	F3	PJ3/MTIOC3C/CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0#	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0#
14	E2	VCL	VCL
15	F4	VBATT	VBATT
16	G3	MD/FINED	MD/FINED
17	F1	XCIN	XCIN
18	F2	XCOUT	XCOUT
19	G2	RES#	RES#
20	G1	P37/XTAL	P37/XTAL
21	C6	VSS	VSS
22	H1	P36/EXTAL	P36/EXTAL
23	B10	VCC	VCC
24	H4	P35/NMI	P35/UPSEL/NMI
25	J1	P34/TRST#/MTIOC0A/TMCI3/PO12/POE2#/SCK6/SCK0/IRQ4	P34/TRST#/MTIOC0A/TMCI3/PO12/POE10#/SCK6/SCK0/ET0_LINKSTA/IRQ4
26	J2	P33/MTIOC0D/TIOCD0/TMRI3/PO11/POE3#/RXD6/RXD0/SMISO6/SMISO0/SSCL6/SSCL0/CRX0/IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/POE4#/POE11#/RXD6/RXD0/SMISO6/SMISO0/SSCL6/SSCL0/CRX0/PCKO/IRQ3-DS

144pin LFQFP	145pin TFLGA	RX630	RX65N
27	J3	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCOUT/RTCIC2/TXD6/TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/CTX0/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCOUT/RTCIC2/POE0#/POE10#/TXD6/TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS
28	K3	P31/TMS/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0/IRQ1-DS	P31/TMS/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS
29	J4	P30/TDI/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB/IRQ0-DS	P30/TDI/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS
30	K1	P27/TCK/FINEC/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB	P27/TCK/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB-A
31	K2	P26/TDO/CS6#/MTIOC2A/TMO1/PO6/TXD1/CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/MOSIB	P26/TDO/CS6#/MTIOC2A/TMO1/PO6/TXD1/CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/MOSIB-A
32	L1	P25/CS5#/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/ADTRG0#	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/HSYNC/ADTRG0#/(SDHI_CD)*1
33	L4	P24/CS4#/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/PIXCLK/(SDHI_WP)*1
34	L2	P23/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/SSDA3	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/SSDA3/PIXD7/(SDHI_D1-C) *1
35	M1	P22/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB/PIXD6/(SDHI_D0-C)*1
36	N1	P21/MTIOC1B/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/SCL1/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/USB0_EXICEN/PIXD5/IRQ9/(SCL1/SDHI_CLK-C)*1
37	N2	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/SDA1/IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/USB0_ID/PIXD4/IRQ8/(SDA1/SDHI_CMD-C)*1
38	M2	P17/MTIOC3A/MTIOC3B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/MISOA/SDA2-DS/IETXD/IRQ7/ADTRG#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/PIXD3/IRQ7/ADTRG1#/(SDHI_D3-C) *1
39	N3	P87/TIOCA2	P87/MTIOC4C/TIOCA2/TXD10/SMOSI10/SSDA10/PIXD2/(SDHI_D2-C)*1
40	L3	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/SMISO3/SSDA1/SSCL3/MOSIA/SCL2-DS/IERXD/USB0_VBUS/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/SMISO3/SSDA1/SSCL3/SCL2-DS/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0#
41	M3	P86/TIOCA0	P86/MTIOC4D/TIOCA0/RXD10/SMISO10/SSCL10/PIXD1
42	K4	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/CRX1-DS/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/CRX1-DS/PIXD0/IRQ5

144pin LFQFP	145pin TFLGA	RX630	RX65N
43	N4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_DPUPE/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/IRQ4
44	L5	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG#	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG1#
45	M4	P12/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/IRQ2	P12/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/IRQ2
46	M5	VCC_USB	VCC_USB
47	N5	USB0_DM	USB0_DM
48	N6	USB0_DP	USB0_DP
49	M6	VSS_USB	VSS_USB
50	L6	P56/MTIOC3C/TIOCA1	P56/EDACK1/MTIOC3C/TIOCA1/(SCK7)*1
51	N7	P55/TRDATA3/WAIT#/MTIOC4D/TMO3/CRX1/IRQ10	P55/TRDATA3/WAIT#/EDREQ0/MTIOC4D/TMO3/CRX1/ET0_EXOUT/IRQ10/(D0[A0/D0]/TXD7/SMOSI7/SSDA7)*1
52	K5	P54/TRDATA2/ALE/MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/CTX1	P54/TRDATA2/ALE/EDACK0/MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/CTX1/ET0_LINKSTA/(D1[A1/D1])*1
53	K6	P53/BCLK	P53/BCLK
54	L7	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A
55	K7	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A
56	M7	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A
57	C13	VSS	VSS
58	L8	P83/TRCLK/MTIOC4C/CTS10#/RTS10#/SS10#	P83/TRCLK/EDACK1/MTIOC4C/CTS10#/SS10#/ET0_CRS/RMII0_CRS_DV/SCK10
59	D5	VCC	VCC
60	N9	PC7/A23/CS0#/MTIOC3A/MTCLKB/TIOCB6/TMO2/PO31/TXD8/SMOSI8/SSDA8/MISOA/IRQ14	PC7/UB/A23/CS0#/MTIOC3A/MTCLKB/TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/SSDA8/MISOA-A/ET0_COL/TXD10/SMOSI10/SSDA10/MMC_D7-A/IRQ14
61	M8	PC6/A22/CS1#/MTIOC3C/MTCLKA/TIOCA6/TMCI2/PO30/RXD8/SMISO8/SSCL8/MOSIA/IRQ13	PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/TIC0/PO30/RXD8/SMISO8/SSCL8/MOSIA-A/ET0_ETXD3/RXD10/SMISO10/SSCL10/MMC_D6-A/IRQ13/(D2[A2/D2])*1
62	L9	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TIOCD6/TCLKF/TMRI2/PO29/SCK8/RSPCKA	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/PO29/SCK8/RSPCKA-A/ET0_ETXD2/SCK10/MMC_D5-A/(D3[A3/D3])*1
63	N10	P82/TRSYNC/MTIOC4A/PO28/TXD10/SMOSI10/SSDA10	P82/TRSYNC/EDREQ1/MTIOC4A/PO28/TXD10/SMOSI10/SSDA10/ET0_ETXD1/RMII0_TXD1/MMC_D4-A
64	M9	P81/TRDATA1/MTIOC3D/PO27/RXD10/SMISO10/SSCL10	P81/TRDATA1/EDACK0/MTIOC3D/PO27/RXD10/SMISO10/SSCL10/ET0_ETXD0/RMII0_TXD0/MMC_D3-A/SDHI_CD-A/QIO3-A/(SDHI_CD)*1

144pin LFQFP	145pin TFLGA	RX630	RX65N
65	K9	P80/TRDATA0/MTIOC3B/PO26/SCK10	P80/TRDATA0/EDREQ0/MTIOC3B/PO26/SCK10/RTS10#/ET0_TX_EN/RMII0_TXD_EN/MMC_D2-A/SDHI_WP-A/QIO2-A/(SDHI_WP)*1
66	L10	PC4/A20/CS3#/MTIOC3D/MTCLKC/TIOCC6/TCLKE/TMCI1/PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0-A/ET0_TX_CLK/CTS10#/RTS10#/SS10#/MMC_D1-A/SDHI_D1-A/SDSI_D1-A/QIO1-A/QMI-A
67	N11	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/SMOSI5/SSDA5/IETXD	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/SMOSI5/SSDA5/ET0_TX_ER/MMC_D0-A/SDHI_D0-A/SDSI_D0-A/QIO0-A/QMO-A
68	M10	P77/CS7#/PO23/TXD11/SMOSI11/SSDA11	P77/TRDATA7/CS7#/PO23/TXD11/SMOSI11/SSDA11/ET0_RX_ER/RMII0_RX_ER/MMC_CLK-A/SDHI_CLK-A/SDSI_CLK-A/QSPCLK-A
69	K10	P76/CS6#/PO22/RXD11/SMISO11/SSCL11	P76/TRDATA6/CS6#/PO22/RXD11/SMISO11/SSCL11/ET0_RX_CLK/REF50CK0/MMC_CMD-A/SDHI_CMD-A/SDSI_CMD-A/QSSL-A
70	L11	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/SMISO5/SSCL5/SSLA3/IERXD	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/SMISO5/SSCL5/SSLA3-A/ET0_RX_DV/MMC_CD-A/SDHI_D3-A/SDSI_D3-A
71	N12	P75/CS5#/PO20/SCK11	P75/TRSYNC1/CS5#/PO20/SCK11/RTS11#/ET0_ERXD0/RMII0_RXD0/MMC_RES#-A/SDHI_D2-A/SDSI_D2-A
72	N13	P74/CS4#/PO19/CTS11#/RTS11#/SS11#	P74/TRDATA5/A20/CS4#/PO19/CTS11#/SS11#/ET0_ERXD1/RMII0_RXD1
73	M12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/SSLA2/SDA3/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/SSLA2-A/ET0_ERXD2/IRQ12
74	D11	PL1	VCC
75	M11	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1/SCL3/IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14
76	E1	PL0	VSS
77	L12	P73/CS3#/PO16	P73/TRDATA4/CS3#/PO16/ET0_WOL
78	K11	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/SMOSI9/SSDA9	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/SMOSI9/SSDA9/ET0_CRS/RMII0_CRS_DV/TXD11/SMOSI11/SSDA11/SDSI_D1-B
79	K12	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/SMISO9/SSCL9	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/SMISO9/SSCL9/ET0_ETXD1/RMII0_TXD1/RXD11/SMISO11/SSCL11/SDSI_D0-B
80	K13	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE1#/SCK9	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE4#/SCK9/ET0_ETXD0/RMII0_TXD0/SCK11/SDSI_CLK-B/(LCD_CLK-B)*1

144pin LFQFP	145pin TFLGA	RX630	RX65N
81	J11	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/SS9#	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/SS9#/ET0_TX_EN/RMII0_TXD_EN/CTS11#/RTS11#/SS11#/SDSI_CMD-B/(LCD_TCON0-B)*1
82	J10	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE3#/SCK4/SCK6	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ET0_RX_ER/RMII0_RX_ER/SDSI_D3-B/(LCD_TCON1-B)*1
83	J12	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/RTS4#/CTS6#/RTS6#/SS4#/SS6#	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/RTS4#/CTS6#/RTS6#/SS4#/SS6#/ET0_RX_CLK/REF50CK0/SDSI_D2-B/(LCD_TCON2-B)*1
84	J13	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/TXD4/TXD6/SMOSI4/SMOSI6/SSDA4/SSDA6/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/TXD4/TXD6/SMOSI4/SMOSI6/SSDA4/SSDA6/ET0_ERXD0/RMII0_RXD0/IRQ4-DS/(LCD_TCON3-B)*1
85	H10	P72/CS2#	P72/A19/CS2#/ET0_MDC
86	H11	P71/CS1#	P71/A18/CS1#/ET0_MDIO
87	H12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/RXD6/SMISO4/SMISO6/SSCL4/SSCL6/RSPCKA/IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/RXD6/SMISO4/SMISO6/SSCL4/SSCL6/ET0_ERXD1/RMII0_RXD1/IRQ12/(LCD_DATA0-B)*1
88	H13	PA7/A7/TIOCB2/PO23/MISOA	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/(LCD_DATA1-B)*1
89	G11	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE2#/CTS5#/RTS5#/SS5#/MOSIA	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE10#/CTS5#/RTS5#/SS5#/MOSIA-B/ET0_EXOUT/(LCD_DATA2-B)*1
90	G10	PA5/A5/TIOCB1/PO21/RSPCKA	PA5/A5/MTIOC6B/TIOCB1/PO21/RSPCKA-B/ET0_LINKSTA/(LCD_DATA3-B)*1
91	G12	VCC	VCC
92	G13	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/TXD5/SMOSI5/SSDA5/SSLA0/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ET0_MDC/IRQ5-DS/(LCD_DATA4-B)*1
93	F11	VSS	VSS
94	F10	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/RXD5/SMISO5/SSCL5/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/RXD5/SMISO5/SSCL5/ET0_MDIO/IRQ6-DS/(LCD_DATA5-B)*1
95	F13	PA2/A2/PO18/RXD5/SMISO5/SSCL5/SSLA3	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/SSCL5/SSLA3-B/(LCD_DATA6-B)*1
96	F12	PA1/A1/MTIOC0B/MTCLKC/TIOCB0/PO17/SCK5/SSLA2/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/PO17/SCK5/SSLA2-B/ET0_WOL/IRQ11/(LCD_DATA7-B)*1

144pin LFQFP	145pin TFLGA	RX630	RX65N
97	E10	PA0/A0/BC0#/MTIOC4A/TIOCA0/PO16/SSLA1	PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/CACREF/PO16/SSLA1-B/ET0_TX_EN/RMII0_TXD_EN/(LCD_DATA8-B)*1
98	E13	P67/CS7#/CRX2/IRQ15	P67/CS7#/DQM1/MTIOC7C/IRQ15
99	E11	P66/CS6#/CTX2	P66/CS6#/DQM0/MTIOC7D
100	E12	P65/CS5#	P65/CS5#/CKE
101	D10	PE7/D15[A15/D15]/TIOCB11/MISOB/IRQ7/AN5	PE7/D15[A15/D15]/MTIOC6A/TOC1/MISOB-B/MMC_RES#-B/SDHI_WP-B/IRQ7/AN105/(D7[A7/D7]/LCD_DATA9-B)*1
102	D13	PE6/D14[A14/D14]/TIOCA11/CTS4#/RTS4#/SS4#/MOSIB/IRQ6/AN4	PE6/D14[A14/D14]/MTIOC6C/TIC1/MOSIB-B/MMC_CD-B/SDHI_CD-B/IRQ6/AN104/(D6[A6/D6]/SDHI_CD/LCD_DATA10-B)*1
103	H2	PK5/TXD4/SMOSI4/SSDA4	VCC
104	C12	P70/SCK4	P70/SDCLK
105	H3	PK4/RXD4/SMISO4/SSCL4	VSS
106	D12	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/TIOCB10/RSPCKB/IRQ5/AN3	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/ET0_RX_CLK/REF50CK0/RSPCKB-B/IRQ5/AN103/(D5[A5/D5]/LCD_DATA11-B)*1
107	B13	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/TIOCA10/PO28/SSLB0/AN2	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/PO28/ET0_ERXD2/SSLB0-B/AN102/(D4[A4/D4]/LCD_DATA12-B)*1
108	A13	PE3/D11[A11/D11]/MTIOC4B/TIOCB9/PO26/POE8#/CTS12#/RTS12#/SS12#/MISOB/AN1	PE3/D11[A11/D11]/MTIOC4B/PO26/POE8#/TOC3/CTS12#/RTS12#/SS12#/ET0_ERXD3/MMC_D7-B/AN101/(D3[A3/D3]/LCD_DATA13-B)*1
109	B12	PE2/D10[A10/D10]/MTIOC4A/TIOCA9/PO23/RXD12/SMISO12/SSCL12/RXDX12/SSLB3/MOSIB/IRQ7-DS/AN0	PE2/D10[A10/D10]/MTIOC4A/PO23/TIC3/RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B/MMC_D6-B/IRQ7-DS/AN100/(D2[A2/D2]/LCD_DATA14-B)*1
110	A12	PE1/D9[A9/D9]/MTIOC4C/TIOCD9/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2/RSPCKB/ANEX1	PE1/D9[A9/D9]/MTIOC4C/MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B/MMC_D5-B/ANEX1/(D1[A1/D1]/LCD_DATA15-B)*1
111	C11	PE0/D8[A8/D8]/TIOCC9/SCK12/SSLB1/ANEX0	PE0/D8[A8/D8]/MTIOC3D/SCK12/SSLB1-B/MMC_D4-B/ANEX0/(D0[A0/D0]/LCD_DATA16-B)*1
112	D9	P64/CS4#	P64/CS4#/WE#/(D3[A3/D3])*1
113	C10	P63/CS3#	P63/CS3#/CAS#/(D2[A2/D2])*1
114	A11	P62/CS2#	P62/CS2#/RAS#/(D1[A1/D1])*1
115	B11	P61/CS1#/CTS9#/RTS9#/SS9#	P61/CS1#/SDCS#/(D0[A0/D0])*1
116	L13	PK3/RXD9/SMISO9/SSCL9	VSS
117	D8	P60/CS0#/SCK9	P60/CS0#
118	K8	PK2/TXD9/SMOSI9/SSDA9	VCC
119	C9	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3/IRQ7/AN7	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3/MMC_D1-B/SDHI_D1-B/QIO1-B/QMI-B/IRQ7/AN107/(SSLC3-A/LCD_DATA17-B)*1

144pin LFQFP	145pin TFLGA	RX630	RX65N
120	A9	PD6/D6[A6/D6]/MTIC5V/POE1#/SSLC2/IRQ6/AN6	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/SSLC2/MMC_D0-B/SDHI_D0-B/QIO0-B/QMO-B/IRQ6/AN106/(SSLC2-A/LCD_DATA18-B)*1
121	D7	PD5/D5[A5/D5]/MTIC5W/POE2#/SSLC1/IRQ5/AN013	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/SSLC1/MMC_CLK-B/SDHI_CLK-B/QSPCLK-B/IRQ5/AN113/(SSLC1-A/LCD_DATA19-B)*1
122	B9	PD4/D4[A4/D4]/POE3#/SSLC0/IRQ4/AN012	PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0/MMC_CMD-B/SDHI_CMD-B/QSSL-B/IRQ4/AN112/(SSLC0-A/LCD_DATA20-B)*1
123	C8	PD3/D3[A3/D3]/TIOCB8/TCLKH/POE8#/RSPCKC/IRQ3/AN011	PD3/D3[A3/D3]/MTIOC8D/POE8#/TOC2/RSPCKC/MMC_D3-B/SDHI_D3-B/QIO3-B/IRQ3/AN111/(RSPCKC-A/LCD_DATA21-B)*1
124	A8	PD2/D2[A2/D2]/MTIOC4D/TIOCA8/MISOC/CRX0/IRQ2/AN010	PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0/MISOC/MMC_D2-B/SDHI_D2-B/QIO2-B/IRQ2/AN110/(MISOC-A/LCD_DATA22-B)*1
125	C7	PD1/D1[A1/D1]/MTIOC4B/TIOCB7/TCLKG/MOSIC/CTX0/IRQ1/AN009	PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0/MOSIC/IRQ1/AN109/(MOSIC-A/LCD_DATA23-B)*1
126	B8	PD0/D0[A0/D0]/TIOCA7/IRQ0/AN008	PD0/D0[A0/D0]/POE4#/IRQ0/AN108/(LCD_EXTCLK-B)*1
127	D6	P93/A19/CTS7#/RTS7#/SS7#/AN017	P93/A19/POE0#/CTS7#/RTS7#/SS7#/AN117
128	A7	P92/A18/RXD7/SMISO7/SSCL7/AN016	P92/A18/POE4#/RXD7/SMISO7/SSCL7/AN116
129	B7	P91/A17/SCK7/AN015	P91/A17/SCK7/AN115
130	N8	VSS	VSS
131	A6	P90/A16/TXD7/SMOSI7/SSDA7/AN014	P90/A16/TXD7/SMOSI7/SSDA7/AN114
132	M13	VCC	VCC
133	B6	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
134	C5	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
135	A5	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
136	E5	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
137	B5	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
138	A4	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
139	C4	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
140	B4	VREFL0	VREFL0
141	A3	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
142	C3	VREFH0	VREFH0
143	B2	AVCC0	AVCC0
144	A2	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
-	G4	BSCANP	BSCANP

*1: Can be used for products with at least 1.5 Mbytes of code flash memory.

3.2 100pin Package

Table 3.2 shows a Comparative Listing of Pin Functions (100pin Package).

Table 3.2 Comparative Listing of Pin Functions (100pin Package)

100pin LFQFP	100pin TFLGA	RX630	RX65N
1	A2	VREFH	AVCC1
2	B1	EMLE	EMLE
3	C2	VREFL	AVSS1
4	C3	PJ3/MTIOC3C/CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0#	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0#
5	C1	VCL	VCL
6	D4	VBATT	VBATT
7	D3	MD/FINED	MD/FINED
8	D1	XCIN	XCIN
9	D2	XCOUT	XCOUT
10	E3	RES#	RES#
11	E1	P37/XTAL	P37/XTAL
12	E2	VSS	VSS
13	F1	P36/EXTAL	P36/EXTAL
14	F2	VCC	VCC
15	F3	P35/NMI	P35/UPSEL/NMI
16	E4	P34/TRST#/MTIOC0A/TMCI3/PO12/POE2#/SCK6/SCK0/IRQ4	P34/TRST#/MTIOC0A/TMCI3/PO12/POE10#/SCK6/SCK0/ET0_LINKSTA/IRQ4
17	G1	P33/MTIOC0D/TIOCD0/TMRI3/PO11/POE3#/RXD6/RXD0/SMISO6/SMISO0/SSCL6/SSCL0/CRX0/IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/POE4#/POE11#/RXD6/RXD0/SMISO6/SMISO0/SSCL6/SSCL0/CRX0/IRQ3-DS
18	F4	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCOUT/RTCIC2/TXD6/TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/CTX0/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCOUT/RTCIC2/POE0#/POE10#/TXD6/TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/CTX0/USB0_VBUSEN/IRQ2-DS
19	G2	P31/TMS/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0/IRQ1-DS	P31/TMS/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS
20	G3	P30/TDI/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB/IRQ0-DS	P30/TDI/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS
21	G4	P27/TCK/FINEC/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB	P27/TCK/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB-A
22	H1	P26/TDO/CS6#/MTIOC2A/TMO1/PO6/TXD1/CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/MOSIB	P26/TDO/CS6#/MTIOC2A/TMO1/PO6/TXD1/CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/MOSIB-A
23	H2	P25/CS5#/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/ADTRG0#	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/ADTRG0#
24	J1	P24/CS4#/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN

100pin LFQFP	100pin TFLGA	RX630	RX65N
25	K1	P23/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/SSDA3	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/SSDA3
26	K2	P22/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB
27	J2	P21/MTIOC1B/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/USB0_EXICEN/IRQ9/(SCL1)*1
28	K3	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/USB0_ID/IRQ8/(SDA1)*1
29	J3	P17/MTIOC3A/MTIOC3B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/MISOA/SDA2-DS/IETXD/IRQ7/ADTRG#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/IRQ7/ADTRG1#
30	H3	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/SMISO3/SSDA1/SSCL3/MOSIA/SCL2-DS/IERXD/USB0_VBUS/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/SMISO3/SSDA1/SSCL3/SCL2-DS/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0#
31	H4	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/CRX1-DS/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/CRX1-DS/IRQ5
32	K4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_DPUPE/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/IRQ4
33	J4	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG#	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG1#
34	F5	P12/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/IRQ2	P12/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/IRQ2
35	J6	VCC_USB	VCC_USB
36	K5	USB0_DM	USB0_DM
37	K6	USB0_DP	USB0_DP
38	J5	VSS_USB	VSS_USB
39	H5	P55/WAIT#/MTIOC4D/TMO3/CRX1/IRQ10	P55/WAIT#/EDREQ0/MTIOC4D/TMO3/CRX1/ET0_EXOUT/IRQ10/(D0[A0/D0])*1
40	H6	P54/ALE/MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/CTX1	P54/ALE/EDACK0/MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/CTX1/ET0_LINKSTA/(D1[A1/D1])*1
41	G5	P53/BCLK	P53/BCLK
42	G6	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A
43	K7	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A
44	J7	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A
45	H7	PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/PO31/TXD8/SMOSI8/SSDA8/MISOA/IRQ14	PC7/UB/A23/CS0#/MTIOC3A/MTCLKB/TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/SSDA8/MISOA-A/ET0_COL/TXD10/SMOSI10/SSDA10/IRQ14

100pin LFQFP	100pin TFLGA	RX630	RX65N
46	H8	PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/PO30/RXD8/SMISO8/SSCL8/MOSIA/IRQ13	PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/TIC0/PO30/RXD8/SMISO8/SSCL8/MOSIA-A/ET0_ETXD3/RXD10/SMISO10/SSCL10/IRQ13/(D2[A2/D2])*1
47	K8	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/PO29/SCK8/RSPCKA	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/PO29/SCK8/RSPCKA-A/ET0_ETXD2/SCK10/(D3[A3/D3])*1
48	J8	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0-A/ET0_TX_CLK/CTS10#/RTS10#/SS10#
49	K9	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/SMOSI5/SSDA5/IETXD	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/SMOSI5/SSDA5/ET0_TX_ER
50	K10	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/SMISO5/SSCL5/SSLA3/IERXD	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/SMISO5/SSCL5/SSLA3-A/ET0_RX_DV
51	J10	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/SSLA2/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/SSLA2-A/ET0_ERXD2/IRQ12
52	J9	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1/IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14
53	H10	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/SMOSI9/SSDA9	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/SMOSI9/SSDA9/ET0_CRS/RMII0_CRS_DV/TXD11/SMOSI11/SSDA11/SDSI_D1-B
54	H9	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/SMISO9/SSCL9	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/SMISO9/SSCL9/ET0_ETXD1/RMII0_TXD1/RXD11/SMISO11/SSCL11/SDSI_D0-B
55	G7	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE1#/SCK9	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE4#/SCK9/ET0_ETXD0/RMII0_TXD0/SCK11/SDSI_CLK-B/(LCD_CLK-B)*1
56	G8	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/SS9#	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/SS9#/ET0_TX_EN/RMII0_TXD_EN/CTS11#/RTS11#/SS11#/SDSI_CMD-B/(LCD_TCON0-B)*1
57	F6	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE3#/SCK6	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE11#/SCK6/ET0_RX_ER/RMII0_RX_ER/SDSI_D3-B/(LCD_TCON1-B)*1
58	F7	PB2/A10/TIOCC3/TCLKC/PO26/CTS6#/RTS6#/SS6#	PB2/A10/TIOCC3/TCLKC/PO26/CTS6#/RTS6#/SS6#/ET0_RX_CLK/REF50CK0/SDSI_D2-B/(LCD_TCON2-B)*1
59	G9	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/TXD6/SMOSI6/SSDA6/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/TXD6/SMOSI6/SSDA6/ET0_ERXD0/RMII0_RXD0/IRQ4-DS/(LCD_TCON3-B)*1
60	G10	VCC	VCC
61	F8	PB0/A8/MTIC5W/TIOCA3/PO24/RXD6/SMISO6/SSCL6/RSPCKA/IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD6/SMISO6/SSCL6/ET0_ERXD1/RMII0_RXD1/IRQ12/(LCD_DATA0-B)*1
62	F10	VSS	VSS

100pin LFQFP	100pin TFLGA	RX630	RX65N
63	F9	PA7/A7/TIOCB2/PO23/MISOA	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/(LCD_DATA1-B)*1
64	E7	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE2#/CTS5#/RTS5#/SS5#/MOSIA	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE10#/CTS5#/RTS5#/SS5#/MOSIA-B/ET0_EXOUT/(LCD_DATA2-B)*1
65	E9	PA5/A5/TIOCB1/PO21/RSPCKA	PA5/A5/MTIOC6B/TIOCB1/PO21/RSPCKA-B/ET0_LINKSTA/(LCD_DATA3-B)*1
66	E8	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/TXD5/SMOSI5/SSDA5/SSLA0/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ET0_MDC/IRQ5-DS/(LCD_DATA4-B)*1
67	E10	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/RXD5/SMISO5/SSCL5/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/RXD5/SMISO5/SSCL5/ET0_MDIO/IRQ6-DS/(LCD_DATA5-B)*1
68	E6	PA2/A2/PO18/RXD5/SMISO5/SSCL5/SSLA3	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/SSCL5/SSLA3-B/(LCD_DATA6-B)*1
69	D9	PA1/A1/MTIOC0B/MTCLKC/TIOCB0/PO17/SCK5/SSLA2/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/PO17/SCK5/SSLA2-B/ET0_WOL/IRQ11/(LCD_DATA7-B)*1
70	D10	PA0/A0/BC0#/MTIOC4A/TIOCA0/PO16/SSLA1	PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/CACREF/PO16/SSLA1-B/ET0_TX_EN/RMII0_TXD_EN/(LCD_DATA8-B)*1
71	D8	PE7/D15[A15/D15]/MISOB/IRQ7/AN5	PE7/D15[A15/D15]/MTIOC6A/TOC1/MISOB-B/MMC_RES#-B/SDHI_WP-B/IRQ7/AN105/(D7[A7/D7]/LCD_DATA9-B)*1
72	D7	PE6/D14[A14/D14]/MOSIB/IRQ6/AN4	PE6/D14[A14/D14]/MTIOC6C/TIC1/MOSIB-B/MMC_CD-B/SDHI_CD-B/IRQ6/AN104/(D6[A6/D6]/SDHI_CD/LCD_DATA10-B)*1
73	C9	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/RSPCKB/IRQ5/AN3	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/ET0_RX_CLK/REF50CK0/RSPCKB-B/IRQ5/AN103/(D5[A5/D5]/LCD_DATA11-B)*1
74	C10	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/PO28/SSLB0/AN2	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/PO28/ET0_ERXD2/SSLB0-B/AN102/(D4[A4/D4]/LCD_DATA12-B)*1
75	B10	PE3/D11[A11/D11]/MTIOC4B/PO26/POE8#/CTS12#/RTS12#/SS12#/MISOB/AN1	PE3/D11[A11/D11]/MTIOC4B/PO26/POE8#/TOC3/CTS12#/RTS12#/SS12#/ET0_ERXD3/MMC_D7-B/AN101/(D3[A3/D3]/LCD_DATA13-B)*1
76	A10	PE2/D10[A10/D10]/MTIOC4A/PO23/RXD12/SMISO12/SSCL12/RXDX12/SSLB3/MOSIB/IRQ7-DS/AN0	PE2/D10[A10/D10]/MTIOC4A/PO23/TIC3/RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B/MMC_D6-B/IRQ7-DS/AN100/(D2[A2/D2]/LCD_DATA14-B)*1
77	A9	PE1/D9[A9/D9]/MTIOC4C/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2/RSPCKB/ANEX1	PE1/D9[A9/D9]/MTIOC4C/MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B/MMC_D5-B/ANEX1/(D1[A1/D1]/LCD_DATA15-B)*1

100pin LFQFP	100pin TFLGA	RX630	RX65N
78	A8	PE0/D8[A8/D8]/SCK12/SSLB1/ANEX0	PE0/D8[A8/D8]/MTIOC3D/SCK12/SSLB1-B/MMC_D4-B/ANEX0/(D0[A0/D0]/LCD_DATA16-B)*1
79	B9	PD7/D7[A7/D7]/MTIC5U/POE0#/IRQ7/AN7	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3/MMC_D1-B/SDHI_D1-B/QIO1-B/QMI-B/IRQ7/AN107/(SSLC3-A/LCD_DATA17-B)*1
80	B8	PD6/D6[A6/D6]/MTIC5V/POE1#/IRQ6/AN6	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/SSLC2/MMC_D0-B/SDHI_D0-B/QIO0-B/QMO-B/IRQ6/AN106/(SSLC2-A/LCD_DATA18-B)*1
81	C8	PD5/D5[A5/D5]/MTIC5W/POE2#/IRQ5/AN013	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/SSLC1/MMC_CLK-B/SDHI_CLK-B/QSPCLK-B/IRQ5/AN113/(SSLC1-A/LCD_DATA19-B)*1
82	A7	PD4/D4[A4/D4]/POE3#/IRQ4/AN012	PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0/MMC_CMD-B/SDHI_CMD-B/QSSL-B/IRQ4/AN112/(SSLC0-A/LCD_DATA20-B)*1
83	B7	PD3/D3[A3/D3]/POE8#/IRQ3/AN011	PD3/D3[A3/D3]/MTIOC8D/POE8#/TOC2/RSPCKC/MMC_D3-B/SDHI_D3-B/QIO3-B/IRQ3/AN111/(RSPCKC-A/LCD_DATA21-B)*1
84	C7	PD2/D2[A2/D2]/MTIOC4D/CRX0/IRQ2/AN010	PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0/MISOC/MMC_D2-B/SDHI_D2-B/QIO2-B/IRQ2/AN110/(MISOC-A/LCD_DATA22-B)*1
85	B6	PD1/D1[A1/D1]/MTIOC4B/CTX0/IRQ1/AN009	PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0/MOSIC/IRQ1/AN109/(MOSIC-A/LCD_DATA23-B)*1
86	A6	PD0/D0[A0/D0]/IRQ0/AN008	PD0/D0[A0/D0]/POE4#/IRQ0/AN108/(LCD_EXTCLK-B)*1
87	C6	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
88	D6	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
89	D5	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
90	B5	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
91	A5	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
92	C5	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
93	E5	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
94	A4	VREFL0	VREFL0
95	B4	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
96	C4	VREFH0	VREFH0
97	B3	AVCC0	AVCC0
98	A3	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
99	B2	AVSS0	AVSS0
100	A1	P05/IRQ13/DA1	P05/IRQ13/DA1

*1: Can be used for products with at least 1.5 Mbytes of code flash memory.

3.3 176/177pin Package

Table3.3 shows a Comparative Listing of Pin Functions (176/177pin Package).

Table 3.3 Comparative Listing of Pin Functions (176/177pin Package)

176pin LFQFP	176/177 pin TFLGA LFBGA	RX630	RX65N (Code flash more than 1.5 MB)
1	A1	AVSS0	AVSS0
2	B1	P05/ IRQ13/ DA1	P05/ IRQ13/ DA1
3	C2	VREFH	AVCC1
4	D3	P03/ IRQ11/ DA0	P03/ IRQ11/ DA0
5	C1	VREFL	AVSS1
6	D2	P02/ TMCI1/ SCK6/ IRQ10/ AN020	P02/ TMCI1/ SCK6/ IRQ10/ AN120
7	D1	P01/ TMCI0/ RXD6/ SMISO6/ SSCL6/ IRQ9/ AN019	P01/ TMCI0/ RXD6/ SMISO6/ SSCL6/ IRQ9/ AN119
8	D4	P00/ TMRI0/ TXD6/ SMOSI6/ SSDA6/ IRQ8/ AN018	P00/ TMRI0/ TXD6/ SMOSI6/ SSDA6/ IRQ8/ AN118
9	E3	PF5/ IRQ4	PF5/ IRQ4
10	E2	EMLE	EMLE
11	E1	PJ5	PJ5/ POE8#/ CTS2#/ RTS2#/ SS2#
12	A7	VSS	VSS
13	F3	PJ3/ MTIOC3C/ CTS6#/ RTS6#/ CTS0#/ RTS0#/ SS6#/ SS0#	PJ3/ EDACK1/ MTIOC3C/ ET0_EXOUT/ CTS6#/ RTS6#/ SS6#/ CTS0#/ RTS0#/ SS0#
14	F2	VCL	VCL
15	F1	VBATT	VBATT
16	-	NC	NC
17	G4	TRST#/ PF4	TRST#/ PF4
18	G3	MD/ FINED	MD/ FINED
19	G1	XCIN	XCIN
20	G2	XCOUT	XCOUT
21	H3	RES#	RES#
22	H1	XTAL/ P37	XTAL/ P37
23	E4/B12	VSS	VSS
24	J1	EXTAL/ P36	EXTAL/ P36
25	A6	VCC	VCC
26	H4	P35/ NMI	UPSEL/ P35
27	J3	P34/ MTIOC0A/ TMCI3/ PO12/ POE2#/ SCK6/ SCK0/ IRQ4	P34/ MTIOC0A/ TMCI3/ PO12/ POE10#/ ET0_LINKSTA/ SCK6/ SCK0/ IRQ4
28	K1	P33/ MTIOC0D/ TIOCD0/ TMRI3/ PO11/ POE3#/ RXD6/ RXD0/ SMISO6 / SMISO0/ SSCL6/ SSCL0/ CRX0/ IRQ3-DS	P33/ EDREQ1/ MTIOC0D/ TIOCD0/ TMRI3/ PO11/ POE4#/ POE11#/ RXD6/ SMISO6/ SSCL6/ RXD0/ SMISO0/ SSCL0/ CRX0/ PCKO/ IRQ3-DS

176pin LFQFP	176/177 pin TFLGA LFBGA	RX630	RX65N (Code flash more than 1.5 MB)
29	K2	P32/ MTIOC0C/ TIOCC0/ TMO3/ PO10/ RTCOUT/ RTCIC2/ TXD6/ TXD0/ SMOSI6/ SMOSI0/ SSDA6/ SSDA0/ CTX0/ IRQ2-DS	P32/ MTIOC0C/ TIOCC0/ TMO3/ PO10/ RTCIC2/ RTCOUT/ POE0#/ POE10#/ TXD6/ SMOSI6/ SSDA6/ TXD0/ SMOSI0/ SSDA0/ CTX0/ USB0_VBUSEN/ VSYNC/ IRQ2-DS
30	J4	TMS/ PF3	TMS/ PF3
31	K3	TDI/ PF2/ RXD1/ SMISO1/ SSCL1	TDI/ PF2/ RXD1/ SMISO1/ SSCL1
32	L1	P31/ MTIOC4D/ TMCI2/ PO9/ RTCIC1/ CTS1#/ RTS1#/ SS1#/ SSLB0/ IRQ1-DS	P31/ MTIOC4D/ TMCI2/ PO9/ RTCIC1/ CTS1#/ RTS1#/ SS1#/ SSLB0-A/ IRQ1-DS
33	L2	P30/ MTIOC4B/ TMRI3/ PO8/ RTCIC0/ POE8#/ RXD1/ SMISO1/ SSCL1/ MISOB/ IRQ0-DS	P30/ MTIOC4B/ TMRI3/ PO8/ RTCIC0/ POE8#/ RXD1/ SMISO1/ SSCL1/ MISOB-A/ IRQ0-DS
34	K4	TCK/ FINEC/ PF1/ SCK1	TCK/ PF1/ SCK1
35	L3	TDO/ PF0/ TXD1/ SMOSI1/ SSDA1	TDO/ PF0/ TXD1/ SMOSI1/ SSDA1
36	M1	P27/ CS7#/ MTIOC2B/ TMCI3/ PO7/ SCK1/ RSPCKB	P27/ CS7#/ MTIOC2B/ TMCI3/ PO7/ SCK1/ RSPCKB-A
37	M2	P26/ CS6#/ MTIOC2A/ TMO1/ PO6/ TXD1/ CTS3#/ RTS3#/ SMOSI1/ SS3#/ SSDA1/ MOSIB	P26/ CS6#/ MTIOC2A/ TMO1/ PO6/ TXD1/ SMOSI1/ SSDA1/ CTS3#/ RTS3#/ SS3#/ MOSIB-A
38	L4	P25/ CS5#/ MTIOC4C/ MTCLKB/ TIOCA4/ PO5/ RXD3/ SMISO3/ SSCL3/ ADTRG0#	P25/ CS5#/ EDACK1/ MTIOC4C/ MTCLKB/ TIOCA4/ PO5/ RXD3/ SMISO3/ SSCL3/ SDHI_CD/ HSYNC/ ADTRG0#
39	N1/A9	PH5	VCC
40	M3	P24/ CS4#/ MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/ PO4/ SCK3	P24/ CS4#/ EDREQ1/ MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/ PO4/ SCK3/ USB0_VBUSEN/ SDHI_WP/ PIXCLK
41	P1/C14	PH4	VSS
42	N2	P23/ MTIOC3D/ MTCLKD/ TIOCD3/ PO3/ TXD3/ CTS0#/ RTS0#/ SMOSI3/ SS0#/ SSDA3	P23/ EDACK0/ MTIOC3D/ MTCLKD/ TIOCD3/ PO3/ TXD3/ SMOSI3/ SSDA3/ CTS0#/ RTS0#/ SS0#/ SDHI_D1-C/ PIXD7
43	N3	P22/ MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/ PO2/ SCK0	P22/ EDREQ0/ MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/ PO2/ SCK0/ USB0_OVRCURB/ SDHI_D0-C/ PIXD6
44	R1	P21/ MTIOC1B/ TIOCA3/ TMCI0/ PO1/ RXD0/ SMISO0/ SSCL0/ SCL1/ IRQ9	P21/ MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/ PO1/ RXD0/ SMISO0/ SSCL0/ SCL1/ USB0_EXICEN/ SDHI_CLKC/ PIXD5/ IRQ9
45	R2	P20/ MTIOC1A/ TIOCB3/ TMRI0/ PO0/ TXD0/ SMOSI0/ SSDA0/ SDA1/ IRQ8	P20/ MTIOC1A/ TIOCB3/ TMRI0/ PO0/ TXD0/ SMOSI0/ SSDA0/ SDA1/ USB0_ID/ SDHI_CMD-C/ PIXD4/ IRQ8

176pin LFQFP	176/177 pin TFLGA LFBGA	RX630	RX65N (Code flash more than 1.5 MB)
46	P2	P17/ MTIOC3A/ MTIOC3B/ TIOCB0/ TCLKD/ TMO1/ PO15/ POE8#/ SCK1/ TXD3/ SMOSI3/ SSDA3/ MISOA/ SDA2-DS/ IETXD/ IRQ7/ ADTRG#	P17/ MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/ TMO1/ PO15/ POE8#/ SCK1/ TXD3/ SMOSI3/ SSDA3/ SDA2-DS/ SDHI_D3-C/ PIXD3/ IRQ7/ ADTRG1#
47	P3	P87/ TIOCA2	P87/ MTIOC4C/ TIOCA2/ SMOSI10/ SSDA10/ TXD10/ SDHI_D2-C/ PIXD2
48	R3	P16/ MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/ TMO2/ PO14/ RTCOUT/ TXD1/ RXD3/ SMOSI1/ SMISO3/ SSDA1/ SSCL3/ MOSIA/ SCL2-DS/ IERXD/ USB0_VBUS/ IRQ6/ ADTRG0#	P16/ MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/ TMO2/ PO14/ RTCOUT/ TXD1/ SMOSI1/ SSDA1/ RXD3/ SMISO3/ SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB/ IRQ6/ ADTRG0#
49	M4	P86/ TIOCA0	P86/ MTIOC4D/ TIOCA0/ SMISO10/ SSCL10/ RXD10/ PIXD1
50	N4	P15/ MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/ TMCI2/ PO13/ RXD1/ SCK3/ SMISO1/ SSCL1/ CRX1-DS/ IRQ5	P15/ MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/ TMCI2/ PO13/ RXD1/ SMISO1/ SSCL1/ SCK3/ CRX1-DS/ PIXD0/ IRQ5
51	P4	P14/ MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/ TMRI2/ PO15/ CTS1#/ RTS1#/ SS1#/ CTX1/ USB0_DPUPE/ IRQ4	P14/ MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/ TMRI2/ PO15/ CTS1#/ RTS1#/ SS1#/ CTX1/ USB0_OVRCURA/ LCD_CLK-A/ IRQ4
52	R4	P85	P13/ WR2#/ BC2#/ MTIOC0B/ TIOCA5/ TMO3/ PO13/ TXD2/ SMOSI2/ SSDA2/ SDA0[FM+]/ LCD_TCON0-A/ IRQ3/ ADTRG1#
53	M5/N5	P13/ MTIOC0B/ TIOCA5/ TMO3/ PO13/ TXD2/ SMOSI2/ SSDA2/ SDA0[FM+]/ IRQ3/ ADTRG#	P12/ WR3#/ BC3#/ MTIC5U/ TMCI1/ RXD2/ SMISO2/ SSCL2/ SCL0[FM+]/ LCD_TCON1-A/ IRQ2
54	N5/P6	P12/ MTIC5U/ TMCI1/ RXD2/ SMISO2/ SSCL2/ SCL0[FM+]/ IRQ2	VCC_USB
55	R5	P11/ MTIC5V/ TMCI3/ SCK2/ IRQ1	USB0_DM
56	P5/R6	P10/ MTIC5W/ TMRI3/ IRQ0	USB0_DP
57	P6/P5	VCC_USB	VSS_USB
58	R6/M5	USB0_DM	PJ2/ TXD8/ SMOSI8/ SSDA8/ SSLC3-B/ LCD_TCON2-A
59	R7/M6	USB0_DP	PJ1/ MTIOC6A/ RXD8/ SMISO8/ SSCL8/ SSLC2-B/ LCD_TCON3-A
60	P7/N6	VSS_USB	PJ0/ MTIOC6B/ SCK8/ SSLC1-B/ LCD_DATA0-A
61	N6/M7	P57/ WAIT#/ WR3#/ BC3#	P85/ MTIOC6C/ TIOCC0/ LCD_DATA1-A
62	M6/N7	P56/ WR2#/ BC2#/ MTIOC3C/ TIOCA1	P84/ MTIOC6D/ LCD_DATA2-A

176pin LFQFP	176/177 pin TFLGA LFBGA	RX630	RX65N (Code flash more than 1.5 MB)
63	R8/P7	PL4	P57/ RXD7/ SMISO7/ SSCL7/ SSLC0-B/ LCD_DATA3-A
64	P8/R7	PL3	P56/ EDACK1/ MTIOC3C/ TIOCA1/ SCK7/ RSPCKC-B/ LCD_DATA4-A
65	N8/M8	PL2	P55/ D0[A0/D0]/ EDREQ0/ MTIOC4D/ TMO3/ ET0_EXOUT/ TXD7/ SMOSI7/ SSDA7/ MISOC-B/ CRX1/ LCD_DATA5-A/ IRQ10
66	N7/N8	P55/ WAIT#/ MTIOC4D/ TMO3/ CRX1/ IRQ10	P54/ D1[A1/D1]/ EDACK0/ MTIOC4B/ TMCI1/ ET0_LINKSTA/ CTS2#/ RTS2#/ SS2#/ MOSIC-B/ CTX1/ LCD_DATA6-A
67	M7/R8	P54/ ALE/ MTIOC4B/ TMCI1/ CTS2#/ RTS2#/ SS2#/ CTX1	P11/ MTIC5V/ TMCI3/ SCK2/ LCD_DATA7-A/ IRQ1
68	M8/P8	BCLK/ P53	P10/ ALE/ MTIC5W/ TMRI3/ IRQ0
69	R9	P84	P53/ BCLK
70	P9	P52/ RD#/ RXD2/ SMISO2/ SSCL2/ SSLB3	P52/ RD#/ RXD2/ SMISO2/ SSCL2/ SSLB3-A
71	N9	P51/ WR1#/ BC1#/ WAIT#/ SCK2/ SSLB2	P51/ WR1#/ BC1#/ WAIT#/ SCK2/ SSLB2-A
72	M9	P50/ WR0#/ WR#/ TXD2/ SMOSI2/ SSDA2/ SSLB1	P50/ WR0#/ WR#/ TXD2/ SMOSI2/ SSDA2/ SSLB1-A
73	F15/D8	VSS	VSS
74	P10	P83/ MTIOC4C/ CTS10#/ RTS10#/ SS10#	P83/ EDACK1/ MTIOC4C/ ET0_CRS/ RMII0_CRS_DV/ SCK10/ SS10#/ CTS10#/ LCD_DATA8-A
75	G15/C11	VCC	VCC
76	N10	PC7/ A23/ CS0#/ MTIOC3A/ MTCLKB/ TIOCB6/ TMO2/ PO31/ TXD8/ SMOSI8/ SSDA8/ MISOA/ IRQ14	UB/ PC7/ A23/ CS0#/ MTIOC3A/ MTCLKB/ TMO2/ PO31/ TOC0/ CACREF/ ET0_COL/ TXD8/ SMOSI8/ SSDA8/ SMOSI10/ SSDA10/ TXD10/ MISOA-A/ MMC_D7-A/ LCD_DATA9-A/ IRQ14
77	P11	PC6/ A22/ CS1#/ MTIOC3C/ MTCLKA/ TIOCA6/ TMCI2/ PO30/ RXD8/ SMISO8/ SSCL8/ MOSIA/ IRQ13	PC6/ D2[A2/D2]/ A22/ CS1#/ MTIOC3C/ MTCLKA/ TMCI2/ PO30/ TIC0/ ET0_ETXD3/ RXD8/ SMISO8/ SSCL8/ SMISO10/ SSCL10/ RXD10/ MOSIA-A/ MMC_D6-A/ LCD_DATA10-A/ IRQ13
78	M10	PC5/ A21/ CS2#/ WAIT#/ MTIOC3B/ MTCLKD/ TIOCD6/ TCLKF/ TMRI2/ PO29/ SCK8/ RSPCKA	PC5/ D3[A3/D3]/ A21/ CS2#/ WAIT#/ MTIOC3B/ MTCLKD/ TMRI2/ PO29/ ET0_ETXD2/ SCK8/ SCK10/ RSPCKA-A/ MMC_D5-A/ LCD_DATA11-A

176pin LFQFP	176/177 pin TFLGA LFBGA	RX630	RX65N (Code flash more than 1.5 MB)
79	M10	P82/ MTIOC4A/ PO28/ TXD10/ SMOSI10/ SSDA10	P82/ EDREQ1/ MTIOC4A/ PO28/ ET0_ETXD1/ RMII0_TXD1/ SMOSI10/ SSDA10/ TXD10/ MMC_D4-A/ LCD_DATA12-A
80	M11	P81/ MTIOC3D/ PO27/ RXD10/ SMISO10/ SSCL10	P81/ EDACK0/ MTIOC3D/ PO27/ ET0_ETXD0/ RMII0_TXD0/ SMISO10/ SSCL10/ RXD10/ QIO3-A/ SDHI_CD/ MMC_D3-A/ LCD_DATA13-A
81	R12	P80/ MTIOC3B/ PO26/ SCK10	P80/ EDREQ0/ MTIOC3B/ PO26/ ET0_TX_EN/ RMII0_TXD_EN/ SCK10/ RTS10#/ QIO2-A/ SDHI_WP/ MMC_D2-A/ LCD_DATA14-A
82	P12	PC4/ A20/ CS3#/ MTIOC3D/ MTCLKC/ TIOCC6/ TCLKE/ TMCI1/ PO25/ POE0#/ SCK5/ CTS8#/ RTS8#/ SS8#/ SSLA0	PC4/ A20/ CS3#/ MTIOC3D/ MTCLKC/ TMCI1/ PO25/ POE0#/ ET0_TX_CLK/ SCK5/ CTS8#/ RTS8#/ SS8#/ SS10#/ CTS10#/ RTS10#/ SSLA0-A/ QMI-A/ QIO1-A/ SDHI_D1-A/ SDSI_D1-A/ MMC_D1-A/ LCD_DATA15-A
83	N12	PC3/ A19/ MTIOC4D/ TCLKB/ PO24/ TXD5/ SMOSI5/ SSDA5/ IETXD	PC3/ A19/ MTIOC4D/ TCLKB/ PO24/ ET0_TX_ER/ TXD5/ SMOSI5/ SSDA5/ QMO-A/ QIO0-A/ SDHI_D0-A/ SDSI_D0-A/ MMC_D0-A/ LCD_DATA16-A
84	M12	P77/ CS7#/ PO23/ TXD11/ SMOSI11/ SSDA11	P77/ CS7#/ PO23/ ET0_RX_ER/ RMII0_RX_ER/ SMOSI11/ SSDA11/ TXD11/ QSPCLK-A/ SDHI_CLKA/ SDSI_CLKA/ MMC_CLKA/ LCD_DATA17-A
85	R13	P76/ CS6#/ PO22/ RXD11/ SMISO11/ SSCL11	P76/ CS6#/ PO22/ ET0_RX_CLK/ REF50CK0/ SMISO11/ SSCL11/ RXD11/ QSSL-A/ SDHI_CMD-A/ SDSI_CMDA/ MMC_CMD-A/ LCD_DATA18-A
86	P13	PC2/ A18/ MTIOC4B/ TCLKA/ PO21/ RXD5/ SMISO5/ SSCL5/ SSLA3/ IERXD	PC2/ A18/ MTIOC4B/ TCLKA/ PO21/ ET0_RX_DV/ RXD5/ SMISO5/ SSCL5/ SSLA3-A/ SDHI_D3-A/ SDSI_D3-A/ MMC_CD-A/ LCD_DATA19-A
87	P14	P75/ CS5#/ PO20/ SCK11	P75/ CS5#/ PO20/ ET0_ERXD0/ RMII0_RXD0/ SCK11/ RTS11#/ SDHI_D2-A/ SDSI_D2-A/ MMC_RES#-A/ LCD_DATA20-A
88	R14	P74/ CS4#/ PO19/ CTS11#/ RTS11#/ SS11#	P74/ A20/ CS4#/ PO19/ ET0_ERXD1/ RMII0_RXD1/ SS11#/ CTS11#/ LCD_DATA21-A

176pin LFQFP	176/177 pin TFLGA LFBGA	RX630	RX65N (Code flash more than 1.5 MB)
89	R15	PC1/ A17/ MTIOC3A/ TCLKD/ PO18/ SCK5/ SSLA2/ SDA3/ IRQ12	PC1/ A17/ MTIOC3A/ TCLKD/ PO18/ ET0_ERXD2/ SCK5/ SSLA2-A/ LCD_DATA22-A/ IRQ12
90	P15/D13	PL1	VCC
91	N13	PC0/ A16/ MTIOC3C/ TCLKC/ PO17/ CTS5#/ RTS5#/ SS5#/ SSLA1/ SCL3/ IRQ14	PC0/ A16/ MTIOC3C/ TCLKC/ PO17/ ET0_ERXD3/ CTS5#/ RTS5#/ SS5#/ SSLA1-A/ IRQ14
92	N15/E4	PL0	VSS
93	N14	P73/ CS3#/ PO16	P73/ CS3#/ PO16/ ET0_WOL/ LCD_EXTCLK-A
94	M13	PB7/ A15/ MTIOC3B/ TIOCB5/ PO31/ TXD9/ SMOSI9/ SSDA9	PB7/ A15/ MTIOC3B/ TIOCB5/ PO31/ ET0_CRS/ RMII0_CRS_DV/ TXD9/ SMOSI9/ SSDA9/ SMOSI11/ SSDA11/ TXD11/ SDSI_D1-B
95	L12	PB6/ A14/ MTIOC3D/ TIOCA5/ PO30/ RXD9/ SMISO9/ SSCL9	PB6/ A14/ MTIOC3D/ TIOCA5/ PO30/ ET0_ETXD1/ RMII0_TXD1/ RXD9/ SMISO9/ SSCL9/ SMISO11/ SSCL11/ RXD11/ SDSI_D0-B
96	M14	PB5/ A13/ MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/ PO29/ POE1#/ SCK9	PB5/ A13/ MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/ PO29/ POE4#/ ET0_ETXD0/ RMII0_TXD0/ SCK9/ SCK11/ SDSI_CLKB/ LCD_CLK-B
97	M15	PB4/ A12/ TIOCA4/ PO28/ CTS9#/ RTS9#/ SS9#	PB4/ A12/ TIOCA4/ PO28/ ET0_TX_EN/ RMII0_TXD_EN/ CTS9#/ RTS9#/ SS9#/ SS11#/ CTS11#/ RTS11#/ SDSI_CMDB/ LCD_TCON0-B
98	L13	PB3/ A11/ MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/ TMO0/ PO27/ POE3#/ SCK4/ SCK6	PB3/ A11/ MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/ TMO0/ PO27/ POE11#/ ET0_RX_ER/ RMII0_RX_ER/ SCK4/ SCK6/ SDSI_D3-B/ LCD_TCON1-B
99	K12	PB2/ A10/ TIOCC3/ TCLKC/ PO26/ CTS4#/ RTS4#/ CTS6#/ RTS6#/ SS4#/ SS6#	PB2/ A10/ TIOCC3/ TCLKC/ PO26/ ET0_RX_CLK/ REF50CK0/ CTS4#/ RTS4#/ SS4#/ CTS6#/ RTS6#/ SS6#/ SDSI_D2-B/ LCD_TCON2-B
100	L14	PB1/ A9/ MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/ PO25/ TXD4/ TXD6/ SMOSI4/ SMOSI6/ SSDA4/ SSDA6/ IRQ4-DS	PB1/ A9/ MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/ PO25/ ET0_ERXD0/ RMII0_RXD0/ TXD4/ SMOSI4/ SSDA4/ TXD6/ SMOSI6/ SSDA6/ LCD_TCON3-B/ IRQ4-DS
101	L15	P72/ CS2#	P72/ A19/ CS2#/ ET0_MDC/ LCD_DATA23-A
102	K13	P71/ CS1#	P71/ A18/ CS1#/ ET0_MDIO
103	K14/G15	PK7	VCC

176pin LFQFP	176/177 pin TFLGA LFBGA	RX630	RX65N (Code flash more than 1.5 MB)
104	K15	PB0/ A8/ MTIC5W/ TIOCA3/ PO24/ RXD4/ RXD6/ SMISO4/ SMISO6/ SSCL4/ SSCL6/ RSPCKA/ IRQ12	PB0/ A8/ MTIC5W/ TIOCA3/ PO24/ ET0_ERXD1/ RMII0_RXD1/ RXD4/ SMISO4/ SSCL4/ RXD6/ SMISO6/ SSCL6/ LCD_DATA0-B/ IRQ12
105	J13/F15	PK6	VSS
106	J14	PA7/ A7/ TIOCB2/ PO23/ MISOA	PA7/ A7/ TIOCB2/ PO23/ ET0_WOL/ MISOA-B/ LCD_DATA1-B
107	J15	PA6/ A6/ MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/ PO22/ POE2#/ CTS5#/ RTS5#/ SS5#/ MOSIA	PA6/ A6/ MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/ PO22/ POE10#/ ET0_EXOUT/ CTS5#/ RTS5#/ SS5#/ MOSIA-B/ LCD_DATA2-B
108	J12	PA5/ A5/ TIOCB1/ PO21/ RSPCKA	PA5/ A5/ MTIOC6B/ TIOCB1/ PO21/ ET0_LINKSTA/ RSPCKA-B/ LCD_DATA3-B
109	H12	PA4/ A4/ MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/ PO20/ TXD5/ SMOSI5/ SSDA5/ SSLA0/ IRQ5-DS	PA4/ A4/ MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/ PO20/ ET0_MDC/ TXD5/ SMOSI5/ SSDA5/ SSLA0-B/ LCD_DATA4-B/ IRQ5-DS
110	H13	PA3/ A3/ MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/ PO19/ RXD5/ SMISO5/ SSCL5/ IRQ6-DS	PA3/ A3/ MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/ PO19/ ET0_MDIO/ RXD5/ SMISO5/ SSCL5/ LCD_DATA5-B/ IRQ6-DS
111	H15	TRDATA3/ PG7/ D31	TRDATA3/ PG7/ D31
112	H14	PA2/ A2/ PO18/ RXD5/ SMISO5/ SSCL5/ SSLA3	PA2/ A2/ MTIOC7A/ PO18/ RXD5/ SMISO5/ SSCL5/ SSLA3-B/ LCD_DATA6-B
113	G13	TRDATA2/ PG6/ D30	TRDATA2/ PG6/ D30
114	G14	PA1/ A1/ MTIOC0B/ MTCLKC/ TIOCB0/ PO17/ SCK5/ SSLA2/ IRQ11	PA1/ DQM3/ A1/ MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/ PO17/ ET0_WOL/ SCK5/ SSLA2-B/ LCD_DATA7-B/ IRQ11
115	J2	VCC	VCC
116	G12	TRCLK/ PG5/ D29	TRCLK/ PG5/ D29
117	H2	VSS	VSS
118	F14	PA0/ A0/ BC0#/ MTIOC4A/ TIOCA0/ PO16/ SSLA1	PA0/ DQM2/ BC0#/ A0/ MTIOC4A/ MTIOC6D/ TIOCA0/ PO16/ CACREF/ ET0_TX_EN/ RMII0_TXD_EN/ SSLA1-B/ LCD_DATA8-B
119	F13	TRSYNC/ PG4/ D28	TRSYNC/ PG4/ D28
120	E15	P67/ CS7#/ CRX2/ IRQ15	P67/ DQM1/ CS7#/ MTIOC7C/ IRQ15
121	E14	TRDATA1/ PG3/ D27	TRDATA1/ PG3/ D27
122	F12	P66/ CS6#/ CTX2	P66/ DQM0/ CS6#/ MTIOC7D
123	E13	TRDATA0/ PG2/ D26	TRDATA0/ PG2/ D26
124	D15	P65/ CS5#	P65/ CKE/ CS5#

176pin LFQFP	176/177 pin TFLGA LFBGA	RX630	RX65N (Code flash more than 1.5 MB)
125	D14	PE7/ D15[A15/D15]/ TIOCB11/ MISOB/ IRQ7/ AN5	PE7/ D15[A15/D15]/ D7[A7/D7]/ MTIOC6A/ TOC1/ MISOB-B/ SDHI_WP/ MMC_RES#-B/ LCD_DATA9-B/ IRQ7/ AN105
126	E12	PE6/ D14[A14/D14]/ TIOCA11/ CTS4#/ RTS4#/ SS4#/ MOSIB/ IRQ6/ AN4	PE6/ D14[A14/D14]/ D6[A6/D6]/ MTIOC6C/ TIC1/ MOSIB-B/ SDHI_CD/ MMC_CD-B/ LCD_DATA10-B/ IRQ6/ AN104
127	D13/K14	PK5/ TXD4/ SMOSI4/ SSDA4	VCC
128	C15	P70/ SCK4	P70/ SDCLK
129	C14/J13	PK4/ RXD4/ SMISO4/ SSCL4	VSS
130	D12	PE5/ D13[A13/D13]/ MTIOC4C/ MTIOC2B/ TIOCB10/ RSPCKB/ IRQ5/ AN3	PE5/ D13[A13/D13]/ D5[A5/D5]/ MTIOC4C/ MTIOC2B/ ET0_RX_CLK/ REF50CK0/ RSPCKB-B/ LCD_DATA11-B/ IRQ5/ AN103
131	C13	PE4/ D12[A12/D12]/ MTIOC4D/ MTIOC1A/ TIOCA10/ PO28/ SSLB0/ AN2	PE4/ D12[A12/D12]/ D4[A4/D4]/ MTIOC4D/ MTIOC1A/ PO28/ ET0_ERXD2/ SSLB0-B/ LCD_DATA12-B/ AN102
132	B15	PE3/ D11[A11/D11]/ MTIOC4B/ TIOCB9/ PO26/ POE8#/ CTS12#/ RTS12#/ SS12#/ MISOB/ AN1	PE3/ D11[A11/D11]/ D3[A3/D3]/ MTIOC4B/ PO26/ TOC3/ POE8#/ ET0_ERXD3/ CTS12#/ RTS12#/ SS12#/ MMC_D7-B/ LCD_DATA13-B/ AN101
133	A15	PE2/ D10[A10/D10]/ MTIOC4A/ TIOCA9/ PO23/ RXD12/ SMISO12/ SSCL12/ RXDX12/ SSLB3/ MOSIB/ IRQ7-DS/ AN0	PE2/ D10[A10/D10]/ D2[A2/D2]/ MTIOC4A/ PO23/ TIC3/ RXD12/ SMISO12/ SSCL12/ RXDX12/ SSLB3-B/ MMC_D6-B/ LCD_DATA14-B/ IRQ7-DS/ AN100
134	A14	PE1/ D9[A9/D9]/ MTIOC4C/ TIOCD9/ PO18/ TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12/ SSLB2/ RSPCKB/ ANEX1	PE1/ D9[A9/D9]/ D1[A1/D1]/ MTIOC4C/ MTIOC3B/ PO18/ TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12/ SSLB2-B/ MMC_D5-B/ LCD_DATA15-B/ ANEX1
135	B14	PE0/ D8[A8/D8]/ TIOCC9/ SCK12/ SSLB1/ ANEX0	PE0/ D8[A8/D8]/ D0[A0/D0]/ MTIOC3D/ SCK12/ SSLB1-B/ MMC_D4-B/ LCD_DATA16-B/ ANEX0
136	B13	P64/ CS4#	P64/ WE#/ D3[A3/D3]/ CS4#
137	A13	P63/ CS3#	P63/ CAS#/ D2[A2/D2]/ CS3#
138	C12	P62/ CS2#	P62/ RAS#/ D1[A1/D1]/ CS2#
139	D11	P61/ CS1#/ CTS9#/ RTS9#/ SS9#	P61/ SDCS#/ D0[A0/D0]/ CS1#
140	B12/N15	PK3/ RXD9/ SMISO9/ SSCL9	VSS
141	A12	P60/ CS0#/ SCK9	P60/ CS0#
142	C11/N1	PK2/ TXD9/ SMOSI9/ SSDA9	VCC

176pin LFQFP	176/177 pin TFLGA LFBGA	RX630	RX65N (Code flash more than 1.5 MB)
143	D10	PD7/ D7[A7/D7]/ MTIC5U/ POE0#/ SSLC3/ IRQ7/ AN7	PD7/ D7[A7/D7]/ MTIC5U/ POE0#/ SSLC3-A/ QMI-B/ QIO1-B/ SDHI_D1-B/ MMC_D1-B/ LCD_DATA17-B/ IRQ7/ AN107
144	B11	PG1/ D25	TRDATA7/ PG1/ D25
145	A11	PD6/ D6[A6/D6]/ MTIC5V/ POE1#/ SSLC2/ IRQ6/ AN6	PD6/ D6[A6/D6]/ MTIC5V/ MTIOC8A/ POE4#/ SSLC2-A/ QMO-B/ QIO0-B/ SDHI_D0-B/ MMC_D0-B/ LCD_DATA18-B/ IRQ6/ AN106
146	C10	PG0/ D24	TRDATA6/ PG0/ D24
147	D9	PD5/ D5[A5/D5]/ MTIC5W/ POE2#/ SSLC1/ IRQ5/ AN013	PD5/ D5[A5/D5]/ MTIC5W/ MTIOC8C/ POE10#/ SSLC1-A/ QSPCLK-B/ SDHI_CLKB/ MMC_CLKB/ LCD_DATA19-B/ IRQ5/ AN113
148	B10	PD4/ D4[A4/D4]/ POE3#/ SSLC0/ IRQ4/ AN012	PD4/ D4[A4/D4]/ MTIOC8B/ POE11#/ SSLC0-A/ QSSL-B/ SDHI_CMD-B/ MMC_CMD-B/ LCD_DATA20-B/ IRQ4/ AN112
149	A10	P97/ A23/ D23	TRSYNC1/ P97/ D23/ A23
150	C9	PD3/ D3[A3/D3]/ TIOCB8/ TCLKH/ POE8#/ RSPCKC/ IRQ3/ AN011	PD3/ D3[A3/D3]/ MTIOC8D/ TOC2/ POE8#/ RSPCKC-A/ QIO3-B/ SDHI_D3-B/ MMC_D3-B/ LCD_DATA21-B/ IRQ3/ AN111
151	D8/P1	PK1	VSS
152	B9	P96/ A22/ D22	TRDATA5/ P96/ D22/ A22
153	A9/P15	PK0	VCC
154	C8	PD2/ D2[A2/D2]/ MTIOC4D/ TIOCA8/ MISOC/ CRX0/ IRQ2/ AN010	PD2/ D2[A2/D2]/ MTIOC4D/ TIC2/ MISOC-A/ CRX0/ QIO2-B/ SDHI_D2-B/ MMC_D2-B/ LCD_DATA22-B/ IRQ2/ AN110
155	D7	P95/ A21/ D21	TRDATA4/ P95/ D21/ A21
156	B8	PD1/ D1[A1/D1]/ MTIOC4B/ TIOCB7/ TCLKG/ MOSIC/ CTX0/ IRQ1/ AN009	PD1/ D1[A1/D1]/ MTIOC4B/ POE0#/ MOSIC-A/ CTX0/ LCD_DATA23-B/ IRQ1/ AN109
157	A8	P94/ A20/ D20	P94/ D20/ A20
158	C7	PD0/ D0[A0/D0]/ TIOCA7/ IRQ0/ AN008	PD0/ D0[A0/D0]/ POE4#/ LCD_EXTCLK-B/ IRQ0/ AN108
159	D6	P93/ A19/ D19/ CTS7#/ RTS7#/ SS7#/ AN017	P93/ D19/ A19/ POE0#/ CTS7#/ RTS7#/ SS7#/ AN117
160	B7	P92/ A18/ D18/ RXD7/ SMISO7/ SSCL7/ AN016	P92/ D18/ A18/ POE4#/ RXD7/ SMISO7/ SSCL7/ AN116
161	B6	P91/ A17/ D17/ SCK7/ AN015	P91/ D17/ A17/ SCK7/ AN115
162	R10	VSS	VSS
163	C6	P90/ A16/ D16/ TXD7/ SMOSI7/ SSDA7/ AN014	P90/ D16/ A16/ TXD7/ SMOSI7/ SSDA7/ AN114
164	R11	VCC	VCC

176pin LFQFP	176/177 pin TFLGA LFBGA	RX630	RX65N (Code flash more than 1.5 MB)
165	B5	P47/ IRQ15-DS/ AN007	P47/ IRQ15-DS/ AN007
166	A5	P46/ IRQ14-DS/ AN006	P46/ IRQ14-DS/ AN006
167	C5	P45/ IRQ13-DS/ AN005	P45/ IRQ13-DS/ AN005
168	D5	P44/ IRQ12-DS/ AN004	P44/ IRQ12-DS/ AN004
169	C4	P43/ IRQ11-DS/ AN003	P43/ IRQ11-DS/ AN003
170	A4	P42/ IRQ10-DS/ AN002	P42/ IRQ10-DS/ AN002
171	B4	P41/ IRQ9-DS/ AN001	P41/ IRQ9-DS/ AN001
172	A3	VREFL0	VREFL0
173	B3	P40/ IRQ8-DS/ AN000	P40/ IRQ8-DS/ AN000
174	C3	VREFH0	VREFH0
175	A2	AVCC0	AVCC0
176	B2	P07/ IRQ15/ ADTRG0#	P07/ IRQ15/ ADTRG0#
-	F4	BSCANP	BSCANP

4. Notes on Migration

4.1 Operating Voltage Range

4.1.1 V_{BATT} Power Supply Voltage

On the RX65N Group, please use within VBATT=2.0V to 3.6V.

4.2 Notes on Pin Design

4.2.1 VCL Pin (External Capacitor)

Connect a smoothing capacitor rated at 0.22 μF to the VCL pin of the RX65N Group for stabilization of the internal power supply.

4.2.2 Main Clock Oscillator

When connecting an oscillator to EXTAL pin and XTAL pin of RX65N Group, frequency should be in a range of 8 MHz to 24 MHz.

On the RX65N Group, according to the frequency, it is necessary to set the driving ability in main clock oscillator driving ability 2 switching bits (MODRV2[1:0]) of main clock oscillator forced oscillation control register (MOFCR).

For details on driving ability setting of main clock oscillator, see RX65N Group, RX651 Group User's Manual: Hardware, listed in section 5, Reference Documents.

4.2.3 Inputting an External Clock

On the RX630 Group, it was permissible, when inputting an external clock, to input on the XTAL pin the reverse phase of the clock input on the EXTAL pin. However, this is not permitted on the RX65N Group. Please keep this in mind when designing systems.

On the RX65N Group, it is necessary to set the main clock oscillator switching bit (MOSEL) of main clock oscillator forced oscillation control register (MOFCR) to 1 when inputting an external clock.

4.2.4 Sub-Clock Oscillator

On the RX65N Group, according to the load capacitance of oscillator, it is necessary to set the driving capacity in sub-clock oscillator drive capacity control bits (RTCDV[2:0]) of RTC control register 3 (RCR3)

For details on drive capacity setting of sub-clock oscillator, see RX65N Group, RX651 Group User's Manual: Hardware, listed in section 5, Reference Documents.

4.2.5 On-Chip USB DP/DM Pull-Up/Pull-Down Resistors

The RX65N Group has on-chip USB DP/DM pull-up and pull-down resistors. This means that the external connection circuits are different from those of the RX630 Group.

For details on external connection circuits, see RX65N Group, RX651 Group User's Manual: Hardware, listed in section 5, Reference Documents.

4.2.6 Transition to Boot Mode (FINE Interface)

The RX630 Group supports user boot mode. However, the RX65N Group doesn't support user boot mode.

On the RX65N Group, the chip enters boot mode (FINE interface) when the MD pin is set to the low level at the time of release from the reset state and then the pin is switched to the high level within 20 to 100 msec.

For details on operating modes, see RX65N Group, RX651 Group User's Manual: Hardware, listed in section 5, Reference Documents.

4.3 Notes on Function Settings

4.3.1 Changing Option-Setting Memory by Self-Programming

Making changes to the option-setting memory by self-programming on the RX65N Group is accomplished by programming the configuration setting area in the option-setting memory using the configuration setting command.

For details on the configuration setting command, see RX65N Group, RX651 Group Flash Memory User's Manual: Hardware Interface, listed in section 5, Reference Documents.

4.3.2 Setting Number of Flash Memory Access Wait States

On the RX65N Group it is necessary to specify the number of access wait states to be used when accessing the flash memory, based on the system clock (ICLK) frequency of the microcontroller. This setting is made to the ROMWT register.

Table 4.1 shows The Number of Flash Memory Access Wait States.

Table 4.1 The Number of Flash Memory Access Wait States

Item	ICLK ≤ 50 MHz	50 MHz < ICLK ≤ 100 MHz	100 MHz < ICLK ≤ 200 MHz
Wait states	0 to 2	1 or 2	2

Note: For details on register setting and the detail of specifications, see RX65N Group User's Manual: Hardware, listed in section 5, Reference Documents.

4.3.3 Selectable Interrupts

A selectable interrupt function has been added to the RX65N Group. From among multiple peripheral module interrupt sources, the user may assign one each to interrupt vector numbers 128 to 255.

For details on selectable interrupt function, see RX65N Group, RX651 Group User's Manual: Hardware, listed in section 5, Reference Documents.

4.3.4 Transferring Firmware to the FCU RAM

On the RX630 Group, FCU commands could only be used if the FCU RAM holds the firmware for the FCU. However, this is not necessary on the RX65N Group.

4.3.5 Command of Flash Memory Usage

On the RX630 Group, the Flash memory can be programmed or erased by issuing FCU commands to FCU.

On the RX65N Group, the Flash memory can be programmed or erased by setting the FACI commands specified in the FACI command issuing area and by controlling the FCU.

Table 4.2 shows The Specification Comparison Between FCU Commands and FACI Commands.

Table 4.2 The Specification Comparison Between FCU Commands and FACI Commands

Item	FCU Commands (RX630)	FACI commands (RX65N)
Command issuing area	Address for programming/erasure (00E0 0000h to 00FF FFFFh)	FACI command issuing area (007E 0000h)
Available commands	• P/E normal mode transition • Status read mode transition • Lock bit read mode transition • Peripheral clock notification • Programming • Block erase • P/E suspend • P/E resume • Status register clear • Lock bit read 2 • Lock bit programming • Blank checking	• Program • Block erase • P/E suspend • P/E resume • Status clear • Forced stop • Configuration setting

4.3.6 Flash Access Window Setting Register (FAW)

On the RX65N Group, once 0 is written to the access window protection bit (FSPR) in flash access window setting register (FAW), the bit can never be restored to 1.

For details, see RX65N Group, RX651 Group User's Manual: Hardware, listed in section 5.

4.3.7 Flash Area Erasing by ID Code Protection

On the RX630 Group, in the case of ID codes do not match while ID code protection is enabled, all blocks in the user area and data area can be erased. However, ID code protection* on the RX65N Group does not erase the code flash area even if ID codes do not match.

Note *: ID code protection of RX65N cannot be disabled.

5. Reference Documents

User's Manual: Hardware

RX630 Group User's Manual: Hardware Rev.1.60 (R01UH0040EJ)
(The latest version can be downloaded from the Renesas Electronics website.)

RX65N Group, RX651 Group User's Manual: Hardware Rev.2.10 (R01UH0590EJ)
(The latest version can be downloaded from the Renesas Electronics website.)

RX65N Group, RX651 Group Flash Memory User's Manual: Hardware Interface Rev.2.00 (R01UH0602EJ)
(The latest version can be downloaded from the Renesas Electronics website.)

Application Note

Migration Design Guide between RX Families: Package Dimensions Difference (R01AN4591EJ)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The technical updates issued after each referenced user manual are not reflected in this application note, so obtain latest version from the Renesas Electronics website.)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Dec. 01, 2016	-	First edition issued
2.00	Nov. 06, 2017	All pages	Supports RX65N with at least 1.5 Mbytes of code flash memory
2.10	Sep. 26, 2018	All pages	Confirmed the contents of the description again (Addition of description mistake etc.)
2.20	Mar. 18, 2019	All pages	Confirmed the contents of the description again (Addition of description mistake etc.)
		7	Add memory map comparison of address space
		11	Add area comparison of option setting memory
		20	Add Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode
		27	Add comparison of exception handling

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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