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M16C/64 Group

Operation of Timer A (event counter mode, free run type)

1. Abstract

In event counter mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

2. Introduction

This application note is applied to the M16C/64 group microcomputers.

This program can be operated under the condition of M16C family products with the same SFR (Special Function Register) as M16C/64 Group products. Because some functions may be modified of the M16C family products, see the user's manual. When using the functions shown in this application note, evaluate them carefully for an operation



3. Chosen functions

Table 1. Chosen functions

Item	Set-up	
Count source	0	Input signal to TAilN (counting falling edges)
		Input signal to TAilN (counting rising edges)
		Timer overflow (TB2/TAj overflow)
Pulse output function	0	No pulses output
		Pulses output
Count operation type		Reload type
	0	Free-run type

Note: j = i - 1, but j = 4 when i = 0.

4. Operation

- (1) Setting the count start flag to "1" causes the counter to count the falling edges of the count source.
- (2) Even if an underflow occurs, the content of the reload register is not reloaded to the counter, but the count continues. At this time, the timer Ai interrupt request bit goes to "1".
- (3) If switching from an up count to a down count or vice versa while a count is in progress, the switch takes effect from the next effective edge of the count source.
- (4) Even if an overflow occurs, the content of the reload register is not reloaded to the counter, but the count continues. At this time, the timer Ai interrupt request bit goes to "1".

Figure 1 shows the operation timing.

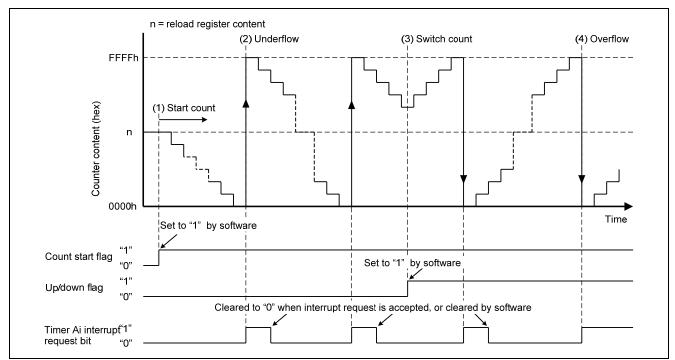
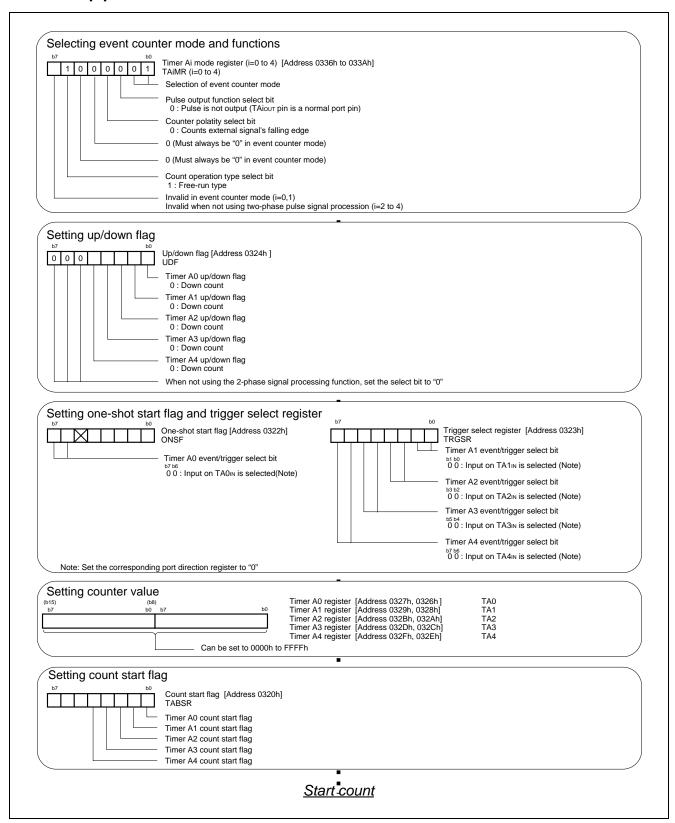


Figure 1. Operation timing of event counter mode, free run type selected



5. Set-up procedure





6. Reference

Hardware manual

M16C/64 Group Hardware Manual

(Use the most recent version of the document on the Renesas Technology Web site.)

Technical news/Technical update

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