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April 1st, 2010
Renesas Electronics Corporation

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M16C/64 Group

Operation of serial I/O (reception in UART mode)

1. Abstract

In receiving data in UART mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

2. Introduction

This application note is applied to the M16C/64 group microcomputers.

This program can be operated under the condition of M16C family products with the same SFR (Special Function Register) as M16C/64 Group products. Because some functions may be modified of the M16C family products, see the user's manual. When using the functions shown in this application note, evaluate them carefully for an operation.

3. Chosen functions

Table 1. Chosen functions

Item	Set-up		Item	Set-up	
Transfer clock source	O	Internal clock (f_{1SIO}/f_{2SIO}/f_{8SIO}/f_{32SIO})	Data logic select function	O	No reverse
		External clock (CLKi pin)			Reverse
$\overline{RTS}$ function	O	$\overline{RTS}$ function enabled	TXD, RXD I/O polarity reverse bit	O	No reverse
		$\overline{RTS}$ function disable			Reverse
			Bus collision detection function	O	Not selected
					Selected

4. Operation

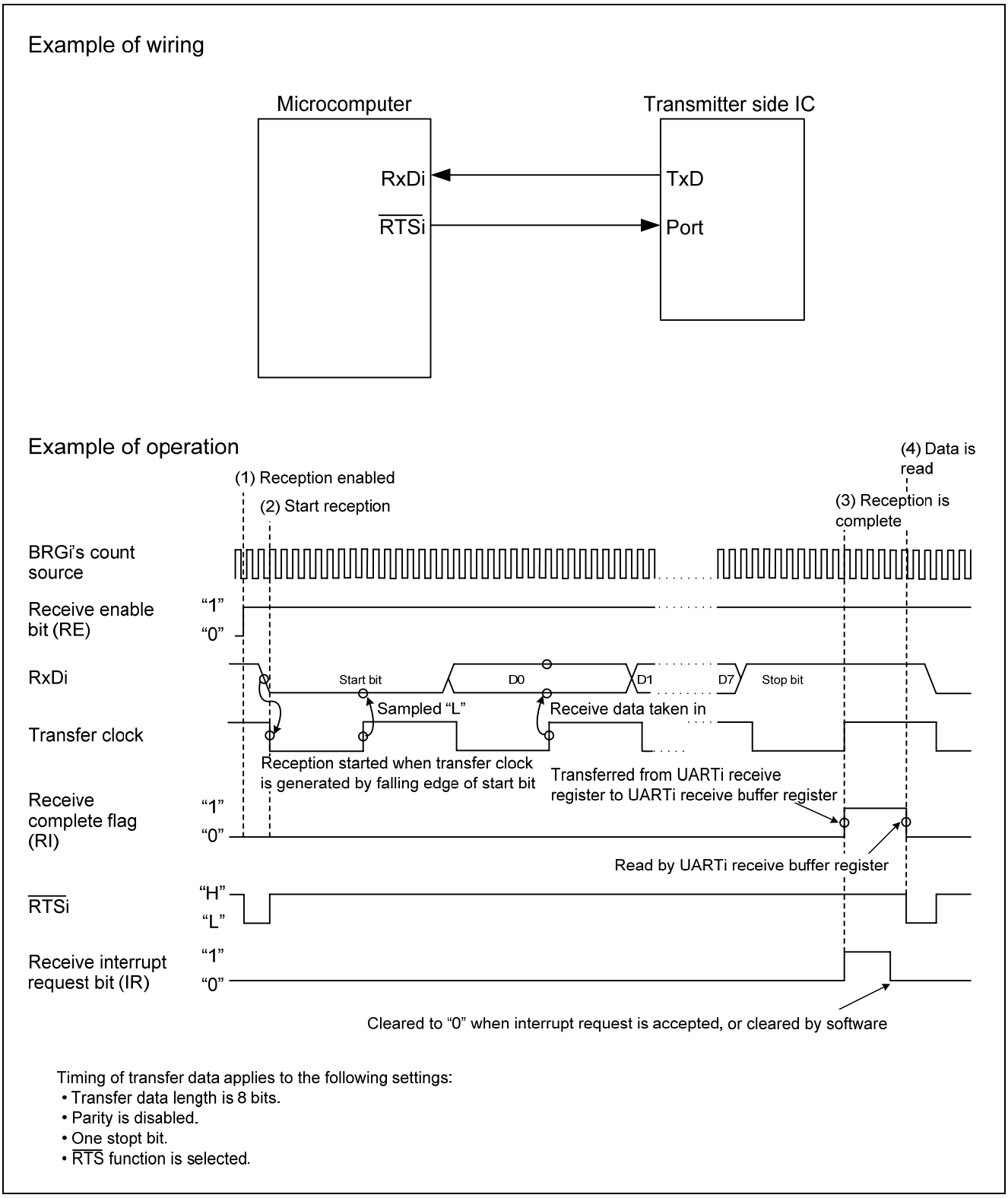
(1) Setting the receive enable bit to “1” readies data-receivable status. At this time, output from the $\overline{RTSi}$ pin goes to “L” level to inform the transmission side that the receivable status is ready.

(2) When the first bit (the start bit) of reception data is received from the RxDi pin, output from the $\overline{RTS}$ goes to “H” level. Then, data is received, bit by bit, in sequence: LSB, ····, MSB, and stop bit(s).

(3) When the stop bit(s) is (are) received, the content of the UARTi receive register is transmitted to the UARTi receive buffer register. At this time, the receive complete flag goes to “1” to indicate that the reception is completed, the UARTi receive interrupt request bit goes to “1”.

(4) When the lower-order byte of the UARTi buffer register is read, the receive complete flag goes to “0”, and output from the $\overline{RTS}$ pin goes to “L” level.

Figure 1 shows the operation timing.

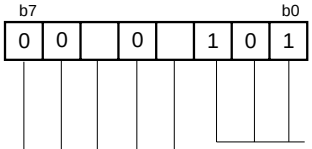


Timing of transfer data applies to the following settings:
- Transfer data length is 8 bits.
- Parity is disabled.
- One stopt bit.
- $\overline{\text{RTS}}$ function is selected.

Figure 1. Operation timing of reception in UART mode

5. Set-up procedure

Setting UARTi transmit/receive mode register (i = 0 to 2, 5 to 7)



UART0 transmit/receive mode register [Address 0248h] U0MR
UART1 transmit/receive mode register [Address 0258h] U1MR
UART2 transmit/receive mode register [Address 0268h] U2MR
UART5 transmit/receive mode register [Address 0288h] U5MR
UART6 transmit/receive mode register [Address 0298h] U6MR
UART7 transmit/receive mode register [Address 02A8h] U7MR

Serial I/O mode select bit
b2 b1 b0
1 0 1 : Transfer data 8 bits long

Internal/external clock select bit
0 : Internal clock

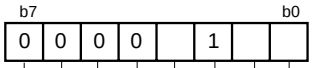
Stop bit length select bit
0 : One stop bit

Valid when bit 6 = “1”

Parity enabled bit
0 : Parity disabled

TxD, RxD I/O polarity reverse bit
Usually set to “0”

Setting UARTi transmit/receive control register (i = 0 to 2, 5 to 7)



UART0 transmit/receive control register [Address 024Ch] U0C0
UART1 transmit/receive control register [Address 025Ch] U1C0
UART2 transmit/receive control register [Address 026Ch] U2C0
UART5 transmit/receive control register [Address 028Ch] U5C0
UART6 transmit/receive control register [Address 029Ch] U6C0
UART7 transmit/receive control register [Address 02ACh] U7C0

UiBRG count source select bit
b1 b0
0 0 : f_{1SIO} or f_{2SIO} is selected
0 1 : f_{8SIO} is selected
1 0 : f_{32SIO} is selected
1 1 : Do not set to this value

$\overline{CTS}/\overline{RTS}$ function select bit (Valid when bit4 = “0”)
1 : $\overline{RTS}$ function is selected

Transmit register empty flag
0 : Data present in transmit register (during transmission)
1 : No data present in transmit register (transmission completed)

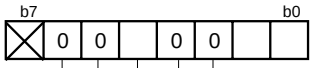
$\overline{CTS}/\overline{RTS}$ disable bit
0 : $\overline{CTS}/\overline{RTS}$ function enabled

Data output select bit
0 : Pins TXDi/SDAi and SCLi are CMOS output
1 : Pins TXDi/SDAi and SCLi are N-channel open-drain output

Must always be “0” in UART mode

Transfer format select bit
0 : LSB first

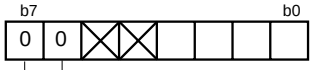
Setting UART transmit/receive control register 2



UART transmit/receive control register 2 [Address 0250h] UCON

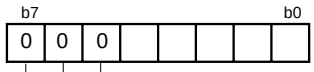
Must always be “0” in UART mode
Must always be “0” in UART mode
Invalid in UART mode
Must always be “0” in UART mode
Separate UART0 $\overline{CTS}/\overline{RTS}$ bit
0 : $\overline{CTS}/\overline{RTS}$ shared pin

Setting UARTi transmit/receive control register 1 (i = 0 to 2, 5 to 7)



UART0 transmit/receive control register 1 [Address 024Dh] U0C1
UART1 transmit/receive control register 1 [Address 025Dh] U1C1

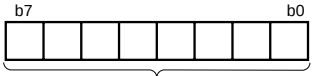
Data logic select bit
0 : No reverse
Error signal output enable bit
0 : Output disabled



UART2 transmit/receive control register 1 [Address 026Dh] U2C1
UART5 transmit/receive control register 1 [Address 028Dh] U5C1
UART6 transmit/receive control register 1 [Address 029Dh] U6C1
UART7 transmit/receive control register 1 [Address 02ADh] U7C1

Must always be “0” in UART mode
Data logic select bit
0 : No reverse
Error signal output enable bit
0 : Output disabled

Setting UARTi bit rate register (i = 0 to 2, 5 to 7)



UART0 bit rate register [Address 0249h] U0BRG
UART1 bit rate register [Address 0259h] U1BRG
UART2 bit rate register [Address 0269h] U2BRG
UART5 bit rate register [Address 0289h] U5BRG
UART6 bit rate register [Address 0299h] U6BRG
UART7 bit rate register [Address 02A9h] U7BRG

Can be set to 00h to FFh (Note)

Note : Write to UARTi bit rate register when transmission/reception is halted.

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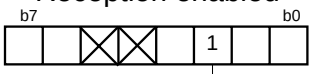
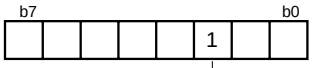
Reception enabled



UART0 transmit/receive control register 1 [Address 024Dh] U0C1
UART1 transmit/receive control register 1 [Address 025Dh] U1C1

Receive enable bit
1 : Reception enabled



UART2 transmit/receive control register 1 [Address 026Dh] U2C1
UART5 transmit/receive control register 1 [Address 028Dh] U5C1
UART6 transmit/receive control register 1 [Address 029Dh] U6C1
UART7 transmit/receive control register 1 [Address 02ADh] U7C1

Receive enable bit
1 : Reception enabled

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Start reception

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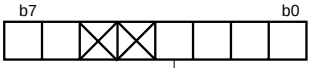
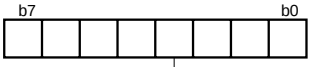
Checking completion of reception



UART0 transmit/receive control register 1 [Address 024Dh] U0C1
UART1 transmit/receive control register 1 [Address 025Dh] U1C1

Receive complete flag
0 : No data present in receive buffer register
1 : Data present in receive buffer register



UART2 transmit/receive control register 1 [Address 026Dh] U2C1
UART5 transmit/receive control register 1 [Address 028Dh] U5C1
UART6 transmit/receive control register 1 [Address 029Dh] U6C1
UART7 transmit/receive control register 1 [Address 02ADh] U7C1

Receive complete flag
0 : No data present in receive buffer register
1 : Data present in receive buffer register

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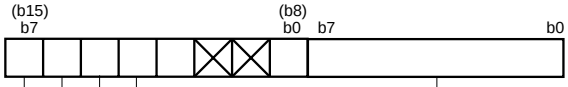
Checking error



UART0 receive buffer register [Address 024Fh, 024Eh] U0RB
UART1 receive buffer register [Address 025Fh, 025Eh] U1RB
UART2 receive buffer register [Address 026Fh, 026Eh] U2RB
UART5 receive buffer register [Address 028Fh, 028Eh] U5RB
UART6 receive buffer register [Address 029Fh, 029Eh] U6RB
UART7 receive buffer register [Address 02AFh, 02AEh] U7RB

Receive data

Overrun error flag
0 : No overrun error
1 : Overrun error found

Framing error flag
0 : No framing error
1 : Framing error found

Parity error flag
0 : No parity error
1 : Parity error found

Error sum flag
0 : No error
1 : Error found

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Processing after reading out reception data

6. Reference

Hardware manual

M16C/64 Group Hardware Manual

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