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April 1st, 2010
Renesas Electronics Corporation

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# M16C/80 Group

## Operation of A-D Converter (in one-shot mode, external op-amp connection mode)

## 1.0 Abstract

In one-shot mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

**Table 1. Choosed functions**

| Item | Set-up | | Item | Set-up | |
|---|---|---|---|---|---|
| Operation clock $\phi_{AD}$ | O | Divided-by-4 $f_{AD}$ / divided-by-2 $f_{AD}$ / $f_{AD}$ | Expanded analog input pin | | Not used |
| | | | | | Either ANEX0 pin or ANEX1 pin |
| Resolution | O | 8-bit / 10-bit | | O | External operation amplifier connection mode |
| Analog input pin | O | One of $AN_0$ pin to $AN_7$ pin | | | |
| Trigger for starting A-D conversion | O | Software trigger | Sample & Hold | | Not activated |
| | | Trigger by $\overline{ADTRG}$ | | O | Activated |

## 2.0 Introduction

Operation (1) Setting the A-D conversion start flag to “1” causes voltage input to the ANi pin to be output from the ANEX0 pin. The A-D conversion is carried out on voltage input to the ANEX1 pin (connect an operation amplifier between the ANEX0 pin and the ANEX1 pin).

(2) After the A-D conversion is completed, the content of the successive comparison register (conversion result) is transmitted to A-D register i corresponding to the ANi pin. At this time, the A-D conversion interrupt request bit goes to “1”.

Figure 1 shows the operation timing

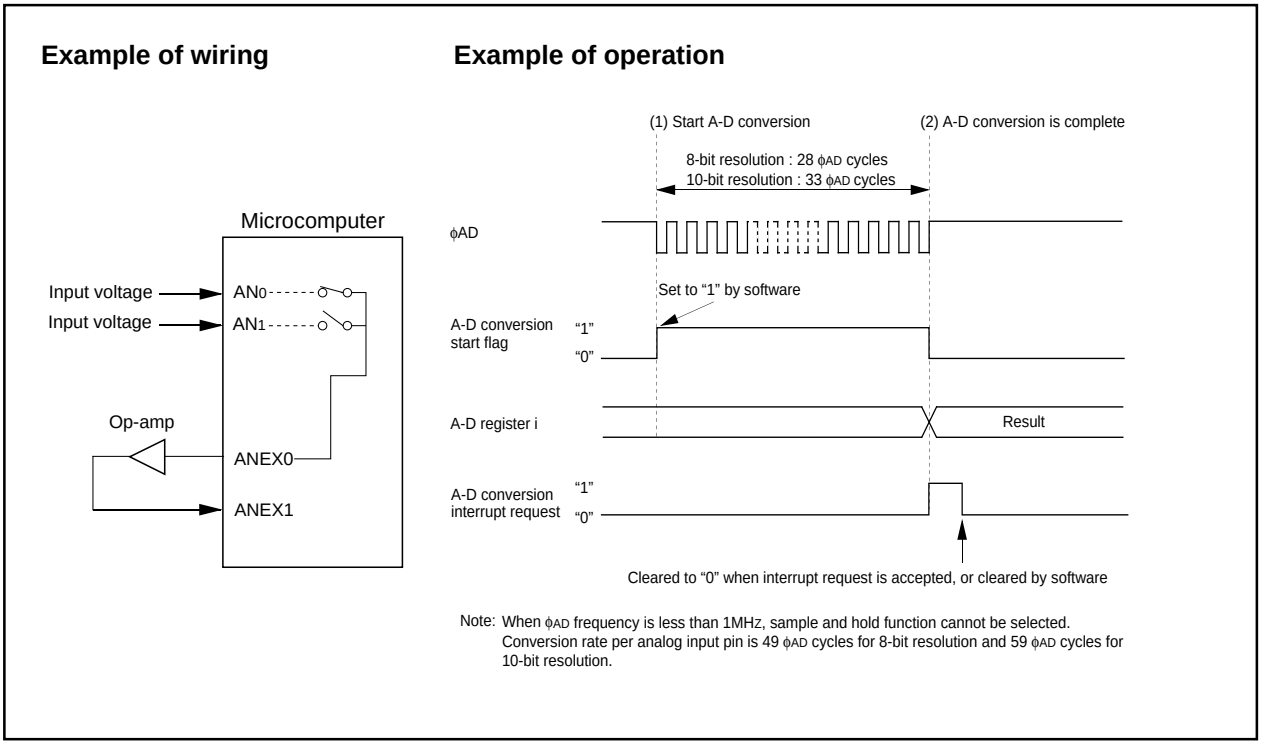
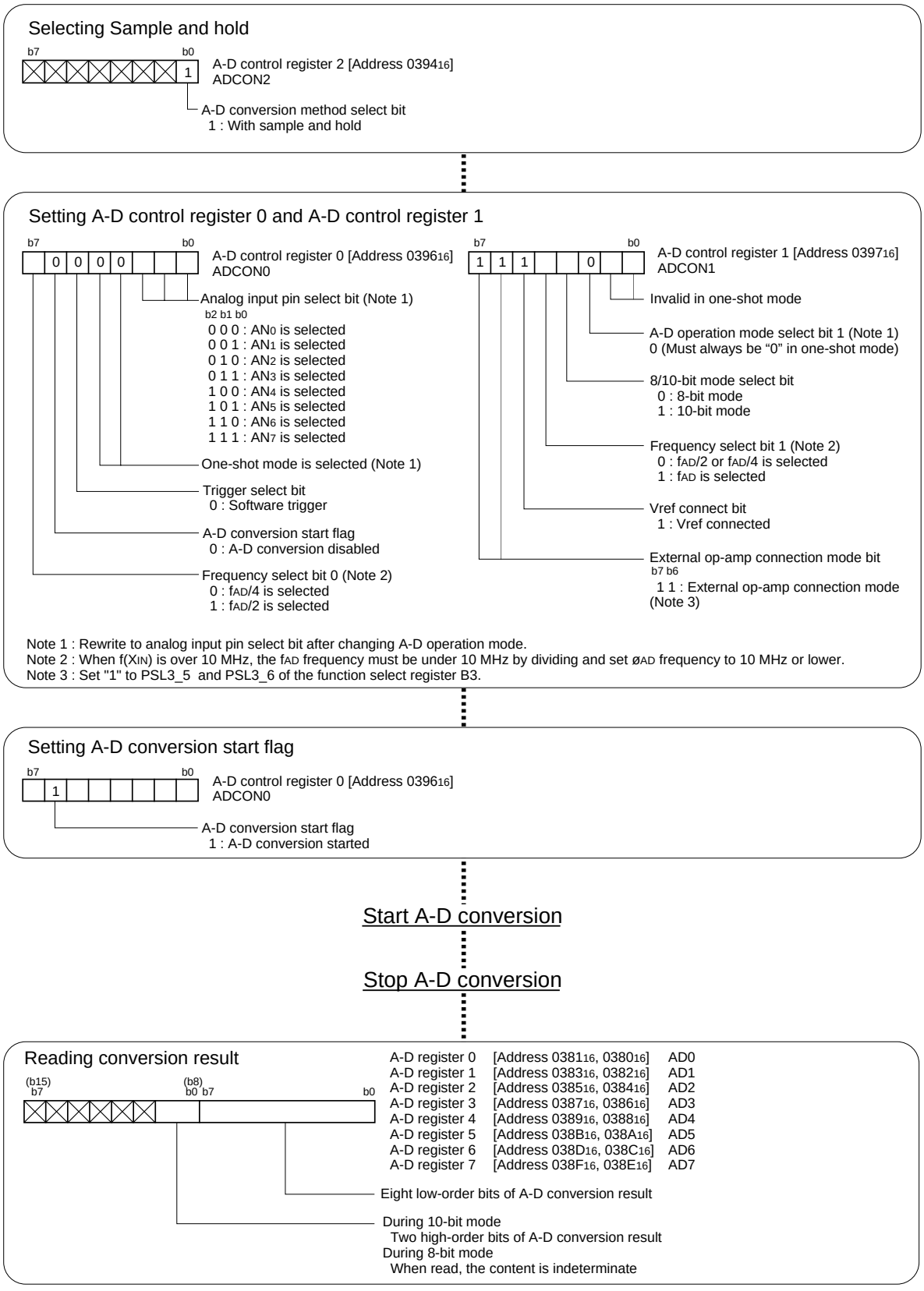



**Figure 1. Operation timing of one-shot mode, with external op-amp connection mode selected**

## 3.0 Set-up procedure



## 4.0 Programming Code

```
;******************************************************************************
;
;   M16C/80 Program Collection
;
;   FILE NAME : rjj05b0478_src.a30
;   CPU       : M16C/80 Group
;   FUNCTION  : Operation of A-D Converter
;               (in one-shot mode, external op-amp connection mode)
;   HISTORY   : 2004.02.02  Ver 1.00
;
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;
;******************************************************************************
;******************************************************************************
;       Include
;******************************************************************************
        .LIST       OFF             ;Stops outputting lines to the assembler list file
        .INCLUDE    sfr80100.inc    ;Reads the file that defined SFR
        .LIST       ON              ;Starts outputting lines to the assembler list file
;
;******************************************************************************
;       Symbol definition
;******************************************************************************
RAM_TOP          .EQU    000400H    ;Start address of RAM
RAM_END          .EQU    002BFFH    ;End address of RAM
ROM_TOP          .EQU    0FFC000H   ;Start address of ROM
FIXED_VECT_TOP   .EQU    0FFFFDCH   ;Start address of fixed vector
;
;******************************************************************************
;       Allocation of work RAM area
;******************************************************************************
        .SECTION    WORKRAM, DATA
        .ORG        RAM_TOP
WORKRAM_TOP:
v_AD_result:    .BLKW   1          ; RAM area where A-D conversion result is stored
WORKRAM_END:
;
;******************************************************************************
;       Program area
;******************************************************************************
;============================================================================
;       Start up
;============================================================================
        .SECTION    PROGRAM, CODE  ;Declares section name and section type
        .ORG        ROM_TOP        ;Declares start address
RESET:
        LDC     #RAM_END+1,ISP     ;Sets initial value in stack pointer
        ; Sets Processor mode, System clock and Main clock division
        MOV.B    #03H, prcr        ;Removes protect
        MOV.B    #10000000B, pm0   ; Single-chip mode
        MOV.B    #11000000B, pm1   ; Flash memory version
        MOV.B    #00001000B, cm0   ; Xcin-Xcout High
        MOV.B    #00100000B, cm1   ; Xin-Xout High
        MOV.B    #00010010B, mcd   ; No division mode
        MOV.B    #00H, prcr        ;Protects all registers
;
        MOV.W    #0, v_AD_result   ;Clear area where A-D conversion result will be stored
```

```
;===============================================================================
;       A-D Converter (in one-shot mode, external op-amp connection mode selected)
;===============================================================================
        ; Disabled A-D conversion interrupt and clear interrupt request bit to "0"
        MOV.B    #00h, adic
        ; Selecting sample and hold
        MOV.B    #00000001B, adcon2
;                       +---------;A-D conversion method select bit
;                                  (1:With sample and hold)
        ; Setting A-D control register 0 and A-D control register 1
        MOV.B    #10000000B, adcon0
;                |||||+++---------;Analog input pin select bit (000:AN0 is selected)
;                |||++------------;One-shot mode is selected
;                ||+--------------;Trigger select bit (0:Software trigger)
;                |+---------------;A-D conversion start flag (0:A-D conversion disabled)
;                +----------------;Frequency select bit 0 (1:fAD/2 is selected)
        MOV.B    #11101000B, adcon1
;                ||||||++---------;Invalid in one-shot mode
;                |||||+-----------;A-D operation mode select bit1
;                |||||             (Must always be "0" in one-shot mode)
;                ||||+------------;8/10-bit mode select bit (1:10-bit mode)
;                |||+-------------;Frequency select bit 1  (0:fAD/2 or fAD/4 is selected)
;                ||+--------------;Vref connect bit (1:Vref connected) (Note)
;                ++---------------;External op-amp connection mode bit
;                                   (11:External op-amp connection mode) (Note)
        ; Setting the direction register of the relevant port to input
        BCLR     pd10_0            ;AN0(P100):Analog input pin
        MOV.B    #00000100B, prcr  ;Clearing the protect (set to write-enabled state)
;                     +-----------;Enables writing to port P9 direction register
        BCLR     pd9_6             ;ANEX1(P96):Expanded analog input pin
        MOV.B    #00000100B, prcr
        BCLR     pd9_5             ;ANEX0(P95):External op-amp connection mode
        ; (Note) Setting function select register B3 & A3 (External op-amp connection mode)
        BSET     psl3_5            ;ANEX0 use
        BSET     psl3_6            ;ANEX1 use
        MOV.B    #00000100B, prcr
        BCLR     ps3_5             ;ANEX0(P95) is I/O port
        MOV.B    #00000100B, prcr
        BCLR     ps3_6             ;ANEX1(P96) is I/O port
;
;-------------------------------------------------------------------------------
;       Start A-D conversion
;-------------------------------------------------------------------------------
        ; (Note) When the Vref connection bit is changed from 0 to 1,
        ;        start A-D conversion after an elapsing of 1 us or longer.
        MOV.W    #10, R0           ; 10 * 2cy = 20cy = 1 us or longer (@20MHz)
PRE_START:
        NOP
        NOP
        ADJNZ.W  #-1, R0, PRE_START
;
START_AD:
        ; Setting A-D conversion start flag
        BSET     adst
;
WAIT_AD_CNV:
        BTST     ir_adic           ; Waiting A-D conversion completing
        JNC      WAIT_AD_CNV
        BCLR     ir_adic           ; Clear to "0" A-D conversion interrupt request
;
COMPLETE_CNV:
        ; Reading conversion result
        MOV.W    ad0,    v_AD_result    ; Read conversion result
        AND.W    #03FFH, v_AD_result    ; Mask 10 bits result
;
STOPPED_AD:
        JMP      STOPPED_AD
;
```

```
;===============================================================================
;       Dummy interrupt processing program
;===============================================================================
dummy:
        REIT
;
;*******************************************************************************
;       Setting of fixed vector
;*******************************************************************************
        .SECTION    F_VECT, ROMDATA
        .ORG        FIXED_VECT_TOP
;
        .LWORD    dummy    ;Undefined instruction
        .LWORD    dummy    ;Overflow
        .LWORD    dummy    ;BRK instruction execution
        .LWORD    dummy    ;Address match
        .LWORD    dummy    ;
        .LWORD    dummy    ;Watchdog timer
        .LWORD    dummy    ;
        .LWORD    dummy    ;NMI
        .LWORD    RESET    ;Reset
;
        .END
```

## 5.0 Reference

**Renesas Technology Corporation Semiconductor Home page**

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**Data Sheet**

M16C/80 group Rev. E3
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