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M16C/5LD, 56D Group

Multi-Master I²C-bus Interface

1. Abstract

The multi-master I²C-bus interface is a serial communication circuit based on the I²C-bus data transmit/receive format, and is equipped with arbitration lost detection that makes multi-master communication possible.

This document describes how to use the I²C-bus interface function.

Note: I²C-bus is a trademark of Philips Electronics N.V.

2. Introduction

The application example described in this document applies to the following MCUs:

- MCUs: M16C/5LD, M16C/56D Group

The sample program in this application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above groups. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Overview

The I²C-bus interface is a serial communication circuit based on the I²C-bus data transmit/receive format, and is equipped with arbitration lost detection and clock synchronous functions.

3.1 General Call

A general call can be detected when the address data is all 0's.⁽¹⁾

Note:

1. The master transmits general call address 00h to all slaves.

3.2 Addressing Format

The 7-bit addressing format is supported.

Only the 7 high-order bits of the I²C address register (slave address) are compared with the address data.

3.3 I²C-bus Interface Related Pins

- SCLMM pins: Clock I/O pins of the I²C-bus interface
- SDAMM pins: Data I/O pins of the I²C-bus interface

3.4 Selectable Functions

The functions below can be selected when using the I²C-bus interface.

(1) Communication mode

There are four communication modes available when performing data communication:

- Master transmission: Start and stop conditions are generated (master mode). Address and control data are output to the SDA in synchronization with the SCLMM clock generated by the master device.
- Master reception: Data from the transmitting device is received in synchronization with the SCLMM clock generated by the master device.
- Slave transmission: Start and stop conditions generated by the master device are received (slave mode).
- Slave reception: Data from the transmitting device is received in synchronization with the clock generated by the master device.

(2) SCL mode

SCL mode can be selected from the following two modes:

- Standard clock mode: The bit rate can be selected in the range 16.1 to 100 kHz.
- High-speed clock mode: The bit rate can be selected in the range 32.3 to 400 kHz.

(3) ACK clock

ACK clock can be selected from the following two modes:

- ACK clock not available: No ACK clocks are generated after a data transfer.
- ACK clock available: The master device generates an ACK clock each time one byte of data is transferred.

(4) Data format

Data format can be selected from the following two modes:

- Addressing format: The received slave address and the bits SAD6 to SAD0 in the S0Di register (i=0 to 2) are compared. When an address match is found, or when a general call is received, an interrupt request is generated and additional data is transmitted and received.
- Free data format: An interrupt request is generated and additional data is transmitted and received regardless of the received slave address.

4.2 Master Transmission

Master Transmission is described in this section. The initial settings are described in 4.1 “Initial Settings”. Initial settings are assumed to be completed. Programs (A) to (C) below refer to (A) to (C) in the following figure.

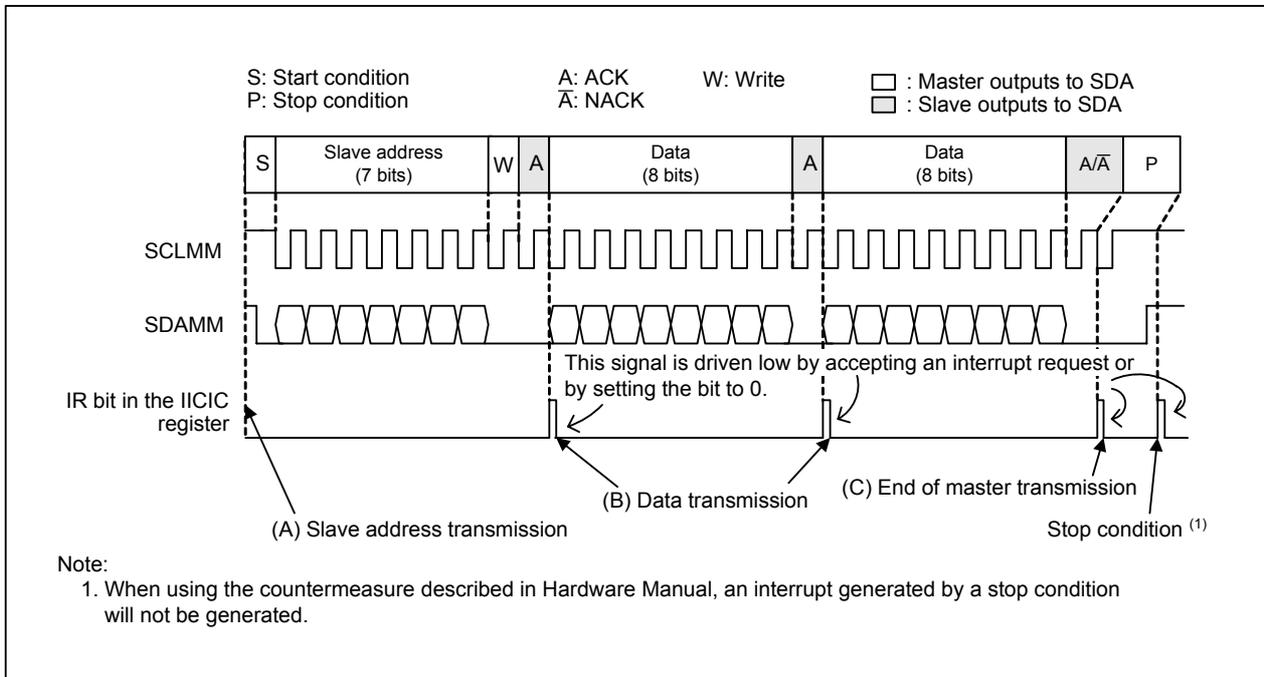


Figure 4.1 Example of Master Transmission

(A) Slave address transmission

- (1) The BB bit in the S10 register must be 0 (bus free).
- (2) Write E0h to the S10 register. (start condition standby)
- (3) Write a slave address to the seven most significant bits (MSB) and a 0 to the least significant bit (LSB). (start condition generated, then slave address transmitted)

Note that after a stop condition is generated and the BB bit becomes 0, the S10 register is write disabled for 1.5 cycle of f_{VIIIC}. Therefore, when writing E0h to the S10 register and a slave address to the S00 register during the 1.5 f_{VIIIC} cycles, a start condition is not generated. When generating a start condition immediately after the BB bit changes from 1 to 0, confirm that both the TRX and MST bits are 1 (transmit mode and master mode) after step(1), and then execute step (2).

(B) Data transmission

- (in the I²C-bus interrupt routine)
- (1) Write transmit data to the S00 register. (data transmission)

(C) Completion of master transmission

- (in the I²C-bus interrupt routine)
- (1) Write C0h to the S10 register. (stop condition standby)
 - (2) Write dummy data to the S00 register. (stop condition generated)

When the transmission is completed or ACK is not returned from the slave device (NACK returned), master transmission should be completed as shown in the example above.

If the slave device or other master device drives the SCLMM line low, use the countermeasure described in the Hardware Manual. In this case, an I²C-bus interface interrupt generated by a stop condition will not be generated.

4.3 Master Reception

Master reception is described in this section. The initial settings are described in 4.1 “Initial Settings”. Initial settings are assumed to be completed. Programs (A) to (D) below refer to (A) to (D) in the following figure.

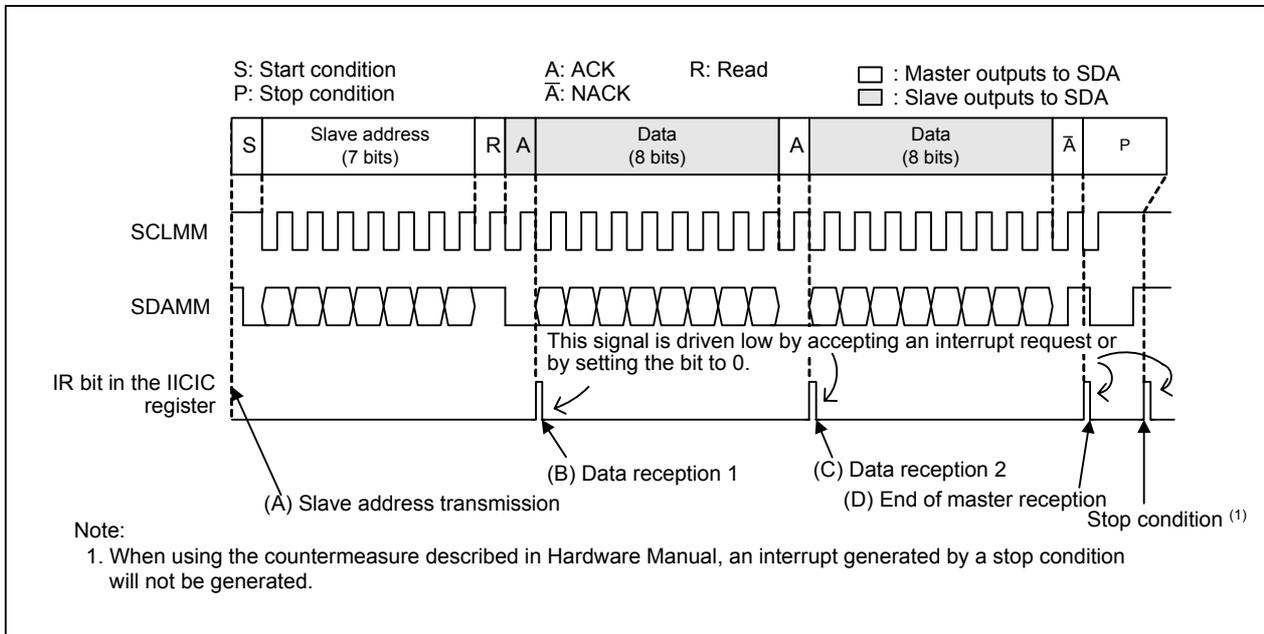


Figure 4.2 Example of Master Reception

(A) Slave address transmission

- (1) The BB bit in the S10 register must be 0 (bus free).
- (2) Write E0h to the S10 register. (start condition standby)
- (3) Write a slave address to the seven most significant bits (MSB) and a 1 to the least significant bit (LSB). (start condition generated, then slave address transmitted)

(B) Data reception 1 (after slave address transmission)

- (in the I²C-bus interrupt routine)
- (1) Write AFh to the S10 register (master receive mode).
 - (2) Set the ACKBIT bit in the S20 register to 0 (ACK is available) because the data is not the last one.
 - (3) Write dummy data to the S00 register.

(C) Data reception 2 (data reception)

- (in the I²C-bus interrupt routine)
- (1) Read the received data from the S00 register.
 - (2) Set the ACKBIT bit in the S20 register to 1 (no ACK) because the data is the last one.
 - (3) Write dummy data to the S00 register.

(D) End of master reception

- (in the I²C-bus interrupt routine)
- (1) Read the received data from the S00 register.
 - (2) Write C0h to the S10 register. (stop condition standby state)
 - (3) Write dummy data to the S00 register. (stop condition generated)

If the slave device or other master device drives the SCLMM line low, use the countermeasure described in the Hardware Manual. In this case, an I²C-bus interface interrupt generated by a stop condition will not be generated.

4.4 Slave Reception

Slave reception is described in this section. The initial settings are described in 4.1 "Initial Settings". Initial settings are assumed to be completed. Programs (A) to (C) below refer to (A) to (C) in the following figure.

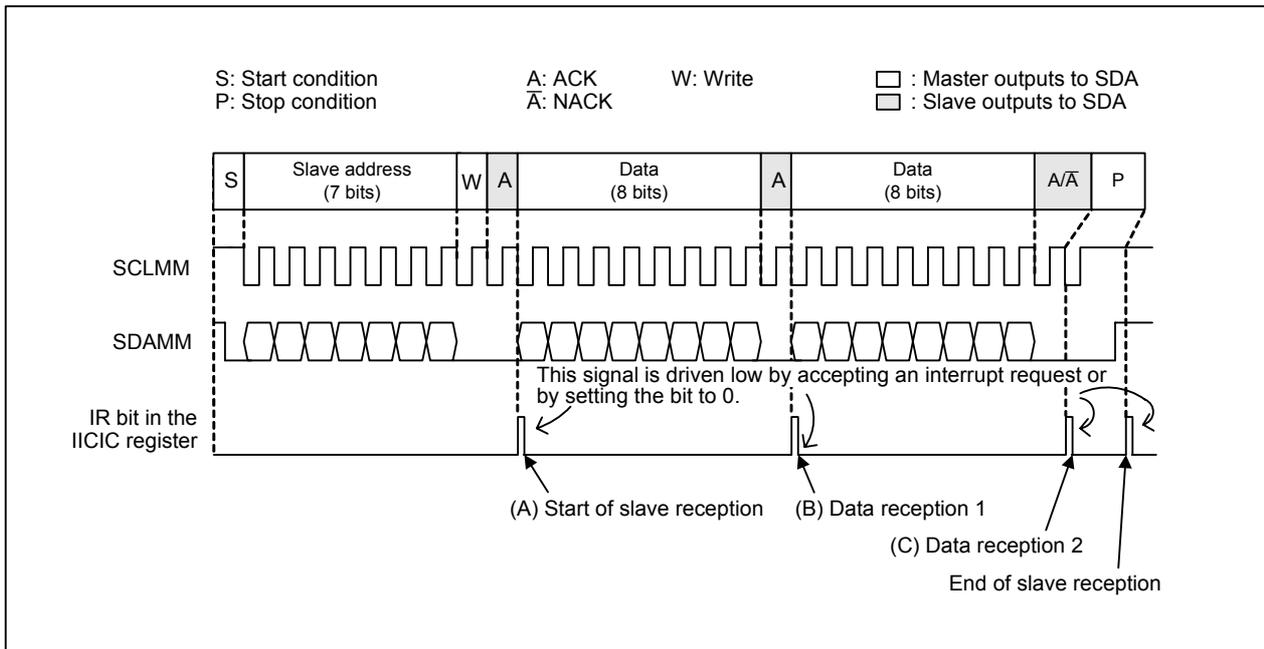


Figure 4.3 Example of Slave Reception

(A) Start of slave reception

(in the I²C-bus interrupt routine)

- (1) Check the content of S10 register. When the TRX bit is 0 (receive mode), the I²C-bus interface is in slave receive mode.
- (2) Write dummy data to the S00 register.

(B) Data reception 1

(in the I²C-bus interrupt routine)

- (1) Read the received data from the S00 register.
- (2) Set the ACKBIT bit in the S20 register to 0 (ACK is available) because the data is not the last one.
- (3) Write dummy data to the S00 register.

(C) Data reception 2

(in the I²C-bus interrupt routine)

- (1) Read the received data from the S00 register.
- (2) Set the ACKBIT bit in the S20 register to 1 (no ACK) because the data is the last one.
- (3) Write dummy data to the S00 register.

4.5 Slave Transmission

Slave transmission is described in this section. The initial settings are described in 4.1 Initial Settings. Initial settings are assumed to be completed. Program (A) and (B) below refer to (A) and (B) in the following figure. When arbitration lost is detected, the TRX bit becomes 0 (receive mode) even when the bit after the slave address is 1 (read). Therefore, after arbitration lost is detected, read the S00 register. When bit 0 in the S00 register is 1, write 4Fh (slave transmit mode) to the S10 register and execute slave transmission.

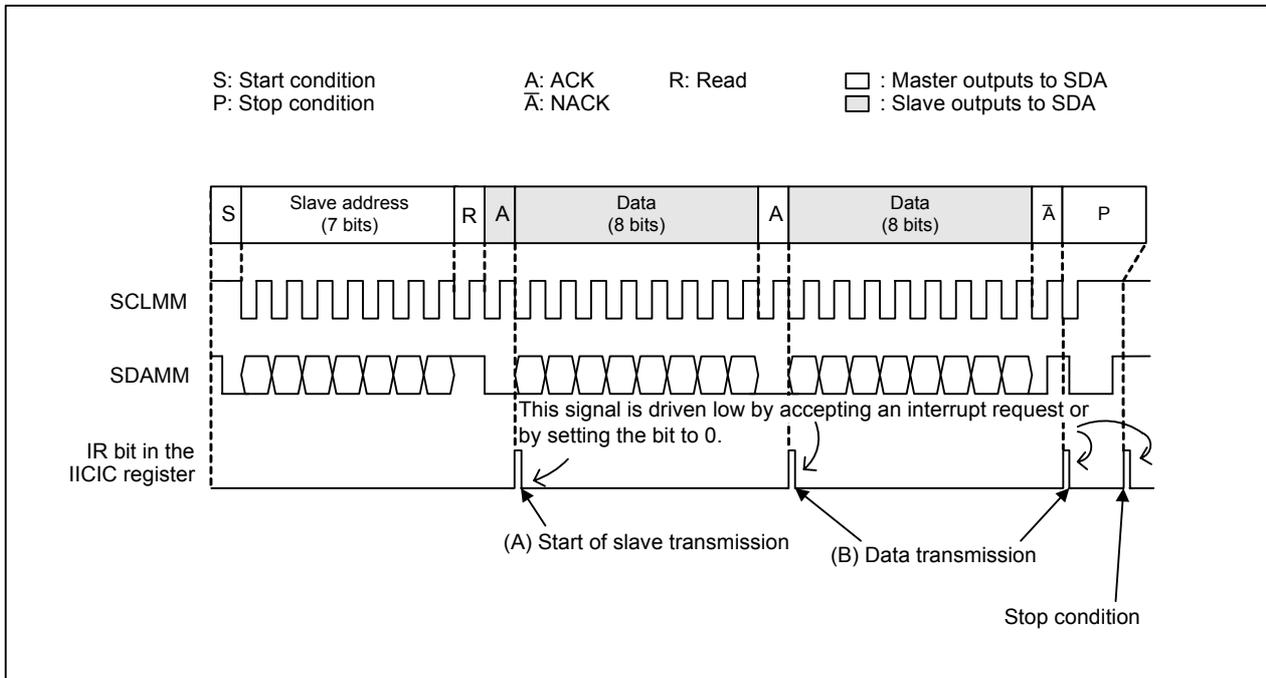


Figure 4.4 Example of Slave Transmission

(A) Start of slave transmission

(in the I²C-bus interrupt routine)

- (1) Check the content of the S10 register. When the TRX bit is 1 (transmit mode), the I²C-bus interface is in slave transmit mode.
- (2) Write transmit data to the S00 register.

(B) Data transmission

(in the I²C-bus interrupt routine)

- (1) Write transmit data to the S00 register.

Write dummy data to the S00 register even if an interrupt occurs at an ACK clock of the last transmitted data. When the S00 register is written, the SCLMM pin becomes high-impedance.

5. Arbitration Lost

The following describes the operation of the I²C-bus interface when arbitration lost occurs. Figure 5.1 shows the Operation Timing of the Arbitration Lost Detect Flag.

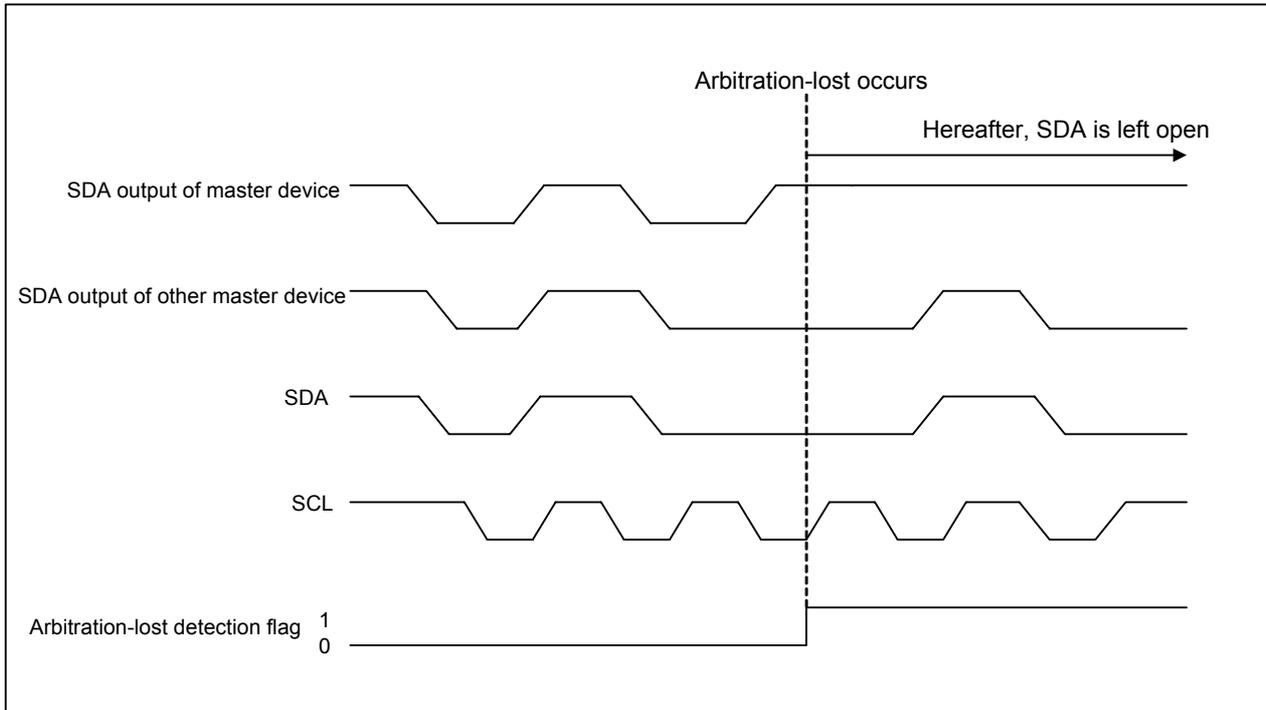


Figure 5.1 Operation Timing of the Arbitration Lost Detect Flag

When arbitration lost occurs, the arbitration lost detect flag becomes 1.

(1) Arbitration lost occurs while transmitting a slave address

When arbitration lost is detected, the communication mode automatically changes to slave reception which enables to receive the slave address. If the selected data format is the addressing format, the slave address can be determined by reading the AAS bit in the S10 register.

(2) Arbitration lost occurs while transmitting data following the slave address

When arbitration lost is detected, the communication mode automatically changes to slave reception, which enables to receive the data.

6. Interrupt

The I²C-bus interface has the following four interrupt sources:

(1) Interrupt when 9-bit transmission/reception is completed (including ACK/NACK)

The interrupt source can be determined by reading the WIT bit in the S3D0 register. When the WIT bit is 0, it is determined that the generated interrupt is attributable to this interrupt source.

(2) Interrupt when 8 bits are received

Setting the WIT bit to 1 enable this interrupt source.

The interrupt source can be determined by reading the WIT bit. When the WIT bit is 1, it is determined that the generated interrupt is attributable to this interrupt source.

If no determination is made of ACK/NACK transmissions, there is no need to use this interrupt.

(3) Interrupt when a stop condition is detected

Setting the SIM bit in the S3D0 register to 1 enables this interrupt source.

The interrupt source can be determined by reading the SCPIN bit in the S4D0 register. When a stop condition is detected, the SCPIN bit becomes 1.

(4) Interrupt when the SCL clock remains high for more than a predetermined time during communication

Setting the TOE bit in the S4D0 register to 1 enables this interrupt source.

The interrupt source can be determined by reading the TOF bit in the S4D0 register.

When the SCL clock remains high for more than a predetermined time during communication, the TOF bit becomes 1.

Figure 6.1 shows the I²C-bus Interface Interrupt Request Generation Timing.

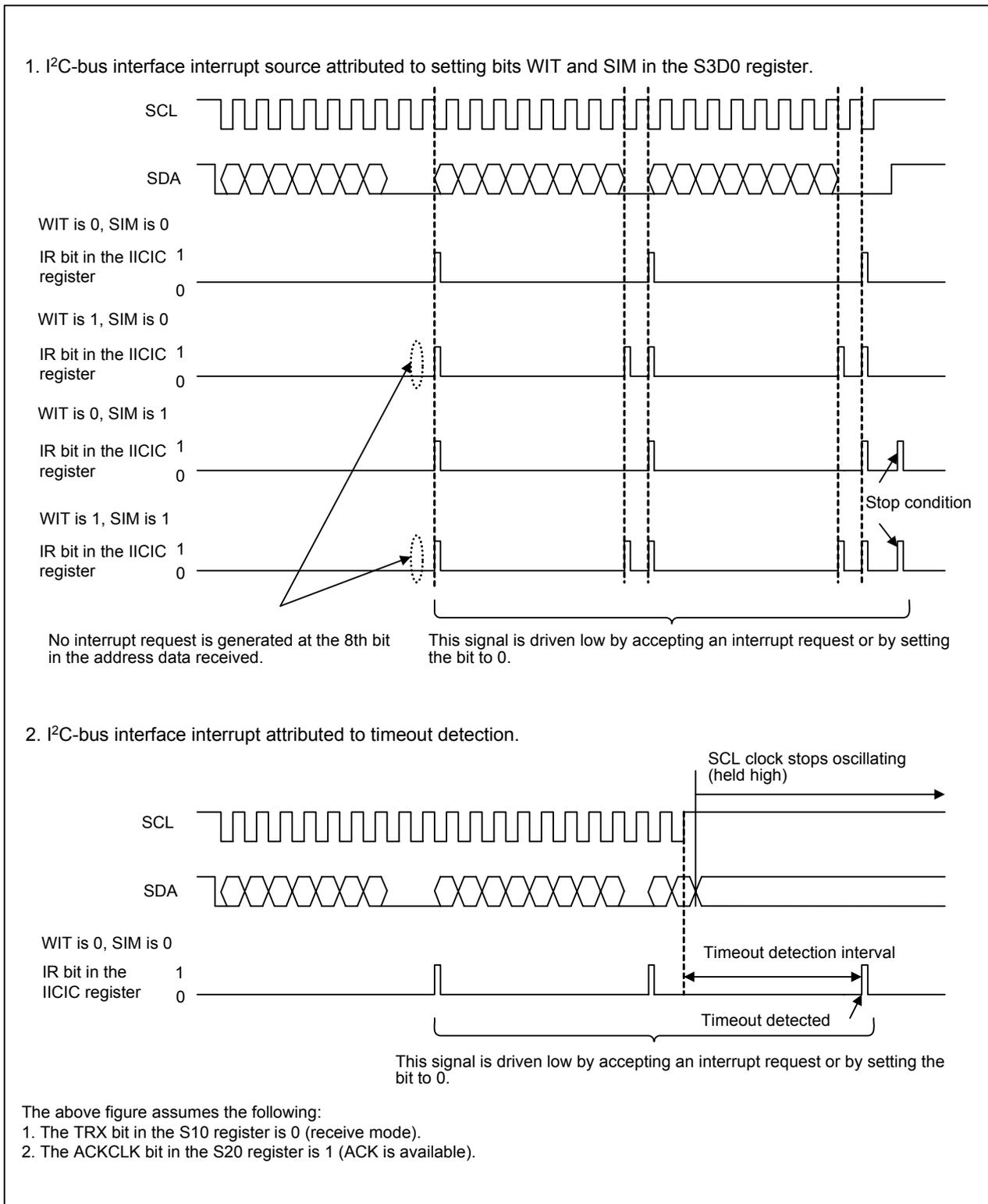


Figure 6.1 I²C-bus Interface Interrupt Request Generation Timing

7. Notes on I²C-bus Interface

7.1 Generating Start Condition

After a stop condition is generated and BB bit becomes 0 (bus free), the S10 register is write disabled for 1.5 cycles of fVIIC. When writing a slave address to the S00 register afterwards, a start condition is not generated. When generating a start condition immediately after the BB bit changes from 1 to 0, confirm that both the TRX and MST bits are 1, and then write a slave address to the S00 register.

8. Sample Program

This sample program is provided for reference purpose only, and is not guaranteed to operate properly in all system. When incorporating it into a system, careful examination is recommended before using this sample program. Furthermore, since its functionality as integral part of a system cannot be evaluated with this program alone, evaluation with the final system is indispensable.

8.1 Connection Example

Figure 8.1 shows the Sample Program Operation Environment.

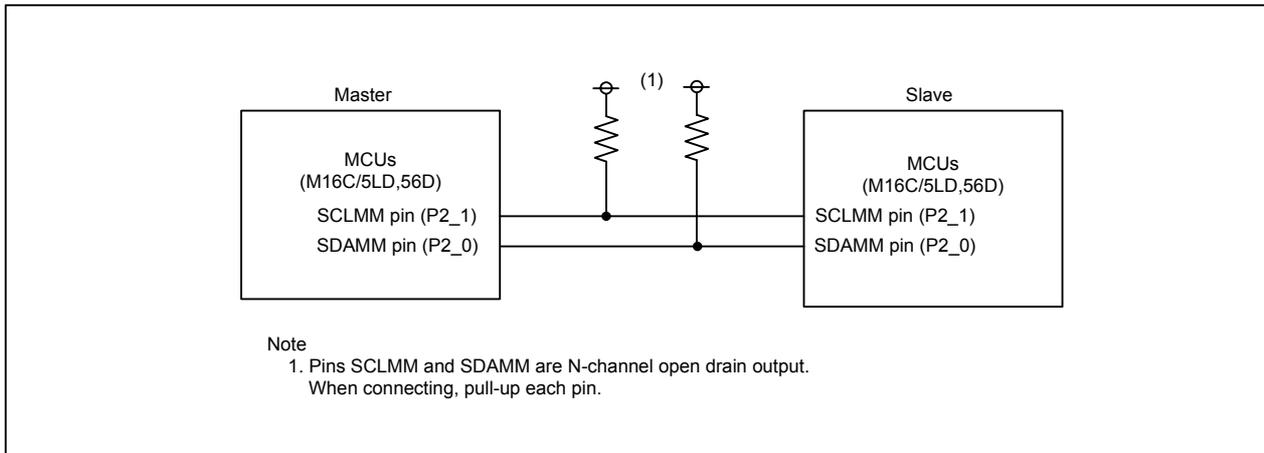


Figure 8.1 Sample Program Operating Environment

8.2 Operation Conditions

Table 8.1 lists the Sample Program Operation Conditions.

Table 8.1 Sample Program Operation Conditions

Item	Content
Peripheral function clock (fIIC)	24 MHz (XIN: 6 MHz, PLL clock: Divided-by-2, and then multiplied-by-8)
I ² C-bus system clock (fVIIC)	4 MHz (fIIC divided-by-6)
Bit rate	100 kbps (fVIIC divided-by-8 and further divided-by-5)
SCL mode	Standard clock mode
Data format	Addressing mode
Slave address compare	S0D0 register only
Stop condition detect interrupt	Enabled
Data receive interrupt	Enabled
Timeout detection function	Enabled

8.3 Sample Program Setting

Four communication modes can be used in the sample program: master transmission, master reception, slave reception, and slave transmission. When calling the "mode_ini" function, the communication modes can be selected by setting arguments.

Set the other slave address and own slave address in define declaration area in the sample program.

Figure 8.2 shows the Setting Example of Master Transmission. Figure 8.3 shows the Setting Example of Slave Address(0x09) and Own Slave Address(0x10).

```

/*func comment*****
/* Main Program
/*func comment end*****
void main(void){
- Omitted -
/*=====*/
/*= Modify start
/*=====*/
mode_ini(MASTER,SND); /* First argument */
                        /* MASTER : master */
                        /* SLAVE : slave */
                        /* Second argument */
                        /* SND : transfer */
                        /* REV : receive */
/*=====*/
/*= Modify end
/*=====*/

```

Set the master (MASTER)/slave (SLAVE) as the first argument and send (SND)/receive (REV) as the second argument.

Figure 8.2 Communication Mode Setting Example

```

/*=====*/
/* DEFINE
/*=====*/
/*=====*/
/*= Modify start
/*=====*/
#define SLAVE_ADD 0x09 /* Other slave address(7bit) */
#define SELF_ADD 0x10 /* My slave address(7bit) */
/*=====*/
/*= Modify end
/*=====*/

```

Figure 8.3 Slave Address Setting Example

8.4 Operation Example

8.4.1 Master Transmission and Slave Reception

Figure 8.4 shows the Master Transmission and Slave Reception Operation Example.

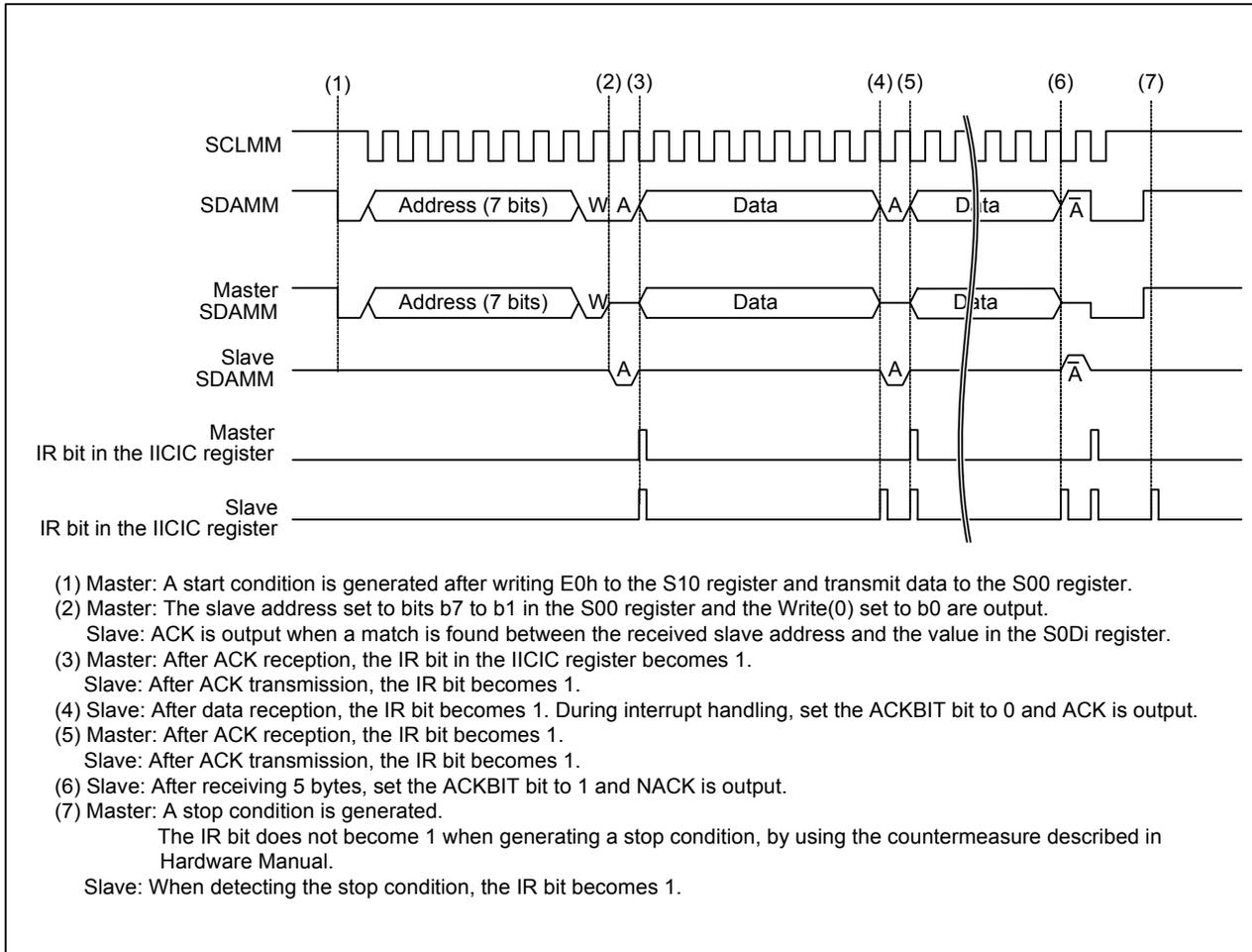


Figure 8.4 Master Transmission and Slave Reception Operation Example

8.4.2 Master Reception and Slave Transmission

Figure 8.5 shows the Master Reception and Slave Transmission Operation.

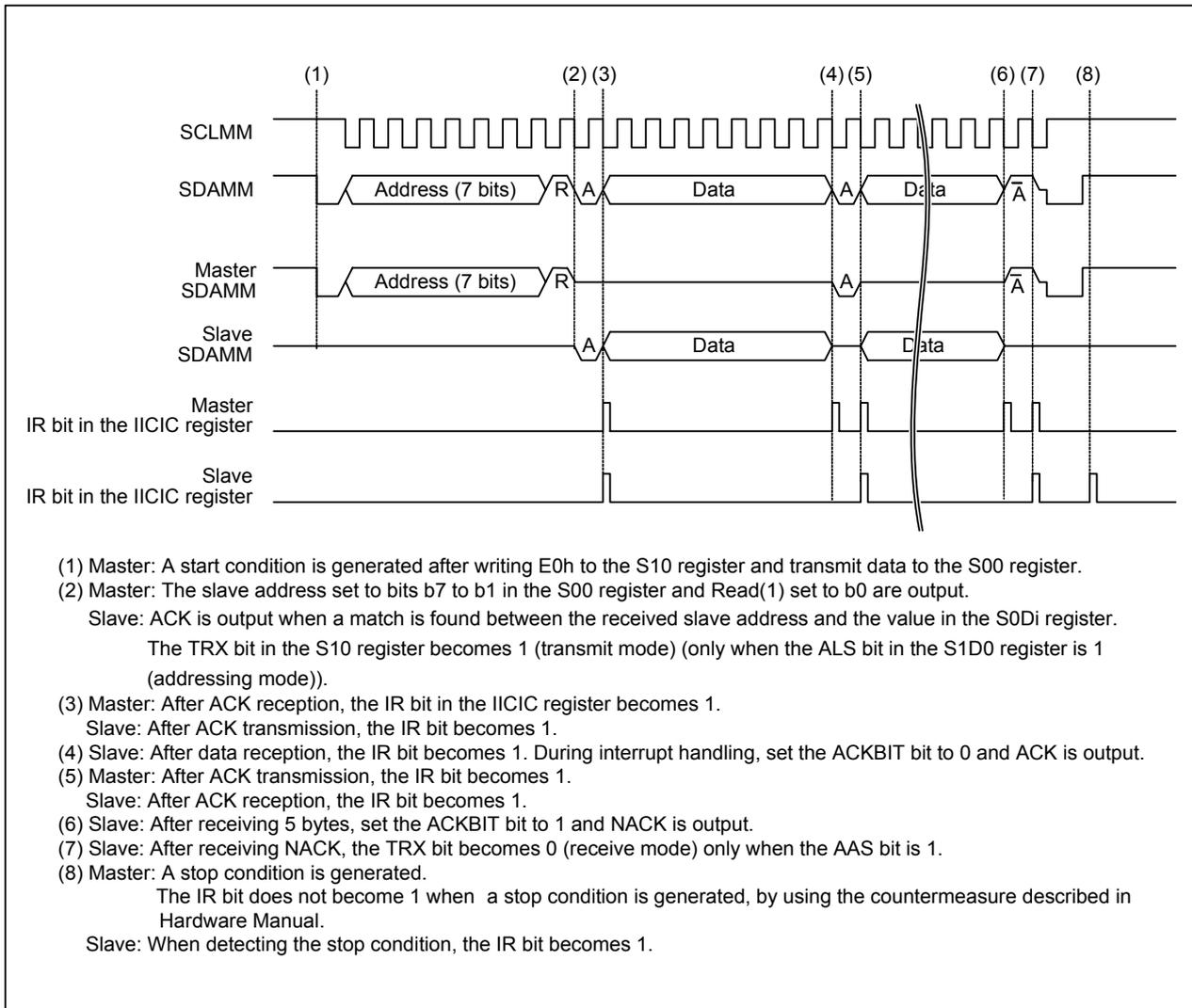


Figure 8.5 Master Reception and Slave Transmission Operation

8.5 Function Tables

Declaration	void iic_ini(unsigned char ini,unsigned char sub_address)	
Outline	I ² C-bus initialization function	
Argument	Argument name	Meaning
	ini	I ² C-bus function enabled/disabled
		ENABLED: I ² C-bus function enabled DISABLED: I ² C-bus function disabled
sub_address	Slave address setting	
Variable(global)	Variable name	Content
	iic_mode	For selecting communication mode
	iic_index	For the number of transfers
Returned value	None	
Function	<p>When Argument ini = ENABLED (I²C-bus function enabled), initializes the I²C-bus before enabling interrupts.</p> <p>When Argument ini = DISABLED (I²C-bus function disabled), disables the I²C-bus interface and the interrupt.</p>	

Declaration	void mode_ini(unsigned char ms, unsigned char sr)	
Outline	Function for setting respective communication modes	
Argument	Argument name	Meaning
	ms	Select master or slave.
		MASTER: Master SLAVE: Slave
	sr	Select transmission or reception
SND: Transmit mode REV: Receive mode		
Variable(global)	Variable name	Content
	iic_ram[]	Data storage alignment for master transmit
	iic_length	For transmit and receive size
Returned value	None	
Function	Sets the respective communication modes.	

Declaration	unsigned char iic_master_start(unsigned char slave, unsigned char sr, unsigned char *buf, unsigned char len)			
Outline	Master start function			
Argument	Argument name	Meaning		
	slave	Specified slave address(0x00 to 0x7f)		
	sr	Select transmission or reception		
		SND: Transmit mode REV: Receive mode		
	*buf	Pointer to transmit buffer		
len	Transmit/receive data size (0x00 to 0xff)			
Variable(global)	Variable name	Content		
	iic_slave	Variable for storing slave address		
	iic_length	For transmit and receive size		
	iic_pointer	Pointer to transmit buffer		
	iic_mode	For selecting communication mode		
Returned value	Type	Meaning		
			unsigned char	Master start failure/start successful
			FALSE: Master start failure	
			TRUE: Master start successful	
Function	Transmits the start condition and slave address after master setting.			

Declaration	void master_transfer(void)	
Outline	Master transmit function	
Argument	None	
Variable(global)	Variable name	Content
	iic_mode	For selecting communication mode
	iic_length	For transmit and receive size
	iic_pointer	Transmit buffer pointer
Returned value	None	
Function	Detects arbitration lost, confirms ACK/NACK reception, and transmits data.	

Declaration	void master_receive(void)	
Outline	Master receive function	
Argument	None	
Variable(global)	Variable name	Content
	iic_length	For selecting communication mode
	iic_index	For transmit and receive size
	iic_pointer	Receive buffer pointer
Returned value	None	
Function	Detects arbitration lost, transmits ACK/NACK, and receives data.	

Declaration	void slave_receive(void)	
Outline	Slave receive function	
Argument	None	
Variable(global)	Variable name	Content
	iic_length	For transmit and receive size
	iic_index	Number of transfers
	iic_pointer	Receive buffer pointer
Returned value	None	
Function	Receives data and transmits ACK/NACK.	

Declaration	void slave_transfer(void)	
Outline	Slave transmit function	
Argument	None	
Variable(global)	Variable name	Content
	iic_length	For transmit and receive size
	iic_index	Number of transfers
	iic_pointer	Transmit buffer pointer
Returned value	None	
Function	Receives data and transmits ACK/NACK.	

Declaration	void idle_mode(void)	
Outline	Transmit and receive mode select function	
Argument	None	
Variable(global)	Variable name	Content
	iic_mode	For selecting communication mode
Returned value	None	
Function	Selects transmit mode or receive mode when receiving data.	

Declaration	unsigned char* select_buffer(unsigned char RW)	
Outline	Function for obtaining transmit and receive buffer addresses	
Argument	Argument name	Meaning
	RW	Select transmit and receive buffer
		0: Slave receive buffer 1: Slave transmit buffer
Variable(global)	None	
Returned value	Type	Meaning
	unsigned char*	Transmit and receive buffer address
Function	Obtains transmit and receive buffer addresses.	

Declaration	void receive_stop_condition(void)	
Outline	Stop condition reception state processing function	
Argument	None	
Variable(global)	Variable name	Content
	iic_mode	For selecting communication mode
	iic_index	Number of transfers
Returned value	None	
Function	Clears the stop condition detection interrupt request bit and initializes the communication mode.	

Declaration	void iic_master_end(unsigned char status)	
Outline	Master control completion function	
Argument	Argument name	Meaning
	status	Status after mater control 0x10: Master transmission completed 0x11: Arbitration lost is detected during master transmission 0x12: NACK is received during master transmission 0x20: Master reception completed 0x21: Arbitration lost is detected during master reception 0x22: NACK is received during master reception
Variable(global)	None	
Returned value	None	
Function	Carries out the processing after master control is completed. This application note does not include any processing. Add if the need arises.	

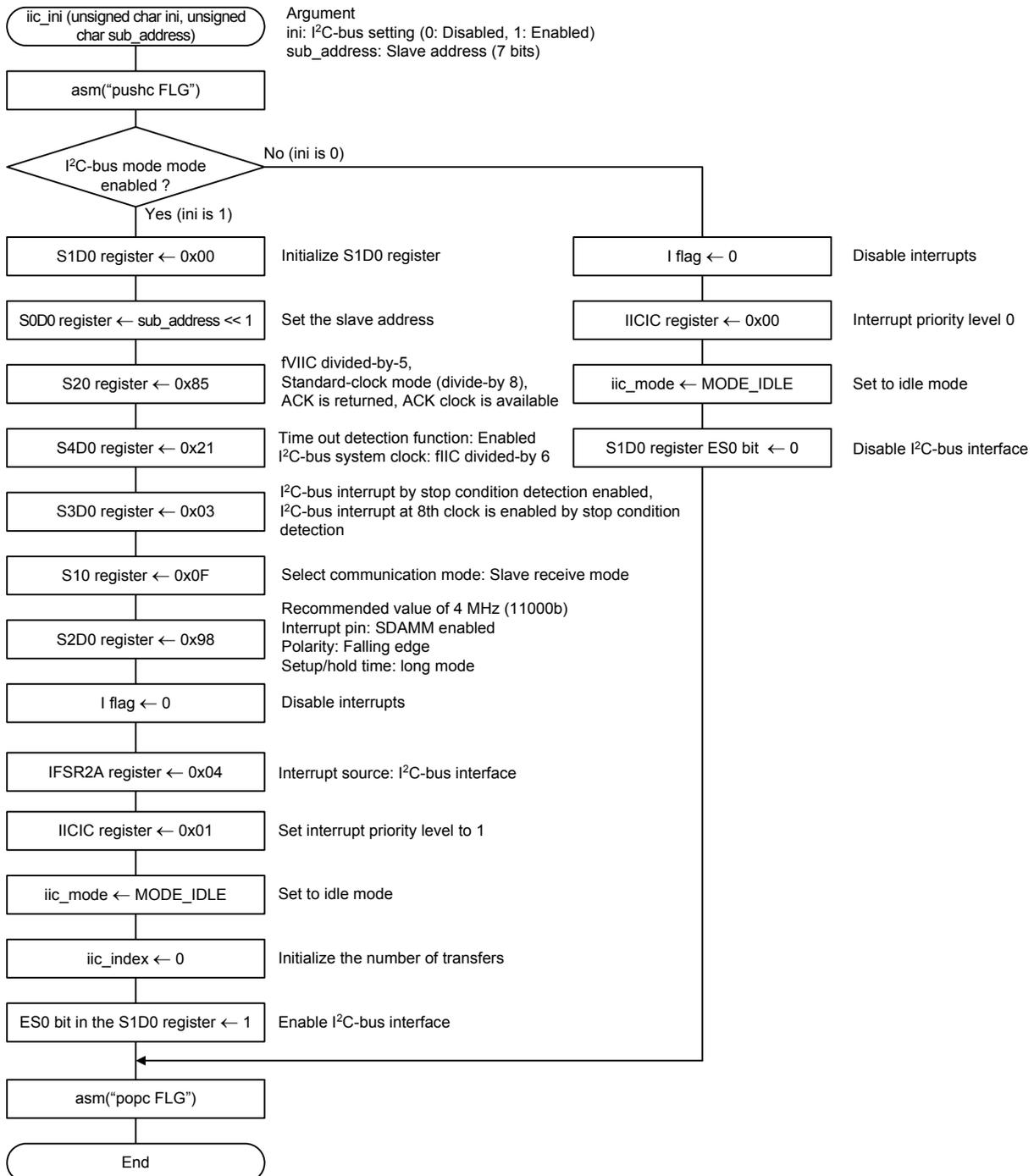
Declaration	void iic_slave_end(unsigned char status)	
Outline	Slave control completion function	
Argument	Argument name	Meaning
	status	Status after slave control completed 0x10: Master transmission completed
Variable(global)	None	
Returned value	None	
Function	Carries out the processing after slave control is completed. This application note does not include any processing. Add if the need arises.	

Declaration	void stop_condition(void)
Outline	Stop condition generation function
Argument	None
Variable(global)	None
Returned value	None
Function	Generates a stop condition by using the method of the Generate Stop Condition process that described in the Hardware Manual.

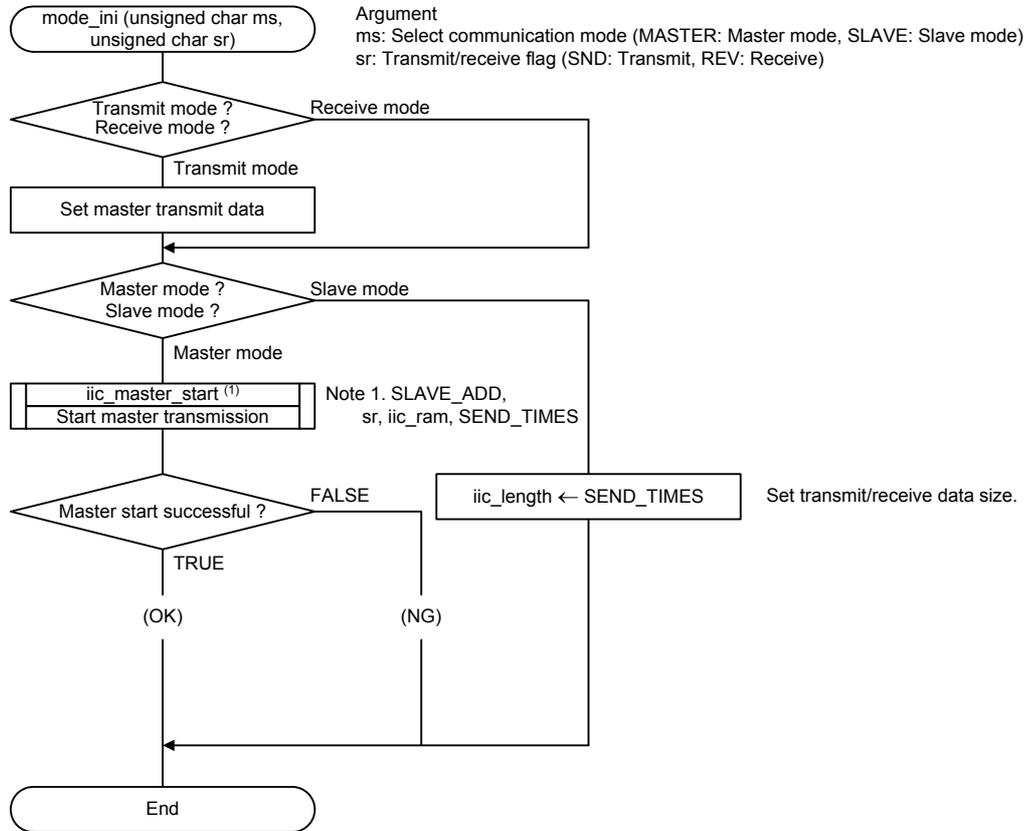
Declaration	void soft_wait(unsigned int time)	
Outline	Software wait function	
Argument	Argument name	Meaning
	time	Wait time
		SETUP_TIME: Setup time for generating a stop condition WAIT_TIME: Wait time (approx. 5 μsec)
Variable(global)	None	
Returned value	None	
Function	Generates wait time.	

8.6 Flowcharts

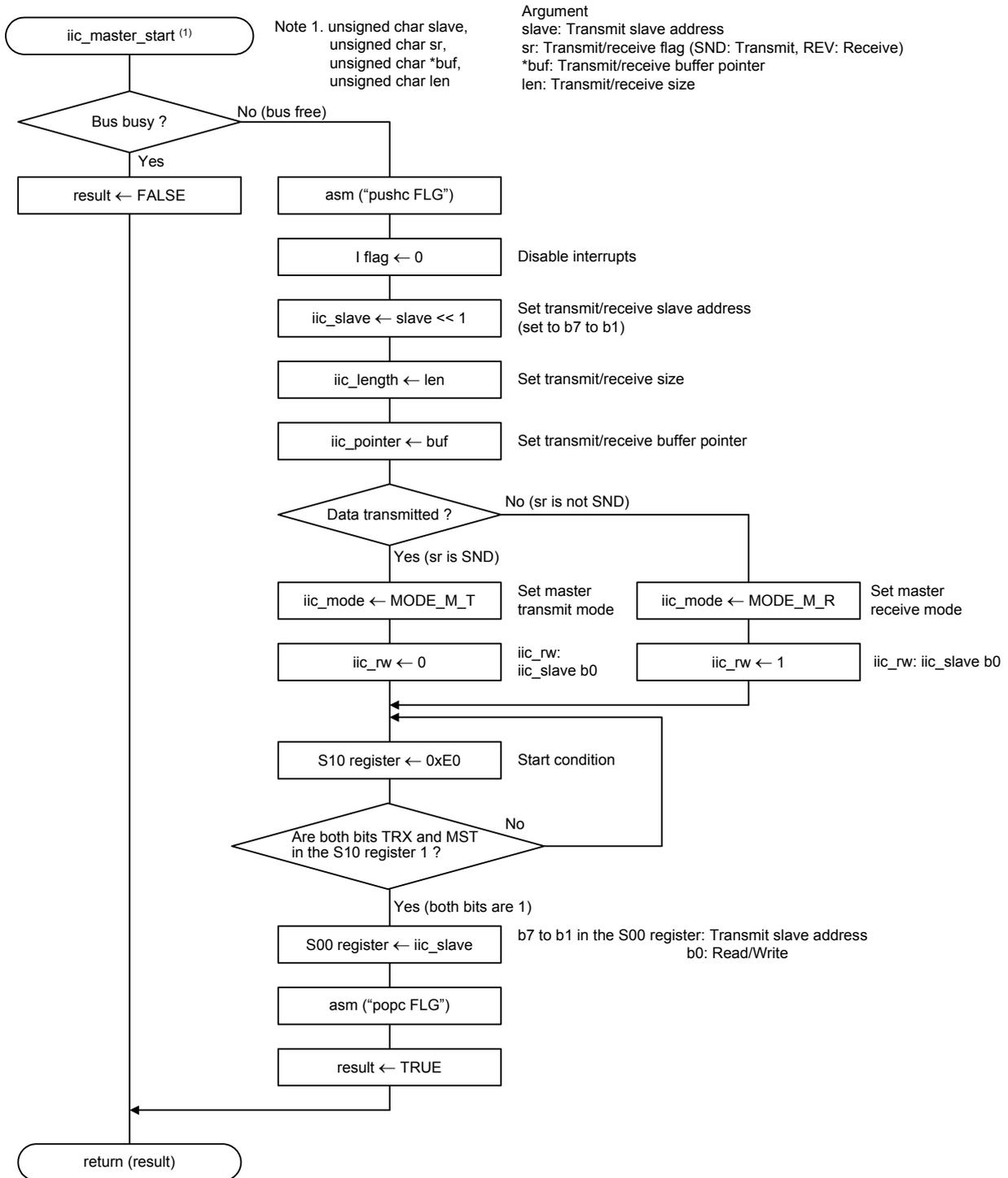
8.6.1 I²C-bus Initialization Function



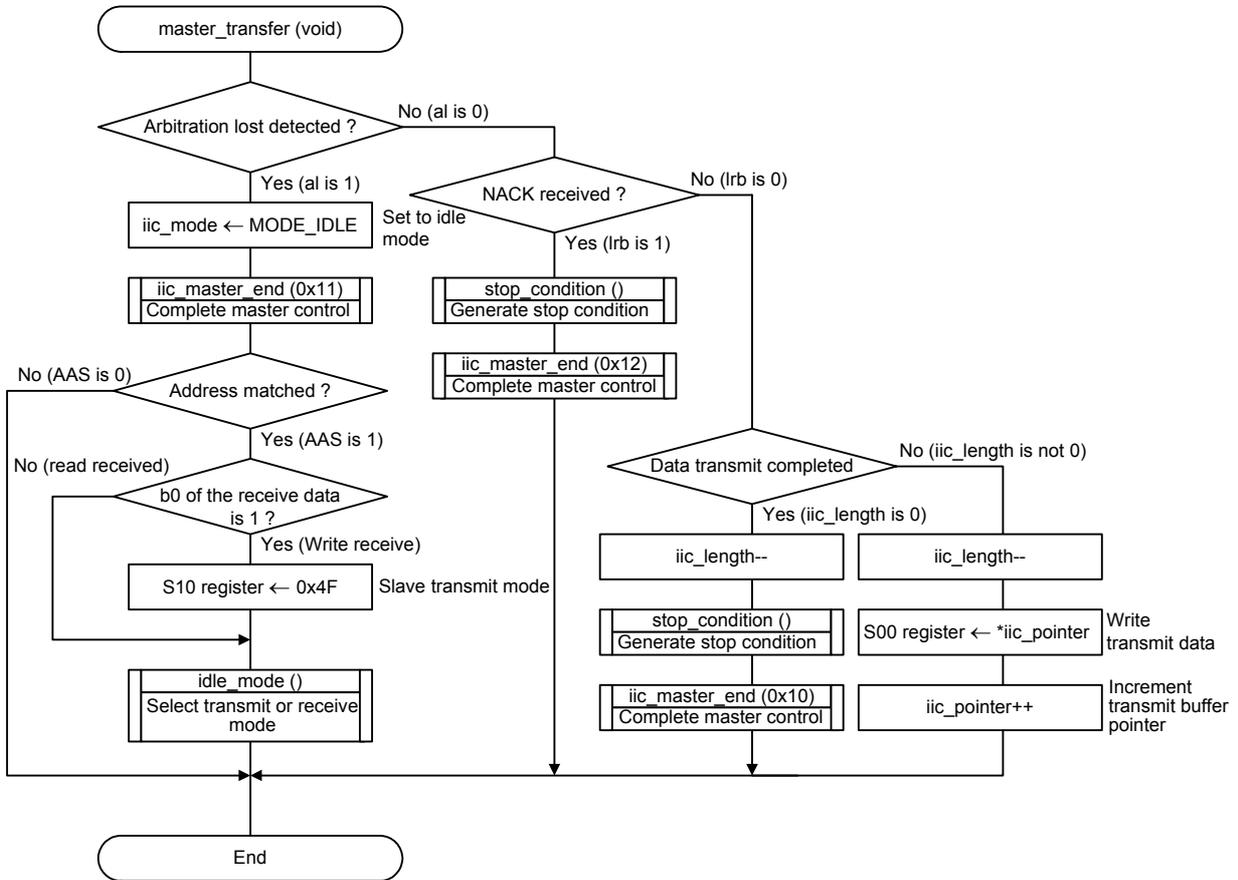
8.6.2 Function for Setting Respective Communication Modes



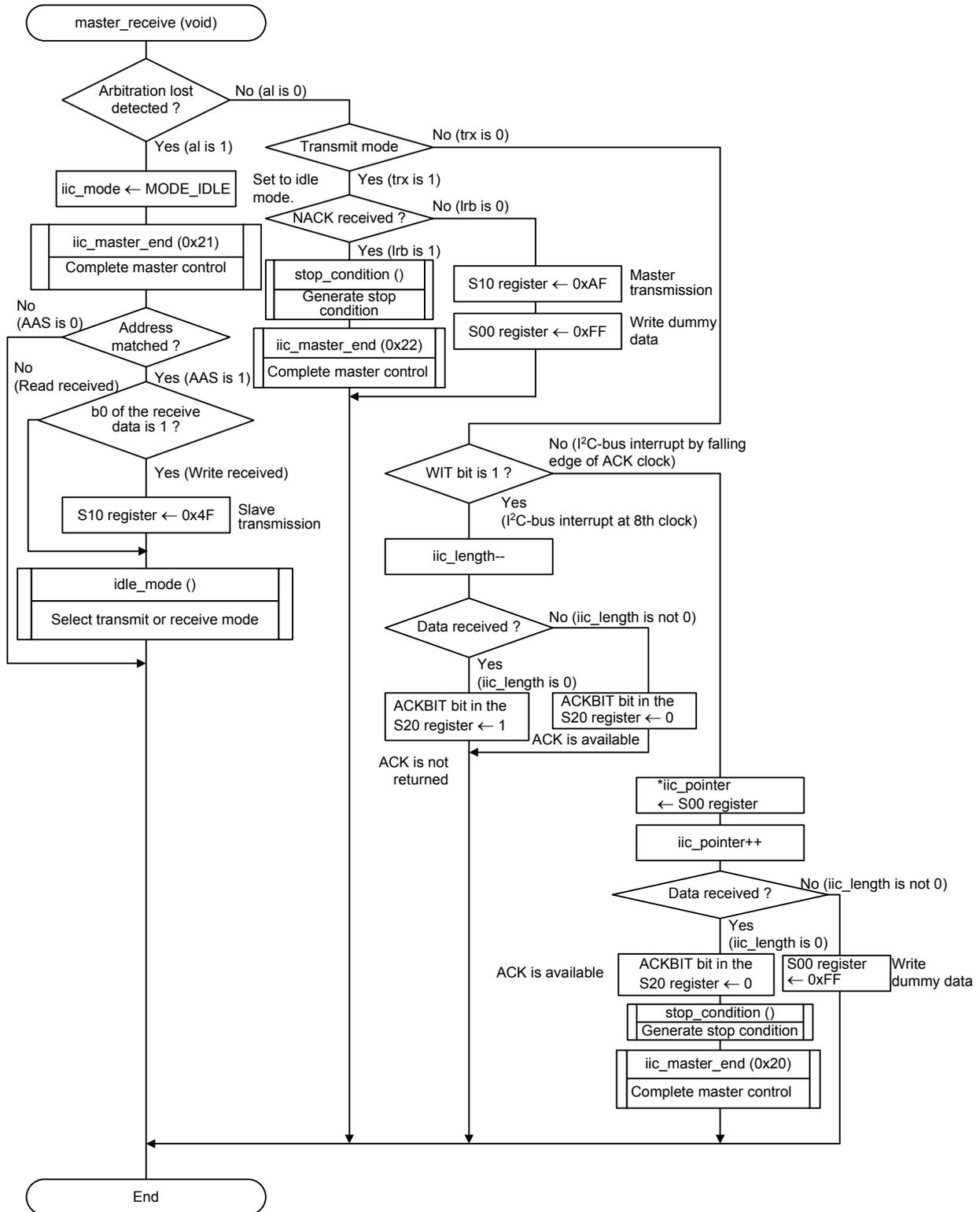
8.6.3 Master Start Function



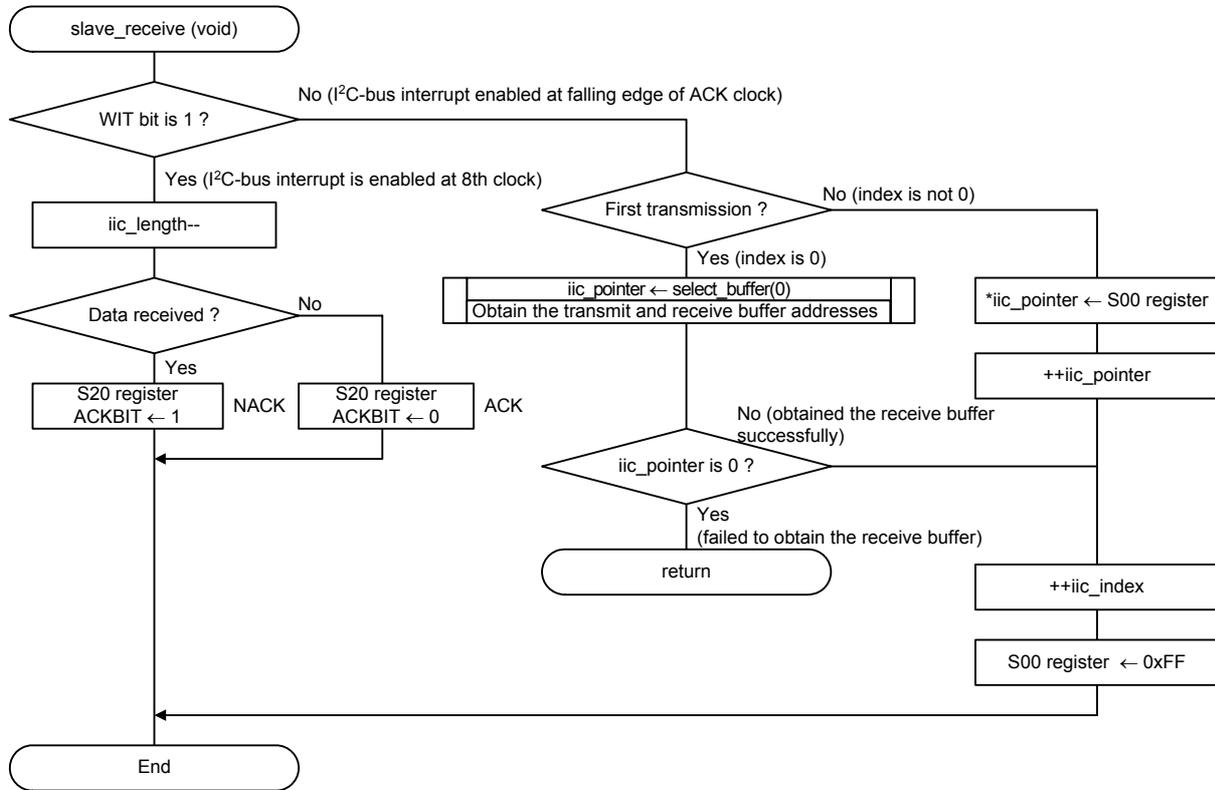
8.6.4 Master Transmit Function



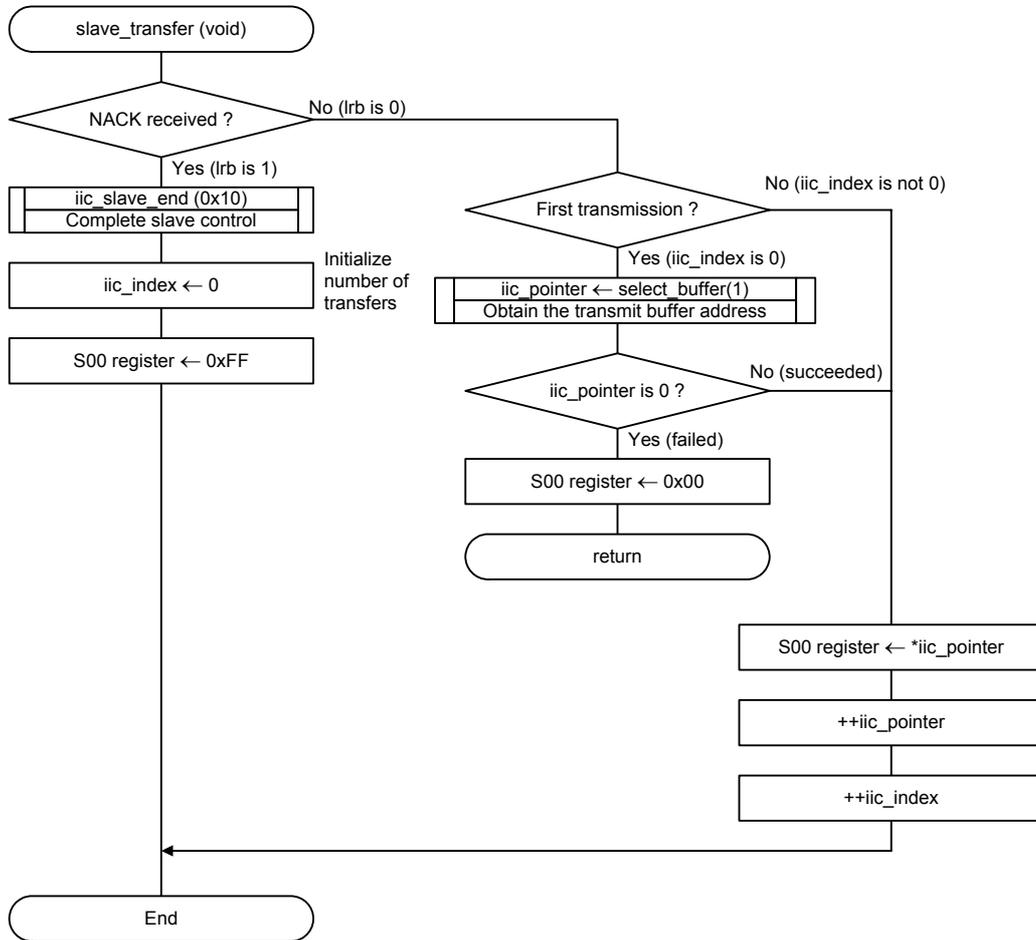
8.6.5 Master Receive Function



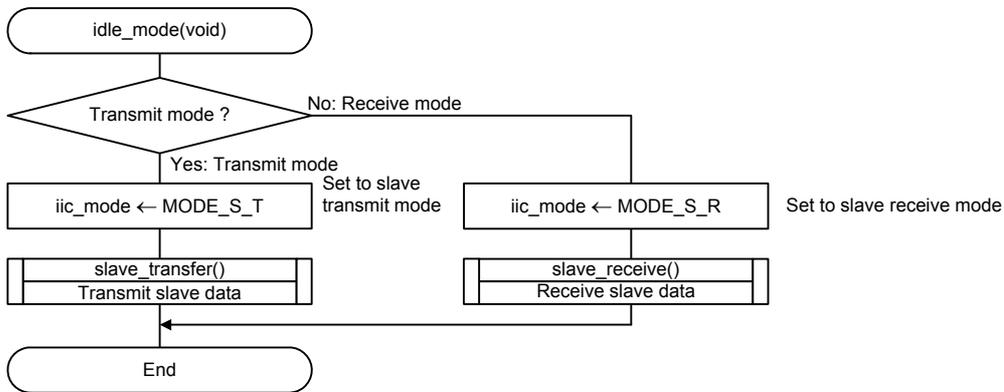
8.6.6 Slave Receive Function



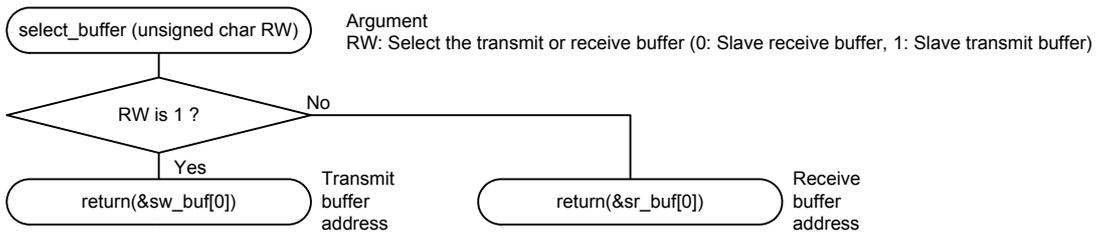
8.6.7 Slave Transmit Function



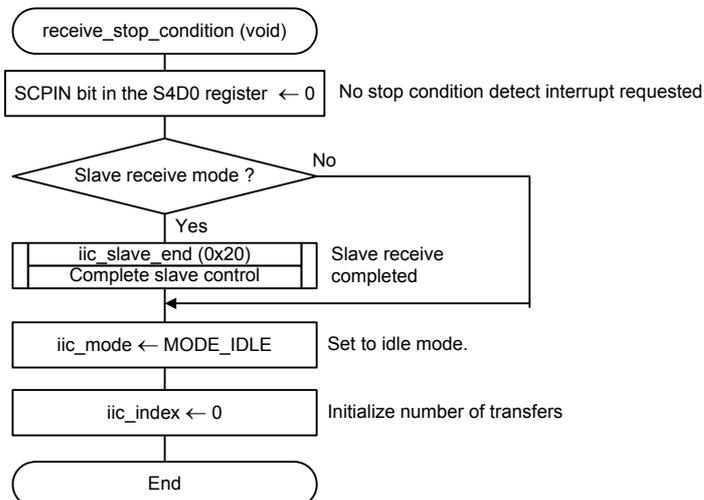
8.6.8 Transmit and Receive Mode Select Function



8.6.9 Function for Obtaining Transmit and Receive Buffer Addresses



8.6.10 Stop Condition Reception State Processing Function



8.6.11 I²C-bus Interface Interrupt Handling



9. Sample Program

A sample program can be downloaded from the Renesas Technology website. To download, click "Application Notes" in the left-hand side menu of the M16C Family page.

10. Reference Documents

Hardware Manual

M16C/5LD Group, M16C/56D Group Hardware Manual Rev.0.70

The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Technology website.

C Compiler Manual

M16C Series, R8C Family C Compiler Package V.5.45 C Compiler User's Manual Rev.1.00

The latest version can be downloaded from the Renesas Technology website.

Website and Support

Renesas Technology Website
<http://www.renesas.com/>

Inquiries
<http://www.renesas.com/inquiry>
csc@renesas.com

REVISION HISTORY	M16C/5LD, 56D Group Multi-Master I ² C-bus Interface
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Rev.	Date	Description	
		Page	Summary
1.00	Dec 02, 2009	–	First edition issued

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