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SH7080 Group

External Pulse Width Measurement Using Channel 5 of the MTU2

Introduction

This application note describes external pulse width measurement using channel 5 of the multi-function timer pulse unit 2 (MTU2). Please use this application note as a guide in designing user programs.

Although the programs given in this application note have been verified for correct operation, we strongly recommend that the user confirm correct operation before applying the programs in the actual application.

Target Device

SH7085

Contents

1. Specifications

In this sample application, the external pulse measuring function using channel 5 of the MTU2 is used to measure the high-level width of the signal input from the TIC5U pin. Figure 1 shows the basic specifications of this sample task.

- Channel 5 of the MTU2 is set up for external pulse width measurement to measure the high pulse duration of the input signal on the TIC5U pin. Timer counter TCNTU_5 counts up while the input signal is high and halts while low.
- Channels 3 and 4 of the MTU2 are placed in complementary PWM mode to output six-phase PWM waveforms and a toggle waveform synchronized with the PWM period. The PWM period is set to 100 µs (carrier frequency is 10 kHz).
- Capture on channel 5 takes place every 100 µs, at the timing when the operation of timer counter TCNT_3 of channel 3 changes from incrementing to decrementing.
- The captured value of timer counter TCNTU_5 of channel 5 is stored in timer general register TGRU_5. The value indicates the high pulse duration count for the TIC5U pin input signal.
- For the TIC5U pin of channel 5, the complementary PWM output from the TIOC3B pin is input as a dummy input.

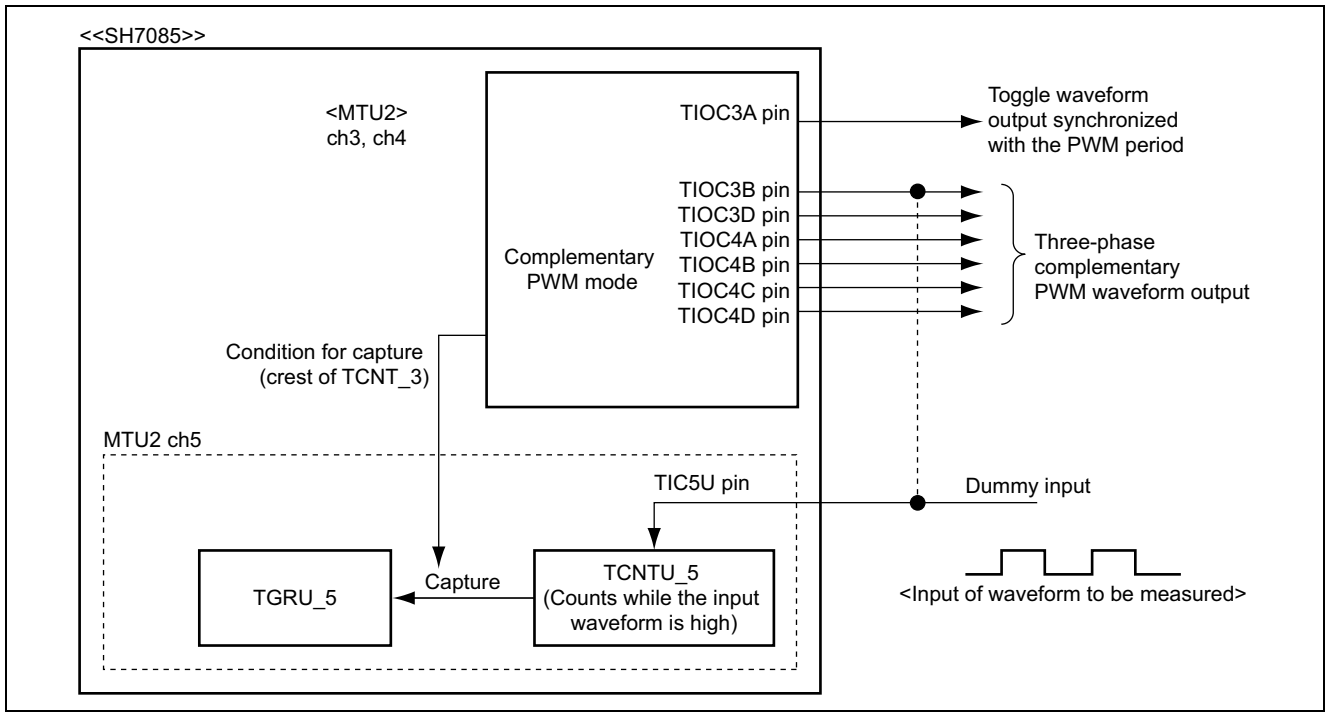


Figure 1 Overview

2. Conditions for Application

Operating frequency:	Internal clock:	80 MHz
	Bus clock:	40 MHz
	Peripheral clock:	40 MHz
	MTU2 clock:	40 MHz
	MTU2S clock:	80 MHz
C compiler:	Version 7.1.04 from Renesas Technology Corp.	

3. MCU Functions Used

This sample application applies the external pulse measurement feature that uses channel 5 of the MTU2 to measure the high pulse duration of the TIC5U pin input signal.

3.1 Channel 5 of Multi-Function Timer Pulse Unit 2 (MTU2)

Channel 5 of the MTU2 measures the high pulse duration of the TIC5U pin input signal. Figure 2 outlines the operation of the functions used.

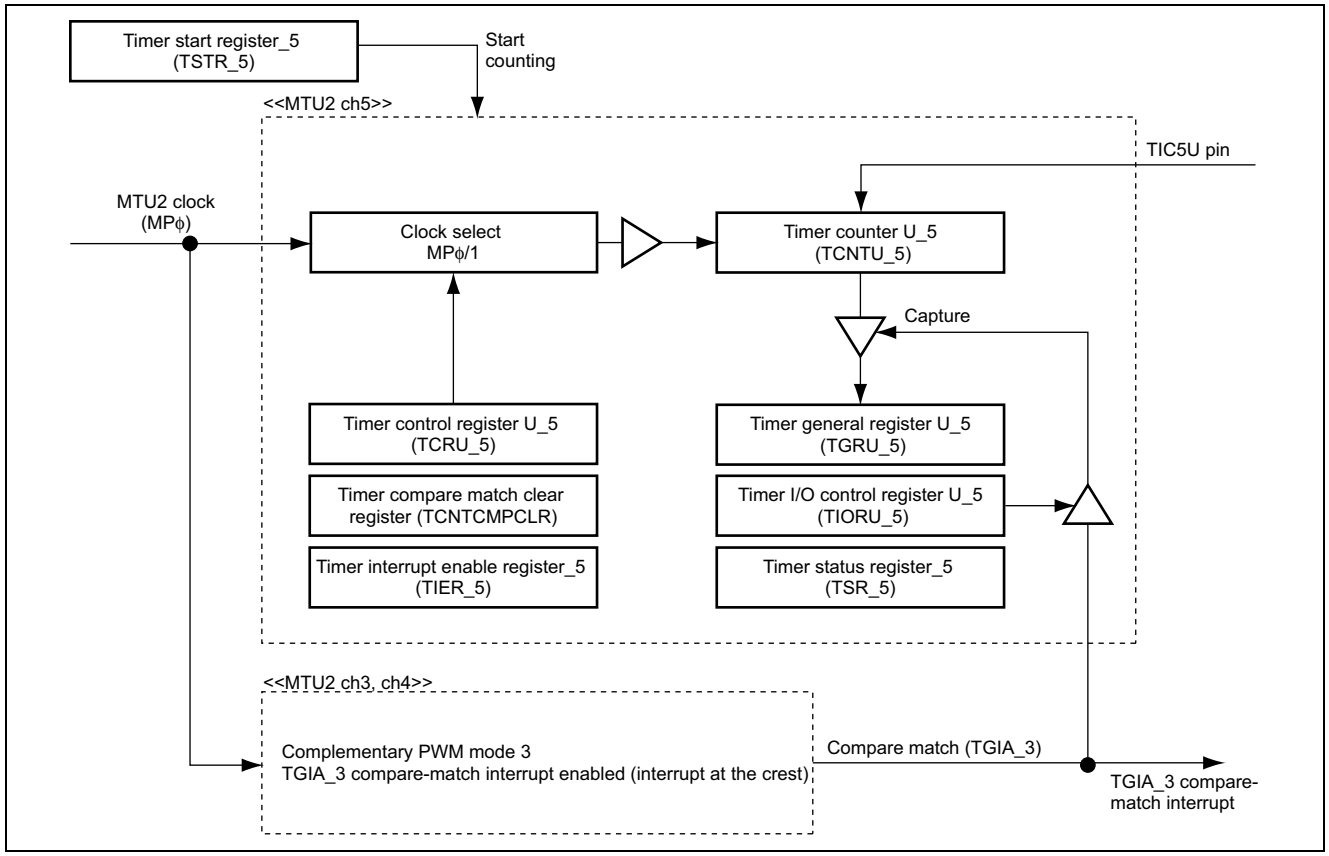
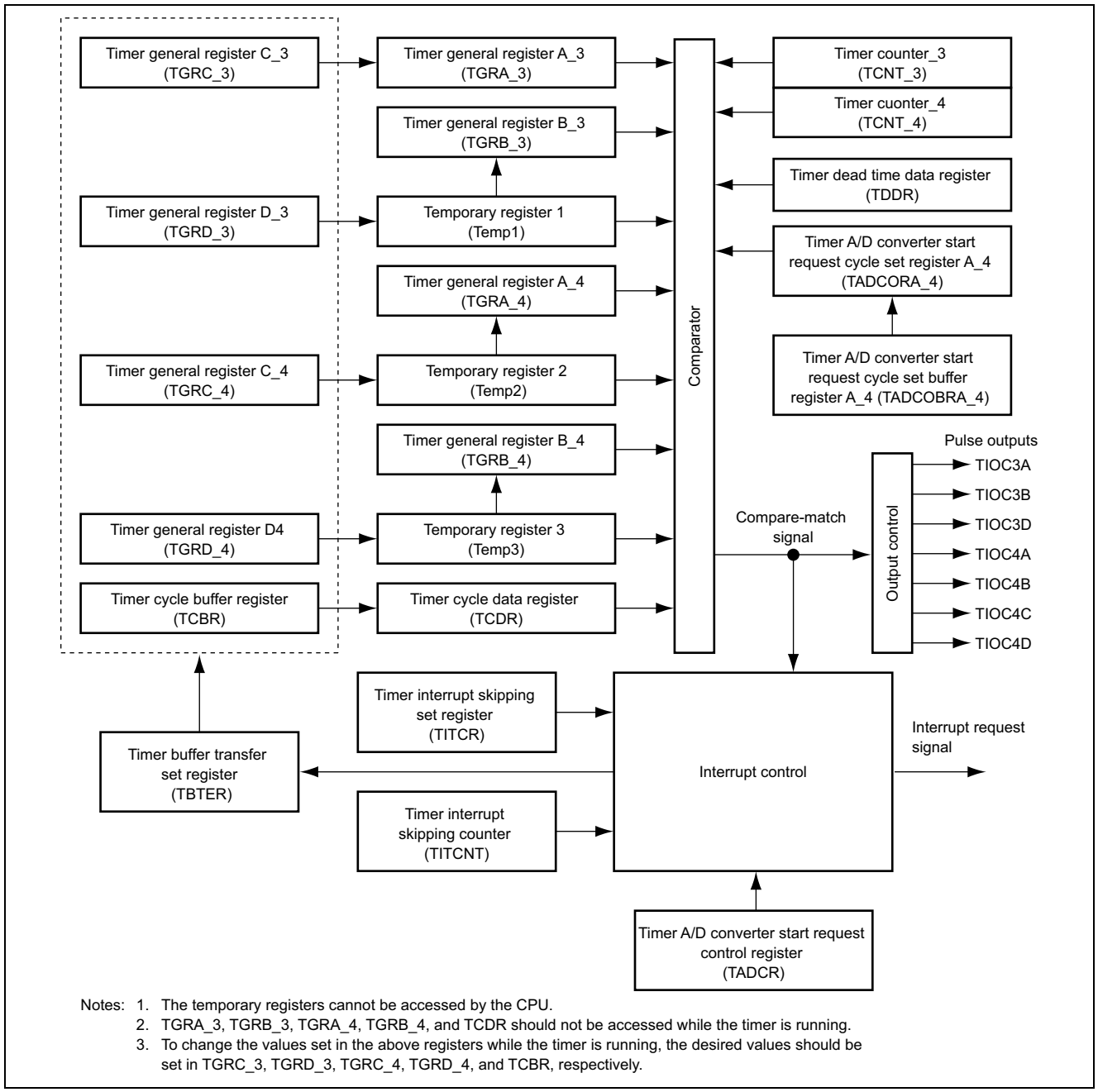


Figure 2 Block Diagram of Channel 5 of MTU2

- Timer counter U_5 (TCNTU_5) is a 16-bit readable/writable counter. TCNTU_5 counts pulses of the MTU2 clock (MPϕ).
- Timer control register U_5 (TCRU_5) is a 16-bit readable/writable register. TCRU_5 selects the clock for TCNTU_5.
- Timer general register U_5 (TGRU_5) is a 16-bit readable/writable register. TGRU_5 can be used in external pulse width measurement. The count value of the pulse duration is stored in TGRU_5.
- Timer I/O control register U_5 (TIORU_5) is an 8-bit readable/writable register. TIORU_5 specifies the functions of TGRU_5 and the TIC5U pin.
- Timer interrupt enable register_5 (TIER_5) is an 8-bit readable/writable register. TIER_5 enables/disables interrupt requests from timer channel 5.
- Timer start register_5 (TSTR_5) is an 8-bit readable/writable register. TSTR_5 starts/stops the timer counter of channel 5.
- Timer compare match clear register (TCNTCMPCLR) is an 8-bit readable/writable register. TCNTCMPCLR enables/disables requests to clear timer counter TCNTU_5.
- Timer status register_5 (TSR_5) is an 8-bit readable/writable register. TSR_5 indicates the status of channel 5.

3.2 Channels 3 and 4 of Multi-Function Timer Pulse Unit 2 (MTU2)

Figure 3 shows a block diagram of channels 3 and 4 of the MTU2 when the external pulse width measurement feature of channel 5 is used.



Notes: 1. The temporary registers cannot be accessed by the CPU.
2. TGRA_3, TGRB_3, TGRA_4, TGRB_4, and TCDR should not be accessed while the timer is running.
3. To change the values set in the above registers while the timer is running, the desired values should be set in TGRC_3, TGRD_3, TGRC_4, TGRD_4, and TCBR, respectively.

Figure 3 Block Diagram of Channels 3 and 4 of MTU2 when External Pulse Width Measurement Feature of Channel 5 is Used

- Timer general register A_3 (TGRA_3) operates as a compare register. Half of the PWM period is set in TGRA_3. To change the set value while the timer is running, the desired value is set in timer general register C_3 (TGRC_3).
- Timer general register B_3 (TGRB_3) operates as a compare register. The duty cycle of the PWM waveform output from the TIOC3B and TIOC3D pins is set in TGRB_3. To change the set value while the timer is running, the desired value should be set in timer general register D_3 (TGRD_3).
- Timer general register C_3 (TGRC_3) operates as a buffer register for TGRA_3. When the timer is running, TGRA_3 reflects the value set in TGRC_3.
- Timer general register D_3 (TGRD_3) operates as a buffer register for TGRB_3. When the value set in TGRD_3 is changed while the timer is running, the new value is transferred to a temporary register (Templ) and reflected in TGRB_3.
- Timer general register A_4 (TGRA_4) operates as a compare register. The duty cycle for the PWM waveforms output from the TIOC4A and TIOC4C pins is set in TGRA_4. To change the set value while the timer is running, the desired value should be set in timer general register C_4 (TGRC_4).
- Timer general register B_4 (TGRB_4) operates as a compare register. The duty cycle for the PWM waveforms output from the TIOC4B and TIOC4D pins is set in TGRB_4. To change the set value while the timer is running, the desired value should be set in timer general register D_4 (TGRD_4).
- Timer general register C_4 (TGRC_4) operates as a buffer register for TGRA_4. When the timer is running, TGRA_4 reflects the value set in TGRC_4.
- Timer general register D_4 (TGRD_4) operates as a buffer register for TGRB_4. When the timer is running, TGRB_4 reflects the value set in TGRD_4.
- Temporary registers 1, 2, and 3 (Temp1, Temp2, and Temp3) are situated between the buffer registers and the compare registers. The data written to the buffer registers are first transferred to the corresponding temporary registers and then to the compare register. The temporary registers cannot be accessed by the CPU.
- Timer counter_3 (TCNT_3) is a 16-bit readable/writable counter. TCNT_3 starts counting down on compare match with TGRA_3, and starts counting up on compare match with the timer dead time data register (TDDR).
- Timer counter_4 (TCNT_4) is a 16-bit readable/writable counter. TCNT_4 starts counting down on compare match with the timer cycle data register (TCDR) value, and starts counting up when it reaches H'0000.
- The timer dead time register (TDDR) is a 16-bit readable/writable register. The dead time for PWM waveform is set in TDDR.
- The timer cycle data register (TCDR) is a 16-bit readable/writable register. Half of the PWM carrier cycle is set in TCDR.
- The timer cycle buffer register (TCBR) operates as a buffer register for TCDR. When the timer is running, TCDR reflects the value set in TCBR.
- The timer interrupt skipping set register (TITCR) enables/disables interrupt skipping and also specifies the skipping count. Skipping is possible for the TCNT_3 compare-match interrupt (TGIA_3) and TCNT_4 underflow interrupt (TCIV_4) in complementary PWM mode. A skipping count of up to seven can be specified.
- The timer interrupt skipping counter (TITCNT) counts the generated interrupts to be skipped. The TITCNT count value is cleared on matching the skipping count specified by TITCR.
- The timer buffer transfer set register (TBTER) enables/disables the transfer from the buffer registers to the temporary registers. When the transfer is enabled, TBTER specifies whether to link the transfer with interrupt skipping operation.

- The timer A/D converter start request control register (TADCR) is a 16-bit readable/writable register. TADCR enables/disables A/D converter start requests and specifies whether to link A/D converter start requests with interrupt skipping operation.
- Timer A/D converter start request cycle set register A_4 (TADCORA_4) is a 16-bit readable/writable register. When the set value matches the TCNT_4 value, the corresponding A/D converter start request is generated.
- Timer A/D converter start request cycle set buffer register A_4 (TADCOBRA_4) operates as buffer register for TADCORA_4. When the timer is running, TADCORA_4 reflects the value set in TADCOBRA_4.

4. Operation

Figure 4 shows the operation of the sample application, and table 1 describes software and hardware processing.

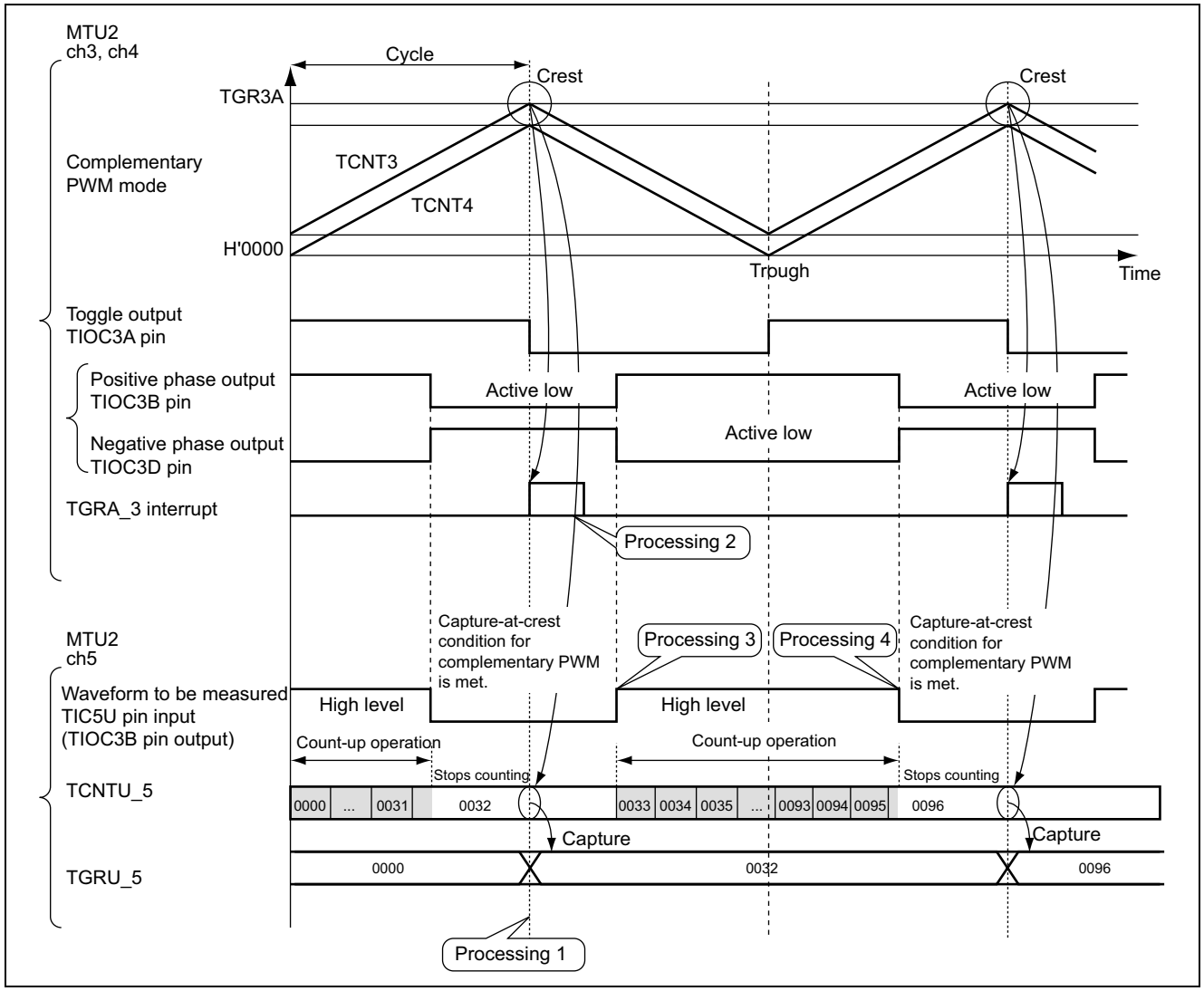


Figure 4 Operation

Table 1 Software and Hardware Processing

	Software Processing	Hardware Processing
Processing 1	—	• Compare match with TGRA_3 (crest) occurs. • Captures the counter value to TGRU_5
Processing 2	• Clears the interrupt flag to 0. • Stores the captured value of the channel 5 counter to a variable.	Generates a TGRA_3 compare-match interrupt (crest)
Processing 3	—	Starts the TCNTU_5 counter (counting operation continues while the TIC5U pin input signal is high).
Processing 4	—	Stops the TCNTU_5 counter (counter operation is suspended while the TIC5U pin input signal is low).

5. Description of Software

5.1 Modules

Table 2 describes the modules used in the sample task.

Table 2 Description of Modules

Module Name	Label Name	Functions
Main routine	main()	Configures channels 3 and 4 of the MTU2 for complementary PWM mode, and makes initial settings of channel 5. Starts the MTU2 timers (channels 3, 4, and 5).
TGRA_3 compare-match interrupt routine	mtu2_tgra3()	Performs processing for the compare-match interrupt on channel 3 of the MTU2. Stores the measured pulse width value to the variable.

5.2 Variable

Table 3 shows the variable used in the sample task.

Table 3 Description of Variable

Label Name of Variable	Function	Used in
High_count	Stores the counter value for high pulse duration, which is the captured value of the timer counter of channel 5.	TGRA_3 input capture interrupt routine

5.3 Register Settings

The register settings used in the sample application are described below. Note that the setting values are used specifically in the sample task and that they are different from the initial values.

5.3.1 Settings for the Clock Pulse Generator (CPG)

- Frequency Control Register (FRQCR)
  - Setting value: H'0241
  - Function: Specifies the frequency division ratios.

Bit	Bit Name	Value	Description
15	—	0	Reserved
14 to 12	IFC[2] to IFC[0]	000	Frequency division ratio for internal clock (Iϕ) 000: ×1 (80 MHz when the input clock frequency is 10 MHz)
11 to 9	BFC[2] to BFC[0]	001	Frequency division ratio for bus clock (Bϕ) 001: ×1/2 (40 MHz when the input clock frequency is 10 MHz)
8 to 6	PFC[2] to PFC[0]	001	Frequency division ratio for peripheral clock (Pϕ) 001: ×1/2 (40 MHz when the input clock frequency is 10 MHz)
5 to 3	MIFC[2] to MIFC[0]	000	Frequency division ratio for MTU2S clock (MIϕ) 000: ×1 (80 MHz when the input clock frequency is 10 MHz)
2 to 0	MPFC[2] to MPFC[0]	001	Frequency division ratio for MTU2 clock (MPϕ) 001: ×1/2 (40 MHz when the input clock frequency is 10 MHz)

5.3.2 Settings for Power-Down Modes

- Standby Control Register 4 (STBCR4)
  - Setting value: H'bf
  - Function: Controls the operation of the modules in power-down modes.

Bit	Bit Name	Value	Description
7	MSTP23	1	1: Stops supply of the clock signal to the MTU2S.
6	MSTP22	0	0: The MTU2 runs.
5	MSTP21	1	1: Stops supply of the clock signal to the CMT.
4, 3	—	11	Reserved
2	MSTP18	1	1: Stops supply of the clock signal to the A/D_2.
1	MSTP17	1	1: Stops supply of the clock signal to the A/D_1.
0	MSTP16	1	1: Stops supply of the clock signal to the A/D_0.

5.3.3 Settings for Channels 3 and 4 of the Multi-Function Timer Pulse Unit 2 (MTU2)

- Timer Control Register_3 (TCR_3)
  - Setting value: H'00
  - Function: Controls TCNT of channel 3.

Bit	Bit Name	Value	Description
7 to 5	CCLR[2] to CCLR[0]	000	These bits select the TCNT clearing source. 000: Clearing of TCNT is disabled.
4, 3	CKEG[1] and CKEG[0]	00	00: TCNT counts rising edges of the clock.
2 to 0	TPSC[2] to TPSC[0]	000	000: TCNT counts edges of internal clock MPϕ/1.

- Timer Control Register_4 (TCR_4)
  - Setting value: H'00
  - Function: Controls TCNT of channel 4.

Bit	Bit Name	Value	Description
7 to 5	CCLR[2] to CCLR[0]	000	These bits select the TCNT clearing source. 000: Clearing of TCNT is disabled.
4, 3	CKEG[1] and CKEG[0]	00	00: TCNT is incremented on the rising edge of the clock.
2 to 0	TPSC[2] to TPSC[0]	000	000: Counting is driven by internal clock MPϕ/1.

- Timer Counter_3 (TCNT_3)
  - Setting value: (DEAD_TIME)
  - Function: A 16-bit counter to which the dead time value is loaded in complementary PWM mode.
- Timer Counter_4 (TCNT_4)
  - Setting value: H'0000
  - Function: A 16-bit counter to which H'0000 is loaded as the initial value in complementary PWM mode.
- Timer General Register B_3 (TGRB_3)
  - Setting value: (DUTY_OFFSET)
  - Function: The PWM duty cycle for the TIOC3B (positive phase)/TIOC3D (negative phase) outputs is set.
- Timer General Register D_3 (TGRD_3)
  - Setting value: (DUTY_OFFSET)
  - Function: A buffer register for TGRB_3 in which the same value as TGRB_3 is set.
- Timer General Register A_4 (TGRA_4)
  - Setting value: (DUTY_OFFSET)
  - Function: The PWM duty cycle for the TIOC4A (positive phase)/TIOC4C (negative phase) outputs is set.
- Timer General Register C_4 (TGRC_4)
  - Setting value: (DUTY_OFFSET)
  - Function: A buffer register for TGRA_4 in which the same value as TGRA_4 is set.

- Timer General Register B_3 (TGRB_3)
  — Setting value: (DUTY_OFFSET)
  — Function: The PWM duty cycle for the TIOC4B (positive phase)/TIOC4D (negative phase) outputs is set.
- Timer General Register D_4 (TGRD_4)
  — Setting value: (DUTY_OFFSET)
  — Function: A buffer register for TGRB_4 in which the same value as TGRB_4 is set.
- Timer Dead Time Data Register (TDDR)
  — Setting value: (DEAD_TIME)
  — Function: Specifies the dead time in complementary PWM mode.
- Timer Cycle Data Register (TCDR)
  — Setting value: (HALF_CARRER)
  — Function: Specifies half of the carrier cycle in complementary PWM mode.
- Timer Cycle Buffer Register (TCBR)
  — Setting value: (HALF_CARRER)
  — Function: A buffer register for the timer cycle data register.
- Timer General Register A_3 (TGRA_3)
  — Setting value: (HALF_CARRER+DEAD_TIME)
  — Function: The upper limit of TCNT_3 (1/2 carrier cycle + dead time) is set.
- Timer General Register C_3 (TGRC_3)
  — Setting value: (HALF_CARRER+DEAD_TIME)
  — Function: A buffer register for TGRA_3 in which the same value as TGRA_3 is set.
- Timer Output Control Register 1 (TOCR1)
  — Setting value: H'40
  — Function: Controls the toggle output and PWM output level in complementary PWM mode.

Bit	Bit Name	Value	Description
7	—	0	Reserved
6	PSYE	1	1: Enables toggle output (TIOC3A pin).
5, 4	—	00	Reserved
3	TOCL	0	0: Enables writing to the TOCS, OLSN, and OLSP bits.
2	TOCS	0	Selects either the TOCR1 or TOCR2 setting to be used as the output level in complementary PWM mode and reset-synchronized PWM mode. 0: Selects the TOCR1 setting.
1	OLSN	0	0: Selects the high level as the initial output level and the low level as the active level for the negative phase output.
0	OLSP	0	0: Selects the high level as the initial output level and the low level as the active level for the positive phase output.

- Timer Mode Register_3 (TMDR_3)
  - Setting value: H'3f
  - Function: Specifies the channel 3 operating mode.

Bit	Bit Name	Value	Description
7	—	0	Reserved
6	—	0	Reserved in channels 1 to 4.
5	BFB	1	1: TGRB and TGRD used together for buffer operation.
4	BFA	1	1: TGRA and TGRC used together for buffer operation.
3 to 0	MD[3] to MD[0]	1111	1111: Complementary PWM mode 3 (transfer at crests and troughs)

- Timer Output Enable Register (TOER)
  - Setting value: H'ff
  - Function: Enables/disables outputs on the PWM output pins.

Bit	Bit Name	Value	Description
7, 6	—	11	Reserved
5	OE4D	1	1: Enables MTU output from the TIOC4D pin.
4	OE4C	1	1: Enables MTU output from the TIOC4C pin.
3	OE3D	1	1: Enables MTU output from the TIOC3D pin.
2	OE4B	1	1: Enables MTU output from the TIOC4B pin.
1	OE4A	1	1: Enables MTU output from the TIOC4A pin.
0	OE3B	1	1: Enables MTU output from the TIOC3B pin.

- Timer Interrupt Enable Register_3 (TIER_3)
  - Setting value: H'01
  - Function: Enables/disables interrupt requests of channel 3.

Bit	Bit Name	Value	Description
7	TTGE	0	0: Disables generation of A/D converter start requests.
6	—	0	Reserved
5	—	0	Reserved
4	TCIEV	0	0: Disables interrupt requests (TCIV) by the TCFV flag.
3	TGIED	0	0: Disables interrupt requests (TGID) by the TGFD flag.
2	TGIEC	0	0: Disables interrupt requests (TGIC) by the TGFC flag.
1	TGIEB	0	0: Disables interrupt requests (TGIB) by the TGFB flag.
0	TGIEA	1	1: Enables interrupt requests (TGIA) by the TGFA flag.

- Timer Start Register (TSTR)
  - Setting value: H'C0
  - Function: Starts/stops the TCNT counters of channels 0 to 4.

Bit	Bit Name	Value	Description
7	CTS4	1	1: Starts counting by TCNT_4.
6	CTS3	1	1: Starts counting by TCNT_3.
5 to 3	—	000	Reserved
2	CTS2	0	0: Stops counting by TCNT_2.
1	CTS1	0	0: Stops counting by TCNT_1.
0	CTS0	0	0: Stops counting by TCNT_0.

5.3.4 Settings for Channel 5 of the Multi-Function Timer Pulse Unit 2 (MTU2)

- Timer Control Register U_5 (TCRU_5)
  - Setting value: H'00
  - Function: Controls TCNTU_5 of channel 5.

Bit	Bit Name	Value	Description
7 to 2	—	000000	Reserved
1, 0	TPSC[1] and TPSC[0]	00	00: TCNTU_5 counts edges of internal clock MPϕ/1.

- Timer Control Register V_5 (TCRV_5)
  - Setting value: H'00
  - Function: Controls TCNTV_5 of channel 5.

Bit	Bit Name	Value	Description
7 to 2	—	000000	Reserved
1, 0	TPSC[1] and TPSC[0]	00	00: TCNTV_5 counts edges of internal clock MPϕ/1.

- Timer Control Register W_5 (TCRW_5)
  - Setting value: H'00
  - Function: Controls TCNTW_5 of channel 5.

Bit	Bit Name	Value	Description
7 to 2	—	000000	Reserved
1, 0	TPSC[1] and TPSC[0]	00	00: TCNTW_5 counts edges of internal clock MPϕ/1.

- Timer Counter U_5 (TCNTU_5)
  - Setting value: H'0000
  - Function: A 16-bit counter.
- Timer Counter V_5 (TCNTV_5)
  - Setting value: H'0000
  - Function: A 16-bit counter.
- Timer Counter W_5 (TCNTW_5)
  - Setting value: H'0000
  - Function: A 16-bit counter.
- Timer General Register U_5 (TGRU_5)
  - Setting value: —
  - Function: A register for shared use in compare match, input capture, and external pulse width measurement operations.
- Timer General Register V_5 (TGRV_5)
  - Setting value: —
  - Function: A register for shared use in compare match, input capture, and external pulse width measurement operations.
- Timer General Register W_5 (TGRW_5)
  - Setting value: —
  - Function: A register for shared use in compare match, input capture, and external pulse width measurement operations.
- Timer I/O Control Register U_5 (TIORU_5)
  - Setting value: H'1e
  - Function: Controls TGRU_5.

Bit	Bit Name	Value	Description
7 to 5	—	000	Reserved
4 to 0	IOC[4] to IOC[0]	11110	11110: TGRU_5 functions as an input capture register. The TIC5U pin is used for measuring the high pulse width of the external input signal. Capture at crests.

- Timer I/O Control Register V_5 (TIORV_5)
  - Setting value: H'00
  - Function: Controls TGRV_5.

Bit	Bit Name	Value	Description
7 to 5	—	000	Reserved
4 to 0	IOC[4] to IOC[0]	00000	00000: TGRV_5 functions as a compare match register. The TIC5V pin is used for compare match operation.

- Timer I/O Control Register W_5 (TIORW_5)
  - Setting value: H'00
  - Function: Controls TGRW_5.

Bit	Bit Name	Value	Description
7 to 5	—	000	Reserved
4 to 0	IOC[4] to IOC[0]	00000	00000: TGRW_5 functions as a compare match register. The TIC5W pin is used for compare match operation.

- Timer Interrupt Enable Register_5 (TIER_5)
  - Setting value: H'00
  - Function: Enables/disables interrupt requests from channel 5.

Bit	Bit Name	Value	Description
7 to 3	—	00000	Reserved
2	TGIE5U	0	0: Disables the TGI5U interrupt requests.
1	TGIE5V	0	0: Disables the TGI5V interrupt requests.
0	TGIE5W	0	0: Disables the TGI5W interrupt requests.

- Timer Compare Clear Register (TCNTCMPCLR)
  - Setting value: H'00
  - Function: Enables/disables requests to clear TCNTU_5, TCNTV_5, and TCNTW_5.

Bit	Bit Name	Value	Description
7 to 3	—	00000	Reserved
2	CMPCLR5U	0	0: Disables clearing of TCNTU_5 to H'0000 on TCNTU_5 and TGRU_5 compare match/input capture.
1	CMPCLR5V	0	0: Disables clearing of TCNTV_5 to H'0000 on TCNTV_5 and TGRV_5 compare match/input capture.
0	CMPCLR5W	0	0: Disables clearing of TCNTW_5 to H'0000 on TCNTW_5 and TGRW_5 compare match/input capture.

- Timer Start Register_5 (TSTR_5)
  - Setting value: H'04
  - Function: Starts/stops TCNT of channel 5.

Bit	Bit Name	Value	Description
7 to 3	—	00000	Reserved
2	CSTU5	1	1: Starts counting by TCNTU_5.
1	CSTV5	0	0: Stops counting by TCNTV_5.
0	CSTW5	0	0: Stops counting by TCNTW_5.

5.3.5 Settings for the Pin Function Controller (PFC) (SH7085)

- Port A Control Register H3 (PACRH3)
  - Setting value: H'0000
  - Function: Selects functions of the multiplexed pins of port A (PA25 and PA24).

Bit	Bit Name	Value	Description
15 to 6	—	All 0	Reserved
5, 4	PA25MD[1] and PA25MD[0]	00	PA25 mode 00: PA25 I/O (port)
3, 2	—	00	Reserved
1, 0	PA24MD[1] and PA24MD[0]	00	PA24 mode 00: PA24 I/O (port)

- Port A Control Register H2 (PACRH2)
  - Setting value: H'0030
  - Function: Selects functions of the multiplexed pins of port A (PA23 to PA20).

Bit	Bit Name	Value	Description
15, 14	—	00	Reserved
13, 12	PA23MD[1] and PA23MD[0]	00	PA23 mode 00: PA23 I/O (port)
11, 10	—	00	Reserved
9, 8	PA22MD[1] and PA22MD[0]	00	PA22 mode 00: PA22 I/O (port)
7, 6	—	00	Reserved
5, 4	PA21MD[1] and PA21MD[0]	11	PA21 mode 11: TIC5U input (MTU2)
3, 2	—	00	Reserved
1, 0	PA20MD[1] and PA20MD[0]	00	PA20 mode 00: PA20 I/O (port)

- Port A Control Register L1 (PACRL1)
  - Setting value: H'0000
  - Function: Selects functions of the multiplexed pins of port A (PA19 to PA16).

Bit	Bit Name	Value	Description
15, 14	—	00	Reserved
13, 12	PA19MD[1] and PA19MD[0]	00	PA19 mode 00: PA19 I/O (port)
11, 10	—	00	Reserved
9, 8	PA18MD[1] and PA18MD[0]	00	PA18 mode 00: PA18 I/O (port)
7, 6	—	00	Reserved
5, 4	PA17MD[1] and PA17MD[0]	00	PA17 mode 00: PA17 I/O (port)
3	—	0	Reserved
2 to 0	PA16MD[2] to PA16MD[0]	000	PA16 mode 000: PA16 I/O (port)

- Port A I/O Register H (PAIORH)
  - Setting value: H'0000
  - Function: Selects the signal directions on the port A pins (PA25 to PA16). 1: output, 0: input

Bit	Bit Name	Value	Description
15, 14	—	00	Reserved
13 to 10	—	0000	Invalid for SH7085
9	PA25IOR	0	PA25 pin is set as input.
8	PA24IOR	0	PA24 pin is set as input.
7	PA23IOR	0	PA23 pin is set as input.
6	PA22IOR	0	PA22 pin is set as input.
5	PA21IOR	0	PA21 pin is set as input.
4	PA20IOR	0	PA20 pin is set as input.
3	PA19IOR	0	PA19 pin is set as input.
2	PA18IOR	0	PA18 pin is set as input.
1	PA17IOR	0	PA17 pin is set as input.
0	PA16IOR	0	PA16 pin is set as input.

- Port E Control Register L4 (PECRL4)
  - Setting value: H'1111
  - Function: Selects functions of the multiplexed pins of port E (PE15 to PE12).

Bit	Bit Name	Value	Description
15	—	0	Reserved
14 to 12	PE15MD[2] to PE15MD[0]	001	PE15 mode 001: TIOC4D input/output (MTU2)
11	—	0	Reserved
10 to 8	PE14MD[2] to PE14MD[0]	001	PE14 mode 001: TIOC4C input/output (MTU2)
7, 6	—	00	Reserved
5, 4	PE13MD[1] and PE13MD[0]	01	PE13 mode 01: TIOC4B input/output (MTU2)
3	—	0	Reserved
2 to 0	PE12MD[2] to PE12MD[0]	001	PE12 mode 001: TIOC4A input/output (MTU2)

- Port E Control Register L3 (PECRL3)
  - Setting value: H'1011
  - Function: Selects functions of the multiplexed pins of port E (PE11 to PE8).

Bit	Bit Name	Value	Description
15	—	0	Reserved
14 to 12	PE11MD[2] to PE11MD[0]	001	PE11 mode 001: TIOC3D input/output (MTU2)
11	—	0	Reserved
10 to 8	PE10MD[2] to PE10MD[0]	000	PE10 mode 000: PE10 I/O (port)
7	—	0	Reserved
6 to 4	PE9MD[2] to PE9MD[0]	001	PE9 mode 001: TIOC3B input/output (MTU2)
3	—	0	Reserved
2 to 0	PE8MD[2] to PE8MD[0]	001	PE8 mode 001: TIOC3A input/output (MTU2)

- Port E Control Register L2 (PECRL2)
  - Setting value: H'0000
  - Function: Selects functions of the multiplexed pins of port E (PE7 to PE4).

Bit	Bit Name	Value	Description
15	—	0	Reserved
14 to 12	PE7MD[2] to PE7MD[0]	000	PE7 mode 000: PE7 I/O (port)
11	—	0	Reserved
10 to 8	PE6MD[2] to PE6MD[0]	000	PE6 mode 000: PE6 I/O (port)
7	—	0	Reserved
6 to 4	PE5MD[2] to PE5MD[0]	000	PE5 mode 000: PE5 I/O (port)
3	—	0	Reserved
2 to 0	PE4MD[2] to PE4MD[0]	000	PE4 mode 000: PE4 I/O (port)

- Port E Control Register L1 (PECRL1)
  - Setting value: H'0000
  - Function: Selects functions of the multiplexed pins of port E (PE3 to PE0).

Bit	Bit Name	Value	Description
15	—	0	Reserved
14 to 12	PE3MD[2] to PE3MD[0]	000	PE3 mode 000: PE3 I/O (port)
11	—	0	Reserved
10 to 8	PE2MD[2] to PE2MD[0]	000	PE2 mode 000: PE2 I/O (port)
7	—	0	Reserved
6 to 4	PE1MD[2] to PE1MD[0]	000	PE1 mode 000: PE1 I/O (port)
3, 2	—	00	Reserved
1, 0	PE0MD[1] and PE1MD[0]	00	PE0 mode 00: PE0 I/O (port)

- Port E I/O Register L (PEIOL)
  - Setting value: H'fb00
  - Function: Selects the signal directions on the port E pins (PE15 to PE0). 1: output, 0: input

Bit	Bit Name	Value	Description
15	PE15IOR	1	PE15/TIOC4D pin is set as output.
14	PE14IOR	1	PE14/TIOC4C pin is set as output.
13	PE13IOR	1	PE13/TIOC4B pin is set as output.
12	PE12IOR	1	PE12/TIOC4A pin is set as output.
11	PE11IOR	1	PE11/TIOC3D pin is set as output.
10	PE10IOR	0	PE10 pin is set as input.
9	PE9IOR	1	PE9/TIOC3B pin is set as output.
8	PE8IOR	1	PE8/TIOC3A pin is set as output.
7	PE7IOR	0	PE7 pin is set as input.
6	PE6IOR	0	PE6 pin is set as input.
5	PE5IOR	0	PE5 pin is set as input.
4	PE4IOR	0	PE4 pin is set as input.
3	PE3IOR	0	PE3 pin is set as input.
2	PE2IOR	0	PE2 pin is set as input.
1	PE1IOR	0	PE1 pin is set as input.
0	PE0IOR	0	PE0 pin is set as input.

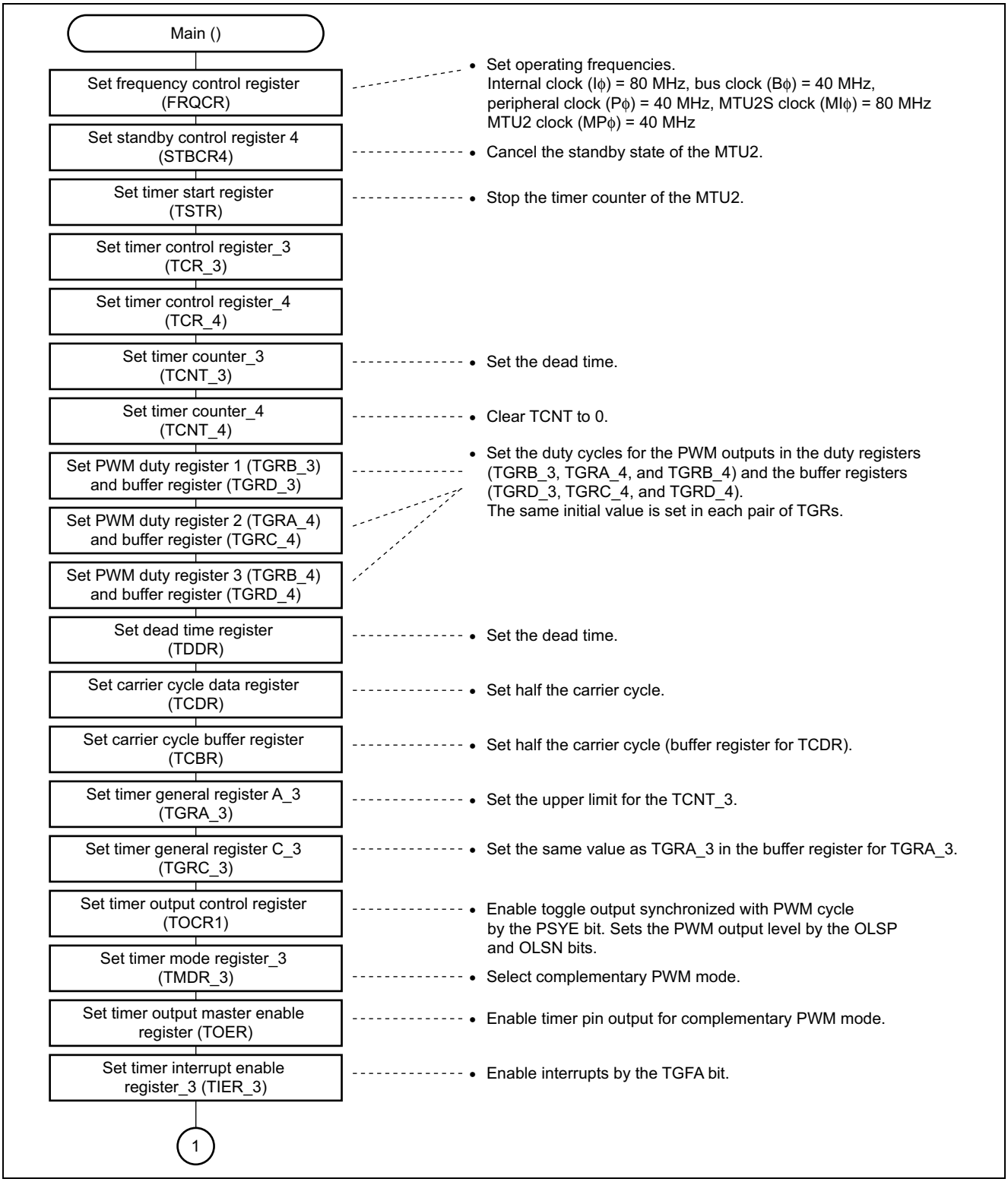
5.3.6 Settings for the Interrupt Controller (INTC)

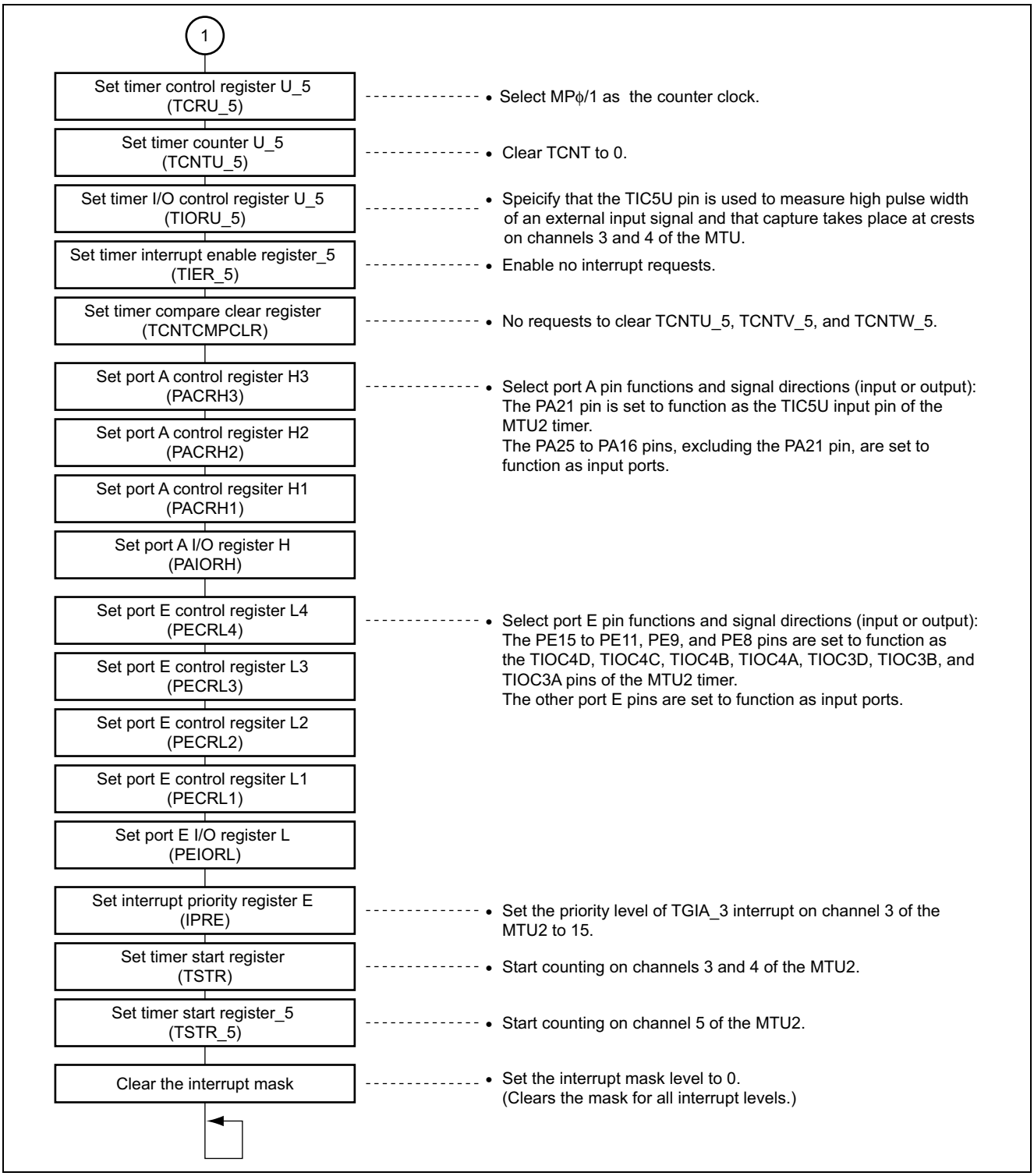
- Interrupt Priority Register E (IPRE)
  - Setting value: H'00f0
  - Function: Sets priority levels of the corresponding interrupt requests.

Bit	Bit Name	Value	Description
15 to 12	IPR[15] to IPR[12]	0000	Priority level 0 is set for the corresponding interrupts.
11 to 8	IPR[11] to IPR[8]	0000	Priority level 0 is set for the corresponding interrupts.
7 to 4	IPR[7] to IPR[4]	1111	Priority level 15 is set for the TGIA_3 (TGIB_3) interrupt on channel 3 of the MTU2.
3 to 0	IPR[3] to IPR[0]	0000	Set priority level 0 is set for the corresponding interrupts.

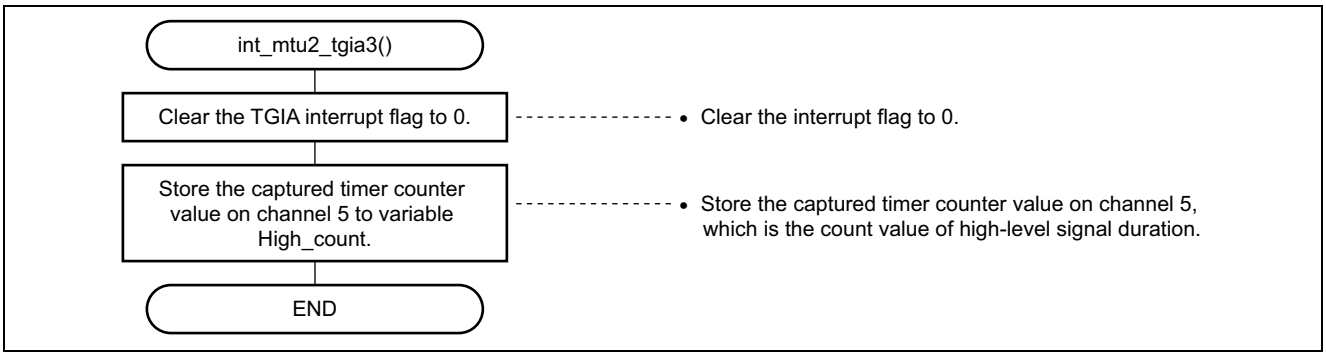
6. Flowcharts

6.1 Main Routine




1
Set timer control register U_5 (TCRU_5)
• Select MPϕ/1 as the counter clock.
Set timer counter U_5 (TCNTU_5)
• Clear TCNT to 0.
Set timer I/O control register U_5 (TIORU_5)
• Speicify that the TIC5U pin is used to measure high pulse width of an external input signal and that capture takes place at crests on channels 3 and 4 of the MTU.
Set timer interrupt enable register_5 (TIER_5)
• Enable no interrupt requests.
Set timer compare clear register (TCNTCMPCLR)
• No requests to clear TCNTU_5, TCNTV_5, and TCNTW_5.
Set port A control register H3 (PACRH3)
Set port A control register H2 (PACRH2)
Set port A control regsiter H1 (PACRH1)
Set port A I/O register H (PAIORH)
• Select port A pin functions and signal directions (input or output): The PA21 pin is set to function as the TIC5U input pin of the MTU2 timer. The PA25 to PA16 pins, excluding the PA21 pin, are set to function as input ports.
Set port E control register L4 (PECRL4)
Set port E control register L3 (PECRL3)
Set port E control regsiter L2 (PECRL2)
Set port E control regsiter L1 (PECRL1)
Set port E I/O register L (PEIORL)
• Select port E pin functions and signal directions (input or output): The PE15 to PE11, PE9, and PE8 pins are set to function as the TIOC4D, TIOC4C, TIOC4B, TIOC4A, TIOC3D, TIOC3B, and TIOC3A pins of the MTU2 timer. The other port E pins are set to function as input ports.
Set interrupt priority register E (IPRE)
• Set the priority level of TGIA_3 interrupt on channel 3 of the MTU2 to 15.
Set timer start register (TSTR)
• Start counting on channels 3 and 4 of the MTU2.
Set timer start register_5 (TSTR_5)
• Start counting on channel 5 of the MTU2.
Clear the interrupt mask
• Set the interrupt mask level to 0. (Clears the mask for all interrupt levels.)

6.2 TGRA_3 Compare-Match Interrupt Routine



Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Sep.05.05	—	First edition issued

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