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SH7730 Group

Example of BSC Interface Connection to NOR-Type Flash Memory

Introduction

This application note describes the normal space interface functionality of the bus state controller (BSC) and provides a practical example of connection with NOR-type flash memory.

Target Device

SH7730

Contents

1. Preface

1.1 Specifications

32-Mbit NOR-type flash memory (2 M × 16 bits) from Spansion™ is connected to the SH7730 with a 16-bit data-bus width.

The bus state controller (BSC) of the SH7730 is used to set up conditions for the execution of read and write operations for an external NOR-type flash memory.

1.2 Module Used

- Bus state controller (BSC)

1.3 Applicable Conditions

Evaluation board	The AP-SH4A-1A board incorporates the SH7730 with SH-4A CPU core and is available from AlphaProject Co., Ltd. External memory (area 0): 4-MB NOR-type flash memory: S29AL032D70TF104 from Spansion (area 3): 32-MB SDR-SDRAM (16 MB × 2): K4S281632F-UC75 from Samsung
• MCU	SH7730 (R8A77301)
• Operating frequency	Internal clock: 266.66 MHz SuperHyway bus clock: 133.33 MHz Bus clock: 66.66 MHz Peripheral clock: 33.33 MHz
• Bus width for area 0	16-bit fixed (with the MD3 pin at the low level)
• Clock operating mode	Mode 2 (with the MD0 pin at the low level, and MD1 pin at the high level)
• Endian	Big endian (with the MD5 pin at the low level)
• Toolchain	SuperH RISC engine Standard Toolchain Ver.9.1.1.0 from Renesas Technology
• Compiler options	Default settings of High-performance Embedded Workshop (-cpu=sh4a -debug -optimize=0 –noinline -gbr=auto -macsave=0 -save_cont_reg=0 -chgincpath –errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 -nologo)

1.4 Related Application Note

The operation of the reference program for this document was confirmed with the setting conditions described in the SH7730 Group Application Note: *Example of Initialization (REJ06B0848)*. Please refer to that document in combination with this one.

2. Description of Sample Application

2.1 Operational Overview of Module Used

The bus state controller (BSC) of the SH7730 is used to control externally connected NOR-type flash memory. Table 1 gives specifications of the S29AL032D70TFI04 NOR-type flash memory chip (hereinafter referred to as simply “flash memory”) used in this application note.

Table 1 Specifications of NOR-type Flash Memory for the SH7730

Item	Description
Type number	S29AL032D70TFI04 from Spansion
Capacity (configuration)	32 Mbits (2 M × 16 bits)
Number of units used	1
Access time	In random access: 70 ns (max.), when not in page mode
Boot block	Bottom-boot devices

Figure 1 shows a memory map.

Memory type and the data-bus width for connection are specifiable per CS space. In this application note, flash memory is connected in the CS0 space. The CS0 space is at the top of the physical address space and can be used for up to 64 MB of memory.

In the sample application, flash memory is at the locations from H'0000 0000 to H'003F FFFF in the physical address space.

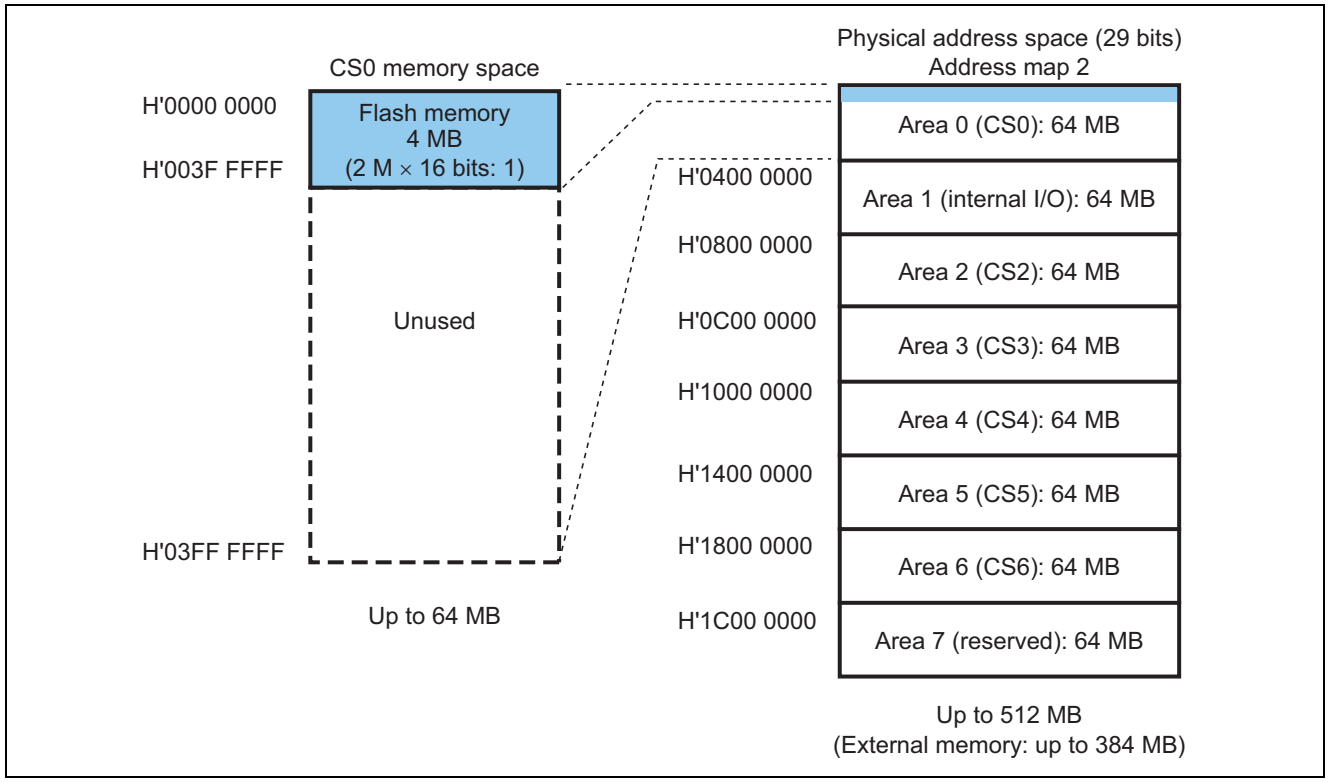

Figure 1 Memory Map

From the software point of view, the physical address space is further mapped onto the virtual address space. Address conversion from the virtual address space to the physical address space differs according to whether the memory management unit (MMU) is or is not in use.

For details, please refer to the section on the bus state controller (BSC) and the memory management unit (MMU) in the *SH7730 Group Hardware Manual* (REJ09B0359).

Figure 2 shows an example of circuitry for flash memory connection.

SH7730 is connected to flash memory with a 16-bit data bus width. To set up flash memory with a data-bus width of 16 bits, the $\overline{\text{BYTE}}$ pin is fixed to the high level. To set up space CS0 of the SH7730 for 16-bit bus width, the MD3 pin is fixed to the low level.

In order to prevent erroneous access to flash memory during the period over which the pin states of the SH7730 are undefined after power is supplied, use an external reset IC etc. and input reset signals on both the $\overline{\text{RESETP}}$ pin of the SH7730 and the $\overline{\text{RESET}}$ pin of the flash memory chip.

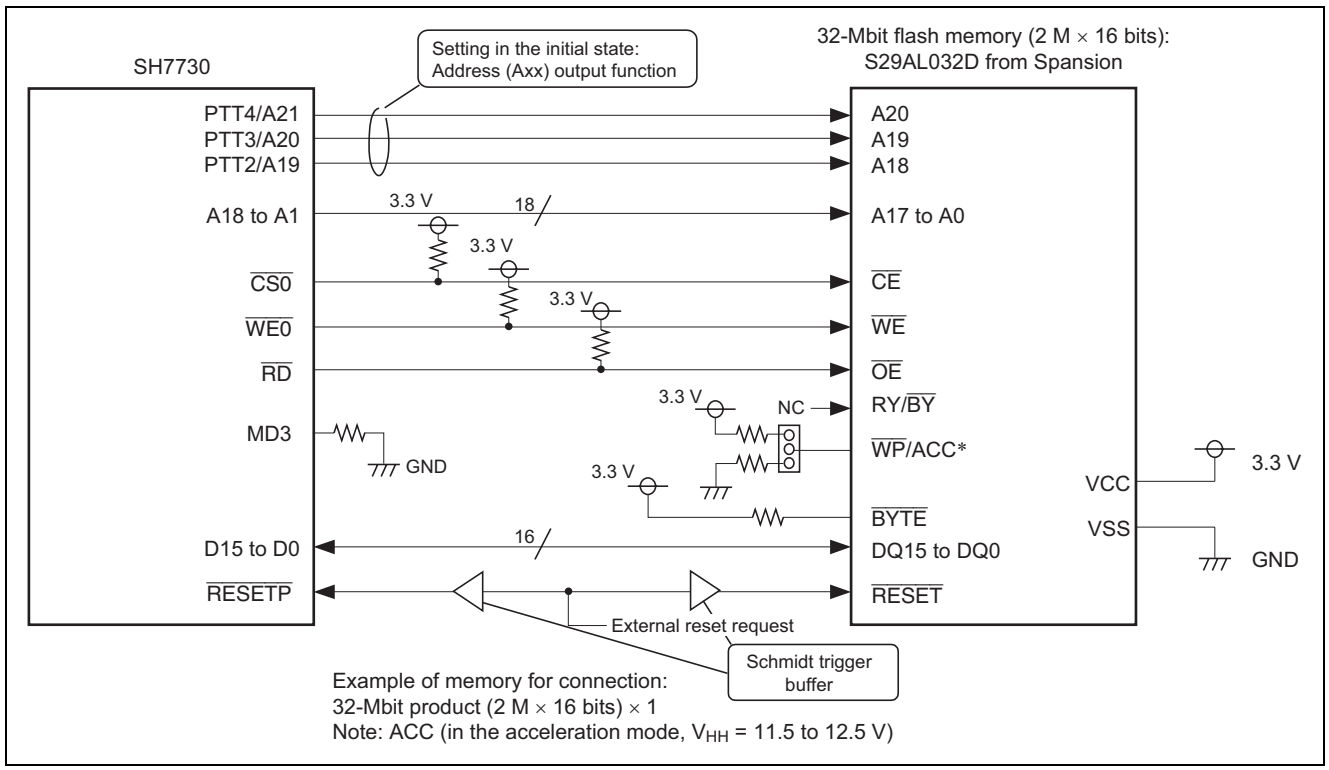

Figure 2 Circuit Example for Flash Memory Connection (4 MB, 16-Bit Bus)

Table 2 gives a list of pin functions of the SH7730. Since the address function is the default for pins PTT2/A19 to PTT4/A21, setting of the pin-function controller (PFC) to switch the pin functions is not required.

Table 2 List of Pin Functions for the SH7730

SH7730 Pin	I/O	Initial Pin Function	Function
PTT4/A21	Output	A21	Address bus
PTT3/A20	Output	A20	Address bus
PTT2/A19	Output	A19	Address bus
A18 to A1	Output	A18 to A1	Address bus
D15 to D0	Input/output	D15 to D0	Data bus
$\overline{RD}$	Output	$\overline{RD}$	Read enable
$\overline{WE0}$	Output	$\overline{WE0}$	Write enable
$\overline{CS0}$	Output	$\overline{CS0}$	Chip selection
MD3	Input	MD3	Selects values for the CS0 space data-bus width. Low level: 16-bit width (setting made in this application note) High level: 32-bit width The CS0 space data-bus width cannot be changed after a power-on reset.

2.2 Procedure for Setting Module Used

Table 3 gives a list of examples for setting the bus state controller. For details on the individual registers, see the section on the bus state controller in the *SH7730 Group Hardware Manual* (REJ09B0359).

Figure 3 shows an example of the procedure for setting the bus state controller.

Table 3 Example of Bus State Controller Settings

Name of Register	Address	Setting	Function
CS0 space bus control register (CS0BCR)	H'FEC1 0004	H'1048 0400	• Specifies the number of idle cycles between write-read cycles and write-write cycles. IWW[2:0] = B'001: 1 cycle The setting must suit the specifications of tWPH, tOEH, and tSR/W for flash memory. • Specifies the number of idle cycles between read-write cycles in different spaces. IWRWD[2:0] = B'001: 1 cycle • Specifies the number of idle cycles between read-write cycles in the same space. IWRWS[2:0] = B'001: 1 cycle In general, settings of the IWRWD and IWRWS bits must suit the specification for tDF. Note: Writing to the BSZ[1:0] bits (to specify the data bus width) is ignored. Use the MD3 pin function to specify the data bus width for the CS0 space.
CS0 space wait control register (CS0WCR)	H'FEC1 0024	H'0000 0A41	• Number of delay cycles from address/$\overline{CS0}$ assertion to $\overline{RD}$/$\overline{WE}$ assertion. SW[1:0] = B'01: 1.5 cycles • Number of access wait cycles. WR[3:0] = B'0100: 4 cycles • External wait mask specification WM = B'1 External wait input is ignored. • Number of delay cycles from $\overline{RD}$/$\overline{WE}$ negation to address/$\overline{CS0}$ negation HW[1:0] = B'01: 1.5 cycles

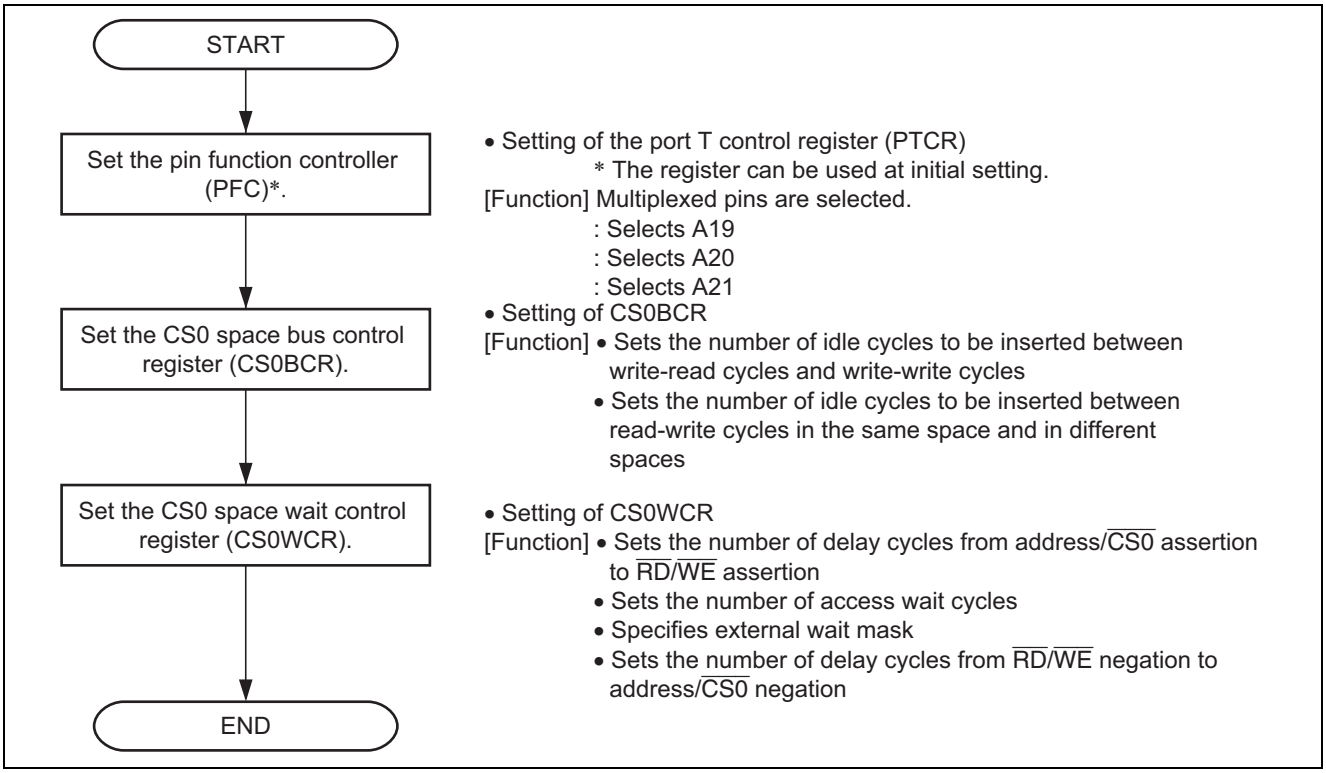

Figure 3 Example of Procedure for Setting Bus State Controller (CS0 Space)

2.3 Settings of Flash Memory Timing in the Application Note

In this application note, the setting for the number of cycles of waiting corresponds to the access speed of the connected memory (S29AL032D70TFI04).

The bus clock for the SH7730 is set to 66.66 MHz (tcyc = 15 ns).

For AC characteristics of the SH7730 and the memory (S29AL032D70TFI04), refer to the datasheets for the individual devices.

Supplementary Delay cycles (determining Th and Tf)

The delay cycles are set in the CS0 space wait control register (CS0WCR).

- SW[1:0]: Cycles of delay from address and $\overline{CS0}$ assertion to $\overline{RD}$ and $\overline{WE}$ assertion (Th)
- HW[1:0]: Cycles of delay from $\overline{RD}$ and $\overline{WE}$ negation to address and $\overline{CS0}$ negation (Tf)

Each of the delay cycles can be set to 0.5, 1.5, 2.5, or 3.5 clock cycles. The AC characteristics of the SH7730 stipulate that the overall delay time for each of the signals starts on a rising edge of CKO.

Figure 4 shows the relations between Th and the delay time and Tf and the delay time. Timing is designed as follows: the number of cycles is obtained by subtracting 0.5 from the number of cycles specified by the SW or HW bits. Then, the delay for respective signals is added to the number of cycles.

In this application note, formulae used to calculate the timing of delay cycles Th and Tf are specified in the following form:

(Setting of the SW or HW bits – 0.5) number of cycles

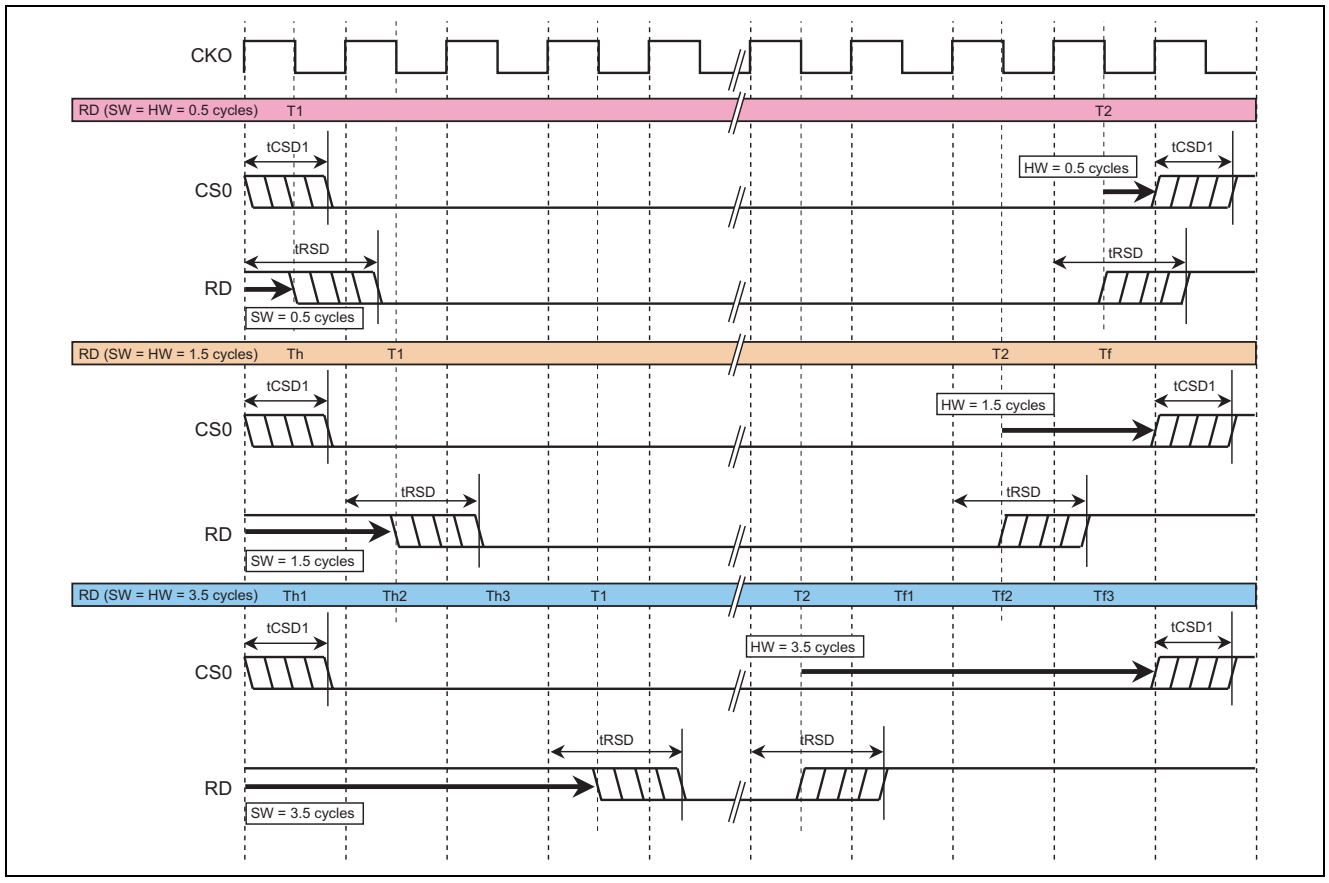

Figure 4 Relations between Delay Cycles and Delay Time

2.3.1 Timing Settings in the Application Note

This section describes settings for the write timing of $\overline{WE}$ ($\overline{WE}$ controlled writing).

1. Cycles of waiting for access
   Cycles of waiting (Tw) are set between the T1 cycle and T2 cycle.
   The formulae below are used to confirm that the relevant settings satisfy conditions for bus timing of the SH7730 and flash memory (in this application note, the setting for cycles of waiting is 4 (Tw = 4)).
   Figure 5 shows the timing chart when tRSD elapses within the T1 cycle, and figure 6 shows the timing chart in cases where tRSD extends beyond the T1 cycle.

   A. Read cycle timing
   - tRC of flash memory (for read cycles)
     $tRC(min) \leq (Th + T1 + Tw + T2 + Tf) \times tcyc - tAD1(max)*^1 + tAD1(min)*^2$ ····· (figure 5) (figure 6)
   - tACC of flash memory (for address access)
     $tACC(max) \leq (Th + T1 + Tw + T2) \times tcyc - tAD1(max) - tRDS1(min)$ ····· (figure 5) (figure 6)
   - tCE of flash memory (for CE#access)
     $tCE(max) \leq (Th + T1 + Tw + T2) \times tcyc - tCSD1(max) - tRDS1(min)$ ····· (figure 5) (figure 6)
   - tOE of flash memory (for OE#access)
     $tOE(max) \leq (T1 + Tw + T2) \times tcyc - tRSD(max) - tRDS1(min)$ ····· (figure 5) (figure 6)
   - tOH of flash memory (for retaining the data output from the previous cycle)
     $tOH(min) \leq tRDH1(min)$ ····· (figure 5) (figure 6)

   B. Write cycle timing
   - tWC of flash memory (for write cycles)
     $tWC(min) \leq (Th + T1 + Tw + T2 + Tf) \times tcyc - tAD1(max)*^1 + tAD1(min)*^2$ ····· (figure 7)
   - tAH of flash memory (for holding the address)
     $tAH(min) \leq (T1 + Tw + T2 + Tf) \times tcyc - tWED1(max) + tAD1(min)$ ····· (figure 7)
   - tWP of flash memory (for write-pulse width)
     $tWP(min) \leq (T1 + Tw) \times tcyc - tWED1(max) + tWED1(min)$ ····· (figure 7)
   - tDS of flash memory (for setting up data)
     $tDS(min) \leq (Th + T1 + Tw) \times tcyc - tWDD1(max) + tWED1(min)$ ····· (figure 7)
   - tDH of flash memory (for holding the data)
     $tDH(min) \leq tWDH4(min)$ ····· (figure 7)

2. Extending the period of CSn assertion

   A. Delay cycles from address/ $\overline{CS0}$ assertion to $\overline{RD}$ / $\overline{WE}$ assertion (Th)

   The formulae below are used to confirm that the relevant settings satisfy conditions for tCS (chip enable setup time) and tAS (address setup time) of the flash memory. In this application note, Th is set to 1.0.

   $tCS(min) \leq Th \times tcyc - tCSD1(max) + tWED1(min)$ ····· (figure 7)

   $tAS(min) \leq Th \times tcyc - tAD1(max) + tWED1(min)$ ····· (figure 7)

   B. Delay cycles from $\overline{RD}$/$\overline{WE}$ negation to address/$\overline{CS0}$ negation (Tf)

   The formula below is used to confirm that the relevant settings satisfy conditions for tCH (chip enable hold time) of the flash memory. In this application note, Tf is set to 1.0.

   $tCH(min) \leq (T2 + Tf) \times tcyc - tWED1(max) + tCSD1(min)$ ····· (figure 7)

3. Wait between access cycles

   Insertion of wait cycles between access cycles for continuous accesses is set.

   The formulae below are used to confirm that the relevant settings satisfy conditions for tWPH ("H" write pulse width), tOEH (output enable hold time), tSR/W (latency between writing and reading operations), and tDF (from output enable[*3] to High-Z output).

   In this application note, a single cycle of waiting is set up between write-read cycles and write-write cycles, read-write cycles in the same space, and read-write cycles in different spaces (Taw = 1).

   - tWPH of flash memory ("H" write pulse width)

     $tWPH(min) \leq (T2 + Tf + Taw + Th) \times tcyc - tWED1(max) + tWED1(min)$ ····· (figure 8)

   - tOEH of flash memory (output enable hold time)

     $tOEH(min) \leq (T2 + Tf + Taw + Th) \times tcyc - tWED1(max) + tRSD(min)$ ····· (figure 9)

   - tSR/W of flash memory (latency between write-read operations)

     $tSR/W(min) \leq (T2 + Tf + Taw) \times tcyc - tWED1(max) + tAD1(min)$ ····· (figure 9)

   - tDF of flash memory (from output enable[*3] to High-Z output)

     $tDF(max) \leq (T2 + Tf + Taw) \times tcyc - tRSD(max) + tWDD1(min)$*[4] ····· (figure 10)

Notes: 1. The longer of tAD1 (max) and tCSD1 (max) applies.
2. The shorter of tAD1 (min) and tCSD1 (min) applies.
3. Whichever of chip enable or output enable has the earlier rising edge applies.
   In the SH7730, since the rising edge of the output enable signal is earlier, the output enable is used in comparison.
4. Pins D0 to D15 must be in the High-Z state by data access of the next cycle.
   The conditions for setting up data in write cycles are more demanding than the conditions for the timing of access in read cycles, we consider operation in write cycles.
   For the time to set up data in successive write cycles, time tWDD1 (min.) must also be added to the value obtained from (T2 + Tf + Taw) × tcyc – tRSD (max.). The total is acceptable if it is tDF (max.) or greater.

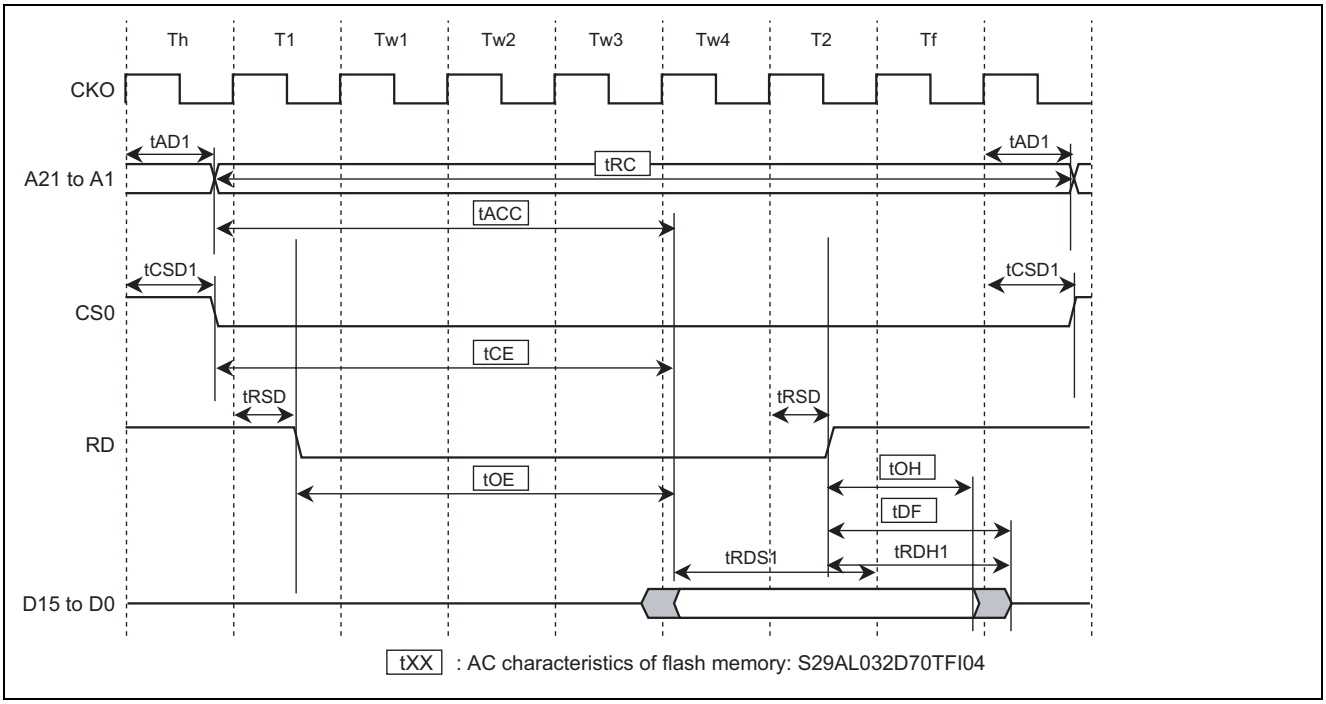

Figure 5 Read Timing for Flash Memory (tRSD = Min.)

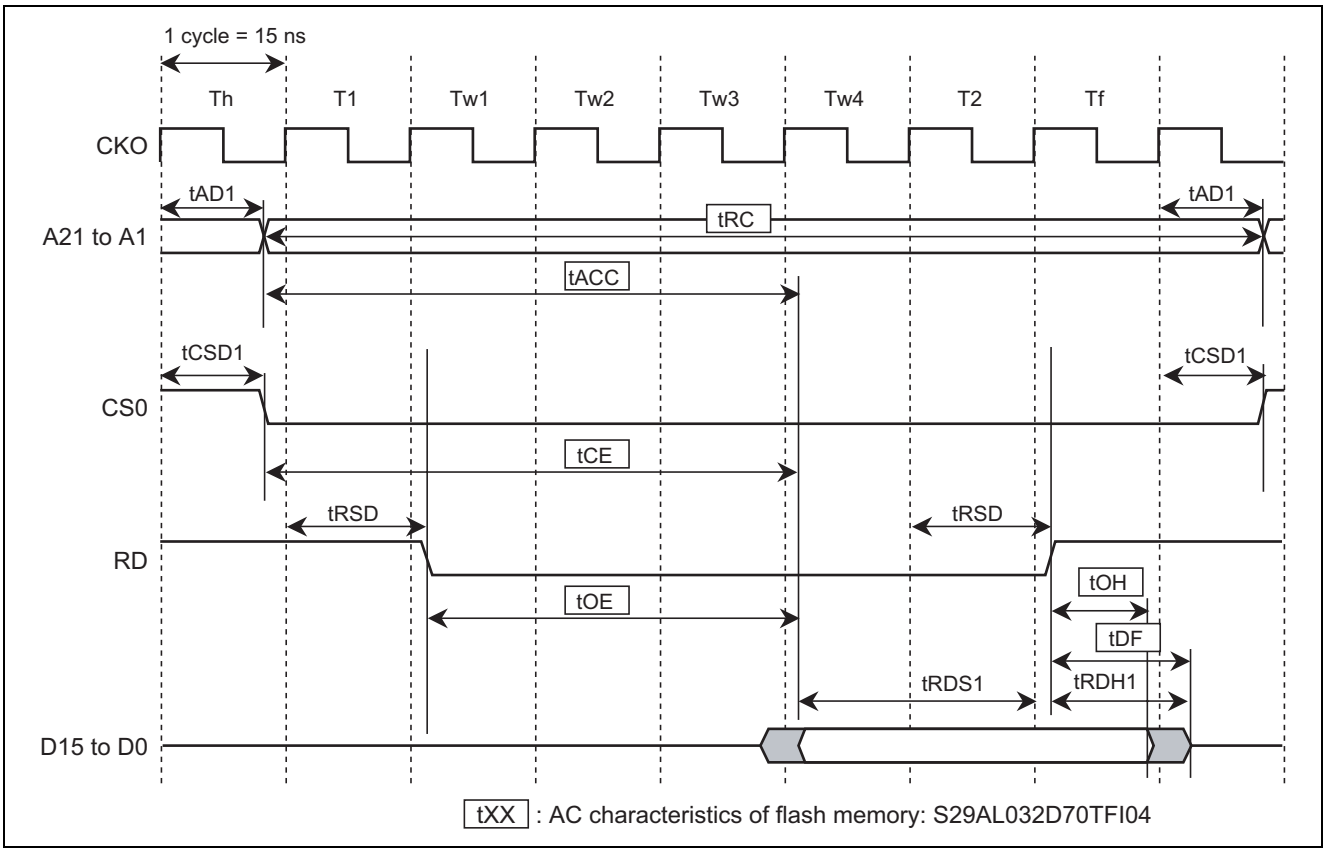

Figure 6 Read Timing for Flash Memory (tRSD = Max.)

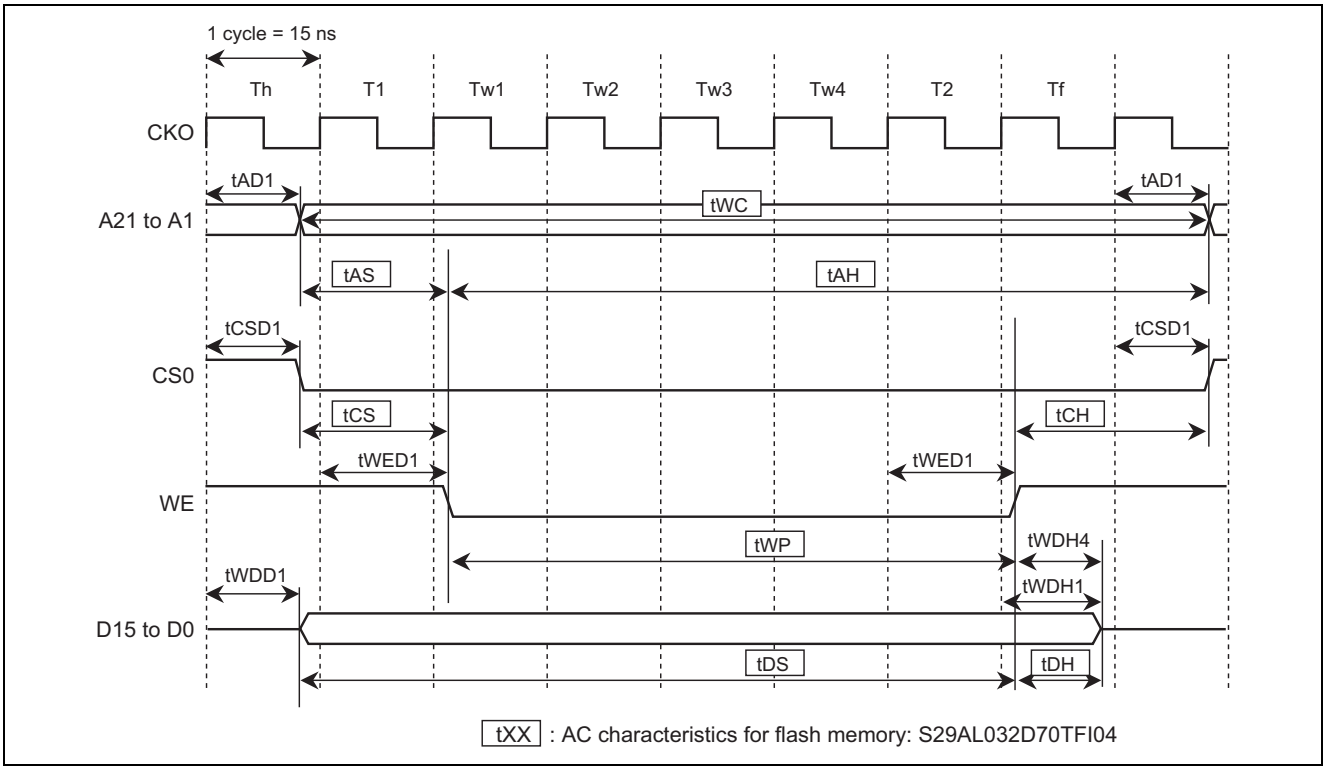

Figure 7 Write Timing for Flash Memory

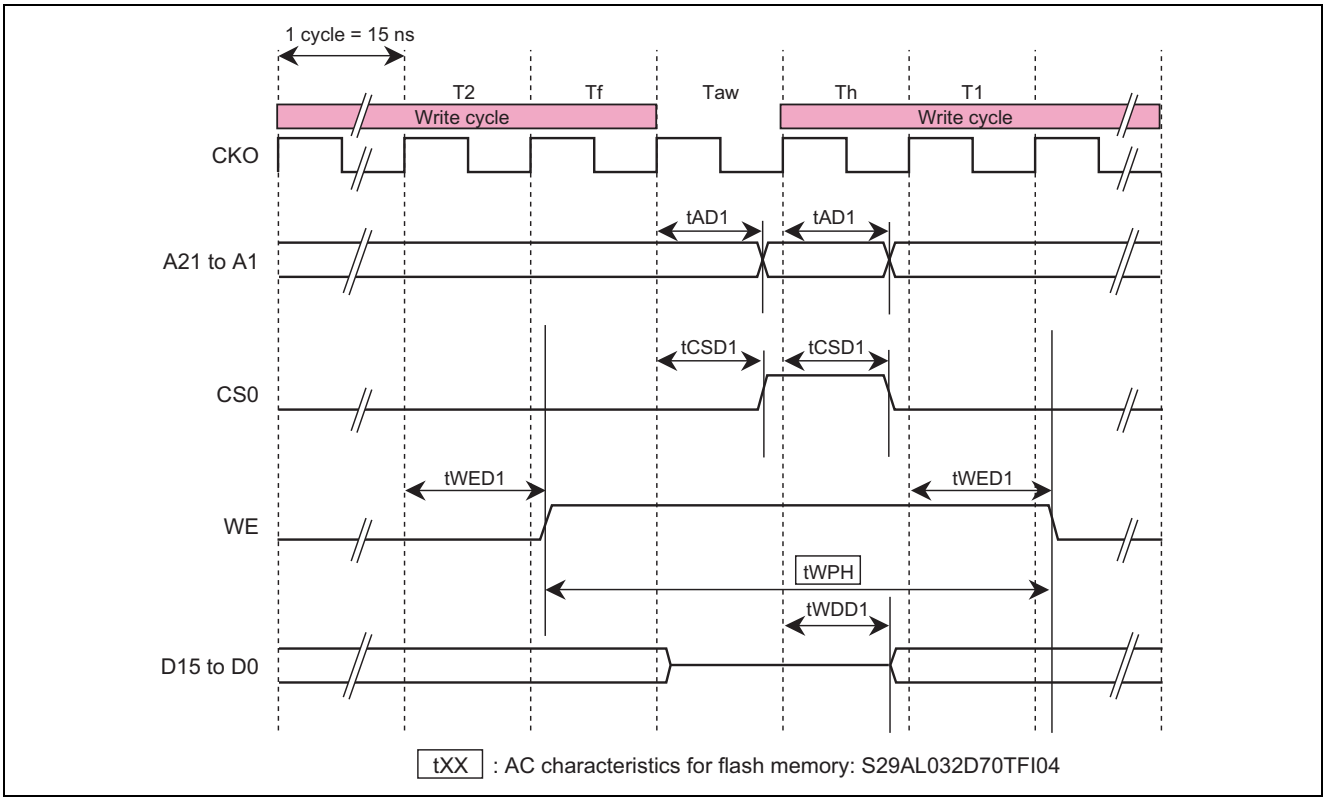

Figure 8 Timing between Write and Write Cycles for Flash Memory

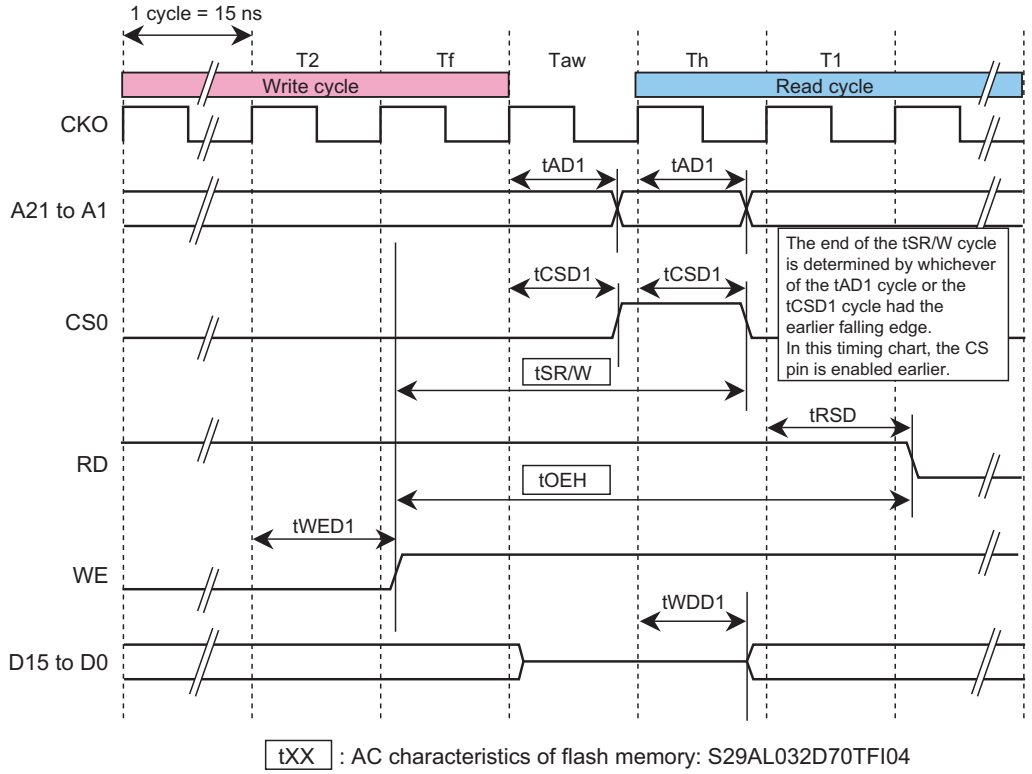

Figure 9 Timing between Write and Read Cycles for Flash Memory

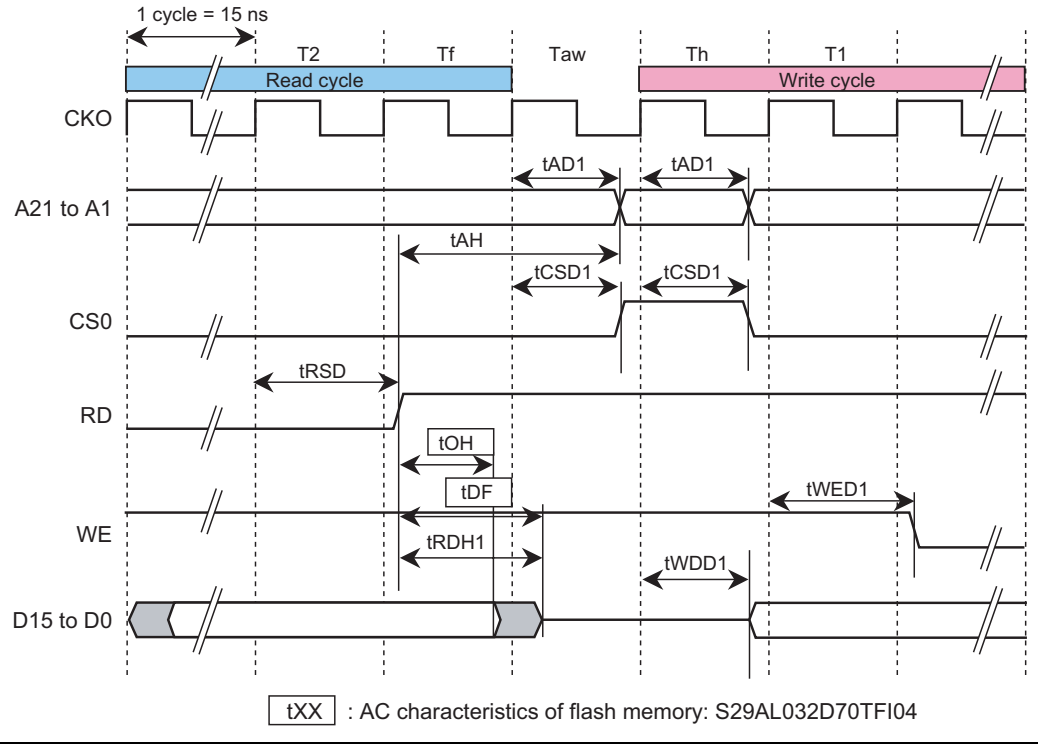

Figure 10 Timing between Read and Write Cycles for Flash Memory

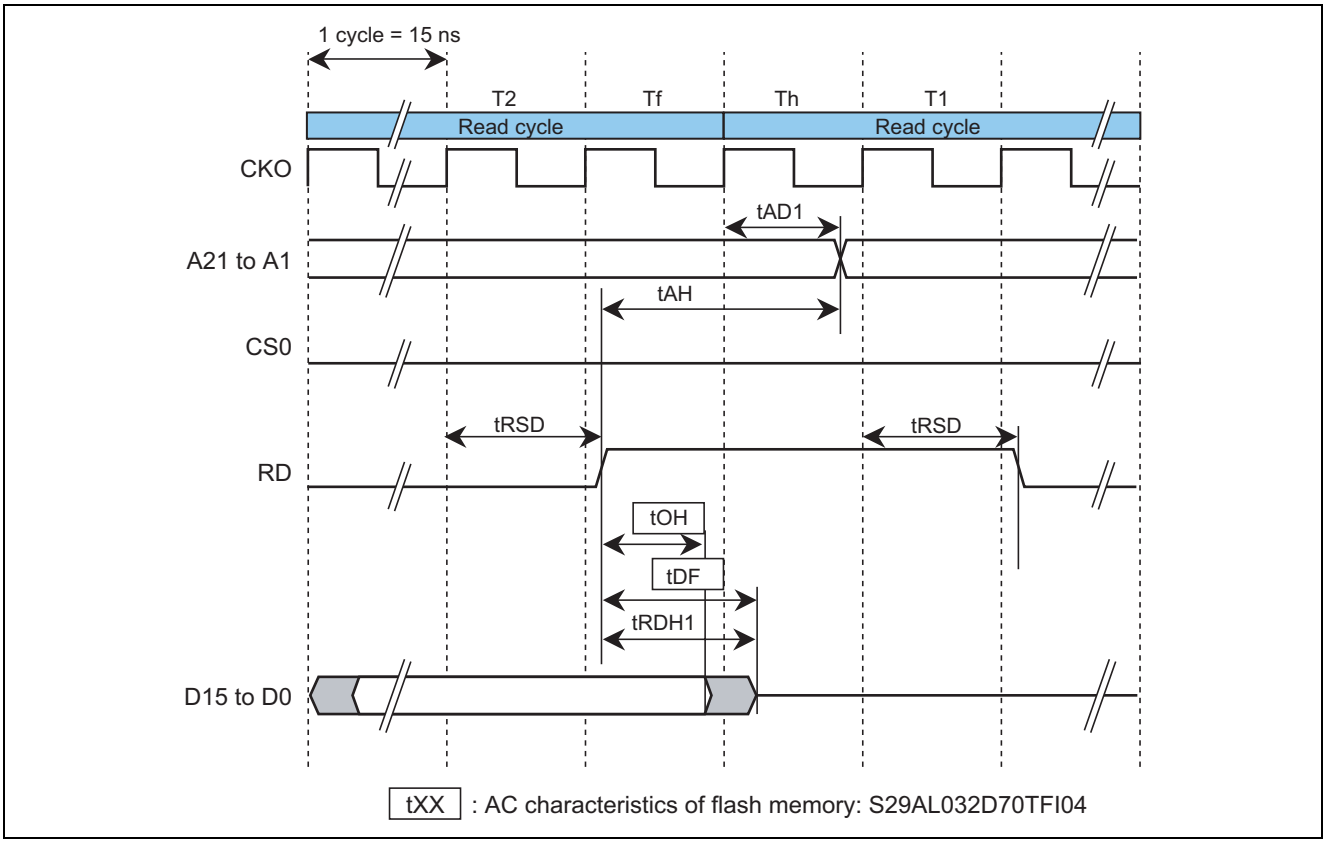

Figure 11 Timing between Read and Read Cycles for Flash Memory

3. Documents for Reference

- Software Manual
  SH-4A Software Manual (REJ09B0003)
  The most up-to-date versions of the documents are available on the Renesas Technology Website.
- Hardware Manual
  SH7730 Group Hardware Manual (REJ09B0359)
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