Application Note

DA9063 Unused Pin Configuration

AN-PM-070

Abstract

This application note describes the recommended configuration for unused pins in an application using the DA9063 power management IC

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1 Introduction

The DA9063 is a highly integrated Power Management IC (PMIC) that includes multiple Buck converters, low dropout linear regulators, GPIOs and ADC channels. In addition, it allows options for controlling the start-up and shutdown sequences, configurable feedback paths, remote sensing and such like.

In the application, some of these functions may not be required and – to minimise any potential issues with these unused functions – the pins related to them need to be correctly configured.

This document provides guidance on how to configure unused connections on the DA9063.

2 Functional Blocks

The following tables describe the recommended configurations in the 'If unused' column. The designation 'Mandatory' means that the pin is used in all applications.

2.1 Power Manager

Table 1: Power Manager Connections

Pin Number	Signal Name	Alternate Function	Type	Description	If Unused
E9	GPIO11		DIO	GPIO11 with high power output and blinking feature	If GPI, tie to non-active state. If GPO, leave floating.
B6	CHG_WAKE		DI/PS	Wake-up signal from companion charger to trigger a start-up and temporary supply voltage for PMIC (VBUS_PROT in case of an inserted supply until charger Buck provides power to VSYS)	Connect to GND
D3	GPIO7		DIO	Sequencer-controlled GPO	If GPI, tie to non-active state. If GPO, leave floating.
J7	nONKEY		DI	On/Off key with optional long press shutdown	Pull-up to VSYS
B9	SYS_EN	GPIO8	DI/DIO	Hardware enable of power domain SYSTEM/GPIO8	If GPI, tie to non-active state. If GPO, leave floating.
C9	PWR_EN	GPIO9	DI/DIO	Hardware enable of power domain POWER / Sequencer controlled GPO	If GPI, tie to non-active state. If GPO, leave floating.
B10	PWR1_EN	GPIO10	DI/DIO	Hardware enable of power domain POWER1/GPIO10 with high power output. Input for power sequencer WAIT ID	If GPI, tie to non-active state. If GPO, leave floating.
J4	nOFF		DI	Active low input from error indication line to initiate fast emergency shutdown	Pull-up to VSYS or VDDCORE
B8	nSHUTDOWN		DI	Active low input from switch or host to initiate shutdown	Pull-up to VSYS or VDDCORE
D9	nRESET		DO	Active low RESET for host	Leave floating
B7	nIRQ		DO	IRQ line for host	Leave floating

Pin Number	Signal Name	Alternate Function	Type	Description	If Unused
A9	nVDD_FAULT	GPIO12	DO/DIO	Indication for low supply voltage / GPIO12 / VDD_MON controlled GPO	If I/P, tie to non-active state. If O/P, leave floating.
E8	GP_FB1	GPIO13	DO/DIO	Status indication for host of a valid wake-up event (EXT_WAKEUP) / indicator for on-going power mode transition (READY) / GPIO13, regulator HW control	If I/P, tie to non-active state. If O/P, leave floating.
C8	GP_FB2		DIO	PWR_OK status indicator: all supervised regulators are in-range / HW input for watchdog supervision / Dual-phase BUCKCORE voltage sense at output capacitor	If I/P, tie to non-active state. If O/P, leave floating.
H9	GP_FB3		DIO	2nd 32K oscillator output: OUT32_2 / VIB_BREAK control signal for vibration motor driver (LDO8)	If I/P, tie to non-active state. If O/P, leave floating.
C4	VDD_IO1		PS	1st supply I/O voltage rail	Mandatory
C3	VDD_IO2		PS	Alternate supply I/O voltage	Mandatory
D5	TP		PS	Test pin: enables 'Power Commander' boot mode and supply pin for OTP fusing voltage	Connect to GND

2.2 4-Wire/2-Wire Interfaces

Table 2: 4-Wire/2-Wire Interface Connections

Pin Number	Signal Name	Alternate Function	Type	Description	If Unused
A4	SO		DO	4-WIRE Data output	Leave floating
A5	SI		DIO	4-WIRE Data input / 2-WIRE Data	Connect to GND
B4	SK		DI	4-WIRE/2-WIRE Clock	Connect to GND
B3	nCS		DI	4-WIRE (active low) chip select	Connect to GND
A7	DATA	GPIO14	DIO	HS-2-WIRE Data / GPIO14 (optional reset if long press in parallel with GPI15) with high power output and blinking feature	Recommend connect to test point if not used.
A8	CLK	GPIO15	DI	HS-2-WIRE Clock / GPIO15 (optional reset if long press in parallel with GPI14) with high power output and blinking feature	Recommend connect to test point if not used.

2.3 Voltage Regulators

Table 3: Voltage Regulator Connections

Pin Number	Signal Name	Alternate Function	Type	Description	If Unused
A3	VSYS		PS	Supply voltage for PMIC and input for voltage supervision (decouple with 1.0 µF)	Mandatory
H3	VDD_LDO1		PS	Supply voltage for LDO1	Connect to GND
H2	VDD_LDO2		PS	Supply voltage for LDO2	Connect to GND
G3	VDD_LDO3		PS	Supply voltage for LDO3	Connect to GND
G4	VDD_LDO4		PS	Supply voltage for LDO4	Connect to GND
G2	VDD_LDO5		PS	Supply voltage for LDO5	Connect to GND
F3	VDD_LDO6		PS	Supply voltage for LDO6	Connect to GND
E2	VDD_LDO7_8		PS	Supply voltage for LDO7 and LDO8	Connect to GND
E3	VDD_LDO9_10		PS	Supply voltage for LDO9 and LDO10	Connect to GND
D2	VDD_LDO11		PS	Supply voltage for LDO11	Connect to GND
K3	VLDO1		AO	Output Voltage from LDO1	Leave floating. Cap not required.
K2	VLDO2		AO	Output voltage from LDO2	Leave floating. Cap not required.
K1	VLDO3		AO	Output voltage from LDO3	Leave floating. Cap not required.
J1	VLDO4		AO	Output voltage from LDO4	Leave floating. Cap not required.
H1	VLDO5		AO	Output voltage from LDO5	Leave floating. Cap not required.
G1	VLDO6		AO	Output voltage from LDO6	Leave floating. Cap not required.
F2	VLDO7		AO	Output voltage from LDO7	Leave floating. Cap not required.
F1	VLDO8		AO	Output voltage from LDO8	Leave floating. Cap not required.
E1	VLDO9		AO	Output voltage from LDO9	Leave floating. Cap not required.
D1	VLDO10		AO	Output voltage from LDO10	Leave floating. Cap not required.
C1	VLDO11		AO	Output voltage from LDO11	Leave floating. Cap not required.
A6	VDDCORE		AO	Regulated supply for internal circuitry (2.2/2.5V) (decouple with 2.2 µF)	Mandatory

2.4 DC/DC Buck Converters

Table 4: DC/DC Buck Converter Connections

Pin Number	Signal Name	Alternate Function	Type	Description	If Unused
H7, H8	VDD_BUCKCORE1		PS	Supply voltage for Buck To be connected to VSYS	Connect to GND
G8, G9	VDD_BUCKCORE2		PS	Supply voltage for Buck To be connected to VSYS	Connect to GND
F8, F9	VDD_BUCKPRO		PS	Supply voltage for Buck To be connected to VSYS	Connect to GND
H5	VDD_BUCKMEM		PS	Supply voltage for Buck To be connected to VSYS	Connect to GND
H6	VDD_BUCKIO		PS	Supply voltage for Buck To be connected to VSYS	Connect to GND
H4	VDD_BUCKPERI		PS	Supply voltage for Buck To be connected to VSYS	Connect to GND
K8	VBUCKCORE1		AI	Sense node for BUCKCORE1	Connect to GND
K9	VBUCKCORE2		AI	Sense node for BUCKCORE2	Connect to GND
K10	VBUCKPRO		AI	Sense node for BUCKPRO	Connect to GND
J3	VBUCKMEM		AI	Sense node for DC/DC BUCKMEM	Connect to GND
K4	VBUCKIO		AI	Sense node for BUCKIO	Connect to GND
J2	VBUCKPERI		AI	Sense node for BUCKPERI	Connect to GND
H10	SWBUCKCORE1_A		AO	Switching node for BUCKCORE1 (Normal)	Leave Floating
J10	SWBUCKCORE1_B		AO	Switching node for BUCKCORE1 (OD)	Leave Floating
F10	SWBUCKCORE2_A		AO	Switching node for BUCKCORE2 (Normal)	Leave Floating
G10	SWBUCKCORE2_B		AO	Switching node for BUCKCORE2 (OD)	Leave Floating
E10	SWBUCKPRO_A		AO	Switching node for BUCKPRO (Normal)	Leave Floating
D10	SWBUCKPRO_B		AO	Switching node for BUCKPRO (OD)	Leave Floating
K6	SWBUCKMEM		AO	Switching node for BUCKMEM	Leave Floating
K7	SWBUCKIO		AO	Switching node for BUCKIO to be connected to SWBUCKMEM for Buck merge	Leave Floating
K5	SWBUCKPERI		AO	Switching node for BUCKPERI	Leave Floating
D4	VDDQ	E_GPI2	AI/DO	BUCKPRO target voltage sense port / State of E_GPI2 controlled GPO	Leave Floating. Set BPRO_VTTR_EN=0

Pin Number	Signal Name	Alternate Function	Type	Description	If Unused
B5	VTTR	CMP1V2	AO/DO	Memory bus termination reference voltage (50% of VDDQ), COMP1V2 controlled GPO	Leave Floating. Set BPRO_VTTR_EN=0

2.5 Ancillary Functions

Table 5: Ancillary Connections

Pin Number	Signal Name	Alternate Function	Type	Description	If Unused
A2	VREF		AIO	Filter node for internal reference voltage (decouple with 2.2 µF)	Mandatory
B2	VLNREF		AIO	Filter node for LN (low noise) reference (decouple with 2.2 µF)	Mandatory
C2	IREF		AO	Connection for bias setting (Configure with high-precision 200 kΩ resistor)	Mandatory
B1	XTAL_IN		AI	32 kHz crystal connection (adjust with 10 pF)	Connect to GND
A1	XTAL_OUT		AIO	32 kHz crystal connection (adjust with 10 pF)	Connect to GND
A10	OUT_32K		DO	32 kHz oscillator buffer	Leave floating
C7	ADCIN1	GPIO0	AI/DIO	Connection to GP ADC auto channel 1 with threshold IRQ and resistor measurement option/GPIO0	If GPI, tie to non-active state. If GPO, leave floating.
C5	ADCIN2	GPIO1	AI/DIO	Connection to GP ADC channel 2 with 1.2 V HW comparator IRQ/GPIO1, regulator HW control	If GPI, tie to non-active state. If GPO, leave floating.
C6	ADCIN3	GPIO2	AI/DIO	Connection to GP ADC channel 3/GPIO2, regulator HW control	If GPI, tie to non-active state. If GPO, leave floating.
J6	CORE_SWG	GPIO3	AIO/DIO	NMOS gate driver for Buck rail switch/GPIO3	If GPI, tie to non-active state. If GPO, leave floating.
J8	CORE_SWS	GPIO4	DIO/AI	BUCKCORE sense node from rail switch output or output capacitor of dual-phase BUCKCORE/ Connection of internal switch to the output of LDO1/GPIO4 pulled down when switch is open	If GPI, tie to non-active state. If GPO, leave floating.
J5	PERI_SWG	GPIO5	AIO/DIO	NMOS gate driver for Buck rail switch/GPIO5	If GPI, tie to non-active state. If GPO, leave floating.
D8	PERI_SWS	GPIO6	DIO/AI	BUCKPERI sense node from rail switch output/ GPIO6 pulled down when switch is open	If GPI, tie to non-active state. If GPO, leave floating.
C10	V_CP		AIO	Charge-pump output bypass (decouple with 10 nF)	Leave Floating. Set CP_EN=0

2.6 GPIO Interrupt Masks

When an unused GPIO is set to be GPI, it is recommended that the respective IRQ mask bit is set to ensure unintentional events are not triggered. This can be done in OTP or, preferably, via software configuration at boot time.

2.7 Backup Battery Charger

Table 6: Backup battery charger connections

Pin number	Signal name	Alternate function	Type	Description	If unused
J9	VBBAT		PS	Backup battery connection Coin-cell or Super-cap (decouple with 470 nF)	Fit 470 nF cap

2.8 VSS

Table 7: VSS Connections

Pin number	Signal name	Alternate function	Type	Description	If unused
D6-7, E4, F4	GND		VSS	VSS_LDO, VSS_ADC, VSS_CORE, VSUB	Mandatory
E5-7, F5-7, G5-7	GND		VSS	VSS_BUCKCORE1_A, VSS_BUCKCORE1_B, VSS_BUCKCORE2_A, VSS_BUCKCORE2_B, VSS_BUCK_PRO_A,	
				VSS_BUCK_PRO_B, VSS_BUCK_IO, VSS_BUCK_MEM, VSS_BUCK_PERI	

3 Conclusion

Adherence to the recommendations of this document can help minimise spurious application issues such as noise and increased current consumption and may avoid device damage due to incorrectly biased pins.

4 Revision History

Revision	Date	Description
1.0	19-Oct-2015	Initial version.
1.1	05-Nov-2015	Minor edit following feedback and – typographical correction.
1.2	04-Jan-2016	Remove ‘Company Confidential’ reference.
1.3	18-Feb-2022	File was rebranded with new logo, copyright and disclaimer

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Status	Definition
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