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CMOS Analog Multiplexers and Switches; Specifications and Application Considerations

Introduction

This article describes several important considerations for the use of CMOS analog multiplexers and switches. It includes selection criteria, parameter definitions, handling and design precautions and interfacing.

Which Switch To Switch To?

Intersil provides a complete line of CMOS analog switches including replacements for most of the available CMOS competition. All types feature rugged no-latch-up construction, uniform characteristics over the analog signal range, and excellent high frequency characteristics.

The HI-200 and HI-201 replace the popular, low cost DG200 and DG201 type dual and quad switches.

The HI-5042 through HI-5051 are low resistance types, offering one to four switches in virtually all combinations. These replace the IH504X series with significantly better performance, and with both 75Ω and 30Ω switches available in all configurations. These are also plug-in replacements for many of the DG180 and DG190 series of FET hybrid switches, offering the advantage of monolithic construction, but with slightly longer switching times.

The analog switches do not contain overvoltage protection on the analog inputs, although they will withstand inputs 2 or 4 volts greater than the supplies. External current limiting should be provided if higher overvoltages are anticipated, such as a resistor in series with the analog input of value: $R(ohms) \geq (V_{IN} - V_{SUPPLY}) \times 50$ where V_{IN} is the maximum expected input voltage. All digital inputs do have overvoltage/static charge protection.

Data Sheet Definitions

A. Absolute Maximum Ratings

As with all integrated circuits, these are maximum conditions which may be applied to a device (one at a time) without resulting in permanent damage. The device may, or may not, operate satisfactorily under these conditions - conditions listed under “Electrical Specifications” are the only ones guaranteed for satisfactory operation.

B. V_S, Analog Signal Range

The input analog signal range over which reasonable accurate switching will take place. For supply voltages lower than nominal, V_S will be equal to the voltage span between the supplies. Note that other parameters such as R_{ON} and leakage currents are guaranteed over a smaller input range, and would tend to degrade towards the V_S limits. All off switches can withstand $+V_S$ applied at an input while $-V_S$ is applied to the output (or vice-versa) without switch breakdown - this is not true for some other manufacturers’ devices.

C. R_{ON}, On Resistance

The effective series on-switch resistance measured from input to output under specified conditions. Note that R_{ON} changes with temperature (highest at high temperature), supply voltage, and to a lesser degree, with signal voltage and current.

D. $I_{S(OFF)}$, $I_{D(OFF)}$, $I_{D(ON)}$, Leakage Currents

Currents measured under conditions illustrated on the data sheet. A guarantee in only worst case high temperature leakages is preferred, because room temperature picoampere levels are virtually impossible to measure repeatably on available automated test equipment. Even under laboratory conditions, fixture and test equipment stray leakages may frequently exceed the device leakage. Leakages tend to double every 10^oC temperature rise, so it is reasonable to assume that the $+25^oC$ figure is about 0.001 times the $+125^oC$ measurement; however, in some cases there may be ohmic leakages, such as on the package surface, which would make the $+25^oC$ reading higher than calculated.

Each of these leakage figures is the algebraic sum of all currents at the point being measured: to each power supply, to ground, and through the switches; so the current direction cannot be predicted. In making an error analysis it should be assumed that all leakages are in the worst-case direction.

In most systems, $I_{D(ON)}$ has the most effect, creating a voltage offset across the closed switch equal to $I_{D(ON)} \times R_{ON}$.

E. V_{AL}, V_{AH}, Input Thresholds

The lower and upper limits for the digital address input voltage at which the switching action takes place. All other parameters will be valid if all “0” addressed inputs are less than V_{AL} and all “1” inputs are greater than V_{AH}. Logic compatibility will be discussed in detail later in this paper.

F. I_A, Input Leakage Current

Current at a digital input, which may be in either direction. Digital inputs are similar to CMOS logic inputs; connection to MOS gates is through resistor-diode protection networks. Unlike some other devices there is no DC negative resistance region which could create an oscillating condition.

G. T_A, T_{ON}, T_{OFF}, Access Time

The logic delay time plus output rise time to the 90% point of a full scale analog output swing. After this time the output will continue to rise, approaching the 100% point on an exponential curve determined by $R_{ON} \times C_{D(OFF)}$.

H. T_{OPEN}, Break-Before-Make Delay

The time delay between one switch turning OFF and another switch turning ON, both switches being commanded simultaneously. This prevents a momentary condition of both switches being ON, generally a very minor problem.

I. $C_{S(OFF)}$, $C_{D(OFF)}$, $C_{D(ON)}$, Input/Output Capacitance

Capacitance with respect to ground measured at the analog input/output terminals. $C_{D(ON)}$ is generally the sum of $C_{S(OFF)}$ and $C_{D(OFF)}$. $C_{D(OFF)}$ is usually the most important term as rise time/settling characteristics are determined by R_{ON} x $C_{D(OFF)}$, as well as the high frequency transmission characteristics.

J. $C_{DS(OFF)}$, Drain to Source Capacitance

The equivalent capacitance shunting an open switch.

K. OFF Isolation

The proportion of a high frequency signal applied to an open switch input appearing at the output:

$$\text{off isolation} = 20 \log \frac{V_{IN}}{V_{OUT}}$$

This feedthrough is transmitted through $C_{DS(OFF)}$ to a load composed of $C_{D(OFF)}$ in parallel with the external load. The isolation generally decreases by 6dB/octave with increasing frequency.

L. C_A, Digital Input Capacitance

Capacitance to ground measured at digital input. This chiefly affects propagation delays when driven by CMOS logic.

M. P_D, Power Dissipation: I+, I-

Quiescent power dissipation, P_D = (V+ x I+) + (V- x I-). This may be specified both operating and standby (“Enable” pin ON/OFF). Note that, as with all CMOS devices, dissipation increases with switching frequency, but that Intersil devices exhibit much less of this effect.

Care And Feeding of Multiplexers And Switches

Dielectrically isolated CMOS ICs require no more care in handling and use than any other semiconductor - bipolar or otherwise. However, they are not indestructible, and reasonable common sense care should be taken.

In a laboratory breadboard, power should be shut off before inserting or removing any IC. It is especially important that supply lines have decoupling capacitors to ground permanently installed at the IC socket pins, as intermittent supply connections can create high voltage spikes through the inductance of a few feet of wire.

Because each of the major manufacturers of CMOS multiplexers and switches uses a radically different process, it is urged that units from all prospective suppliers be equally tested in breadboards and prototypes. It will be interesting to note which types best survive the hazards of a few weeks of breadboard testing.

Particular care of semiconductors during incoming inspection and installation is quite important, because the cost of reworking finished assemblies with even a small percentage of preventable failures can seriously erode profits. All equipment should be periodically inspected for proper grounding. With these devices, it is not usually necessary to shackle personnel to the nearest water pipe, if reasonable attention is paid to clothing and floor coverings; but be alert for periods of unusually high static electricity. If special lines are already set up for handling MOS devices, it wouldn’t hurt to use them.

There are a few good rules for P.C. card layout:

1. Each card or removable subassembly should contain decoupling capacitors for each supply line to ground. This not only helps keep noise away from the analog lines, but gives good protection from static electricity damage when loose cards are handled.
2. When digital inputs come through a card connector, the pull-up resistor should be at the CMOS input. This forces current through the connector and prevents possible dry circuit conditions (see following discussion on digital interface).
3. All unused digital inputs must be tied to logic “0” (ground) or logic “1” (logic supply or device + supply) depending on truth table and action desired. Open inputs tend to oscillate between “0” and “1”. Good design practices also dictate using a series resistor ($\geq 1k\Omega$) when connecting an unused input to a supply other than GND. It would also be best to ground any unused analog inputs/outputs and any uncommitted device pins.

Digital Interface

A. Reference Connection

HI-5042 through HI-5051 and HI-1818A/1828A require connecting the V_L pin to the digital logic supply (+5V to +15V).

The HI-200/201/506A/507A have V_{REF} pins which are normally left open when driving from +5 volt logic (DTL or TTL), but may be connected to higher logic supplies (to +15V) to raise the threshold levels when driving from CMOS or HNIL. The HI-200/201 will have significantly lower power dissipation when V_{REF} is connected to a high level supply.

The HI-506/507/508A/509A do not have V_{REF} terminals, but will operate reliably with any logic supplied from +5 to +15 volts.

B. DTL/TTL Interface

One major difference found in comparisons of similar devices from different manufacturers is the worst-case digital input high threshold (V_{AH} or V_{IH}). These range anywhere from +2V to +5V; and anything greater than +2.4V is obviously not compatible with worst-case TTL output levels. The fact is that no CMOS input is truly TTL compatible unless an external pull-

up resistor is added. TTL output stages were not designed with CMOS loads in mind.

The experienced designer will always add a pull-up resistor from CMOS input to the +5 volt supply when driving from TTL/DTL, for the following reasons:

1. Interchangeability: allows substitution of similar devices from several manufacturers.
2. Noise immunity: a TTL output in the “high” condition can be quite high impedance. Even when voltage noise immunity seems satisfactory, the line is quite susceptible to induced noise. The pull-up resistor will reduce the impedance while increasing voltage noise immunity.
3. Compatibility: one manufacturer does guarantee +2.0 volt minimum V_{AH}. However, this is accomplished with circuitry that is anything but TTL compatible: input current vs. voltage shows an abrupt positive then negative resistance region which is not the kind of load recommended for an emitter follower stage. A pull-up resistor will swamp out the negative resistance. Other CMOS inputs capacitively couple internal switching spikes to the input which could cause double-triggering without the pull-up resistor.
4. Reliability: it shouldn’t happen with carefully processed ICs, but any possible long term degradation of CMOS devices usually involves threshold voltage shifts. The pull-up resistor will help maintain operation if input thresholds drift out of spec. On units without adequate input protection, the resistor also helps protect the device when a loose P.C. card is handled. Where the interface goes through a P.C. connector, the resistor will force current through the connector to break down any insulating film which otherwise might build up and cause erratic dry circuit operation.

A 2kΩ resistor connected from the CMOS input to the +5 volt supply is adequate for any TTL type output. If power consumption is critical, open collector TTL/DTL should be used, allowing a higher value resistor - the voltage drop across the resistor is computed from the sum of specified “1“ level leakage currents at the TTL output and CMOS input.

C. CMOS Interface

The digital input circuitry on all devices is identical to series 4000 and 54C/74C logic inputs, and is compatible with CMOS logic with supplies between +5V and +15V without external pull-up resistors.

D. Electromechanical Interface

When driving inputs from mechanical switches or relays, either a pull-up or pull-down resistor must be connected at the CMOS input to clear the dry circuit film and to damp out any spikes, as illustrated in Figure 1, (b) and (c).

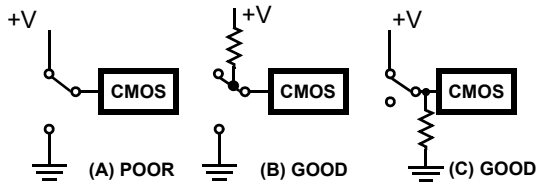

FIGURE 1. PULL-UP/PULL-DOWN RESISTOR CONNECTED AT CMOS INPUT

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Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

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