RX62N, M16C/62P

ADC Migration Guide: M16C/62P to RX62N

REU05B0143-0120
Rev.1.20
Sep 30, 2010

Introduction

The following document describes the differences between the ADC modules found on the Renesas RX62N and M16C/62P devices.

Target Device

RX62N

M16C/62P

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1. Features

Table 1.1 lists the features of the A/D converter modules found on the RX62N and M16C/62P devices. Differences are highlighted.

Table 1.1 – A/D Converter Features

	Specification	
Item	**RX62N**	**M16C/62P**
Number of units	2	1
Channels/Unit	4	8
Total channels	8	8
A/D conversion method	Successive approximation	Successive approximation
Resolution	10-bit [*1]	8 or 10-bit (selectable)
Operating Modes	Single mode One-cycle scan mode Continuous scan mode	Single mode Repeat mode One-cycle scan mode Continuous scan mode Continuous scan mode w/ priority channels (Repeat mode 1)
A/D Conversion Start Condition	Software trigger External trigger (-ADTRG pin) MTU 8-bit timer (TMR)	Software trigger External trigger (-ADTRG pin)
Sample & Hold	Yes	Switchable
Clock sources	PCLK, PCLK/2, PCLK/4, PCLK/8	fAD, fAD/2, fAD/3, fAD/4, fAD/6, fAD/12
Maximum conversion speed	1.0 uS/channel (PCLK = 50 MHz)	8-bit resolution: 2.33 uS 10-bit resolution: 2.75 uS (A/D clock = 12 MHz, Sample & hold on)

Notes:
1. A separate 12-bit A/D converter (S12ADC) is available on the RX62N.

2. General Notes

- Increased conversion speed means that changes in external signal conditioning circuitry may be required; new clocking and conversion options may minimize or eliminate the necessity of such changes in some cases. For more details, see section 5.3 - A/D timing differences between M16C/62P and RX62N.
- Result registers on the M16C/62P are right justified; results may be left or right justified on the RX62N (the default is right justified data).
- A diagnostics register on the RX62N allows reading of the internal reference voltages to verify proper function of the ADC.
- The common external op-amp feature of the M16C/62P that uses pins ANEX0 and ANEX1 is not available on the RX62N.
- Repeat mode (continuous conversions on a single channel) is not available on the RX62N; however, it is possible to perform continuous conversions on one or more channels starting from AN0.

3. References

The hardware manual for the RX62N is:

REJ09B0552: RX62N Group, RX621 Group Hardware Manual

The software manual for the RX62N is:

REJ09B0435: RX Family Software Manual

The hardware manual for the M16C/62P is:

REJ09B0185: M16C/62P Group (M16C/62P, M16C/62PT) Hardware Manual

3.1 Hardware Manual Relevant Chapters

Clock Generation Circuit – for details on how to setup the peripheral clock used by the A/D converter

I/O Registers – provides a complete listing of all registers

Low Power Consumption – for details on the Sleep and other modes affected by the A/D converter

Interrupt Control Unit - for details on the enabling interrupts from the A/D converter to the interrupt controller

10-Bit A/D Converter (ADa) – for details on A/D-specific registers and operating modes

Optional chapters

8-Bit Timer (TMR) – if using TMR to trigger the A/D converter

Multi-Function Timer Pulse Unit 2 (MTU2) – if using the MTU to trigger the A/D converter

3.2 Associated Registers

Table 3.1 - Registers Associated With A/D Converter Operation

Name	Description	H/W Manual Chapter(s)
SYSTEM.SCKR	System Clock Control Register	Clock Generation Circuit
ICU.IR	Interrupt Request Register	Interrupt Control Unit
ICU.IER	Interrupt Request Enable Register	Interrupt Control Unit
ICU.IPR	Interrupt Priority Register	Interrupt Control Unit
ADx.ADDRA	A/D Data Register A	10-Bit A/D Converter (ADa)
ADx.ADDRB	A/D Data Register B	10-Bit A/D Converter (ADa)
ADx.ADDRC	A/D Data Register C	10-Bit A/D Converter (ADa)
ADx.ADDRD	A/D Data Register D	10-Bit A/D Converter (ADa)
ADx.ADCSR	A/D Control/Status Register	10-Bit A/D Converter (ADa)
ADx.ADCR	A/D Control Register	10-Bit A/D Converter (ADa)
ADx.ADDPR	A/D Data Placement Register	10-Bit A/D Converter (ADa)
ADx.ADSSTR	A/D Sampling State Register	10-Bit A/D Converter (ADa)
ADx.ADDIAGR	A/D Self-Diagnostic Register	10-Bit A/D Converter (ADa)

4. Register Comparison by Function

This section provides a graphic overview of the differences between the ADC registers on the MC16C/62P and the RX62N by grouping similar register bits by color. Bits that share the same color between the M16C and RX perform roughly the same function (i.e. all green bits affect A/D trigger settings, blue bits affect timing).

M16C/62P A/D Registers

ADCON0

b7	b6	b5	b4	b3	b2	b1	b0
CKS0	ADST	TRG	MD[1:0]		CH[2:0]		

ADCON1

b7	b6	b5	b4	b3	b2	b1	b0
OPA[1:0]		VCUT	CKS1	BITS	MD2	SCAN[1:0]	

ADCON2

b7	b6	b5	b4	b3	b2	b1	b0
			CKS2	0	ADGSEL[1:0]		SMP

RX62N A/D Registers

ADCSR

b7	b6	b5	b4	b3	b2	b1	b0
	ADIE	ADST		CH[3:0]			

ADCR

b7	b6	b5	b4	b3	b2	b1	b0
TRGS[2:0]				CKS[1:0]		MODE[1:0]	

ADDPR

b7	b6	b5	b4	b3	b2	b1	b0
DPSEL							

ADDSTR

b7	b6	b5	b4	b3	b2	b1	b0
ADDSTR[7:0]							

Legend

- Clock selection (affects conversion speed)
- Mode selection (single shot/sweep/repeat)
- Result resolution & alignment
- Voltage & sample/hold enable
- A/D Trigger Setup
- Channel selection
- Hardware pin selection & setup
- Interrupt enable

Clock selection bits

The CKS bits select the one or more dividers for the base A/D clock. On the RX62N, the A/D Sampling State Register (ADDSTR) allows adjusting of the sampling time to compensate for high impedance sources and the faster conversion times afforded by the higher speed core of the RX.

A/D Trigger Setup

The A/D converter on the RX62N has additional sources that can trigger the start of an A/D conversion, including external sources (ADTRGx pins) and internal peripherals (MTU, TMR).

Mode selection

These bits set the converter for single shot, sweep mode, or continuous scan mode. The sweep and scan modes are different between the RX62N and the M16C/62P.

Channel selection

Channel selection on the RX is simplified, while the M16C/62P allows interleaved scanning of priority channels.

Result resolution & alignment

On the RX62N, the results of the A/D conversion can be left or right justified to provide compatibility with legacy software from other processors. The converter on RX62N is a 10-bit converter (a second 12-bit converter may be used in its place). The ADC on the M16C/62P can be set for 8-bit or 10-bit resolution.

Hardware Pin Selection & Setup

The ADGSEL[1:0] bits allow the user to select one of three groups of pins on the part for A/D conversion. The RX62N has dedicated pins for the A/D converter.

Voltage & sample/hold enable

These bits apply only to the M16C/62P. The sample & hold circuit of the ADC may be disable using the ADCON.SMP bit. The ACON2.VCUT bit powers the resistor chain for the A/D converter; clearing the bit reduces power consumption of the ADC when not in use. The RX has more sophisticated power management; power to the RX62N's ADC is enabled with the Module Stop Control Register.

Interrupt Enable

The interrupt enable bit for the RX is located in the peripheral. Setting ADCSR.ADIE enables ADC conversion complete interrupts to the ICU. The interrupt enable bit in the ICU must be set and a non-zero priority must be assigned to the ADC to generate an interrupt.

5. Usage Notes

5.1 I/O Register Macros

New macros in the iodefine.h for RX family parts make it easier to refer to ICU control registers, module stop registers, DTC enable registers, and interrupt vector numbers by the logical names associated with the peripherals. These macros allow portability across RX family members by hiding specific register and vector numbers. See the documentation contained in iodefine.h for details.

Some examples:

Macro	Usage example
`IR("module name", "bit name")`	`if ( IR(AD0,ADI0) == 1)…`
`IEN("module name", "bit name")`	`IEN(AD0,ADI0) = 1 ;`
`IPR("module name", "bit name")`	`IPR(AD0,ADI0) = 0x02 ;`
`MSTP("module name")`	`MSTP(AD0) = 0 ;`
`VECT("module name", "bit name")`	`#pragma interrupt (MySciTxIsr(vect=VECT(AD0,ADI0))`

5.2 Software Comparison: One-Shot Conversion

The code example below shows one-shot conversion of the A/D converter on the M16C/62P versus the RX62N.

Step	M16C/62P (A/D channel 0)	RX62N (AD0, channel 0)
1. Cancel AD0 stop state		`MSTP(AD0) = 0;`
2. Setup AD Converter	`adcon0 = 0x80;`	`AD0.ADCSR.BYTE = 0x40;`
	`adcon1 = 0x28;`	`AD0.ADCR.BYTE = 0x08;`
	`adcon2 = 0x01;`	`AD0.ADDPR.BYTE = 0x00;`
		`AD0.ADDSTR.BYTE = 0x19 ;`
3. Start AD Converter	`adcon0 |= 0x40;`	`AD0.ADCSR.BIT.ADST = 1;`
4. Wait for conversion to complete	`while (adcon0 & 0x40);`	`while (AD0.ADCSR.BIT.ADST==1);`
5. Read the result	`unsigned short int ad;`	`unsigned short int ad;`
	`ad = ad0_word.word ;`	`ad = AD0.ADDRA;`

5.3 A/D timing differences between M16C/62P and RX62N

Analog conversion speed is dictated by:

1. Signal source impedance
2. Peripheral clock (PCLK) speed setting
3. Configuration settings in the ADC subsystem

When moving applications from the M16C/62P to the RX62N the effects of each of these must be considered. In general terms, as the peripheral clock speed increases conversion time decreases; as conversion time decreases the source impedance must also decrease.

Conversion time on the M16C/62P is specified at 2.75 uS/channel when running with the peripheral clock at 12 MHz. The RX62N increases the maximum PCLK frequency to 50 MHz. The higher PCLK frequency coupled with the reduced internal capacitance of the ADC results in an improved conversion time of 1.0 uS/channel on the RX62N. This improvement, however, requires that external signal conditioning circuitry meets certain design criteria. The impedance of the input source signal must be 1k Ohm or less to achieve the 1.0 uS/channel conversion speed of the RX62N.

	RX62N	M16C/62P
Maximum peripheral clock (PCLK)	50 MHz	24 MHz
Maximum conversion speed	1.0 uS/channel	2.75 uS/channel (10-bit resolution, 12 MHz AD clock sample & hold on)
Maximum source impedance	1.0k Ohm	13.9k Ohm (fAD=10 mHz)

As an alternative to modifying the signal conditioning circuitry driving the analog inputs, it is possible adjust the RX62N's ADC timing through software so that legacy hardware remains unaffected. ADC timing may be adjusted by changing the Peripheral Clock (PCLK) base frequency, by using a post-scaled PCLK as the AD timing reference, and by changing the number of timing states that make up an ADC sample.

The base PCLK frequency is set in the Clock Generation Circuit's System Clock Control Register (SCKCR). An optional post-scaler for PCLK may be selected for the ADC using the CKS[1:0] bits of the A/D Control Register, ADCR. The A/D Sampling State Register (ADSSTR) offers a final adjustment over the AD sampling time, allowing the sampling time to grow to accommodate higher impedance circuits or to shrink to account for slow PCLK settings.

For example:

A legacy application is running on an M16C/62P using a 6 MHz crystal with a bus speed of 24 MHz and an AD clock (PCLK) of 12 MHz. The hardware circuit requires at least 5uS settling time between analog samples.

To move this application to the RX62N using a 12 MHz crystal with a bus speed of 96 MHz and a PCLK of 48 MHz, the registers in the RX62N would be set as follows:

```
SYSTEM.SCKCR.LONG = 0x00020100 ;      // PCLK=(XTAL x 4)=48 MHz, ICLK=96 MHz, BCLK=24 MHz
AD0.ADCR.BYTE = 0x0C;                 // AD clock = PCLK = 48 MHz
AD0.ADSSTR = 240;                     // Sampling time = (240/48) = 5.0 uS
```

Website and Support

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.15.2010	—	First edition issued
1.10	Apr.13.2010	—	Updated to new Renesas Electronics template.
1.20	Sep.30.2010	7	Added section 5.1

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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