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455A Group

Staircase Key Matrix (Using Time-of-Day Clock Operation Mode)

1. Abstract

This document presents the method for using the staircase key matrix of the 455A-group microcomputers and shows an application example.

2. Instruction

The application example explained in this document applies for use with the microcomputers and under the conditions described below.

- Microcomputer : 455A group
- Oscillation frequency : 4 MHz as f(XIN) or 32.767 kHz as subclock f(XCIN)
- System clock : Used in through mode (not frequency divided)

3. Related Registers

3.1 Interrupt Control Register V1

Table 3.1 shows the bit configuration of the Interrupt Control Register V1.
For write to the register V1, first set a value in the register A and then use the TV1A instruction.
Furthermore, the TAV1 instruction may be used to transfer the content of register V1 to the register A.

Table 3.1 Bit Configuration of Interrupt Control Register V1

Interrupt control register V1		at reset : 0000_2		at power down : 0000_2	R/W TAV1/TV1A
$V1_3$	Timer 2 interrupt enable bit	0	Interrupt disabled (SNZT2 instruction is valid))		
		1	Interrupt enabled (SNZT2 instruction is invalid)		
$V1_2$	Timer 1 interrupt enable bit	0	Interrupt disabled (SNZT1 instruction is valid)		
		1	Interrupt enabled (SNZT1 instruction is invalid)		
$V1_1$	Not used	0	This bit has no function, but read/write is enabled.		
		1			
$V1_0$	External 0 interrupt enable bit	0	Interrupt disabled (SNZ0 instruction is valid)		
		1	Interrupt enabled (SNZ0 instruction is invalid)		

Note1: The letter R denotes “readable,” and the letter W denotes “writable.”
Note2: : Unused bits when the staircase key matrix is set

3.2 Interrupt Control Register V2

Table 3.2 shows the bit configuration of the Interrupt Control Register V2.
For write to the register V2, first set a value in the register A and then use the TV2A instruction.
Furthermore, the TAV2 instruction may be used to transfer the content of register V2 to the register A.

Table 3.2 Bit Configuration of Interrupt Control Register V2

Interrupt control register V2		at reset : 0000_2		at power down : 0000_2	R/W TAV2/TV2A
$V2_3$	Not used	0	This bit has no function, but read/write is enabled.		
		1			
$V2_2$	Not used	0	This bit has no function, but read/write is enabled.		
		1			
$V2_1$	Not used	0	This bit has no function, but read/write is enabled.		
		1			
$V2_0$	Timer 3 interrupt enable bit	0	Interrupt disabled (SNZT3 instruction is valid)		
		1	Interrupt enabled (SNZT3 instruction is invalid)		

Note1: The letter R denotes “readable,” and the letter W denotes “writable.”
Note2: : Unused bits when the staircase key matrix is set

3.3 Timer Control Register PA

Table 3.3 shows the bit configuration of the Timer Control Register PA.
For write to the register PA, first set a value in the register A and then use the TPAA instruction.

Table 3.3 Bit Configuration of Timer Control Register PA

Timer control register PA		at reset : 0_2	at power down : 0_2	W TPAA
PA_0	Prescaler control bit	0	Stop (state retained)	
		1	Operating	

Note1: The letter W denotes “writable.”

3.4 Timer Control Register W1

Table 3.4 shows the bit configuration of the Timer Control Register W1.
For write to the register W1, first set a value in the register A and then use the TW1A instruction.
Furthermore, the TAW1 instruction may be used to transfer the content of register W1 to the register A.

Table 3.4 Bit Configuration of Timer Control Register W1

Timer control register W1		at reset : 0000_2		at power down : state retained	R/W TAW1/TW1A
$W1_3$	Timer 1 count auto-stop circuit selection bit (Note 2)	0	Timer 1 count auto-stop circuit not selected		
		1	Timer 1 count auto-stop circuit selected		
$W1_2$	Timer 1 control bit	0	Stop (state retained)		
		1	Operating		
$W1_1$	Timer 1 count source selection bits (Note 3)	$W1_1$	$W1_0$	Count source	
		0	0	PWM signal (PWMOUT)	
		0	1	Prescaler output (ORCLK)	
$W1_0$		1	0	Timer 3 underflow signal (T3UDF)	
		1	1	CNTR input	

Note1: The letter R denotes “readable,” and the letter W denotes “writable.”
Note2: This function is usable only when the timer 1 count start synchronization circuit is selected ($I1_0$ = 1).
Note3: When CNTR input is selected for the timer 1 count source, the output of port C has no effect.
Note4: : Unused bits when the staircase key matrix is set

3.5 Timer Control Register W3

Table 3.5 shows the bit configuration of the Timer Control Register W3.
For write to the register W3, first set a value in the register A and then use the TW3A instruction.
Furthermore, the TAW3 instruction may be used to transfer the content of register W3 to the register A.

Table 3.5 Bit Configuration of Timer Control Register W3

Timer control register W3		at reset : 0000_2			at power down : state retained	R/W TAW3/TW3A
$W3_3$	Timer 3 control bit	0	Stop (initial state)			
		1	Operating			
$W3_2$	Timer 3 count value selection bits	$W3_2$	$W3_1$	$W3_0$	Count value	
		0	0	0	Underflow every 512 count	
		0	0	1	Underflow every 1024 count	
$W3_1$		0	1	0	Underflow every 2048 count	
		0	1	1	Underflow every 4096 count	
		1	0	0	Underflow every 8192 count	
$W3_0$		1	0	1	Underflow every 16384 count	
		1	1	0	Underflow every 32768 count	
		1	1	1	Underflow every 65536 count	

Note1: The letter R denotes “readable,” and the letter W denotes “writable.”

3.6 Timer Control Register W5

Table 3.6 shows the bit configuration of the Timer Control Register W5.
For write to the register W5, first set a value in the register A and then use the TW5A instruction.
Furthermore, the TAW5 instruction may be used to transfer the content of register W5 to the register A.

Table 3.6 Bit Configuration of Timer Control Register W5

Timer control register W5		at reset : 0000_2		at power down : state retained	R/W TAW5/TW5A
$W5_3$	Not used	0	This bit has no function, but read/write is enabled.		
		1	This bit has no function, but read/write is enabled.		
$W5_2$	Not used	0	This bit has no function, but read/write is enabled.		
		1	This bit has no function, but read/write is enabled.		
$W5_1$	Timer 3 count source selection bits	$W5_1$	$W5_0$	Count source	
		0	0	X_{CIN} input	
		0	1	ORCLK input	
$W5_0$		1	0	Low-speed on-chip oscillator	
		1	1	High-speed on-chip oscillator	

Note1: The letter R denotes “readable,” and the letter W denotes “writable.”
Note2: : Unused bits when the staircase key matrix is set

3.7 Port Output Mode Control Register FR1

Table 3.7 shows the bit configuration of the Port Output Mode Control Register FR1.
For write to the register FR1, first set a value in the register A and then use the TFR1A instruction.

Table 3.7 Bit Configuration of Port Output Mode Control Register FR1

Port output structure control register FR1		at reset : 0000_2		at power down : state retained	W TFR1A
$FR1_3$	Ports D_3 output structure selection bit	0	N-channel open-drain output		
		1	CMOS output		
$FR1_2$	Ports D_2 output structure selection bit	0	N-channel open-drain output		
		1	CMOS output		
$FR1_1$	Ports D_1 output structure selection bit	0	N-channel open-drain output		
		1	CMOS output		
$FR1_0$	Ports D_0 output structure selection bit	0	N-channel open-drain output		
		1	CMOS output		

Note1: The letter W denotes “writable.”

3.8 Port Output Mode Control Register FR2

Table 3.8 shows the bit configuration of the Port Output Mode Control Register FR2.
For write to the register FR2, first set a value in the register A and then use the TFR2A instruction.

Table 3.8 Bit Configuration of Port Output Mode Control Register FR2

Port output structure control register FR2		at reset : 0000_2		at power down : state retained	W TFR2A
$FR2_3$	Ports $P3_2$ and $P3_3$ output structure selection bit	0	N-channel open-drain output		
		1	CMOS output		
$FR2_2$	Ports $P3_0$ and $P3_1$ output structure selection bit	0	N-channel open-drain output		
		1	CMOS output		
$FR2_1$	Ports D_5 output structure selection bit	0	N-channel open-drain output		
		1	CMOS output		
$FR2_0$	Ports D_4 output structure selection bit	0	N-channel open-drain output		
		1	CMOS output		

Note1: The letter W denotes “writable.”
Note2: : Unused bits when the staircase key matrix is set

3.9 Key-on Wakeup Control Register K3

Table 3.9 shows the bit configuration of the Key-on Wakeup Control Register K3.
To write to the register K3, set any value in the register A and then use the TK3A instruction.
Furthermore, the content of register K3 can be transferred to the register A using the TAK3 instruction.

Table 3.9 Bit Configuration of the Key-on Wakeup Control Register K3

Key-on wakeup control register K3		at reset : 0000_2		at power down : state retained	R/W TAK3/TK3A
$K3_3$	Ports D_6 and D_7 key-on wakeup control bit	0	Key-on wakeup not used		
		1	Key-on wakeup used		
$K3_2$	Ports D_4 and D_5 key-on wakeup control bit	0	Key-on wakeup not used		
		1	Key-on wakeup used		
$K3_1$	Ports D_2 and D_3 key-on wakeup control bit	0	Key-on wakeup not used		
		1	Key-on wakeup used		
$K3_0$	Ports D_0 and D_1 key-on wakeup control bit	0	Key-on wakeup not used		
		1	Key-on wakeup used		

Note1: The letter R denotes “readable,” and the letter W denotes “writable.”
Note2: : Unused bits when the staircase key matrix is set

3.10 Pullup Control Register PU3

Table 3.10 shows the bit configuration of the Pullup Control Register PU3.
To write to the register PU3, set any value in the register A and then use the TPU3A instruction.
Furthermore, the content of register PU3 can be transferred to the register A using the TAPU3 instruction.

Table 3.10 Bit Configuration of the Pullup Control Register PU3

Pull-up control register PU3		at reset : 0000_2		at power down : state retained	R/W TAPU3/TPU3A
$PU3_3$	Port D_6 and D_7 pull-up transistor control bit	0	Pull-up transistor OFF		
		1	Pull-up transistor ON		
$PU3_2$	Port D_4 and D_5 pull-up transistor control bit	0	Pull-up transistor OFF		
		1	Pull-up transistor ON		
$PU3_1$	Port D_2 and D_3 pull-up transistor control bit	0	Pull-up transistor OFF		
		1	Pull-up transistor ON		
$PU3_0$	Port D_0 and D_1 pull-up transistor control bit	0	Pull-up transistor OFF		
		1	Pull-up transistor ON		

Note1: The letter R denotes “readable,” and the letter W denotes “writable.”
Note2: : Unused bits when the staircase key matrix is set

3.11 Clock Control Register RG

Table 3.11 shows the bit configuration of the Clock Control Register RG.
To write to the register RG, set any value in the register A and then use the TRGA instruction.

Table 3.11 Bit Configuration of the Clock Control Register RG

Clock control register RG		at reset : 1000_2		at power down : state retained	W TRGA
RG_3	Low-speed on-chip oscillator (f(LSOCO)) control bit (Note 3)	0	Low-speed on-chip oscillator (f(LSOCO)) oscillation available		
		1	Low-speed on-chip oscillator (f(LSOCO)) oscillation stop		
RG_2	Sub-clock (f(X_{CIN})) control bit (Note 3)	0	Sub-clock (f(X_{CIN})) oscillation available, ports D_6 and D_7 not selected		
		1	Sub-clock (f(X_{CIN})) oscillation stop, ports D_6 and D_7 selected		
RG_1	Main-clock (f(X_{IN})) control bit (Note 3)	0	Main clock (f(X_{IN})) oscillation available		
		1	Main clock (f(X_{IN})) oscillation stop		
RG_0	High-speed on-chip oscillator (f(HSOCO)) control bit (Note 3)	0	High-speed on-chip oscillator (f(HSOCO)) oscillation available		
		1	High-speed on-chip oscillator (f(HSOCO)) oscillation stop		

Note1: The letter W denotes “writable.”
Note2: : Unused bits when the staircase key matrix is set
Note3: The oscillator circuit selected for the system clock cannot be stopped.

3.12 Clock Control Register MR

Table 3.12 shows the bit configuration of the Clock Control Register MR.
To write to the register MR, set any value in the register A and then use the TMRA instruction.
Furthermore, the content of register MR can be transferred to the register A using the TAMR instruction.

Table 3.12 Bit Configuration of the Clock Control Register MR

Clock control register MR		at reset : 1100_2		at power down : state retained	R/W TAMR/TMRA
MR_3	Operation mode selection bits	MR_3	MR_2	Operation mode	
		0	0	Through mode	
		0	1	Frequency divided by 2 mode	
MR_2		1	0	Frequency divided by 4 mode	
		1	1	Frequency divided by 8 mode	
MR_1	System clock selection bits (Note 2)	MR_1	MR_0	System clock	
		0	0	f(HSOCO)	
		0	1	f(X_{IN})	
MR_0		1	0	f(X_{CIN})	
		1	1	f(LSOCO)	

Note1: The letter R denotes “readable,” and the letter W denotes “writable.”
Note2: No clocks that are turned off can be selected for the system clock.

4. Application Example of the Staircase Key Matrix

The staircase key matrix refers to the one where a key is located at all combinatorial positions of two shorted port pins in a key matrix configuration.

Point : Up to 15 switches can be located at 6 input/output ports.
For the conventional key matrix using the same number of pins (consisting of 3 output ports × 3 input ports), a total number of keys is 9.
Therefore, the staircase key matrix permits a greater number of keys to be arranged than in the conventional key matrix.
However, if two or more keys are pressed at the same time, the matrix cannot determine which key has been depressed.

Specification : The matrix is reawaken by an underflow of a timer, and key numbers (1–15) are stored in RAM according to the depressed key.
Furthermore, when multiple keys are pressed at the same time, key number 255 is assumed; when no keys are entered, key number 0 is assumed.
When the matrix confirms that no keys have been entered, it goes to time-of-day clock operation mode.
Keys are scanned in a cycle of 9.984 ms.
If the scan result matches twice in succession, a key is confirmed to have been pressed and a key input confirmed flag is set.
If the result of successive key scans does not match, no keys are confirmed to have been pressed and a key input confirmed flag is cleared.

Figure 4.4 shows an example of staircase key matrix settings (1). Figure 4.5 shows an example of staircase key matrix settings (2). Figure 4.6 shows an example of staircase key matrix settings (3).

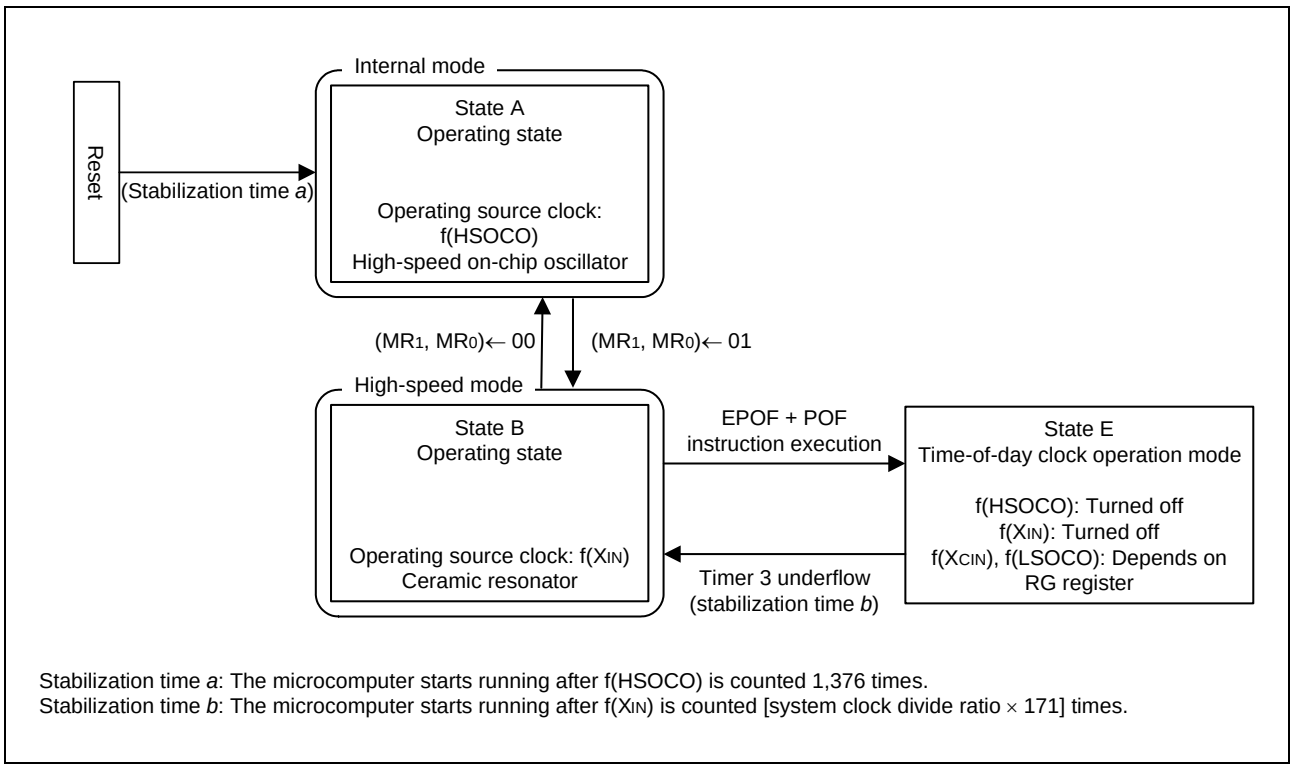
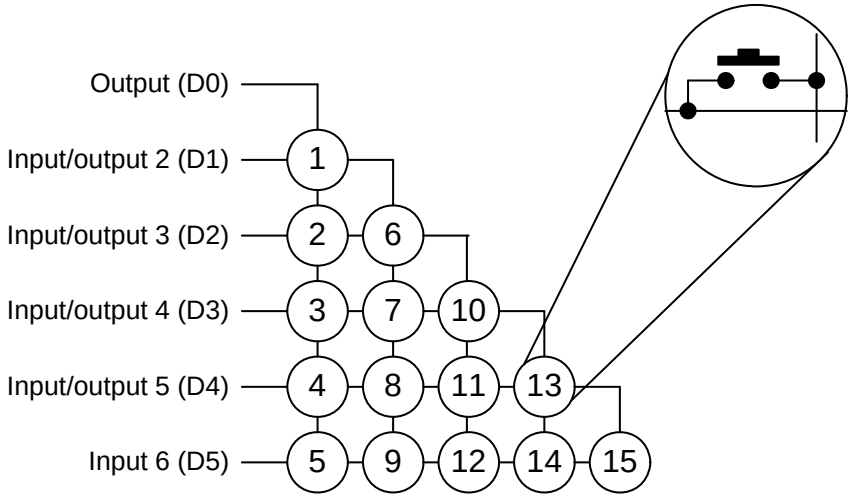


Figure 4.1 State Transition Diagram



<Key number assignments>

Number of low level input ports	Key number	Supplement
0	0	No key input
1	1–15	Single key input
2 or more	255	Multiple keys pressed

<Multiple key depressions>
If two or more keys are pressed at the same time, the matrix cannot determine which key is pressed.

<How to count the number of low level input ports>
(1) Enable all ports (D0–D5) for input.
(Select N-channel open-drain output mode for the ports and set the output latches to 1.)
(2) Output a low signal from the D0 port (setting its output latch to 0) and after waiting for a 100 µs or more, read the status of the D1–D5 ports. (Key scans for key numbers 1–5)
(3) Enable the D0 port for input and terminate key scans on D0 port output.
(4) In the same way, output a low signal from the D1–D4 ports in that order and perform key scans on each port output. At this time, do not check the status of a port that has had a signal already output from it.

<Return from power-save mode (time-of-day clock operation mode>
When using the staircase key matrix, be aware that if after RAM backup mode is entered into for power-save operation an attempt is made to return from power-save mode by a key-on wakeup, the microcomputer may not always be restored. (See *1 below.) For this reason, in the sample program presented herein, the microcomputer enters time-of-day clock operation mode as it goes to power-save mode.
An underflow signal from timer 3 is used to return from time-of-day clock operation mode, so that the microcomputer is restored from power-save mode periodically (every 15.625 ms). Each time the microcomputer is restored from power-save mode, the key matrix is checked for key input.

*1: For the key-on wakeup function to work effectively, the following conditions must be met.
- Scan output ports: Pullup is turned off , the wakeup function is disabled, and the port is set for low level output.
- Scan input ports: Pullup is turned on, the wakeup function is enabled, and the port is placed in the high-impedance state.

In the sample program presented herein, however, since the scan output and scan input ports are not fixed, there is always a key depression that does not cause the microcomputer to reawake by key-on as in the following cases. For this reason, the microcomputer may not always be restored from RAM backup mode by a key-on wakeup.
- A key that shorts the ports together that are set for scan output is depressed.
- A key that shorts the ports together that are set for scan input is depressed.

<About pullup control>
In the sample program presented herein, the key matrix using only the D ports is designed by considering that all SEG pins are used for LCD display. Since the D ports are pulled high 2 bits at a time, there is a low level output from even a port that has no keys depressed during a key scan. Therefore, be aware that the current drain in the ports increases. The ports P2 and P3 can have their pull-ups turned on or off 1 bit at a time, so that use of these ports in key scans help to reduce the current drain in the ports.

Figure 4.2 Key Matrix Arrangement

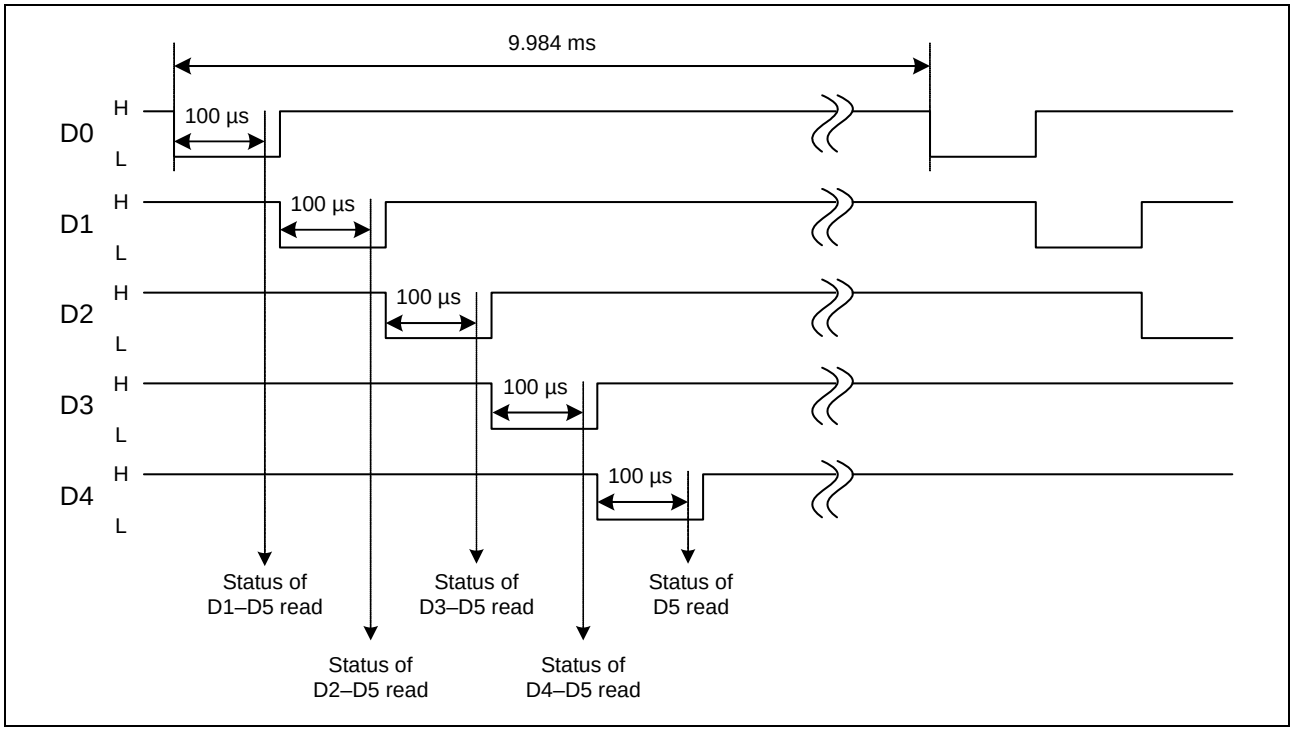


Figure 4.3 Key Scan Timing Chart

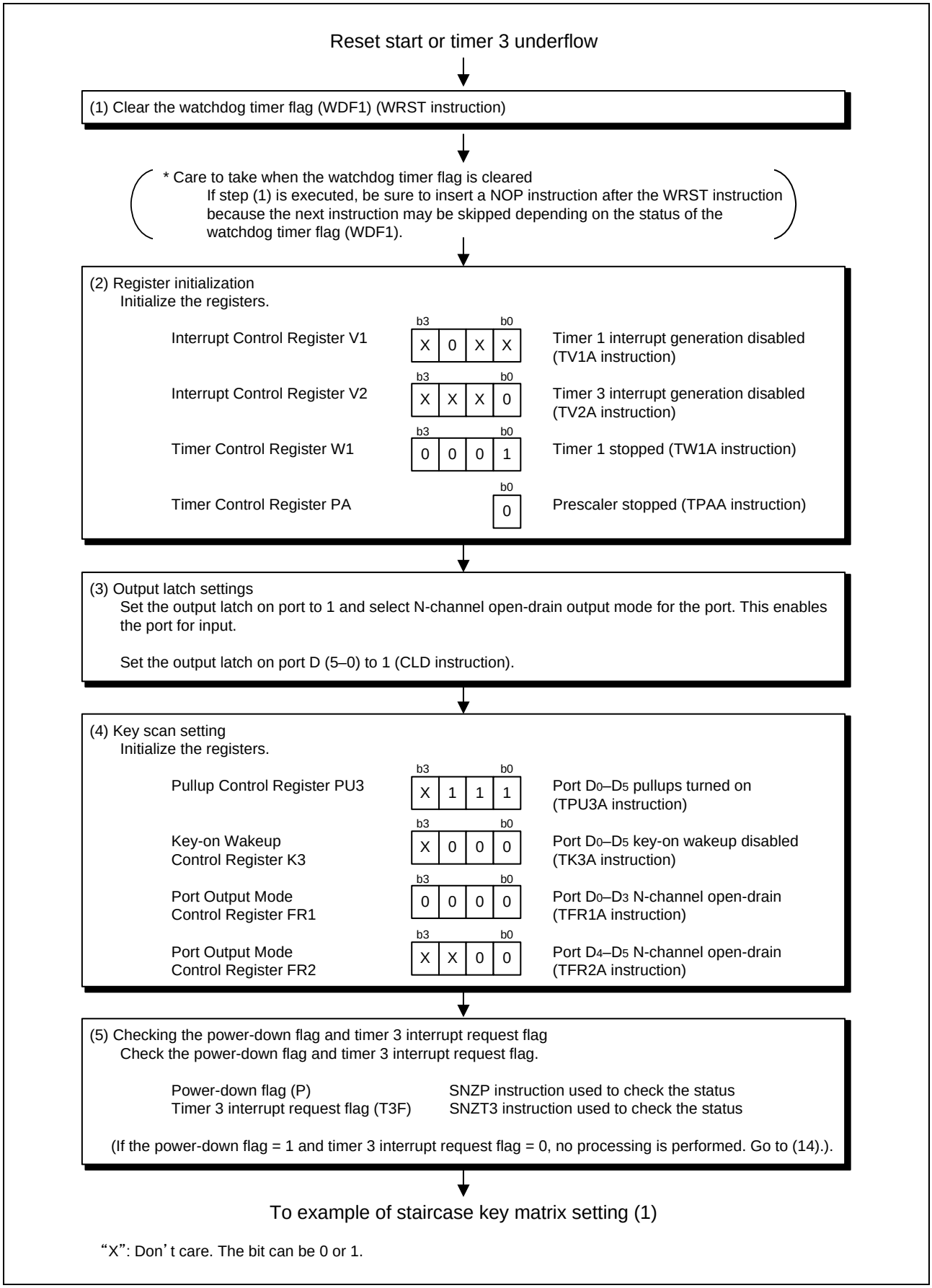


Figure 4.4 Example of Staircase Key Matrix Setting (1)

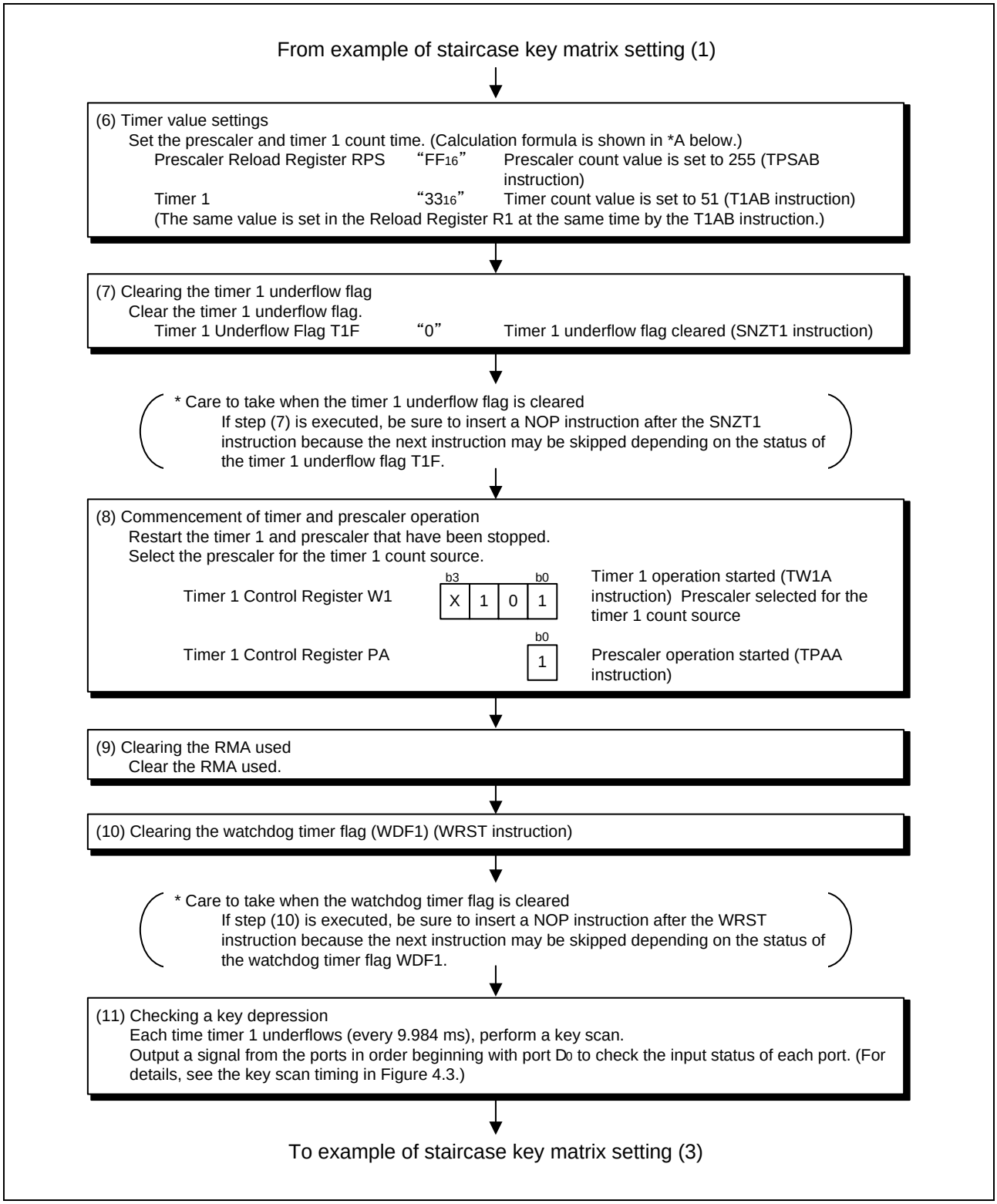


Figure 4.5 Example of Staircase Key Matrix Setting (2)

From example of staircase key matrix setting (2)

(12) Setting key numbers
If no low level inputs are detected, set 0 for the key number. (No keys entered)
If a low level input on one port is detected, set any value (1–15) for the key number corresponding to each port. (Single key input)
If a low level input on two or more ports is detected, set 255 for the key number. (Multiple key depressions)
* The above setting shows the result of one key scan, and determination of whether a key has been pressed is made separately.

(13) Determining a match of two successive key scans
If the key scan result matches twice in succession, determine that a key has been pressed. If the successive key scan results do not match, determine that no keys have been pressed.
If a key is confirmed or not confirmed to have been pressed, perform the respective processing described below.
(When confirmed) Store the key number in the key input confirmed RAM and set the key input confirmed flag.
(When not confirmed) Hold the current key scan result in memory for the comparison to be made next time and clear the key input confirmed flag.

(14) Entering time-of-day clock operation mode
If no key inputs are detected twice in succession, go to power-save mode (time-of-day clock operation mode).
* Timer 3 was turned off when warm started.

Timer Control Register W3 (b3 b0: 0 0 0 0) — Timer 3 count value is set to generate an underflow every 512 counts (TW3A instruction)

Timer Control Register W5 (b3 b0: 0 0 0 0) — XCIN selected for the timer 3 count source (TW5A instruction)

Clear the timer 3 underflow flag.
Timer 3 Underflow Flag T3F “0” Timer 3 underflow flag cleared (SNZT3 instruction)

*To run timer 3 during time-of-day clock operation mode, set bit 3 of register W3 to 1 and then set the duration of time before the POF instruction is executed to one cycle or more of the count source.

Timer Control Register W3 (b3 b0: 1 0 0 0) — Timer 3 starts operating (TW3A instruction)

Clearing the watchdog timer flag (WDF1) — WRST instruction

*Be sure to insert a NOP instruction after the WRST instruction because the next instruction may be skipped depending on the status of the watchdog timer flag WDF1.

Interrupt Enable Flag INTE “0” All interrupts disabled (DI instruction)
Entering power-save mode (time-of-day clock operation mode) — EPOF instruction + POF instruction

In other cases, continue a 9.984 ms cycle key scan. (Return to (10).)

To power-save mode (time-of-day clock operation mode)

*A To generate an interrupt every 9.984 ms, set the prescaler count value and timer 1 count value as shown below.

$$9.984\text{ms} \fallingdotseq \underbrace{(4.0\text{MHz}) - 1}_{\text{System clock (through mode)}} \times \underbrace{3}_{\text{Instruction clock}} \times \underbrace{(255+1)}_{\text{Prescaler count value}} \times \underbrace{(51+1)}_{\text{Timer 1 count value}}$$

“X”: Don’t care. The bit can be 0 or 1.

Figure 4.6 Staircase Key Matrix Setup Example (3)

5. Reference Documents

Data sheet
455A Group Data Sheet
(The latest version is available from the Renesas Technology Web site.)

Technical news / Technical Update
(The latest information is available from the Renesas Technology Web site.)

6. Sample Programs

Sample programs are available from the Renesas Technology Web site.
To download one, click the screen menu “Application Note” on the left side of 455A group Web site.

Renesas Web Site and Where to Contact

Renesas Technology Web site:
http://japan.renesas.com/

Where to contact:
http://japan.renesas.com/inquiry
csc@renesas.com

Revision histor	455A Group Staircase Key Matrix (Using Time-of-Day Clock Operation Mode)

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