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# 455A Group

## Carrier Output

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### 1. Abstract

This document presents the method for using the carrier output of the 455A-group microcomputers and shows an application example.

### 2. Introduction

The application example explained in this document applies for use with the microcomputers and under the conditions described below.

- Microcomputer : 455A group
- Oscillator frequency : 4 MHz as main clock  $f(XCIN)$ , however
- System clock : Used in through mode (not frequency divided)

### 3. Related Registers

#### 3.1 Interrupt Control Register V1

Table 3.1 shows the bit configuration of Interrupt Control Register V1.

For write to the register V1, first set a value in the register A and then use the TV1A instruction.

Furthermore, the TAV1 instruction may be used to transfer the content of register V1 to the register A.

Table 3.1 Bit Configuration of Interrupt Control Register V1

Interrupt Control Register V1		When reset: 0000 <sub>2</sub>	When powered down: 0000 <sub>2</sub>	R/W TAV1/TV1A
V13	Timer 2 interrupt enable bit	0	Disables interrupt generation (SNZT2 instruction effective)	
		1	Enables interrupt generation (SNZT2 instruction has no effect)	
V12	Timer 1 interrupt enable bit	0	Disables interrupt generation (SNZT1 instruction effective)	
		1	Enables interrupt generation (SNZT1 instruction has no effect)	
V11	Unused	0	This bit has no functions assigned, but can be read/written.	
		1		
V10	External 0 interrupt enable bit	0	Disables interrupt generation (SNZ0 instruction effective)	
		1	Enables interrupt generation (SNZ0 instruction has no effect)	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: : Unused bits during carrier output setting.

#### 3.2 Interrupt Control Register I1

Table 3.2 shows the bit configuration of Interrupt Control Register I1.

For write to the register I1, first set a value in the register A and then use the TI1A instruction.

Furthermore, the TAI1 instruction may be used to transfer the content of register I1 to the register A.

Table 3.2 Bit Configuration of Interrupt Control Register I1

Interrupt Control Register I1		When reset: 0000 <sub>2</sub>	When powered down: State retained	R/W TAI1/TI1A
I13	INT pin input control bit <sup>Note 2</sup>	0	Disables input	
		1	Enables input	
I12	INT pin interrupt active waveform/ return level select bit <sup>Note 2</sup>	0	Falling waveform/low level (SNZI0 instruction recognizes low level on INT pin)	
		1	Rising waveform/high level (SNZI0 instruction recognizes high level on INT pin)	
I11	INT pin edge detection circuit control bit	0	Detects one edge	
		1	Detects both edges	
I10	INT pin timer 1 count start synchronizing circuit select bit	0	Deselects timer 1 count start synchronizing circuit	
		1	Selects timer 1 count start synchronizing circuit	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: When the contents of these bits (I12 or I13) are changed, the external interrupt request flag (EXF0) may be set.

Note 3: : Unused bits during carrier output setting.

### 3.3 Timer Control Register W1

Table 3.3 shows the bit configuration of Timer Control Register W1.

For write to the register W1, first set a value in the register A and then use the TW1A instruction.

Furthermore, the TAW1 instruction may be used to transfer the content of register W1 to the register A.

Table 3.3 Bit Configuration of Timer Control Register W1

Timer Control Register W1		When reset: 0000 <sub>2</sub>	When powered down: State retained	R/W TAW1/TW1A
W13	Timer 1 count auto stop circuit select bit Note 2	0	Deselects timer 1 count auto stop circuit	
		1	Selects timer 1 count auto stop circuit	
W12	Timer 1 control bit	0	Stop (state retained)	
		1	Start	
W11	Timer 1 count source select bit Note 3	W11	W10	Count source
		0	0	PWM signal (PWMOU <sub>T</sub> )
		0	1	Prescaler output (ORCLK)
		1	0	Timer 3 underflow signal (T3UDF)
W10		1	1	CNTR input

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: This function is usable only when the timer 1 count start synchronizing circuit is selected (I10 = 1).

Note 3: If CNTR input is selected for the timer 1 count source, port C output is disabled.

### 3.4 Timer Control Register W2

Table 3.4 shows the bit configuration of Timer Control Register W2.

For write to the register W2, first set a value in the register A and then use the TW2A instruction.

Furthermore, the TAW2 instruction may be used to transfer the content of register W2 to the register A.

Table 3.4 Bit Configuration of Timer Control Register W2

Timer Control Register W2		When reset: 0000 <sub>2</sub>	When powered down: 0000 <sub>2</sub>	R/W TAW2/TW2A
W23	CNTR pin output control bit	0	Disables CNTR pin output	
		1	Enables CNTR pin output	
W22	PWM signal high period extend function control bit	0	Disables PWM signal high period extend function	
		1	Enables PWM signal high period extend function	
W21	Timer 2 control bit	0	Stop (state retained)	
		1	Start	
W20	Timer 2 count source select bit	0	X <sub>IN</sub> input	
		1	Prescaler output (ORCLK) divided by 2	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

### 3.5 Timer Control Register W4

Table 3.5 shows the bit configuration of Timer Control Register W4.

For write to the register W4, first set a value in the register A and then use the TW4A instruction.

Furthermore, the TAW4 instruction may be used to transfer the content of register W4 to the register A.

Table 3.5 Bit Configuration of Timer Control Register W4

Timer Control Register W4		When reset: 0000 <sub>2</sub>	When powered down: State retained	R/W TAW4/TW4A
W43	Timer LC control bit	0	Stop (state retained)	
		1	Start	
W42	Timer LC count source select bit	0	Bit 4 of timer 3 (T34)	
		1	System clock (STCK)	
W41	CNTR pin output auto control circuit select bit	0	Deselects CNTR pin output auto control circuit	
		1	Selects CNTR pin output auto control circuit	
W40	CNTR pin input count edge select bit	0	Falling edge	
		1	Rising edge	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: : Unused bits during carrier output setting.

## 4. Carrier Output Application Example

### 4.1 Carrier Output

- Point :
- Timer 2 is used to generate a PWM signal (remote control carrier).
  - Timer 1 is used to control whether or not to output a PWM signal from the CNTR pin.
  - Each time timer 1 underflows after reaching the terminal count, PWM output from the CNTR pin is switched on and off.
  - Timer 1 uses the PWM signal as its count source. The interval time for which PWM output from the CNTR pin is turned on or off can be changed by altering the set value of timer 1.
  - Even when no PWM signals are output from the CNTR pin, the chip is generating a PWM signal internally in it.

Specification : PWM signal: Approx. 33.3 kHz, 1/2 duty cycle

CNTR output: Basic duration  $T = 0.55$  ms; Output on for  $8T$ , output off for  $4T$ , and output on for  $T$

Figure 4.1 shows automatic control of CNTR output. Figure 4.2 shows an example of carrier output setting (example 1). Figure 4.3 shows an example of carrier output setting (example 2).

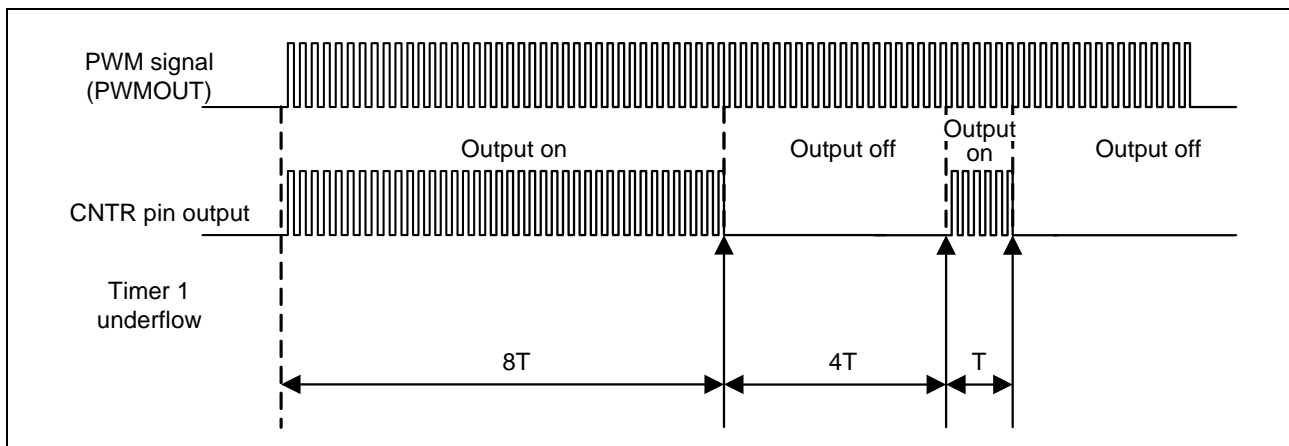


Figure 4.1 Automatic Control of CNTR Output

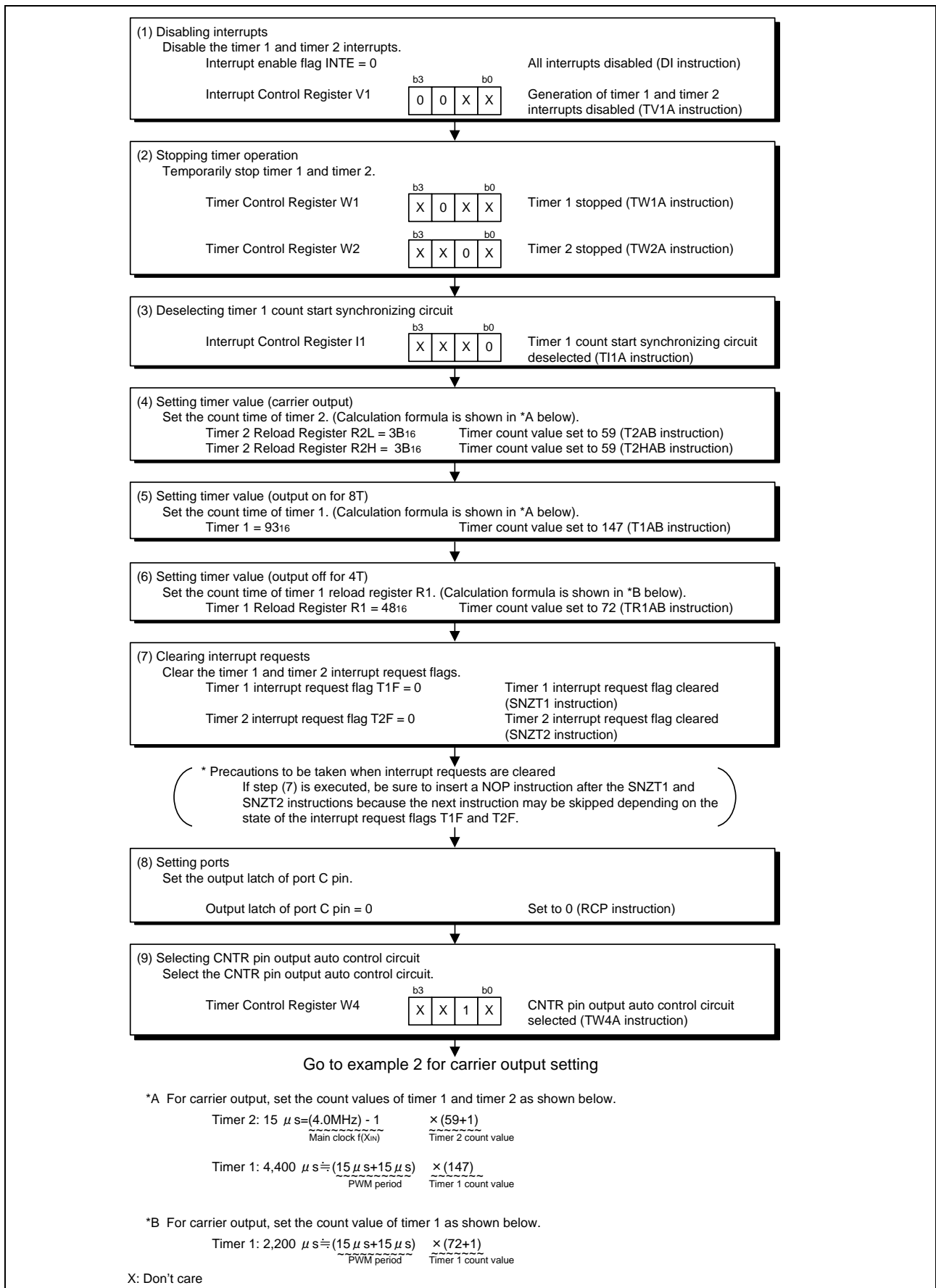


Figure 4.2 Example 1 for Carrier Output Setting



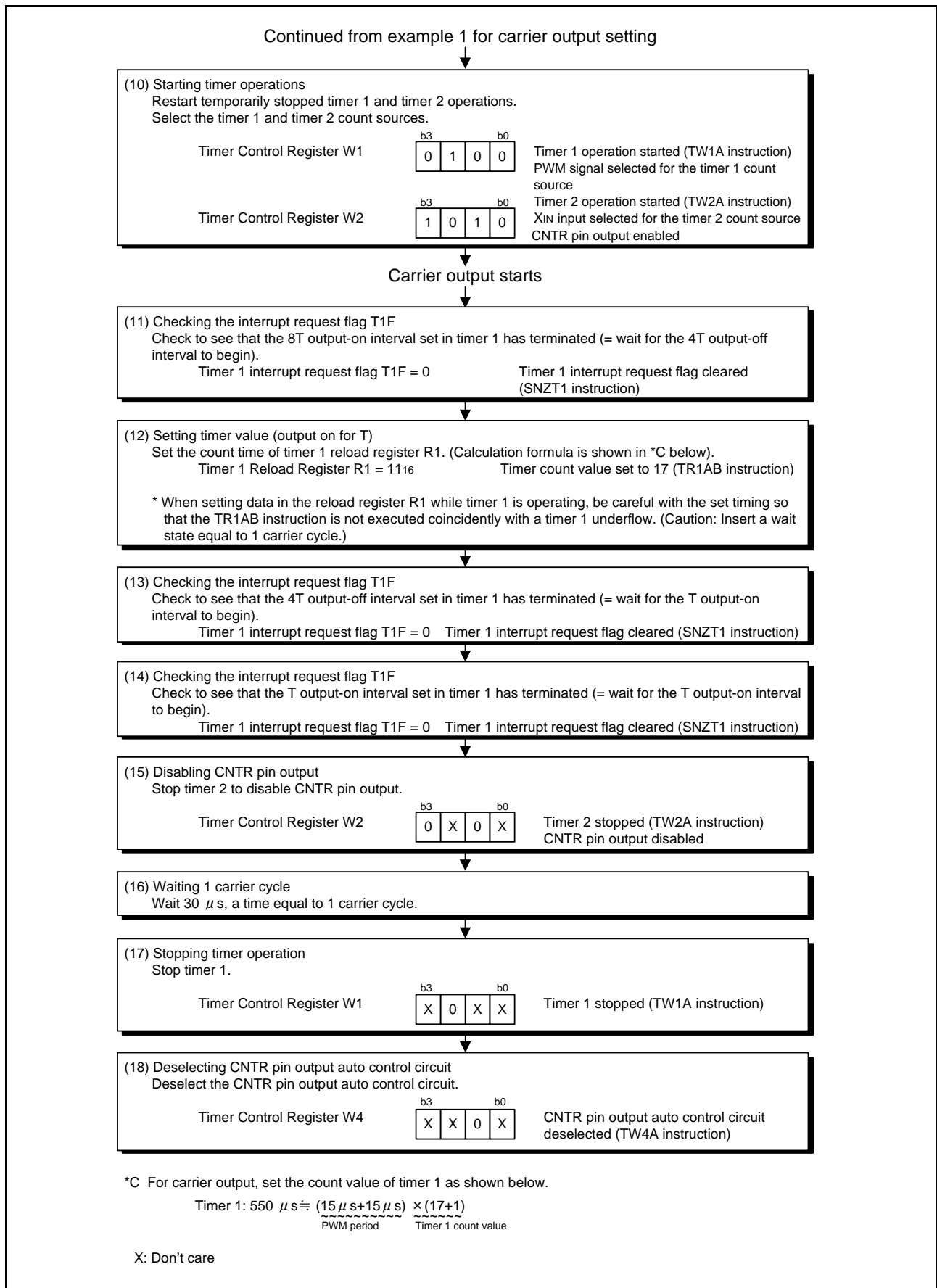


Figure 4.3 Example 2 for Carrier Output Setting

## 5. Reference Documents

Data sheet

455A Group Data Sheet

(The latest version is available from the Renesas Technology Web site.)

Technical news / Technical Update

(The latest information is available from the Renesas Technology Web site.)

## 6. Sample Programs

Sample programs are available from the Renesas Technology Web site.

To download one, click the screen menu “Application Note” on the left side of 455A group Web site.

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Revision history	455A Group Carrier Output
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Rev.	Date	Description	
		Page	Points
1.00	2008.02.29	-	First edition issued

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